MAXIM

Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7126 is a monolithic analog to digital converter with very high input impedance. On-board active components include segment drivers, segment decoders, voltage reference and a clock circuit. The ICL7126 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external display drive circuitry. Significantly reduced power consumption makes the ICL7126 a superior device, especially for portable systems.

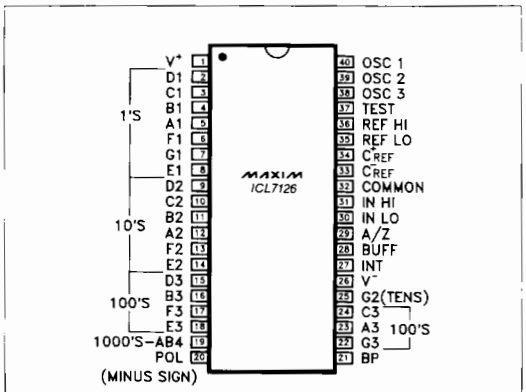
Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7126 eliminates overrange hangover and hysteresis effects. The Zero Integrator phase also allows the use of larger auto zero capacitors reducing noise further. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Pin Configuration



See ICL7106 for 44 Lead PLCC Pin Configuration

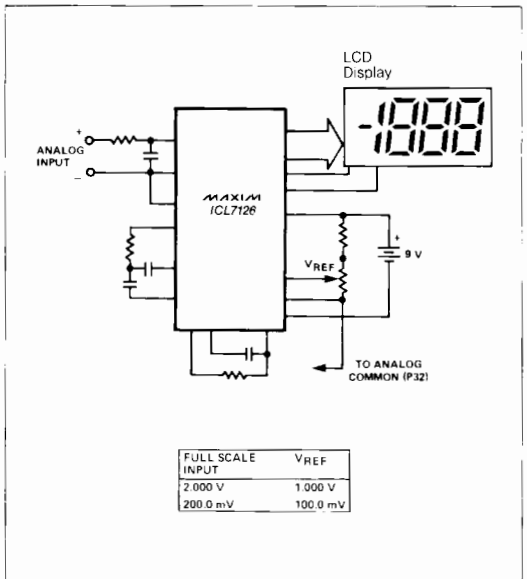
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Power dissipation guaranteed less than 1mW-9V battery life 3000 hours typical**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LCD Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7126CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7126CJL	0°C to +70°C	40 Lead CERDIP
ICL7126CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7126C/D	0°C to +70°C	Dice

Typical Operating Circuit



(Detailed Circuit Diagram—Figure 1 & 2)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Cerdip Package 1000mW
Plastic Package 800mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	-1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		50	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{CLOCK} = 16kHz and are tested in the circuit of Figure 1.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).

Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 9)**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 10)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1; unless noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 8) **0° ≤ T_A ≤ +70°C (Note 12)**	−000.0 **−000.0**	±000.0 **±000.0**	+000.0 **+000.0**	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 8) **0° ≤ T_A ≤ +70°C (Note 12)**	999 **998**	999/1000 **999/1000**	1000 **1001**	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ 200.0mV T_A = 25°C (Note 8) 0° ≤ T_A ≤ +70°C (Note 12)	−1	±.2 ±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		5		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		10		μV
Input Leakage Current	V_{IN} = 0 T_A = 25°C (Note 8) **0° ≤ T_A ≤ +70°C**		1	10 **200**	pA
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ +70°C (Note 8)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C) (Note 8)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0 T_A = 25°C **0° ≤ T_A ≤ +70°C**		60	100 **120**	μA
Analog Common Voltage (with respect to Pos. Supply)	**250kΩ between Common & Pos. Supply**	**2.6**	**2.8**	**3.2**	**V**
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
Test Pin Voltage	**With respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	**V_{IN} changing from ± 10V to 0V**		**0**	**1**	Measurement Cycles

Note 8: Test condition is V_{IN} applied between pins IN-HI and IN-LO through a 1MΩ series resistor as shown in Figure 1.

Note 9: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 10: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 11: Number of measurement cycles for display to give accurate reading.

Note 12: 1MΩ resistor is removed from circuits in Figure 1.

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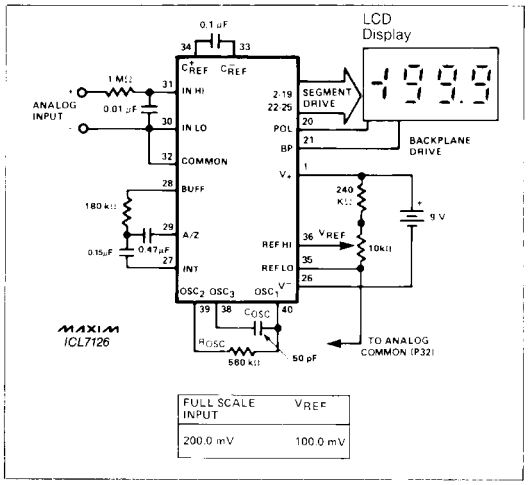

Figure 1. Maxim ICL7126 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)

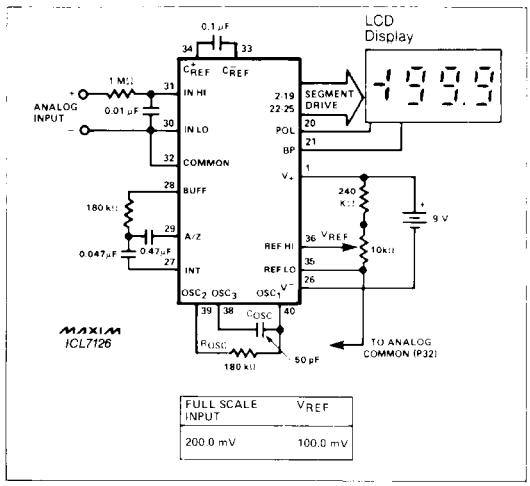

Figure 2. Maxim ICL7126 Typical Operating Circuit Clock Frequency 48kHz (3 readings/sec)

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" over range conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

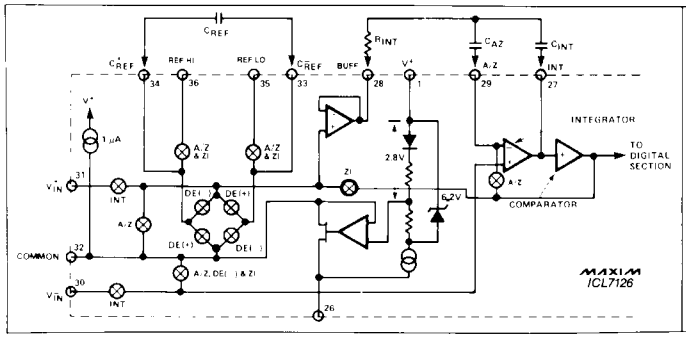

Figure 3. Analog Section ICL7126

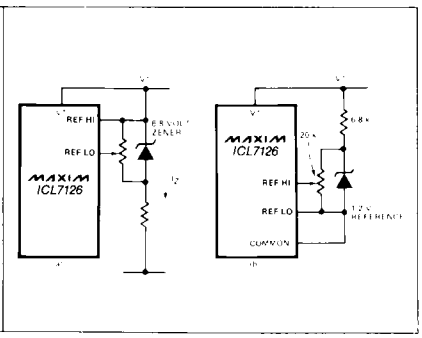

Figure 4. Using an External Reference

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The Analog Common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80 ppm/°C and a low voltage coefficient (.001%).

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from Analog-Common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible Analog Common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, the reference should be referenced to analog common as shown in Figure 4B. This will remove the common-mode voltage from the reference system.

Analog common is internally tied to an N-channel FET that can sink 500 μA or more of current. This will hold the analog common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 1 μA of source current, however, so common may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply on the 7126. This is useful for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD (display) if left in this mode for several minutes.

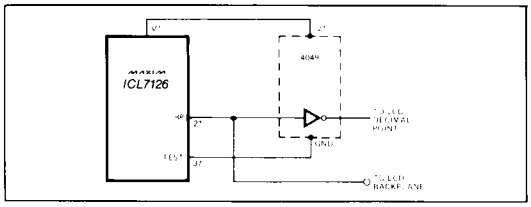

Figure 5. Simple Inverter for Fixed Decimal Point

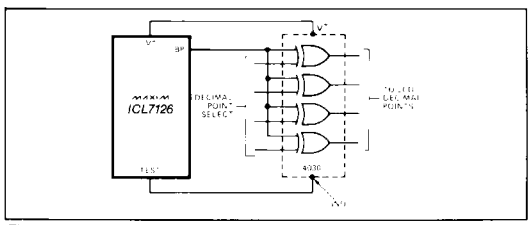

Figure 6. Exclusive "OR" Gate for Decimal Point Drive

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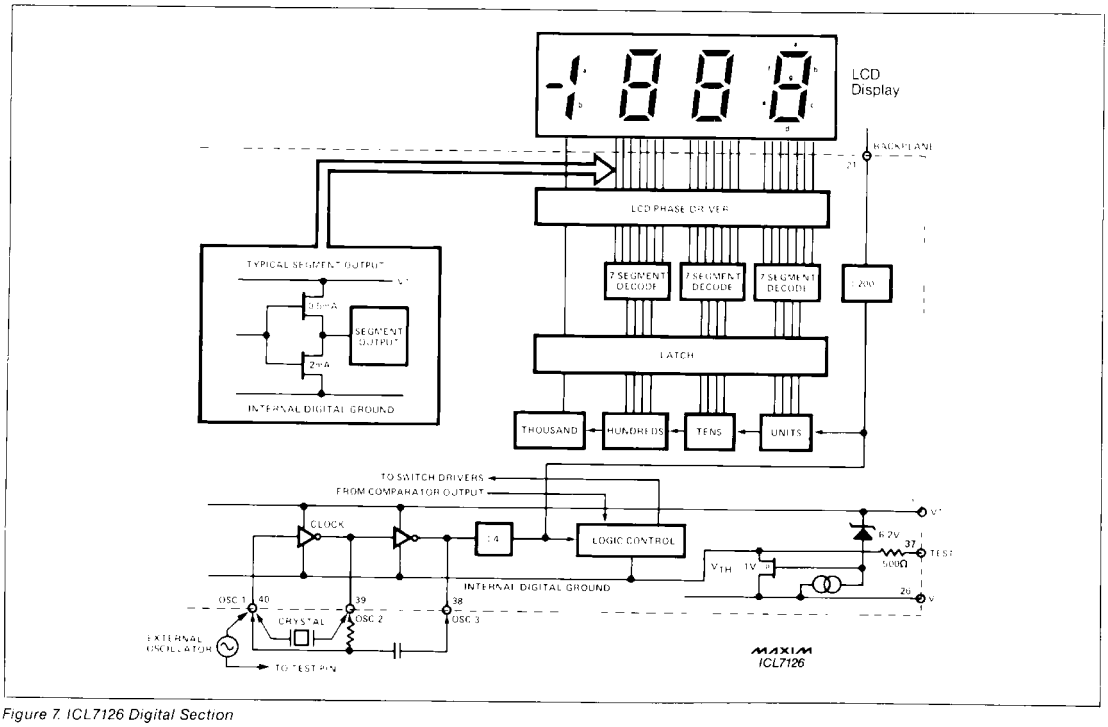

Figure 7. ICL7126 Digital Section

Digital Section

The digital section for the ICL7126 is illustrated in Figure 7. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P channel source follower. This supply is made stiff in effort to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the BP is On and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The polarity indication is "on" for negative analog inputs, for the ICL7126. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7126 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency which is divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80khZ, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000) clock pulses), independent of input voltage. As an example, an oscillator frequency of 16kHz would be used to obtain one reading per second.

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For a 2V scale, a 0.1μF capacitor is adequate. While the Maxim ICL7126 will operate with a 0.33μF capacitor, a 0.47μF capacitor is recommended for the 200mV full scale where noise rejection is very important. Due to the ZI phase, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent roll over error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held to half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable when the analog common is used as a reference. The nominal value for CINT is 0.15μF at one reading per second. (16kHz clock). This value should be changed in inverse proportion to maintain the same output swing if a different oscillator frequency is used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 6μA of quiescent current and can supply 1μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to keep the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 180kΩ resistor is recommended; (2V scale/1.8MEGΩ).

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than the unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. A suitable value of the integrating resistor would be 330kΩ. This provides for a slightly quieter system and avoids a divider network on the input. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset rating can be conveniently generated.

Oscillator Components

A 50pF capacitor is recommended for all ranges of frequency and the resistor is selected from the equation $f \approx 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Typical Applications

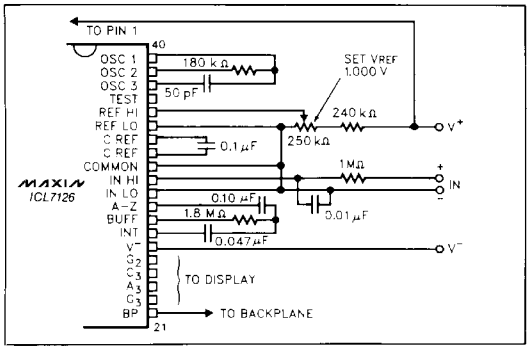

Figure 8. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change CINT, ROSC to values of Figure 1.

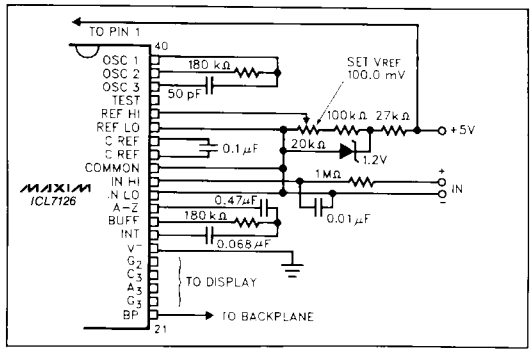

Figure 9. 7126 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V⁺ and V⁻ is insufficient for correct operation of the internal reference.

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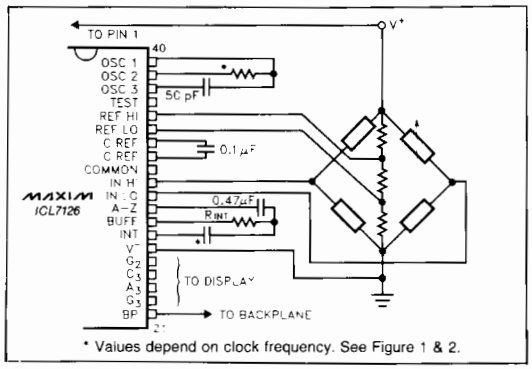


Figure 10. 7126 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

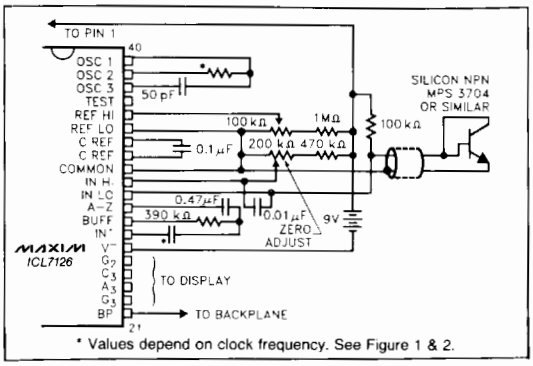
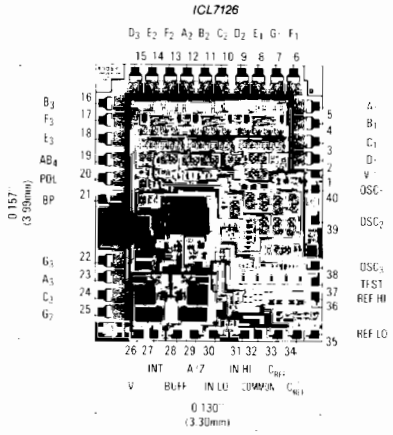


Figure 11. 7126 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/° C/. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

Chip Topography



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В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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