Document Number: MMA81XXEG
Rev 5, 04/2010

RoHS

Digital X-Axis or Z-Axis Accelerometer

The MMA81XXEG (Z-axis) and MMA82XXEG/MMA82XXTEG (X-axis) are members of Freescale's family of DSI 2.0-compatible accelerometers. These devices incorporate digital signal processing for filtering, trim and data formatting.

Features

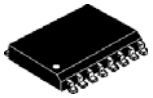
- Available in 20g, 40g, 150g, and 250g (MMA82XXEG, X-axis), 50g and 100g (MMA82XXTEG, X-axis) and 40g, 100g, 150g, and 250g (MMA81XXEG, Z-axis). Additional g-ranges may be available upon request
- 80 customer-accessible OTP bits
- 10-bit digital data output from 8 to 10 bit DSI output
- 6.3 to 30 V supply voltage
- On-chip voltage regulator
- Internal self-test
- Minimal external component requirements
- RoHS compliant (-40 to +125ºC) 16-pin SOIC package
- Automotive AEC-Q100 qualified
- DSI 2.0 Compliant
- Z-axis transducer is overdamped

Typical Applications

- Crash detection (Airbag)
- Impact and vibration monitoring
- Shock detection.

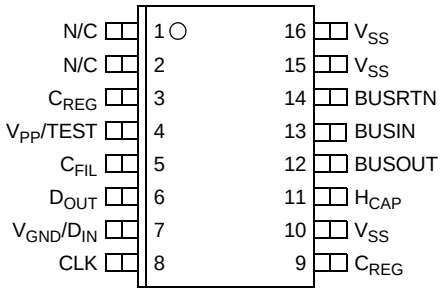
MMA81XXEG
MMA82XXEG
MMA82XXTEG
SERIES

SINGLE-AXIS
DSI 2.0
ACCELEROMETER



EG SUFFIX (Pb-free)
16-LEAD SOIC
CASE 475-01

PIN CONNECTIONS



16-PIN SOIC PACKAGE

freescale semiconductor

ORDERING INFORMATION					
Device Name	**X-axis g-Level**	**Z-axis g-Level**	**Temperature Range**	**SOIC 16 Package**	**Packaging**
MMA8225EGR2	250	—	-40 to +125°C	475-01	Tape & Reel
MMA8225EG	250	—	-40 to +125°C	475-01	Tubes
MMA8215EGR2	150	—	-40 to +125°C	475-01	Tape & Reel
MMA8215EG	150	—	-40 to +125°C	475-01	Tubes
MMA8210TEGR2	100	—	-40 to +125°C	475-01	Tape & Reel
MMA8210TEG	100	—	-40 to +125°C	475-01	Tubes
MMA8205TEGR2	50	—	-40 to +125°C	475-01	Tape & Reel
MMA8205TEG	50	—	-40 to +125°C	475-01	Tubes
MMA8204EGR2	40	—	-40 to +125°C	475-01	Tape & Reel
MMA8204EG	40	—	-40 to +125°C	475-01	Tubes
MMA8202EGR2	20	—	-40 to +125°C	475-01	Tape & Reel
MMA8202EG	20	—	-40 to +125°C	475-01	Tubes
MMA8125EGR2	—	250	-40 to +125°C	475-01	Tape & Reel
MMA8125EG	—	250	-40 to +125°C	475-01	Tubes
MMA8115EGR2	—	150	-40 to +125°C	475-01	Tape & Reel
MMA8115EG	—	150	-40 to +125°C	475-01	Tubes
MMA8110EGR2	—	100	-40 to +125°C	475-01	Tape & Reel
MMA8110EG	—	100	-40 to +125°C	475-01	Tubes
MMA8104EGR2	—	40	-40 to +125°C	475-01	Tape & Reel
MMA8104EG	—	40	-40 to +125°C	475-01	Tubes

SECTION 1 GENERAL DESCRIPTION

MMA81XXEG/MMA82XXEG/MMA82XXTEG family is a satellite accelerometer which is comprised of a single axis, variable capacitance sensing element with a single channel interface IC. The interface IC converts the analog signal to a digital format which is transmitted in accordance with the DSI-2.0 specification.

1.1 OVERVIEW

Signal conditioning begins with a Capacitance to Voltage conversion (C to V) followed by a 2-stage switched capacitor amplifier. This amplifier has adjustable offset and gain trimming and is followed by a low-pass switched capacitor filter with Bessel function. Offset and gain of the interface IC are trimmed during the manufacturing process. Following the filter the signal passes to the output stage. The output stage sensitivity incorporates temperature compensation.

The output of the accelerometer signal conditioning is converted to a digital signal by an A/D converter. After this conversion the resultant digital word is converted to a serial data stream which may be transmitted via the DSI bus. Power for the device is derived from voltage applied to the BUSIN/BUSOUT and V_{SS} pins. Bus voltage is rectified and applied to an external capacitor connected to the H_{CAP} pin. During data transmissions, the device operates from stored charge on the external capacitor. An integrated regulator supplies fixed voltage to internal circuitry.

A self-test voltage may be applied to the electrostatic deflection plate in the sensing element. Self-Test voltage is factory trimmed. Other support circuits include a bandgap voltage reference for the bias sources and the self-test voltage.

A total of 128 bits of One-Time Programmable (OTP) memory, are provided for storage of factory trim data, serial number and device characteristics. Eighty OTP bits are available for customer programming. These eighty OTP bits may be programmed via the DSI Bus or through the serial test/trim interface. OTP integrity is verified through continuous parity checking. Separate parity bits are provided for factory and customer programmed data. In the event that a parity fault is detected, the reserved value of zero is transmitted in response to a Read Acceleration Data command.

A block diagram illustrating the major elements of the device is shown in Figure 1-1.

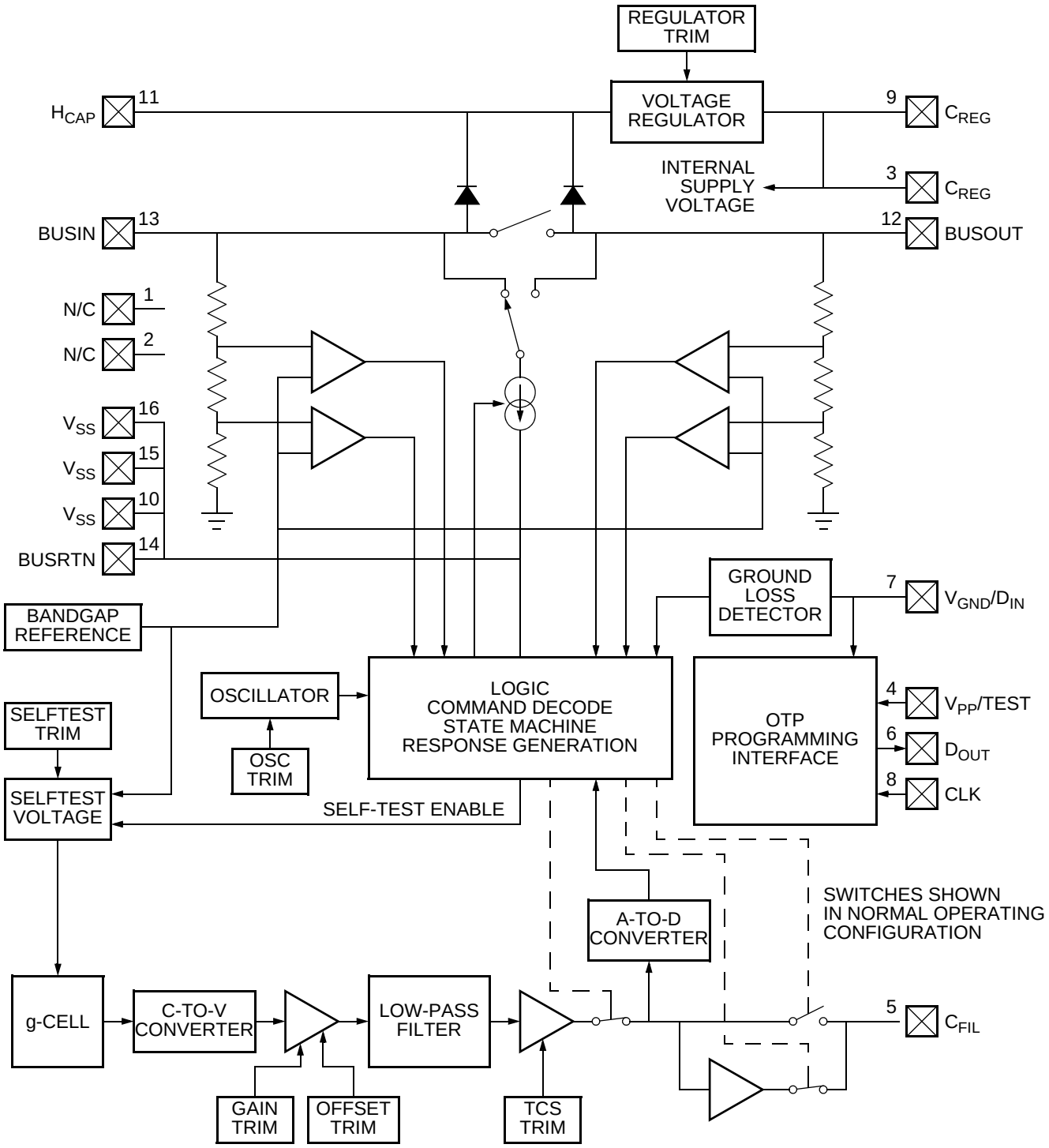
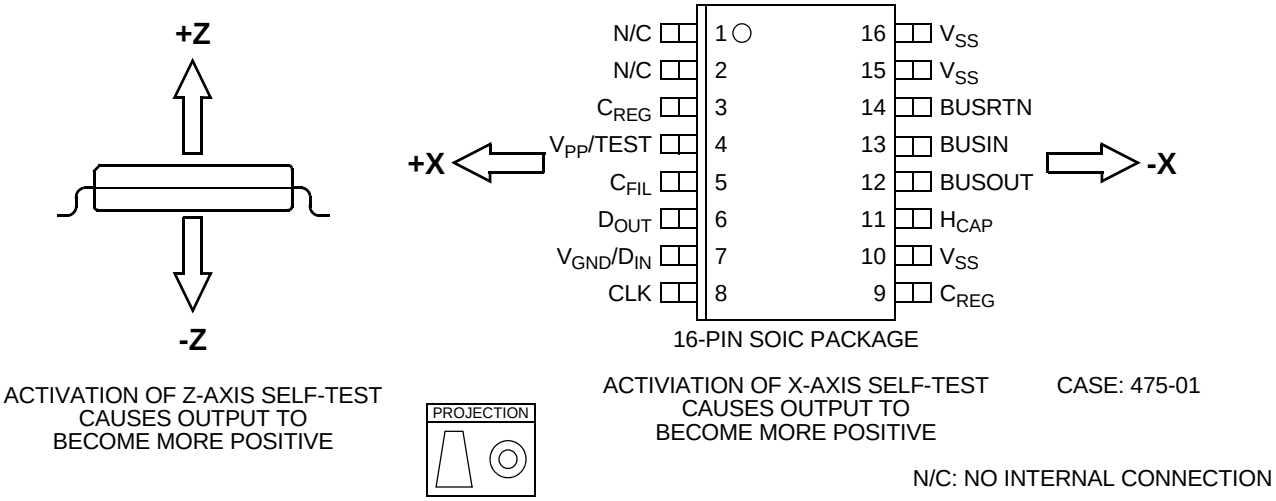


Figure 1-1. Overall Block Diagram

1.2 PACKAGE PINOUT

The pinout for this 16-pin device is shown in Figure 1-2.



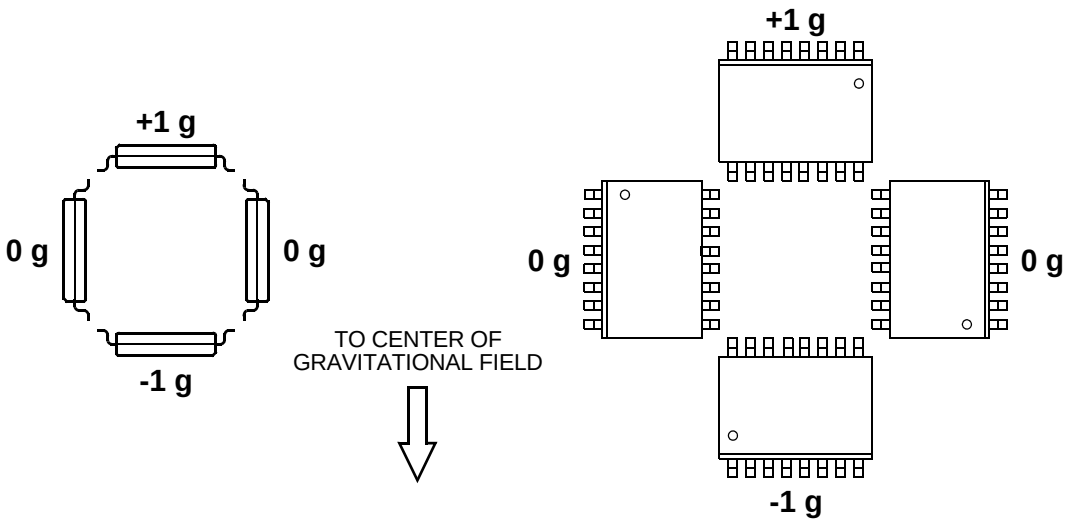


Figure 1-2. Device Pinout

1.3 PIN FUNCTIONS

The following paragraphs provide descriptions of the general function of each pin.

1.3.1 H_{CAP} and V_{SS}

Power is supplied to the ASIC through BUSIN or BUSOUT and BUSRTN. The supply voltage is rectified internally and applied to the H_{CAP} pin. An external capacitor connected to HCAP forms the positive supply for the integrated voltage regulator. V_{SS} is supply return node. All V_{SS} pins are internally connected to BUSRTN. To obtain specified performance, all V_{SS} nodes should be connected to the BUSRTN node on the PWB. To ensure stability of the internal voltage regulator and meet DFMEA requirements, the connection from H_{CAP} to the external capacitor should be as short as possible and should not be routed elsewhere on the printed wiring assembly.

The voltage on H_{CAP} is monitored. If the voltage falls below a specified level, the device will return the value zero in response to a short word Read Acceleration Data command, and report the undervoltage condition by setting the Undervoltage (U) flag. Should the undervoltage condition persist for more than one millisecond, the internal Power-On Reset (POR) circuit is activated and the device will not respond until the voltage at H_{CAP} is restored to operating levels and the device has undergone post-reset initialization.

1.3.2 BUSIN

The BUSIN pin is normally connected to the DSI bus and supports bidirectional communication with the master.

The MMA81XXEG, MMA82XXEG and MMA82XXTEG supports reverse initialization for improved system fault tolerance. In the event that the DSI bus cannot support communication between the master and BUSIN pin, communication with the master may be conducted via the BUSOUT pin and the BUSIN pin can be used to access other DSI devices.

1.3.3 BUSOUT

The BUSOUT pin is normally connected to the DSI bus for daisy-chained bus configurations. In support of fault tolerance at the system level, the BUSOUT pin can be used as an input for reverse initialization and data communication.

The internal bus switch is always open following reset. The bus switch is closed when data bit D6 is set when an Initialization or Reverse Initialization command is received.

1.3.4 BUSRTN

This pin provides the common return for power and signalling.

1.3.5 C_{REG}

The internal voltage regulator requires external capacitance to the V_{SS} pin for stability. This should be a high grade capacitor without excessive internal resistance or inductance. An optional electrolytic capacitor may be required if a longer power down delay is required.

Figure 1-3 illustrates the relationship between capacitance, series resistance and voltage regulator stability. Two C_{REG} pins are provided for redundancy. It is recommended that both C_{REG} pins are connected to the external capacitor(s) for best system reliability.

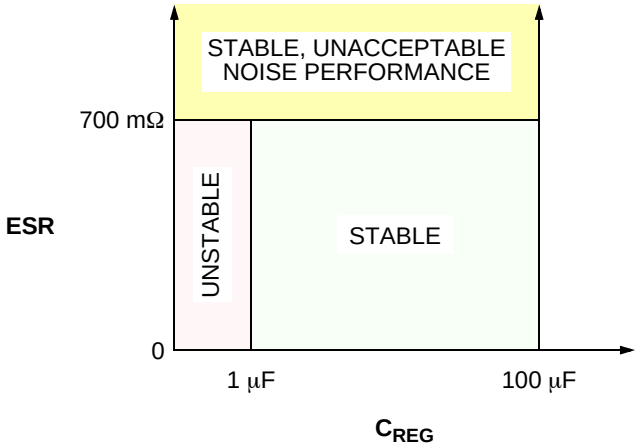


Figure 1-3. Voltage Regulator Capacitance and Series Resistance

1.3.6 C_{FIL}

The output of the sensor interface circuitry can be monitored at the C_{FIL} pin. An internal buffer is provided to provide isolation between external signals and the input to the A/D converter. If C_{FIL} monitoring is desired, a low-pass filter and a buffer with high input impedance located as close to this pin as possible are required. The circuit configuration shown in Figure 1-5 is recommended.

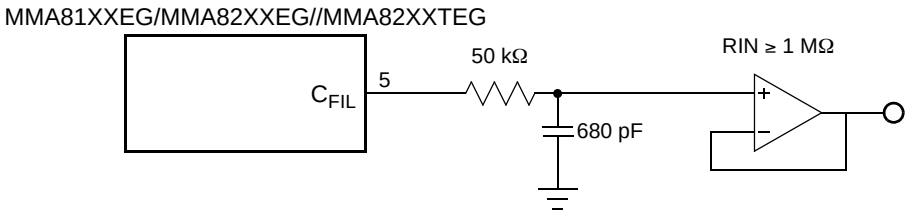


Figure 1-4. C_{FIL} Filter and Buffer Configuration

This pin may be configured as an input to the A/D converter when the MMA81XXEG, MMA82XXEG and MMA82XXTEG devices are in test mode. Refer to Appendix A for further details regarding test mode operation.

1.3.7 Trim/Test Pins (V_{PP}/TEST, CLK, DOUT)

These pins are used for programming the device during manufacturing. These pins have internal pull-up or pull-down devices to drive the input when left unconnected. The following termination is recommended for these pins in the end application:

Table 1-1

PIN	Termination
V_{PP}/TEST	Connect to ground
CLK	Leave unconnected
D_{OUT}	Leave unconnected

CLK may be connected to ground, however this is not advised if the GLDE bit in DEVCFG2 is set, as a short between the adjacent V_{GND}/D_{IN} pin and ground prevents ground loss detection.

1.3.8 GND Detect Pin (V_{GND}/D_{IN})

V_{GND}/D_{IN} may be used to detect an open condition between the satellite module and chassis. The ground loss detector circuit supplies a constant current through V_{GND}/D_{IN} and measures resulting voltage. This determines the resistance between V_{GND}/D_{IN} and the system's virtual ground. A fault condition is signalled if the resistance exceeds specified limits. This pin has no internal pull-down device and must be connected as shown in Figure 1-5.

Ground loss detection circuitry is enabled when the GLDE bit is programmed to a logic '1' state in DEVCFG2. Ground loss detection is not available when the master operates in differential mode. V_{GND}/D_{IN} must be directly connected to BUSRTN if the DSI bus is configured for differential operation. V_{GND}/D_{IN} connection options are illustrated in Figure 1-5.

When ground loss detection is enabled, a constant current is sourced and the voltage at V_{GND} is continuously monitored. An open connection between V_{SS} and chassis ground will cause the voltage to rise. If the voltage indicates that the connection between chassis ground and V_{SS} has opened, a 14-bit counter is enabled. This counter will reverse if the voltage falls below the detection threshold. Should the counter overflow, a ground loss condition is indicated. The counter acts as a digital low-pass filter, to provide immunity from spurious signals.

This pin functions as the SPI data input when the device is in test mode.

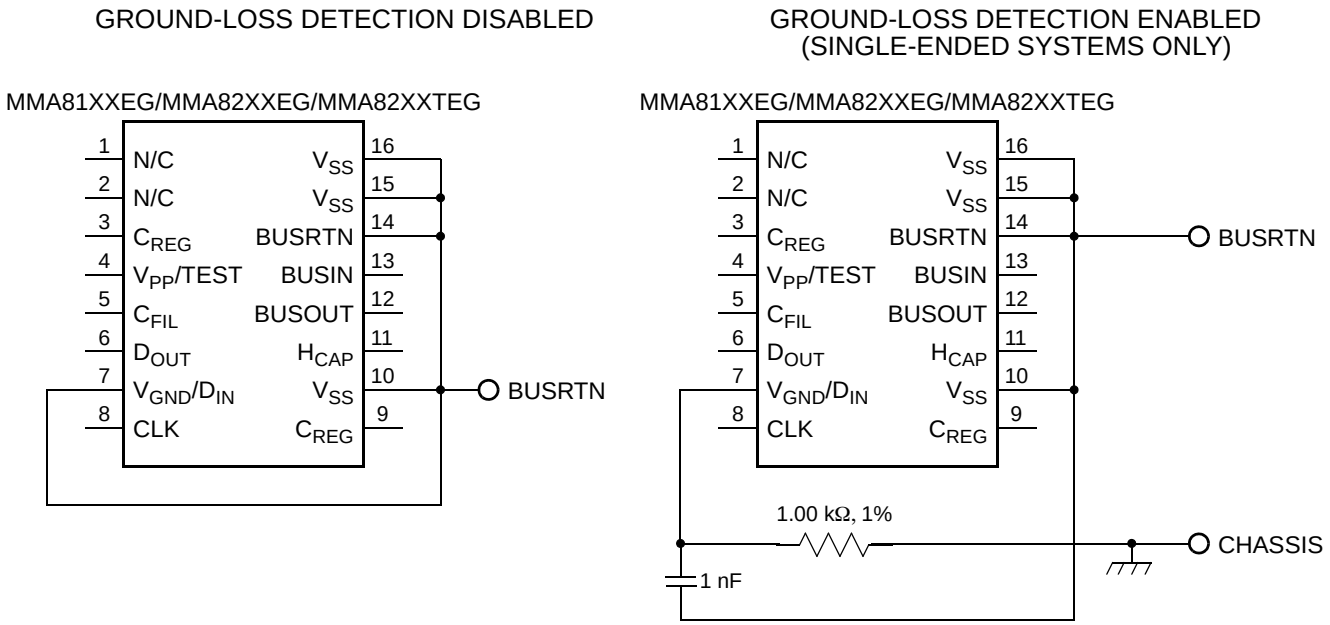
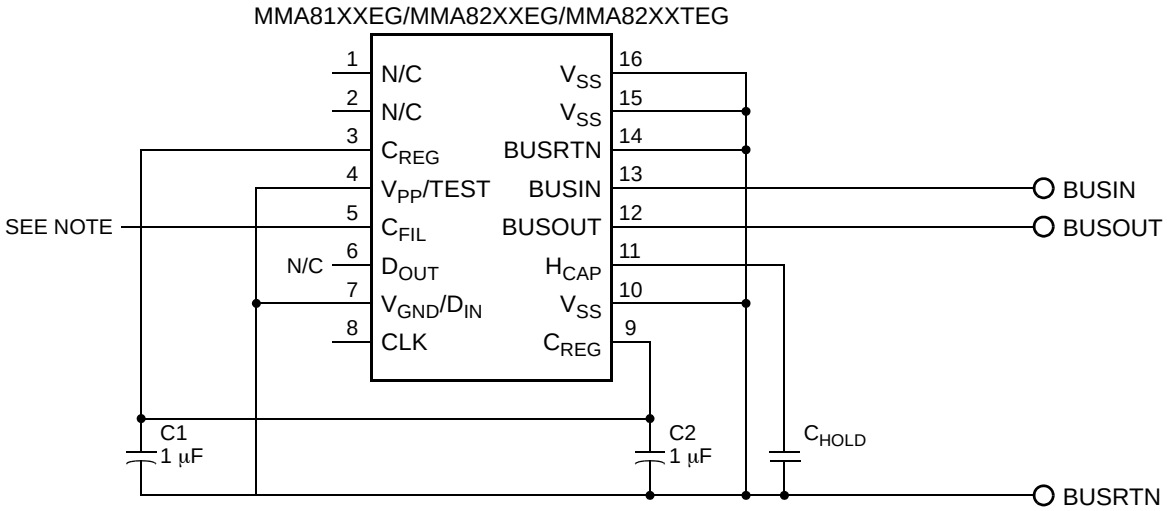


Figure 1-5. V_{GND}/D_{IN} Connection Options

1.4 MODULE INTERCONNECT

A typical satellite module configuration supporting daisy-chain configuration is shown in Figure 1-6. Capacitors C1 and C2 form a filter network for the internal voltage regulator. Two capacitors are shown for redundancy; this configuration improves reliability in the event of an open capacitor connection. A single 1 μF capacitor may be used in place of C1 and C2, however connection from the capacitor to both CREG pins is required. CHOLD stores energy during signal transitions on BUSIN and BUSOUT. The value of this capacitor is typically 1 μF; however, this depends upon data rates and bus utilization.



NOTE: LEAVE OPEN OR CONNECT TO SIGNAL MONITOR.

Figure 1-6. Typical Satellite Module Diagram

1.5 DEVICE IDENTIFICATION

Thirty-two OTP bits are factory-programmed with a unique serial number during the manufacturing and test. Five additional bits are factory-programmed to indicate the full-scale range and axis of sensitivity. Device identification data may be read at any time while the device is active.

SECTION 2 SUPPORT MODULES

2.1 MASTER OSCILLATOR

A temperature-compensated internal oscillator provides a stable timing reference for the device. The oscillator is factory-trimmed to operate at a nominal frequency of 4 MHz.

2.2 VOLTAGE REGULATION

The internal voltage regulator has minimum voltage level detection, which will hold the device in reset and prevent data transmission should the regulator output fall during operation. The regulator also has an input voltage clamp to limit the power dissipated in the regulator during voltage spikes on the H_{CAP} pin which might come from the two or three wire satellite bus.

2.3 BESSEL FILTER

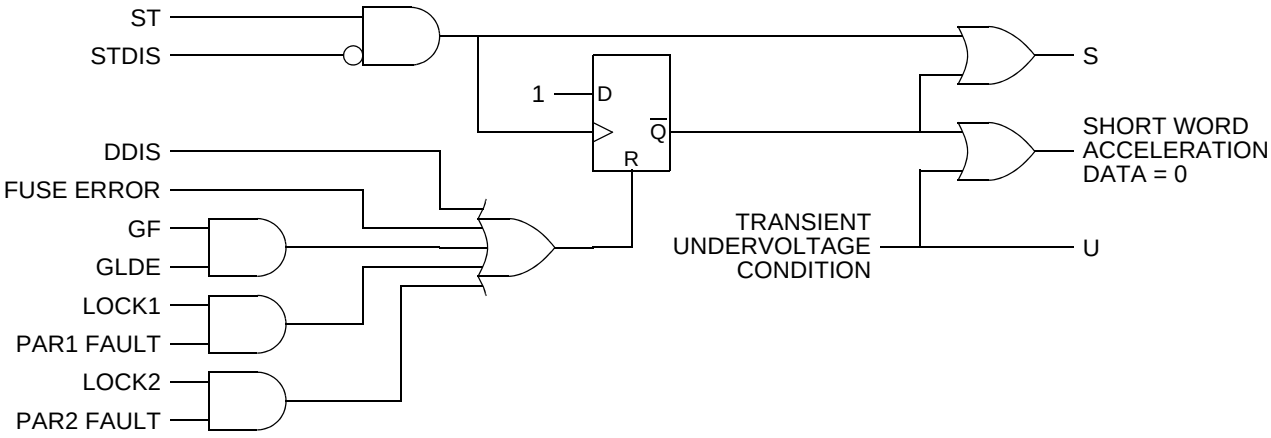
180-Hz, 2-pole and 400 Hz 4-pole Bessel filter options are provided. The low-pass filter is implemented within a two stage switched capacitor amplifier. The overall gain of the Bessel filter is set to a fixed value. The output of the Bessel filter output acts as the input to the A/D converter and is also buffered and made available at the C_{FIL} pin.

2.4 STATUS MONITORING

A number of abnormal conditions are detected by MMA81XXEG/MMA82XXEG/MMA82XXTEG and the behavior of the device altered if a fault is detected. Detected fault conditions and consequent device behavior is summarized in the table below. Certain conditions, e.g. ground loss, are qualified by device configuration. Figure 2-1 provides a representation of fault conditions, applicable qualifiers and effects.

Table 2-1 Fault Condition Response Summary

Condition	Description	Device Behavior
Undervoltage, C_{REG}	Internally regulated voltage below operating level	Device continuously undergoes reset, bus switch open, no response to DSI commands
Sustained Undervoltage, H_{CAP}	Voltage at HCAP below operating level for more than 1 ms	
Frame Timeout	Bus voltage remains below frame threshold (t_{TO}) longer than specified time.	
Transient Undervoltage, H_{CAP}	Voltage at HCAP below operating level for less than 1 ms	Undervoltage (U) flag set, short-word Read Acceleration Data response value equals zero
Fuse Fault	OTP fuse threshold failure	Accelerometer Status (S) flag set, short-word Read Acceleration Data response value equals zero
Parity Fault	Parity failure detected in factory or customer programmed OTP data	
Ground Fault	Ground loss detected for more than 4.096 ms	Accelerometer Status (S) and Ground Fault (GF) flags set, short-word Read Acceleration Data response value equals zero



KEY:	
DDIS	DEVICE DISABLE BIT, DEVCFG2[4]
FUSE FAULT	OTP FUSE THRESHOLD FAILURE
GLDE	GROUND LOSS DETECTION BIT, DEVCFG2[5]
GF	GROUND FAULT DETECTION CONDITION
LOCK1	FACTORY PROGRAMMED OTP LOCK BIT
LOCK2	CUSTOMER PROGRAMMED OTP LOCK BIT
PAR1 FAULT	FACTORY PROGRAMMED OTP PARITY FAULT CONDITION
PAR2 FAULT	CUSTOMER PROGRAMMED OTP PARITY FAULT CONDITION
S	ACCELEROMETER STATUS FLAG
ST	SELF-TEST ACTIVATION CONDITION
STDIS	SELF-TEST DISABLE
U	UNDERVOLTAGE FLAG

Figure 2-1. Status Logic Representation

The signal STDIS in Figure 2-1 is set when self-test lockout is activated through the execution of two consecutive Disable Self-Test Stimulus commands, as described in Section 4.6.6. If self-test lockout has been activated, a DSI Clear command or power-on reset is required to clear a fault condition which results in reset of the D flip-flop.

SECTION 3 OTP MEMORY

MMA81XXEG/MMA82XXEG/MMA82XXTEG family features One-Time-Programmable (OTP) memory implemented via a fuse array. OTP is organized as an array of 96 bits which contains the trim data, configuration data, and serial number for each device. Sixteen bits of the OTP array may be programmed by the customer through the DSI Bus.

3.1 INTERNAL REGISTER ARRAY AND OTP MEMORY

Contents of OTP memory are transferred to a set of registers following power-on reset, after which the OTP array is powered-down. Contents of the register array are static and may be read at any time following the transfer of data from the OTP memory. Write operations to OTP mirror registers are supported when the device is in test mode, however any data stored in the register will be lost when the device is powered down. The mirror registers are also restored when an OTP read operation is performed.

In addition to the registers which mirror OTP memory contents, several other registers are provided. Among these are the OTP Control Registers which controls OTP programming operations and may be used to restore the registers from the OTP memory.

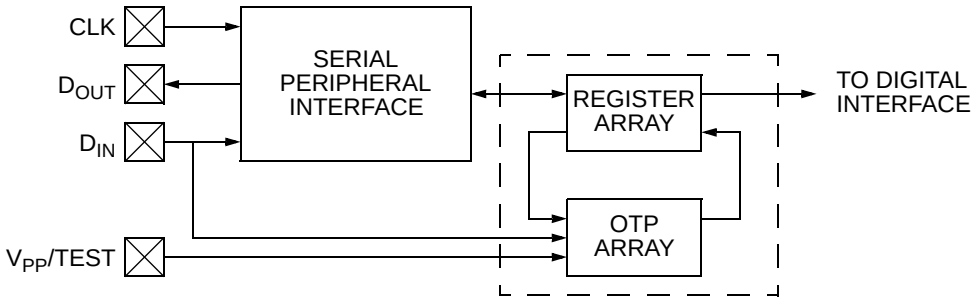


Figure 3-1. OTP Interface Overview

3.2 OTP WORD ASSIGNMENT

Customer-accessible OTP bits are shown in Table 3-1. Unprogrammed OTP bits are read as logic ‘0’ values. DEVCFG1, DEVCFG2 and registers REG-8 through REG-F are programmed by the customer. Other bits are programmed and locked during manufacturing. There is no requirement to program any bits in DEVCFG1 or DEVCFG2 for the device to be fully operational.

Table 3-1 Customer Accessible Data

Location		Bit Function							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$00	SN0	S7	S6	S5	S4	S3	S2	S1	S0
$01	SN1	S15	S14	S13	S12	S11	S10	S9	S8
$02	SN2	S23	S22	S21	S20	S19	S18	S17	S16
$03	SN3	S31	S30	S29	S28	S27	S26	S25	S24
$04	TYPE	ORDER	0	AXIS	0	0	RNG2	RNG1	RNG0
$05	RESERVED	0	0	0	0	0	0	0	0
$06	DEVCFG1	Customer Defined						AT1	AT0
$07	DEVCFG2	LOCK2	PAR2	GLDE	DDIS	AD3	AD2	AD1	AD0
$08	REG-8	Customer Defined							
$09	REG-9	Customer Defined							
$0A	REG-A	Customer Defined							
$0B	REG-B	Customer Defined							
$0C	REG-C	Customer Defined							
$0D	REG-D	Customer Defined							
$0E	REG-E	Customer Defined							
$0F	REG-F	Customer Defined							

3.2.1 Device Serial Number

A unique serial number is programmed into each device during manufacturing. The serial number is composed of the following information.

Table 3-2 Serial Number Assignment

Bit Range	Content
S12 - S0	Serial Number
S31 - S13	Lot Number

Lot numbers begin at 1 for all devices produced and are sequentially assigned. Serial numbers begin at 1 for each lot, and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Not all allowable lot numbers and serial numbers will be assigned.

3.2.2 Type Byte

The Type Byte is programmed at final trim and test to indicate the axis of orientation of the g-cell and the calibrated range of the device.

Table 3-3 Device Type Register

Location		Bit Function							
Address	**Register**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
$04	TYPE	ORDER	0	AXIS	0	0	RNG2	RNG1	RNG0

3.2.2.1 Filter Characteristic Bit (ORDER)

This bit denotes the low-pass filter characteristic.

0 - 400 Hz, 4-pole

1 - 180 Hz, 2-pole

3.2.2.2 Bit 6

Bit 6 is reserved. It will always be read as a logic ‘0’ value.

3.2.2.3 Axis of Sensitivity Bit (AXIS)

The AXIS bit indicates direction of sensitivity

0 - Z-axis

1 - X-axis

3.2.2.4 Bit 4, Bit 3

Bit 4 and Bit 3 are reserved. They will always be read as a logic ‘0’ value.

3.2.2.5 Full-Scale Range Bits (RNG2 - RNG0)

These three bits define the calibrated range of the device as follows:

Table 3-4

RNG2	RNG1	RNG0	Range
0	0	0	Unused
0	0	1	20g
0	1	0	40g
0	1	1	50g
1	0	0	100g
1	0	1	150g
1	1	0	250g
1	1	1	Unused

3.2.3 Configuration Bytes

Two customer-programmable configuration bytes are assigned.

3.2.4 Device Configuration Byte 1 (DEVCFG1)

Table 3-5 Device Configuration Byte 1

Location		Bit Function							
Address	Register	7	6	5	4	3	2	1	0
$06	DEVCFG1	Customer Defined						ATT1	ATT0

Configuration Byte 1 contains three defined bit functions, plus five bits that can be programmed by the customer to designate any coding desired for packaging axis, model, etc.

3.2.5 Attribute Bits (AT1, AT0)

These bits may be assigned by the customer as desired. They are transmitted by MMA81XXEG/MMA82XXEG/MMA82XXTEG in response to Request Status, Disable Self-Test Stimulus or Enable Self-Test Stimulus commands, as described in Section 4.

3.2.6 Device Configuration Byte 2 (DEVCFG2)

Table 3-6 Device Configuration Byte 2

Location		Bit Function							
Address	Register	7	6	5	4	3	2	1	0
$07	DEVCFG2	LOCK2	PAR2	GLDE	DDIS	AD3	AD2	AD1	AD0

Configuration Byte 2 contains six bits that can be programmed by the customer to control device configuration, along with parity and lock bits for DEVCFG1 and DEVCFG2.

3.2.6.1 Customer Data Lock Bit (LOCK2)

The bits in configuration bytes 1 and 2 are frozen when the LOCK2 bit is programmed. The LOCK2 bit is not included in the parity check. Locking does not take effect after this bit is programmed until the device has been subsequently reset.

0 - Customer-programmed data area unlocked.

1 - Programming operations inhibited.

The DDIS bit is not affected by LOCK2 and may be programmed at any time.

3.2.6.2 Customer Data Parity Bit (PAR2)

The PAR2 parity bit is used for detecting changes in configuration bytes 1 and 2 along with registers REG-8 through REG-F (addresses $06 through $0F, inclusive). A fault condition is indicated if a change to parity-protected register data is detected. The PAR2 bit follows an “even” parity scheme (number of logical HIGH bits including parity bit is even).

If an internal parity error is detected, the device will respond to Read Acceleration Data commands with zero in the data field, as described in Section 4.5.4. The Status (S) bit will be set in either short word or long word responses to indicate the fault condition.

A parity fault may result from a bit failure within the OTP or the registers which store an image of the OTP during operation. In the latter case, power-on reset will clear the fault when the registers are re-loaded. A parity fault associated with the OTP array is a non-recoverable failure.

The parity status of customer programmed data is not monitored if the LOCK2 bit is not programmed to a logic ‘1’ state.

3.2.6.3 Ground Loss Detection Enable (GLDE)

When this bit is programmed to a logic ‘1’ value, ground loss errors will be reported if a ground fault condition is detected.

1 - Ground-loss detection circuitry enabled

0 - Ground-loss detection disabled.

3.2.6.4 Device Disable Bit (DDIS)

This bit may be programmed at any time, regardless of the state of LOCK2. This bit is intended to be programmed when a module has been determined by the DSI Bus Master to be defective. Programming this bit after LOCK2 has been set will cause the device to respond to short word Read Acceleration Data commands with a zero response. Acceleration results are not affected by this bit when long word Read Acceleration Data commands are executed, however the Status (S) bit will be set in the response.

1 - Device responds to Read Acceleration Data command with zero value

0 - Device responds normally to Read Acceleration Data command

3.2.6.5 Device Address (AD3 - AD0)

These bits define the pre-programmed DSI Bus device address.

3.3 OTP PROGRAMMING

Two different methods of programming the eighty customer defined bits are supported. In test mode, these may be programmed in the same manner as factory programmed OTP bits. Additionally, the Read Write NVM DSI bus command may be used. Test mode programming operations are described in Appendix A.3. Read Write NVM command operation is described in Section 4.6.3.

SECTION 4 PHYSICAL LAYER AND PROTOCOL

MMA81XXEG/MMA82XXEG/MMA82XXTEG family is compliant with the DSI Bus Standard, Version 2.0. MMA81XXEG/ MMA82XXEG/MMA82XXTEG is designed to be compatible with either DSI Version 2 or DSI Version 1.1 compliant bus masters.

4.1 DSI NETWORK PHYSICAL LAYER INTERFACE

Refer to **Section 3** of the DSI Bus Standard for information regarding the physical layer interface.

4.2 DSI NETWORK DATA LINK LAYER

Refer to **Section 4** of the DSI Bus Standard for information regarding the DSI network data link layer interface. Both standard and enhanced command structures are supported for short word and long word commands.

4.3 DSI BUS COMMANDS

DSI Bus Commands which are recognized by MMA81XXEG and the MMA82XXEG/MMA82XXTEG are summarized in Table 4-1. Detailed descriptions of each supported command are described in subsequent sections of this document. If a CRC error is detected, or a reserved or unimplemented command is received, the device will not respond.

Following all messages, MMA81XXEG and the MMA82XXEG/MMA82XXTEG disregards the DSI bus voltage level for approximately 18.5 μs. Within this time, all supported commands except Initialization and Reverse Initialization are guaranteed to be executed and the device will be ready for the next message. When the bus voltage falls below the signal high logic level (see Section 5) after the 18.5 μs period has elapsed, the device will respond as appropriate to a command sent to it in the previous message. Exactly one response is attempted; if a noise spike or corrupted transfer occurs, the response is not retried.

If an Initialization or Reverse Initialization command is executed and the Bus Switch (BS) bit is set, MMA81XXEG, MMA82XXEG and MMA82XXTEG will disregard the bus voltage level for a nominal period of 180 μs. This interval allows for the bus voltage to recover following closure of the bus switch, while the hold capacitor of a downstream slave charges.

Table 4-1 DSI Bus Command Summary

Command						Size	Data							
Binary				Hex	Description									
C3	C2	C1	C0				D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	$0	Initialization	LW	NV	BS	B1	B0	PA3	PA2	PA1	PA0
0	0	0	1	$1	Request Status	SW	—	—	—	—	—	—	—	—
0	0	1	0	$2	Read Acceleration Data	SW	—	—	—	—	—	—	—	—
0	0	1	1	$3	Not Implemented	N/A	Not Applicable							
0	1	0	0	$4	Request ID Information	SW	—	—	—	—	—	—	—	—
0	1	0	1	$5	Not Implemented	N/A	Not Applicable							
0	1	1	0	$6	Not Implemented	N/A	Not Applicable							
0	1	1	1	$7	Clear	SW	—	—	—	—	—	—	—	—
1	0	0	0	$8	Not Implemented	N/A	Not Applicable							
1	0	0	1	$9	Read Write NVM	LW	RA3	RA2	RA1	RA0	RD3	RD2	RD1	RD0
1	0	1	0	$A	Format Control	LW	R/W	FA2	FA1	FA0	FD3	FD2	FD1	FD0
1	0	1	1	$B	Read Register Data	LW	0	0	0	0	RA3	RA2	RA1	RA0
1	1	0	0	$C	Disable Self-Test Stimulus	SW	—	—	—	—	—	—	—	—
1	1	0	1	$D	Activate Self-Test Stimulus	SW	—	—	—	—	—	—	—	—
1	1	1	0	$E	Reserved	N/A	Not Applicable							
1	1	1	1	$F	Reverse Initialization	LW	NV	BS	B1	B0	PA3	PA2	PA1	PA0

Legend:

BS: Bus Switch Control (0: open, 1: close)

NV: Nonvolatile memory control (1: program NVM)

PA3 - PA0: Device address assigned during Initialization or Reverse Initialization

RA3 - RA0: Internal user data register address

FA2 - FA0: Format register address

FD3 - FD0: Format register data content

4.4 COMMAND RESPONSE SUMMARIES

The device incorporates an analog-to-digital converter which translates the low-pass filtered acceleration signal to a 10-bit binary value. The 10-bit digital result is referred to as AD9 through AD0 in the response tables which follow.

4.4.1 Short Word Response Summary

Short word responses for all commands are summarized below. Detailed DSI command descriptions may be found in Section 4.5.

Table 4-2 Short-Word Response Summary

Command		Response							
Hex	**Description**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
$0	Initialization	Not Applicable							
$1	Request Status	NV	U	ST	BS	AT1	AT0	S	GF
$2	Read Acceleration Data	See Section 4.5.4							
$3	Not Implemented	No Response							
$4	Request ID Information	V2	V1	V0	0	0	1	0	0
$5	Not Implemented	No Response							
$6	Not Implemented	No Response							
$7	Clear	No Response							
$8	Not Implemented	No Response							
$9	Read/Write NVM	Not Valid							
$A	Format Control	Not Valid							
$B	Read Register Data	Not Valid							
$C	Disable Self-Test Stimulus	NV	U	ST	BS	AT1	AT0	S	GF
$D	Activate Self-Test Stimulus	NV	U	ST	BS	AT1	AT0	S	GF
$E	Reserved	No Response							
$F	Reverse Initialization	Not Valid							

Legend:

AT1 - AT0: Attribute codes (see Section 4.5.1.3)

NV: State of fuse program control bit

BS: State of Bus Switch (0: open, 1: closed)

S: Accelerometer status flag (1: internal error)

ST: Self-Test flag (1: self-test active)

U - Undervoltage condition

V2 - V0: Version ID

4.4.2 Long Word Response Summary

Long word responses for all commands are summarized below. Detailed DSI command descriptions may be found in Section 4.5.

Table 4-3 Long-Word Response Summary

Command		Response															
Hex	**Description**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
$0	Initialization	A3	A2	A1	A0	0	0	0	BF	NV	BS	B1	B0	PA3	PA2	PA1	PA0
$1	Request Status	A3	A2	A1	A0	0	0	0	0	NV	U	ST	BS	AT1	AT0	S	GF
$2	Read Acceleration Data	A3	A2	A1	A0	GF	S	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
$3	Not Implemented	No Response															
$4	Request ID Information	A3	A2	A1	A0	0	0	0	0	V2	V1	V0	0	0	1	0	0
$5	Not Implemented	No Response															
$6	Not Implemented	No Response															
$7	Clear	No Response															
$8	Not Implemented	No Response															
$9	Read/Write NVM	A3	A2	A1	A0	See Section 4.6.3											
$A	Format Control	A3	A2	A1	A0	0	1	1	0	R/W	FA2	FA1	FA0	FD3	FD2	FD1	FD0
$B	Read Register Data	A3	A2	A1	A0	RA3	RA2	RA1	RA0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
$C	Disable Self-Test Stimulus	A3	A2	A1	A0	0	0	0	0	NV	U	ST	BS	AT1	AT0	S	GF
$D	Activate Self-Test Stimulus	A3	A2	A1	A0	0	0	0	0	NV	U	ST	BS	AT1	AT0	S	GF
$E	Reserved	No Response															
$F	Reverse Initialization	A3	A2	A1	A0	0	0	0	BF	NV	BS	B1	B0	PA3	PA2	PA1	PA0

Legend:

A3 - A0: Device address

AD9 - AD0: 10-bit acceleration data result

AT1 - AT0: Attribute codes (see Section 4.5.1.3)

BF: Bus Fault flag (1: bus fault)

BS: State of Bus Switch (0: open, 1: closed)

FA2 - FA0: Format register address

FD3 - FD0: Format register data content

GF: Ground fault detected

NV: State of fuse program control bit

PA3 - PA0: Device address assigned during Initialization/Reverse Initialization

RA3 - RA 0: Internal user data register address

RD7 - RD0: Internal user data register contents

R/W: Read/Write flag for Format Control Register access

S: Accelerometer Status Flag (1: internal error)

ST: Self-Test Flag (1: self-test active)

U - Undervoltage condition

V2 - V0: Version ID

4.5 DSI COMMAND DETAIL

Detailed descriptions of command formats and responses are provided in this section.

4.5.1 DSI COMMAND AND RESPONSE BIT DESCRIPTIONS

The following abbreviations are used in the descriptions of DSI commands and responses.

4.5.1.1 DSI Device Address - (A3 - A0)

DSI device address. This address will be set to the pre-programmed device address following reset, or zero if no pre-programmed address has been assigned. If zero, the device address may be assigned during initialization or reverse initialization.

4.5.1.2 Acceleration Data - (AD9 - AD0)

Ten-bit acceleration result produced by the device. This value is returned by the Read Acceleration Data command, described in Section 4.5.4.

4.5.1.3 Attribute Code Bits (AT1, AT0)

These bits indicate the contents of DEVCFG1 bits 1 and 0 in response to a Request Status, Activate Self-Test Stimulus or Disable Self-Test Stimulus command.

Table 4-4 Attribute Code Bit Assignments

LOCK2	DEVGFG1[1]	DEVGFG1[0]	AT1	AT0
0	X	X	1	0
1	0	0	0	0
	0	1	0	1
	1	0	1	0
	1	1	1	1

4.5.1.4 Bank Select (B1, B0)

These bits are assigned during initialization or reverse initialization to select specific fields within the customer accessible data registers. Bank selection affects Read/Write NVM command operation. Invalid combinations of B1 and B0 result in no response from the device to the associated initialization or reverse initialization command.

Refer to Section 4.6.3 for further details regarding register programming and bank selection.

4.5.1.5 Bus Fault Bit (BF)

This bit indicates the success or failure of the bus test which is performed as part of an Initialization or Reverse Initialization command.

1 - Bus fault detected

0 - Bus test passed

4.5.1.6 Bus Switch Control/Status Bit (BS)

This bit controls the state of the bus switch during an Initialization or Reverse Initialization command. It also indicates the state of the bus switch in response to the Initialization, Request Status, Disable Self-Test Stimulus, Activate Self-Test Stimulus and Reverse Initialization commands.

1 - Close bus switch, or bus switch closed

0 - Leave bus switch open, or bus switch opened

4.5.1.7 Format Control Register Address (FA2 - FA0)

This three-bit field selects one of eight format control registers. Format control registers are described in Section 4.6.4.3.

4.5.1.8 Format Register Data (FD3 - FD0)

Contents of a format control register. This is the data to be written to the register by a Format Control command, or the contents read from the register in response to a Format Control command.

4.5.1.9 Ground Fault Flag (GF)

If ground loss detection has been enabled and a ground fault condition is detected, this bit will be set in the response to Request Status, Read Acceleration Data, Disable Self-Test Stimulus or Activate Self-Test Stimulus commands. If ground loss detection is not enabled, this bit will always be read as a logic ‘0’ value.

1 - Ground fault condition detected

0 - Ground connection within specified limits, or ground loss detection disabled.

4.5.1.10 Nonvolatile Memory Program Control Bit (NV)

This bit enables programming of customer-programmed OTP locations when set during an Initialization or Reverse Initialization command. Data to be programmed are transferred to the device during subsequent Read Write NVM commands.

1 - Enable OTP programming

0 - OTP programming circuitry disabled

4.5.1.11 Assigned Device Address (PA3 - PA0)

This field contains the device address to be assigned during an Initialization or Reverse Initialization command. The address assigned is reported by the device in response to the Initialization or Reverse Initialization command.

4.5.1.12 Register Address (RA3 - RA0)

This field determines the register associated with a Read Write NVM or Read Register Data command. The two Bank Select bits (B1, B0) are used to additionally specify a nibble or bit when a Read Write NVM command is executed.

4.5.1.13 Register Data (RD7 - RD0)

RD3 - RD0 contain data to be written to an OTP location when a Read Write NVM command is executed if the NV bit is set. RD3 - RD0 contain the data read from the selected register in response to a Read Write NVM command if the NV bit is cleared. RD7 - RD0 indicate the contents of the selected register in response to a Read Register Data command.

4.5.1.14 Format Control Register Read/Write Bit (R/W)

This bit controls the operation performed by a Format Control command.

1 - Write Format Control register selected by FA2 - FA0

0 - Read Format Control register unless global command

4.5.1.15 Accelerometer Status Flag (S)

This bit provides a cumulative indication of the various error conditions which are monitored by the device.

1 - Either one or more error conditions have been detected and/or the internal Self-Test stimulus circuitry is active

0 - No error condition has been detected

The following conditions will cause the status flag to be set:

*Internal Self-Test stimulus circuitry is active

OTP array parity fault

OTP fuse threshold fault (partially-programmed fuse)

Transient undervoltage condition

Ground fault (if GLDE bit in DEVCFG2 is set)

4.5.1.16 Self-Test State (ST)

This bit indicates whether internal self-test stimulus circuitry is active in response to Request Status, Disable Self-Test Stimulus and Activate Self-Test Stimulus commands.

1 - Self-Test stimulus active

0 - Self-Test stimulus disabled

4.5.1.17 Undervoltage Flag (U)

This flag is set if the voltage at HCAP is below a specified threshold. Refer to Section 1.3.1 and Section 5 for further details.

4.5.2 Initialization Command

The initialization command conforms to the description provided in **Section 6.2.1** of the DSI Bus Standard, Version 2.0. At power-up the device is fully compliant with the DSI 1.1 protocol. The initialization command must be transmitted as a DSI 1.1 compliant long command structure. Features of the DSI 2.0 protocol can not be accessed until a valid DSI 1.1 compliant initialization sequence is performed and the enhanced mode format registers are properly configured.

Table 4-5 Initialization Command Structure

Data								Address				Command				CRC
D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	
NV	BS	B1	B0	PA3	PA2	PA1	PA0	A3	A2	A1	A0	0	0	0	0	4 bits

Figure 4-1 illustrates the sequence of operations performed following negation of internal Power-On Reset (POR) and execution of a DSI Initialization command. Initialization commands are recognized only at BUSIN. The BUSOUT node is tested for a bus short to battery high voltage condition, and the Bus Fault (BF) flag set if an error condition is detected. If no bus fault condition is detected and the BS bit is set in the command structure, the bus switch will be closed. If the BS bit is set, the DSI bus voltage level is disregarded for approximately 180 μs following initialization to allow the hold capacitor on a downstream slave to charge.

If the device has been pre-programmed, PA3 - PA0 and A3 - A0 must match the pre-programmed address. If no device address has been previously programmed into the OTP array, PA3 - PA0 contain the device address, while A3 - A0 must be zero. If any addressing condition is not met, the device address is not assigned, the bus switch will remain open and the device will not respond to the Initialization command.

Table 4-6 Initialization Command Response

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	0	0	0	BF	NV	BS	B1	B0	A3	A2	A1	A0	4 bits

In the response, bits D15 - D12 and D3 - D0 will contain the device address. If the device was unprogrammed when the initialization command was issued, the device address is assigned as the command executes. Both fields will contain the value PA3 - PA0 to indicate successful device address assignment.

Initialization or reverse initialization commands which attempt to assign device address zero are ignored.

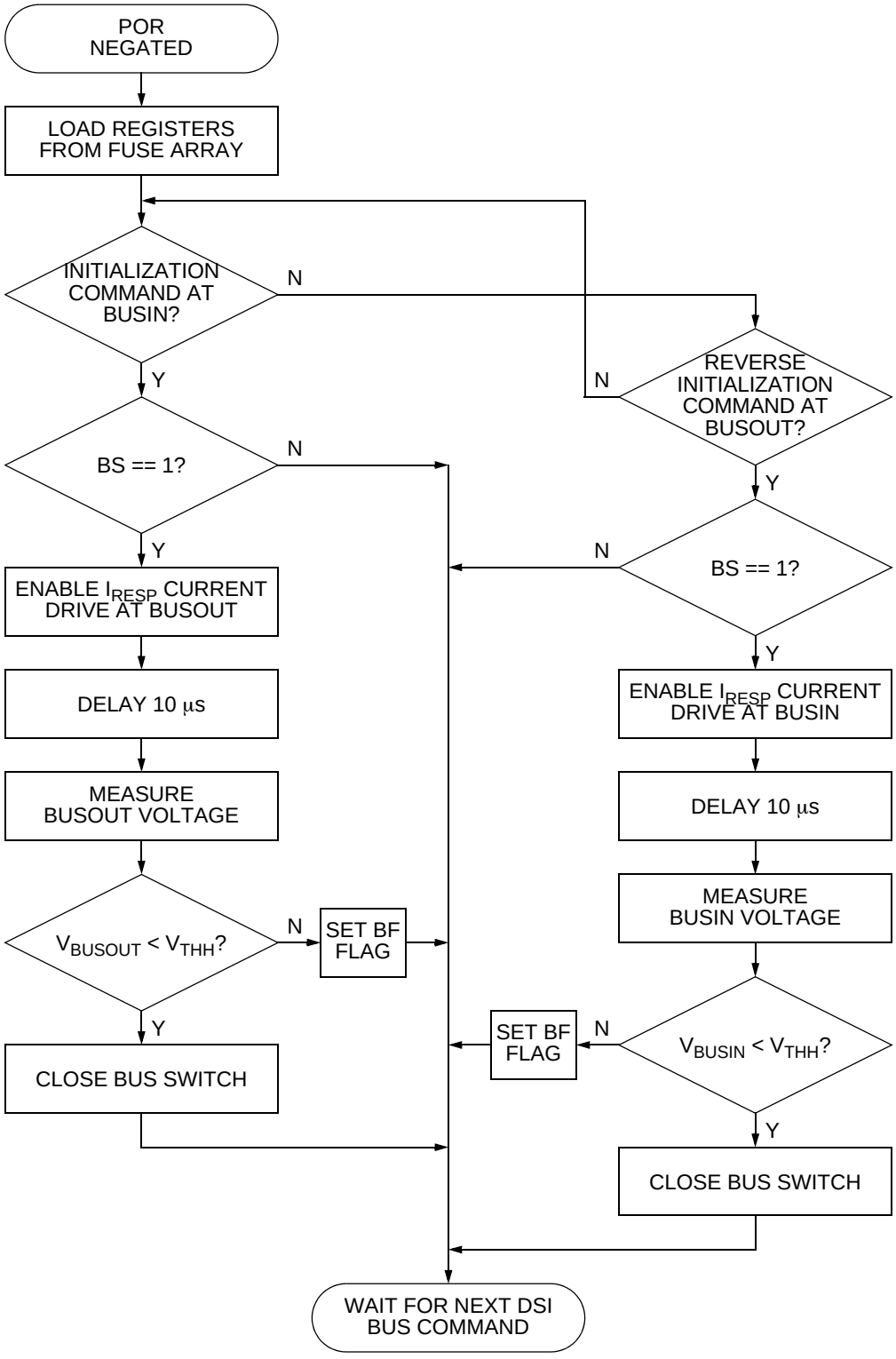


Figure 4-1. Initialization Sequence

4.5.3 Request Status Command

The Request Status command may be transmitted as either a DSI long command structure or a DSI short command structure of any length. The data field in the command structure is ignored but is included in the CRC calculation. No action is taken if this command is sent to the DSI Global Device Address.

Table 4-1 Request Status Command Structure

Address				Command				CRC
A3	A2	A1	A0	C3	C2	C1	C0	
A3	A2	A1	A0	0	0	0	1	0 to 8 bits

Table 4-2 Short Response Structure - Request Status Command

Response Length	Response														
	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8								NV	U	ST	BS	AT1	AT0	S	GF
9							0								
10						0									
11					0										
12				0											
13			0												
14		0													
15	0														

Table 4-3 Long Response Structure - Request Status Command

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	0	0	0	0	NV	U	ST	BS	AT1	AT0	S	GF	0 to 8 bits

4.5.4 Read Acceleration Data Command

The Read Acceleration Data command may be transmitted as either a DSI long command structure or a DSI short command structure of any length. The data field in the command structure is ignored but is included in the CRC calculation. No action is taken if this command is sent to the DSI Global Device Address.

Table 4-4 Read Acceleration Data Command Structure

Address				Command				CRC
A3	A2	A1	A0	C3	C2	C1	C0	
A3	A2	A1	A0	0	0	1	0	0 to 8 bits

Table 4-5 Short Response Structure - Read Acceleration Data Command

Response Length	Response														
	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8								AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
9							AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1

Table 4-5 Short Response Structure - Read Acceleration Data Command

Response Length	Response														
	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
10						AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
11					S										
12				GF											
13			ST												
14		DEVCFG1[0]													
15	DEVCFG1[1]														

Table 4-6 Long Response Structure - Read Acceleration Data Command

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	GF	S	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0 to 8 bits

Data returned in response to a Read Acceleration Data command varies, as illustrated in Table 4-5 and Table 4-6. The result is also affected by the state of the self-test circuitry and internal parity. If the self-test circuitry is enabled, the ST bit will be set in data bit D12 of a short word response. If a transient undervoltage condition, parity fault, ground fault or device disable condition exists, the reserved data value of zero will be reported in response to a short word command structure to indicate that a fault condition has been detected. The data value is not affected by a fault condition when a long word response is reported, however the S and GF bits will be set as appropriate.

If the self-test circuitry is active, acceleration data is reported regardless of parity faults. The Status (S) bit will be set in either short word or long word responses if a parity fault is detected.

4.5.4.1 ACCELERATION DATA REPRESENTATION

Acceleration values may be determined from the 10-bit digital output (DV) as follows:

$a = sensitivity \times (DV - 512)$

Sensitivity is determined by nominal full-scale range (FSR), linear range of digital values and a scaling factor to compensate for sensitivity error.

The linear range of digital values for MMA81XXEG/MMA82XXEG/MMA82XXTEG is 1 to 1023. The digital value of 0 is reserved as an error
indicator.

For the linear ranges of digital values indicated, the nominal value of 1 LSB for each full-scale range is shown in the table below.

Table 4-7 Nominal Sensitivity (10-bit data)

Full-Scale Range (g)	Nominal Sensitivity (g/digit)
250	0.61
150	0.366
100	0.244
50	0.122
40	0.0976
20	0.0488

4.6 ACCELERATION MEASUREMENT TIMING

Upon verification of the CRC associated with a Read Acceleration Data command, MMA81XXEG/MMA82XXEG/MMA82XXTEG initiates an analog-to-digital conversion. The conversion occurs during the inter frame separation (IFS) and involves a delay during which the BUSIN line is allowed to stabilize, a sample period and finally the translation of the analog signal level to a digital result.

4.6.1 Request ID Information Command

The Request ID Information command may be transmitted as either a DSI long command structure or a DSI short command structure of any length. The data field in the command structure is ignored but is included in the CRC calculation. No action is taken by MMA81XXEG/MMA82XXEG/MMA82XXTEG if this command is sent to the DSI Global Device Address.

Table 4-8 Request ID Information Command Structure

Address				Command				CRC
A3	A2	A1	A0	C3	C2	C1	C0	
A3	A2	A1	A0	0	1	0	0	0 to 8 bits

Table 4-9 Short Response Structure - Request ID Information Command

Response Length	Response														
	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8								V2	V1	V0	0	0	1	0	0
9							0								
10						0									
11					0										
12				0											
13			0												
14		0													
15	0														

Table 4-10 Long Response Structure - Request ID Information Command

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	0	0	0	0	V2	V1	V0	0	0	1	0	0	0 to 8 bits

4.6.2 Clear Command

The Clear command may be transmitted as either a DSI long command structure or a DSI short command structure of any length. The data field in the command structure is ignored but is included in the CRC calculation.

Table 4-11 Clear Command Structure

Address				Command				CRC
A3	A2	A1	A0	C3	C2	C1	C0	
A3	A2	A1	A0	0	1	1	1	0 to 8 bits

When a Clear Command is successfully decoded and the address field matches either the assigned device address or the DSI Global Device Address, the bus switch is opened and the device undergoes a full reset operation.

There is no response to the Clear Command.

4.6.3 Read/Write NVM Command

The Read/Write NVM command must be transmitted as a DSI long command structure. No action is taken by MMA81XXEG/ MMA82XXEG/MMA82XXTEG if this command is sent to the DSI Global Device Address.

Table 4-12 Read Write NVM Command Structure

Data								Address				Command				CRC
D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	
RA3	RA2	RA1	RA0	RD3	RD2	RD1	RD0	A3	A2	A1	A0	1	0	0	1	0 to 8 bits

Table 4-13 Long Response Structure - Read/Write NVM Command (NV = 1)

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	RA3	RA2	RA1	RA0	1	1	B1	B0	RD3	RD2	RD1	RD0	0 to 8 bits

Table 4-14 Long Response Structure - Read/Write NVM Command (NV = 0)

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	0	0	0	0	1	1	1	1	A3	A2	A1	A0	0 to 8 bits

There is no response if the Read/Write NVM Command is received within a DSI short command structure.

OTP data are accessed by fields, where a field is a combination of register address (RA3 - RA0) and bank select (B1, B0) bits. Bank select bits are assigned during an Initialization or Reverse Initialization command. Individual bits with predefined functions (the upper four bits of DEVCFG2) each have their own field address. The remaining OTP data are grouped into four-bit fields. Field addresses are shown in Table 4-15.

The structure of the OTP array results in data being programmed in 16-bit groups. DEVCFG1 and DEVCFG2 are in the same group. As a result, a non-zero device address assigned during Initialization or Reverse Initialization will be permanently programmed into the OTP array when any field within the two device configuration bytes is programmed.

To avoid programming a non-zero device address, ensure that device address 0 is assigned during Initialization or Reverse Initialization before programming any other bit(s) in DEVCFG1 or DEVCFG2.

OTP programming operations occur when the Read/Write NVM command is executed after the NV bit has been set during a preceding Initialization or Reverse Initialization command.

The minimum DSI Bus idle voltage must exceed 14 V when programming the OTP array.

When this command is executed while the NV bit is cleared, the DSI device address will be returned regardless of the state of the register address and bank select bits. The Read Register Data command (described in Section 4.6.5) may be used to access the full range of customer accessible data.

Table 4-15 OTP Field Assignments

Register Address				Bank Select		Register	Definition
RA3	RA2	RA1	RA0	B1	B0		
0	1	1	0	0	1	DEVCFG1[3:0]	User Defined
				1	0	DEVCFG1[7:4]	
0	1	1	1	0	0	DEVCFG2[7]	LOCK2
				0	1	DEVCFG2[3:0]	DSI Bus Device Address
				1	0	DEVCFG2[5]	GLDE
				1	1	DEVCFG2[6]	PAR2
1	0	0	0	0	1	REG8[3:0]	User Defined
				1	0	REG8[7:4]	
1	0	0	1	0	1	REG9[3:0]	User Defined
				1	0	REG9[7:4]	
1	0	1	0	0	1	REGA[3:0]	User Defined
				1	0	REGA[7:4]	
1	0	1	1	0	1	REGB[3:0]	User Defined
				1	0	REGB[7:4]	
1	1	0	0	0	1	REGC[3:0]	User Defined
				1	0	REGC[7:4]	
1	1	0	1	0	1	REGD[3:0]	User Defined
				1	0	REGD[7:4]	
1	1	1	0	0	1	REGE[3:0]	User Defined
				1	0	REGE[7:4]	
1	1	1	1	0	1	REGF[3:0]	User Defined
				1	0	REGF[7:4]	
				1	1	DEVCFG[4]	DDIS

4.6.4 Format Control Command

The Format Control command must be transmitted as a DSI long command structure. No change to the format registers occurs if the Format Control Command is received within a DSI short command structure.

If this command is sent to the DSI Global Device Address, the format registers are updated, however there is no response.

The Format Control command conforms to the DSI 2.0 Specification.

Table 4-16 Format Control Command Structure

Data								Address				Command				CRC
D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	
R/W	FA2	FA1	FA0	FD3	FD2	FD1	FD0	A3	A2	A1	A0	1	0	1	0	0 to 8 bits

4.6.4.1 Format Register Read/Write Control Bit (R/W)

1 - Write Format Control register selected by FA2 - FA0

0 - Read Format Control register unless global command

4.6.4.2 Format Control Register Selection (FA2 - FA0)

This three-bit field selects one of eight format control registers. Format control registers are described in Section 4.6.4.3.

Table 4-17 Long Response Structure - Format Control Command

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	0	1	1	0	R/W	FA2	FA1	FA0	FD3	FD2	FD1	FD0	0 to 8 bits

There is no response if the Format Control Command is received within a DSI short command structure.

4.6.4.3 Format Control Registers

The seven 4-bit format control registers defined in the DSI 2.0 Bus Specification are shown in Table 4-18 below. The default values assigned to each register following reset are indicated.

Table 4-18 Format Control Registers

Format Control Register					Default Value			
Name	Address							
	Decimal	FA2	FA1	FA0	FD3	FD2	FD1	FD0
CRC Polynomial - Low Nibble	0	0	0	0	0	0	0	1
CRC Polynomial - High Nibble	1	0	0	1	0	0	0	1
Seed - Low Nibble	2	0	1	0	1	0	1	0
Seed - High Nibble	3	0	1	1	0	0	0	0
CRC Length (0 to 8)	4	1	0	0	0	1	0	0
Short Word Data Length (8 to 15)	5	1	0	1	1	0	0	0
Reserved	6	1	1	0	0	0	0	0
Format Selection	7	1	1	1	0	0	0	0

The following restrictions apply to format control register operations, in accordance with the DSI 2.0 Bus Specification:

- Attempting to write a value greater than eight to the CRC Length Register will cause the write to be ignored. The contents of the register will remain unchanged.
- Attempting to write a value less than eight to the Short Word Data Length register will cause the write to be ignored. The contents of the register will remain unchanged.
- The contents of the Format Selection register determine whether standard DSI values or the values contained in the remaining format control registers will be used. The values contained in the remaining format control registers become effective when this register is successfully written to ‘1111’. If the register is currently cleared, and one of the data bits FD3 - FD0 is not received as a logic ‘1’, the data in the register will remain all zeroes and the device will continue to use standard DSI format settings. If the register bits FD3 - FD0 are all set and one of the bits is received as a logic ‘0’ value, the data in the register will remain ‘1111’ and the values contained in the remaining format control registers will continue to be used.

4.6.5 Read Register Data Command

The Read Register Data command must be transmitted as a DSI long command structure.

Table 4-19 Read Register Data Command Structure

Data								Address				Command				CRC
D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	
0	0	0	0	RA3	RA2	RA1	RA0	A3	A2	A1	A0	1	0	1	1	0 to 8 bits

Table 4-20 Long Response Structure - Read Register Data Command

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	RA3	RA2	RA1	RA0	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	0 to 8 bits

There is no response if the Read Register Data Command is received within a DSI short command structure or if this command is sent to the DSI Global Device Address.

The sixteen registers shown in Table 3-1 may be accessed using this command. Register address combinations are listed below.

Table 4-21 Read Register Data Command Address Assignment

RA3	RA2	RA1	RA0	Register
0	0	0	0	SN0
0	0	0	1	SN1
0	0	1	0	SN2
0	0	1	1	SN3
0	1	0	0	TYPE
0	1	0	1	Reserved
0	1	1	0	DEVCFG1
0	1	1	1	DEVCFG2
1	0	0	0	REG-8
1	0	0	1	REG-9
1	0	1	0	REG-A
1	0	1	1	REG-B
1	1	0	0	REG-C
1	1	0	1	REG-D
1	1	1	0	REG-E
1	1	1	1	REG-F

4.6.6 Disable Self-Test Stimulus Command

The Disable Self-Test Stimulus command may be transmitted as either a DSI long command structure or a DSI short command structure of any length. The data field in the command structure is ignored but is included in the CRC calculation.

Table 4-22 Disable Self-Test Stimulus Command Structure

Address				Command				CRC
A3	A2	A1	A0	C3	C2	C1	C0	
A3	A2	A1	A0	1	1	0	0	0 to 8 bits

Table 4-23 Short Response Structure - Disable Self-Test Stimulus Command

Response Length	Response														
	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8								NV	U	ST	BS	AT1	AT0	S	GF
9							0								
10						0									
11					0										
12				0											
13			0												
14		0													
15	0														

Table 4-24 Long Response Structure - Disable Self-Test Stimulus Command

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	0	0	0	0	NV	U	ST	BS	AT1	AT0	S	GF	0 to 8 bits

This command will execute if either the device specific address or DSI global device address (address $0) is provided. A secondary function, self-test lockout, is activated when two consecutive Disable Self-Test Stimulus commands are received. Following self-test lockout, the internal self-test circuitry is disabled until a Clear command is received or the device undergoes power-on reset.

4.6.7 Enable Self-Test Stimulus Command

The Enable Self-Test Stimulus command may be transmitted as either a DSI long command structure or a DSI short command structure of any length. The data field in the command structure is ignored but is included in the CRC calculation. No action is taken by the device if this command is sent to the DSI Global Device Address.

Table 4-25 Enable Self-Test Stimulus Command Structure

Address				Command				CRC
A3	A2	A1	A0	C3	C2	C1	C0	
A3	A2	A1	A0	1	1	0	1	0 to 8 bits

Table 4-26 Short Response Structure - Enable Self-Test Stimulus Command

Response Length	Response														
	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8								NV	U	ST	BS	AT1	AT0	S	GF
9							0								
10						0									
11					0										
12				0											
13			0												
14		0													
15	0														

Table 4-27 Long Response Structure - Enable Self-Test Stimulus Command

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	0	0	0	0	NV	U	ST	BS	AT1	AT0	S	GF	0 to 8 bits

If self-test locking has been activated, the ST bit will be cleared in the response from the device. Self-Test locking is described in Section 4.6.6.

4.6.8 Reverse Initialization Command

The reverse initialization command conforms to the description provided in Section 6.2.1 of the DSI Bus Standard, Version 2.0. At power-up the device is fully compliant with the DSI 1.1 protocol. The initialization command must be transmitted as a DSI 1.1 compliant long command structure. Features of the DSI 2.0 protocol can not be accessed until a valid DSI 1.1 compliant initialization sequence is performed and the enhanced mode format registers are properly configured.

Table 4-28 Reverse Initialization Command Structure

Data								Address				Command				CRC
D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0	C3	C2	C1	C0	
NV	BS	B1	B0	PA3	PA2	PA1	PA0	A3	A2	A1	A0	1	1	1	1	4 bits

Figure 4-1 illustrates the sequence of operations performed following negation of internal power-on reset (POR) and execution of a DSI Reverse Initialization command. Reverse Initialization commands are recognized only at BUSOUT. The BUSIN node is tested for a bus short to battery high voltage condition, and the bus fault (BF) flag set if an error condition is detected. If no bus fault condition is detected and the BS bit is set in the command structure, the bus switch will be closed.

If the device has been pre-programmed, PA3 - PA0 and A3 - A0 must match the pre-programmed address. If no device address has been previously programmed into the OTP array, PA3 - PA0 contain the device address, while A3 - A0 must be zero. If any addressing condition is not met, the device address is not assigned, the bus switch will remain open and the device will not respond to the Reverse Initialization command. If the BS bit is set, the DSI bus voltage level is disregarded for approximately 180 μs following reverse initialization to allow hold capacitors on downstream slaves to charge.

Table 4-29 Long Response Structure - Reverse Initialization Command

Data																CRC
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
A3	A2	A1	A0	0	0	0	BF	NV	BS	B1	B0	A3	A2	A1	A0	4 bits

In the response, bits D15 - D12 and D3 - D0 will contain the device address. If the device was unprogrammed when the reverse initialization command was issued, the device address is assigned as the command executes. Both fields will contain the value PA3 - PA0 to indicate successful device address assignment.

Initialization or reverse initialization commands which attempt to assign device address zero are ignored.

SECTION 5 PERFORMANCE SPECIFICATIONS

5.1 MAXIMUM RATINGS

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it. The device contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table below.

Table 5-1

Ref	Rating	Symbol	Value	Unit	
	Supply Voltages				
1	H_{CAP}	V_{HCAP}	-0.3 to +40	V	(3)
2	BUSIN, BUSOUT	V_{BUS}	-0.3 to +40	V	(3)
3	Voltage at Programming/Test Mode Entry pin	V_{PP}/TEST	-0.3 to +11	V	(3)
4	Voltage at C_{REG}, D_{IN}, CLK, C_{FIL}, D_{OUT}	V_{IN}	-0.3 to +3.0	V	(3)
5	Voltage at V_{GND}	V_{GND}	-0.3 to +3.0	V	(3)
	BUSIN, BUSOUT, BUSRTN and H_{CAP} Current				
6	Maximum duration 1 s	I_{IN}	400	mA	(3)
7	Continuous	I_{IN}	200	mA	(3)
8	Current Drain per Pin Excluding V_{SS}, BUSIN, BUSOUT, BUSRTN	I	±10	mA	(3)
	Acceleration (without hitting internal g-cell stops)				
9	Z-axis g-cell	g_{max}	±1400	g	(3)
10	X-axis g-cell (40g, 70g)	g_{max}	±950	g	(3)
11	X-axis g-cell (100g - 250g)	g_{max}	±2200	g	(3)
12	Powered Shock (six sides, 0.5 ms duration)	g_{pms}	±1500	g	(3)
13	Unpowered Shock (six sides, 0.5 ms duration)	g_{shock}	±2000	g	(3)
14	Drop Shock (to concrete surface)	h_{DROP}	1.2	m	(3)
	Electrostatic Discharge				
15	Human Body Model (HBM)	V_{ESD}	±2000	V	(3)
16	Charge Device Model (CDM)	V_{ESD}	±500	V	(3)
17	Machine Model (MM)	V_{ESD}	±200	V	(3)
	Temperature Range				
18	Storage	T_{stg}	-40 to +125	°C	(3)
19	Junction	T_J	-40 to +150	°C	(3)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.
4. (*) Indicates a customer critical characteristic or Freescale important characteristic.

5.2 THERMAL CHARACTERISTICS

Ref	Characteristic	Symbol	Min	Typ	Max	Units	
20	Thermal Resistance	θ_{JA}	—	—	85	°C/W	(3)
		θ_{JC}	—	—	46	°C/W	(3)

5.3 OPERATING RANGE

The operating ratings are the limits normally expected in the application and define the range of operation.

Ref	Characteristic	Symbol	Min	Typ	Max	Units	
	Supply Voltage (Note 9)		V_L		V_H		
21	V_{HCAP} (Note 5)	V_{HCAP}	6.3	—	30	V	(1)
22	BUSIN, BUSOUT	V_{BUS}	-0.3	—	30	V	(1)
	V_{HCAP} Undervoltage Detection (see Figure 5-1)						
23	Undervoltage Detection Threshold	V_{LVD}	—	—	6.2	V	(1)
24	V_{HCAP} Recovery Threshold	V_{LVR}	—	—	6.3	V	(1)
25	Hysteresis (V_{LVR} - V_{LVD})	V_{LVH}	—	100	—	mV	(3)
	C_{REG} Undervoltage Detection (see Figure 5-2)	V_{LVD}	—	2.25	—	V	(3)
26	Undervoltage Detection Threshold	V_{LVR}	—	2.35	—	V	(3)
27	C_{REG} Recovery Threshold	V_{LVH}	—	100	—	mV	(3)
28	Hysteresis (V_{LVR} - V_{LVD})						
29	Test Mode Activation Voltage	V_{TEST}	4.5	—	10	V	(3)
	Programming Voltage						
30	via SPI	V_{PP}/TEST	7.5	8.0	8.5	V	(3)
31	via DSI	V_{BUS}	14	—	30	V	(3)
32	OTP Programming Current	I_{PROG}	—	—	85	mA	(3)
	Operating Temperature Range		T_L		T_H		
33	Standard Temperature Range	T_A	-40	—	+125	°C	(6)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.
4. (*) Indicates a customer critical characteristic or Freescale important characteristic.
5. Minimum operating voltage may be reduced pending characterization.
6. Device fully characterized at +105 °C and +125 °C. Production units tested +105 °C, with operation at +125 °C guaranteed through correlation with characterization results.
9. Maximum voltage characterized. Minimum voltage tested 100% at final test. Maximum voltage tested 100% to 24 V at final test.

5.4 ELECTRICAL CHARACTERISTICS

The unit *digit* is defined to be 1 least significant bit (LSB) of the 10-bit digital value, or 1 LSB of the equivalent 8-bit value if explicitly stated.

$V_L \le (V_{BUS} - V_{SS}) \le V_H$, $V_L \le (V_{HCAP} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, unless otherwise specified.

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Ref	Characteristic		Symbol	Min	Typ	Max	Units	
	Digital Output Sensitivity							
34	20g Range	*	SENS	—	0.0488	—	g/digit	(7)
35	40g Range	*	SENS	—	0.0976	—	g/digit	(7)
36	50g Range	*	SENS	—	0.122	—	g/digit	(7)
37	100g Range	*	SENS	—	0.244	—	g/digit	(7)
38	150g Range	*	SENS	—	0.366	—	g/digit	(7)
39	250g Range	*	SENS	—	0.610	—	g/digit	(7)
	C_{FIL} Output Sensitivity (T_A = 25 °C)							
40	20g Range	*	SENS	—	20.1	—	mV/V/g	(3)
41	40g Range	*	SENS	—	10.0	—	mV/V/g	(3)
42	50g Range	*	SENS	—	8.02	—	mV/V/g	(3)
43	100g Range	*	SENS	—	4.01	—	mV/V/g	(3)
44	150g Range	*	SENS	—	2.67	—	mV/V/g	(3)
45	250g Range	*	SENS	—	1.60	—	mV/V/g	(3)
	Sensitivity Error							
46	T_A = 25 °C	*	ΔSENS	-5	0	+5	%	(1)
47	$T_L \le T_A \le T_H$	*	ΔSENS	-7	0	+7	%	(1)
	Offset (measured in 0g orientation)							
48	T_A = 25 °C (8-bit)	*	OFF_8	122	128	134	digit	(7)
49	$T_L \le T_A \le T_H$ (8-bit)	*	OFF_8	116	128	140	digit	(7)
50	T_A = 25 °C (10-bit)		OFF_{10}	488	512	536	digit	(1)
51	$T_L \le T_A \le T_H$ (10-bit)		OFF_{10}	464	512	560	digit	(1)
	Full-Scale Range, including sensitivity and offset errors							
52	20g Range		FSR	21.0	24.9	26.6	g	(3)
53	40g Range		FSR	42.0	49.9	53.4	g	(3)
54	50g Range		FSR	52.5	62.3	66.7	g	(3)
55	100g Range		FSR	105	124.7	133	g	(3)
56	150g Range		FSR	158	187	200	g	(3)
57	250g Range		FSR	263	312	334	g	(3)
	Range of Output							
58	Normal (10-bit)		RANGE	1	—	1023	digit	(3)
59	Normal (8-bit)		RANGE	1	—	255	digit	(3)
60	Fault		FAULT	—	0	—	digit	(8)
	Nonlinearity							
61	Measured at C_{FIL} output, T_A = 25 °C		NL_{OUT}	-1	0	+1	%	(3)
	Internal Voltage Regulator							
62	Output Voltage		V_{CREG}	2.37	2.5	2.63	V	(1)
63	Line regulation		REG_{LINE}	—	—	6	mV	(3)
64	Load regulation (I_{REG} < 6 mA)		REG_{LOAD}	0.45	—	2	mV/mA	(3)
	Ripple rejection							
65	(DC ≤ f_{RIPPLE} ≤ 10 kHz, C_{REG} ≥ 0.9 μF)		RR	60	—	—	dB	(3)
66	C_{REG} capacitance		C_{REG}	0.9	—	—	μF	(3)
67	Effective series resistance, C_{REG} capacitor		ESR	—	—	700	mΩ	(3)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.
4. (*) Indicates a customer critical characteristic or Freescale important characteristic.
7. Tested 100% at 10-bit output. 8-bit value verified via scan.
8. Functionality verified 100% via scan.

5.5 ELECTRICAL CHARACTERISTICS (continued)

$V_L \le (V_{BUS} - V_{SS}) \le V_H$, $V_L \le (V_{HCAP} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, unless otherwise specified.

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Ref	Characteristic		Symbol	Min	Typ	Max	Units	
	Input Voltage							
68	LOW (CLK,D_{IN})		V_{IL}	—	—	$0.3xV_{Creg}$	V	(3)
69	HIGH (CLK,D_{IN})		V_{IH}	$0.7xV_{Creg}$	—	—	V	(3)
	Output Voltage (I_{OUT} = 200 μA)							
70	LOW (D_{OUT})		V_{OL}	—	—	V_{SS}+ 0.1	V	(3)
71	HIGH (D_{OUT})		V_{OH}	V_{Creg}- 0.1	—	—	V	(3)
	Output Loading, C_{FIL} pin (Note 10)							
72	Resistance to V_{CREG}, V_{SS}		R_{LOAD}	50	—	—	kΩ	(3)
73	Capacitance to V_{CREG}, V_{SS}		C_{LOAD}	—	—	20	pF	(3)
74	Output voltage range		V_{OUT}	V_{SS} + 50 mV	—	V_{CREG}-50mV	V	(3)
75	Bus Switch Resistance	*	R_{SW}	—	4.0	8.0	Ω	(1)
76	Rectifier Forward Resistance	*	R_{FWD}	—	—	2.5	Ω	(3)
77	Rectifier Leakage Current	*	I_{RLKG}	—	—	100	μA	(1)
	BUSIN or BUSOUT to H_{CAP} Rectifier Voltage Drop (V_{BUS} = 26 V)							
78	I_{BUSIN} or I_{BUSOUT} = -15 mA	*	V_{RECT}	—	—	1.0	V	(3)
79	I_{BUSIN} or I_{BUSOUT} = -100 mA	*	V_{RECT}	—	—	1.2	V	(3)
	(VBUS = 7 V)							
80	I_{BUSIN} or I_{BUSOUT} = -15 mA		V_{RECT}	—	—	1.0	V	(1)
81	I_{BUSIN} or I_{BUSOUT} = -100 mA		V_{RECT}	—	—	1.2	V	(1)
	BUSIN + BUSOUT Bias Current	*						
82	V_{BUSIN} or V_{BUSOUT} = 8.0 V, V_{HCAP} = 9.0 V		I_{BIAS}	—	—	100	mA	(1)
83	V_{BUSIN} or V_{BUSOUT} = 0.5 V, V_{HCAP} = 24 V		I_{BIAS}	—	—	20	μA	(1)
	BUSIN and BUSOUT Logic Thresholds							
84	Signal Low	*	V_{THL}	2.7	3.0	3.3	V	(1)
85	Signal High	*	V_{THH}	5.4	6.0	6.6	V	(1)
	BUSIN and BUSOUT Hysteresis							
86	Signal	*	V_{HYSS}	30	—	90	mV	(3)
87	Frame	*	V_{HYSF}	100	—	300	mV	(3)
	BUSIN + BUSOUT Response Current	*						
88	V_{BUSIN} and/or V_{BUSOUT} = 4.0 V		I_{RESP}	9.9	11	12.1	mA	(1)
89	Quiescent Current	*	I_Q	—	—	7.5	mA	(1)
90	Internal pull-down resistance CLK		R_{PD}	20	60	100	kΩ	(2)
91	Internal pull-down resistance V_{PP}/TEST		R_{PD}		437		kΩ	(2)
	GND Loss Detect (with external 3 kΩ resistor)							
92	Measurement Current		I_{GNDETC}	309	340	371	μA	(1)
93	Detection Resistance		$R_{GNDDETC}$	1	—	10	kΩ	(1)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.
4. (*) Indicates a customer critical characteristic or Freescale important characteristic.
10. The external circuit configuration shown in Section 1.3.6 is recommended.

5.6 ELECTRICAL CHARACTERISTICS (continued)

$V_L \le (V_{BUS} - V_{SS}) \le V_H$, $V_L \le (V_{HCAP} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, unless otherwise specified.

.

Ref	Characteristic		Symbol	Min	Typ	Max	Units	
	Total Noise (see Figure 5-3)							
	400 Hz, 4-pole filter, 20g range							
94	RMS, 100 samples		n_{RMS}	—	—	2	digit	(3)
95	P-P, 100 samples		n_{P-P}	—	—	8	digit	(3)
	180 Hz, 2-pole filter, 20g range							
96	RMS, 100 samples		n_{RMS}	—	—	2	digit	(3)
97	P-P, 100 samples		n_{P-P}	—	—	7	digit	(3)
	Cross-Axis Sensitivity							
98	X-axis, X-axis to Y-axis		V_{XY}	-5	—	+5	%	(3)
99	X-axis, X-axis to Z-axis		V_{XZ}	-5	—	+5	%	(3)
100	Y-axis, Y-axis to X-axis		V_{YX}	-5	—	+5	%	(3)
101	Y-axis, Y-axis to Z-axis		V_{YZ}	-5	—	+5	%	(3)
	Analog to digital converter							
102	Relative accuracy		INL	-2	—	+2	digit	(3)
103	Differential nonlinearity		DNL	-1	—	+1	digit	(3)
104	Gain error		GAINERR	-1	—	+1	%FSR	(2)
105	Offset error ($V_{IN} = V_{CREG}/2$)		OFST	-3	—	+3	digit	(3)
106	Noise (RMS, 100 samples)		n_{RMS}	-1	—	+1	digit	(3)
107	Noise (peak)		n_{P-P}	-3	—	+3	digit	(3)
	Deflection (Self-Test Output - Offset, average of 30 samples, measured in 0g orientation, T_A = 25° C)							
108	X-axis, 20g Range	*	ΔDFLCT	—	246	—	digit	(7)
109	X-axis, 40g Range	*	ΔDFLCT	—	123	—	digit	(7)
110	X-axis, 50g Range	*	ΔDFLCT	—	98	—	digit	(7)
111	X-axis, 100g Range	*	ΔDFLCT	—	49	—	digit	(7)
112	X-axis, 150g Range	*	DDFLCT	—	82	—	digit	(7)
113	X-axis, 250g Range	*	DDFLCT	—	49	—	digit	(7)
114	Z-axis, 40g Range	*	ΔDFLCT	—	307	—	digit	(7)
115	Z-axis, 100g Range	*	ΔDFLCT	—	299	—	digit	(7)
116	Z-axis, 150g Range	*	ΔDFLCT	—	205	—	digit	(7)
117	Z-axis, 250g Range	*	ΔDFLCT	—	123	—	digit	(7)
118	Self-Test deflection range, T_A = 25 °C, measured in 0g orientation		ΔDFLCT	-10	—	+10	%	(1)
119	Self-Test deflection range, $T_L \le T_A \le T_H$, measured in 0g orientation		ΔDFLCT	-20	—	+20	%	(1)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.
4. (*) Indicates a customer critical characteristic or Freescale important characteristic.
7. Tested 100% at 10-bit output. 8-bit value verified via scan.

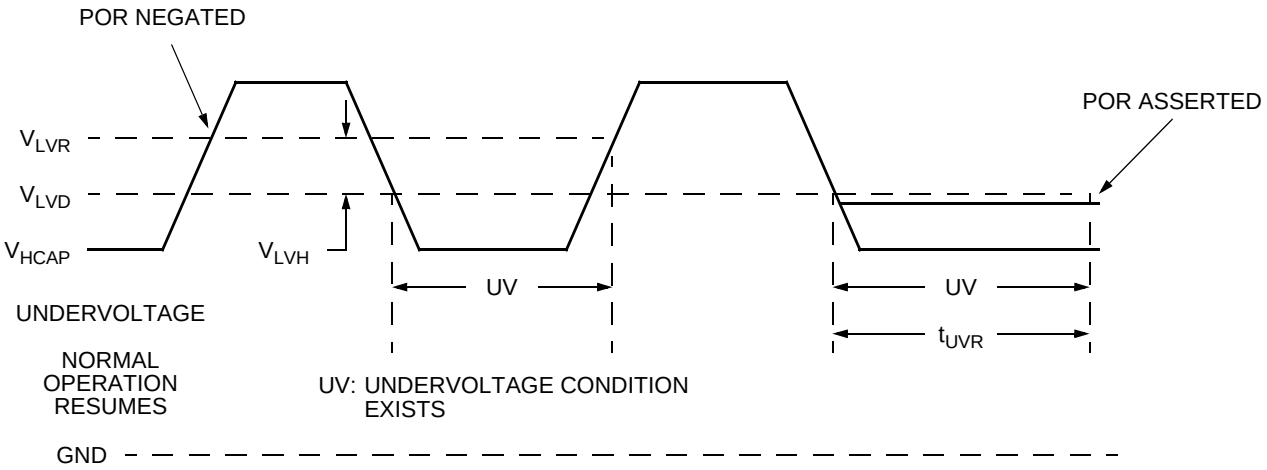


Figure 5-1. V_{HCAP} Undervoltage Detection

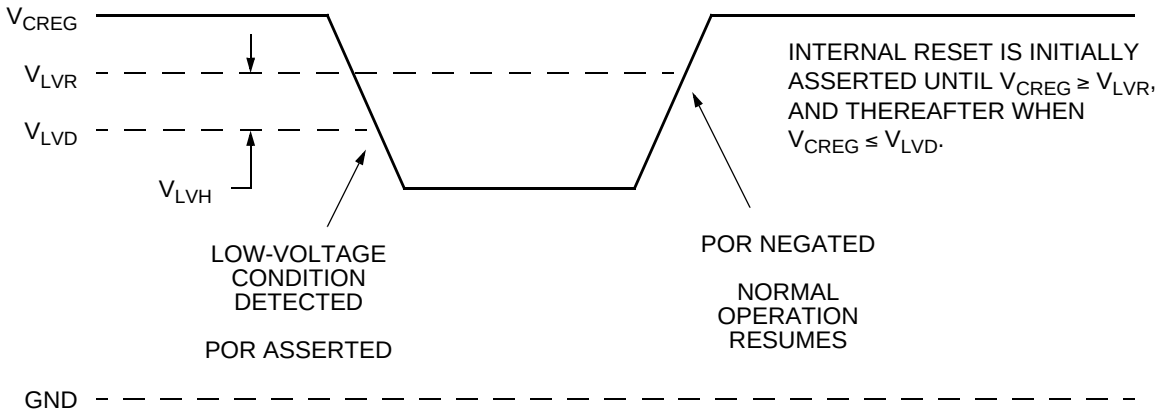


Figure 5-2. V_{CREG} Undervoltage Detection

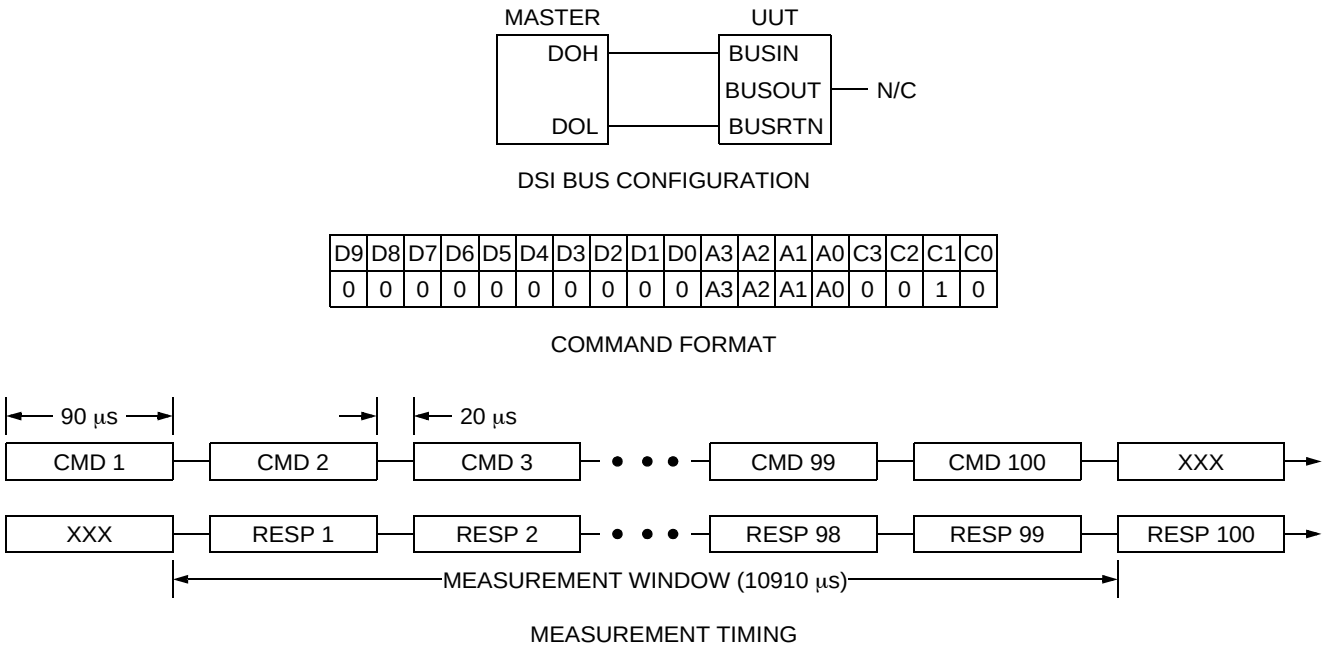


Figure 5-3. Total Noise Measurement Conditions

5.7 CONTROL TIMING

$V_L \le (V_{BUS} - V_{SS}) \le V_H$, $V_L \le (V_{HCAP} - V_{SS}) \le V_H$,$T_L \le T_A \le T_H$, unless otherwise specified.

Ref	Characteristic	Symbol	Min	Typ	Max	Units	
120	VHCAP Undervoltage Reset Period (see Figure 5-1) $V_{HCAP} < V_{RA}$ to POR assertion	t_{UVR}	0.95	1.0	1.05	ms	(8)
	Analog to digital converter (see Figure 5-4)						
121	Sample time	t_{SAMPLE}	4.28	4.5	4.73	µs	(8)
122	Conversion time	$t_{CONVERT}$	7.13	7.5	7.88	µs	(8)
123	Delay following bus idle	t_{DELAY}	2.85	3.0	3.15	µs	(8)
	BUSIN and BUSOUT response current transition						
124	1.0 mA to 9.0 mA, 9.0 to 1.0 mA	t_{ITR}	4.5	—	7.5	mA/µs	(3)
125	Initialization to Bus Switch Closing	t_{BS}	89	—	138	µs	(3)
126	Signal Bit Transition Time	t_{BIT}	5	—	200	µs	(3)
	Loss of Signal Reset Time						
127	Maximum time below frame threshold	t_{TO}	—	—	10	ms	(8)
	BUSIN or BUSOUT Timing to Response Current						
128	BUSIN or BUSOUT ≤ V_{THL} to I_{BUS} ≥ 7 mA	t_{RSPH}	—	—	3.0	µs	(3)
129	BUSIN or BUSOUT ≤ V_{THH} to I_{BUS} ≤ 5 mA	t_{RSPL}	—	—	3.0	µs	(3)
	Interframe Separation Time (see Figure 5-5)						
130	Following Read Write NVM Command	t_{IFS}	2	—	—	ms	(3)
	Following Initialization or Reverse Initialization						
131	BS = 1	t_{IFS}	200	—	—	µs	(3)
132	BS = 0	t_{IFS}	20	—	—	µs	(3)
133	Following other DSI bus commands	t_{IFS}	20	—	—	µs	(3)
	Low Pass Filter						
134	(4-pole, -3 db Rolloff Frequency)	BW_{OUT}	360	400	440	Hz	(1)
135	(2-pole, -3 db Rolloff Frequency)	BW_{OUT}	162	180	198	Hz	(1)
	Ground Loss Detection Filter Time		—		—		
136	Cycles of f_{OSC}	t_{GNDETC}		16384		cycles	(8)
137	Time	t_{GNDETC}		4.096		ms	(8)
	Reset Recovery Time						
138	POR negated to Initialization Command	t_{RESET}	—	—	100	µs	(8)
139	POR negated to 180 Hz Data Valid	t_{RESET}	—	5.3	—	ms	(3)
140	POR negated to 400 Hz Data Valid	t_{RESET}	—	2.4	—	ms	(3)
141	Internal Oscillator Frequency	f_{OSC}	3.80	4.0	4.20	MHz	(1)
	Logic Duty Cycle						
142	Logic ‘0’ *	D_{CL}	10	33	40	%	(8)
143	Logic ‘1’ *	D_{CH}	60	67	90	%	(8)
144	OTP Programming, SPI program control	t_{PROG}	—	—	2	ms	(8)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.
4. (*) Indicates a customer critical characteristic or Freescale important characteristics.
8. Functionality verified 100% via scan. Timing is directly determined by internal oscillator frequency.

5.8 CONTROL TIMING (continued)

$V_L \le (V_{BUS} - V_{SS}) \le V_H$, $V_L \le (V_{HCAP} - V_{SS}) \le V_H$, $T_L \le T_A \le T_H$, unless otherwise specified.

Ref	Characteristic	Symbol	Min	Typ	Max	Units	
	SPI Timing (see Figure 5-6)						
145	CLK period	t_{CLK}	500	—	—	ns	(3)
146	D_{IN} to CLK setup	t_{DC}	50	—	—	ns	(3)
147	CLK to D_{IN} hold	t_{CDIN}	50	—	—	ns	(3)
148	CLK to D_{OUT}	t_{CDOUT}	—	—	20	ns	(3)
	Sensing Element Resonant Frequency						
149	Z-axis g-cell	f_{GCELL}	—	22.0	—	kHz	(3)
150	X-axis medium-g g-cell (20-50g)	f_{GCELL}	11.2	12.8	15.3	kHz	(3)
151	X-axis high-g g-cell (100-250g)	f_{GCELL}	18.0	20.6	24.2	kHz	(3)
	Sensing Element Rolloff Frequency (-3 db)						
152	Z-axis g-cell	BW_{GCELL}	—	1.58	—	kHz	(3)
153	X-axis medium-g g-cell (20-50g)	BW_{GCELL}	—	19	—	kHz	(3)
154	X-axis high-g g-cell (100-250g)	BW_{GCELL}	—	32	—	kHz	(3)
	Gain at Package Resonance						
155	Z-axis	Q	—	10	—	kHz	(3)
156	X-axis	Q	—	12	—	kHz	(3)
	Package Resonance						
157	Z-axis	f	—	45	—	kHz	(3)
158	X-axis	f	—	9.5	—	kHz	(3)

1. Parameters tested 100% at final test.
2. Parameters tested 100% at unit probe.
3. Verified by characterization, not tested in production.
4. (*) Indicates a customer critical characteristic or Freescale important characteristics.
8. Functionality verified 100% via scan. Timing is directly determined by internal oscillator frequency.

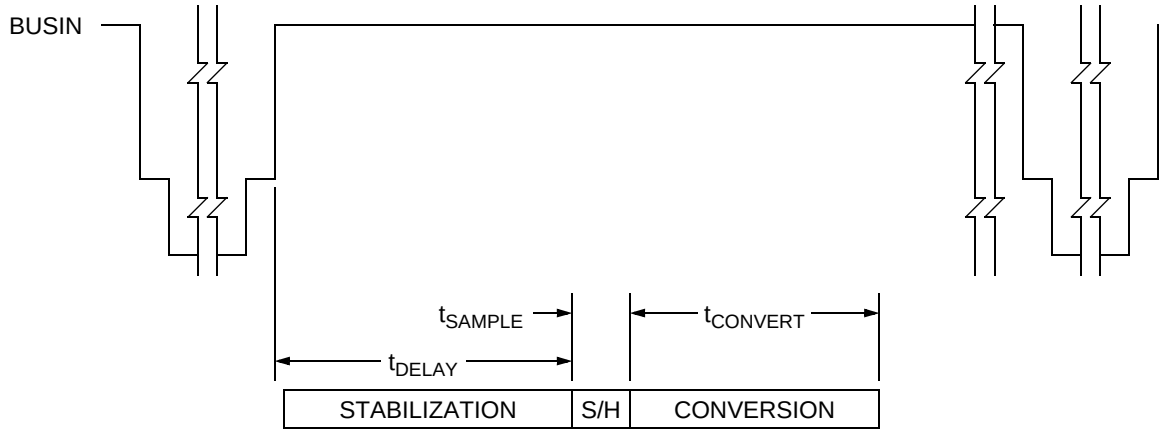


Figure 5-4. A-to-D Conversion Timing

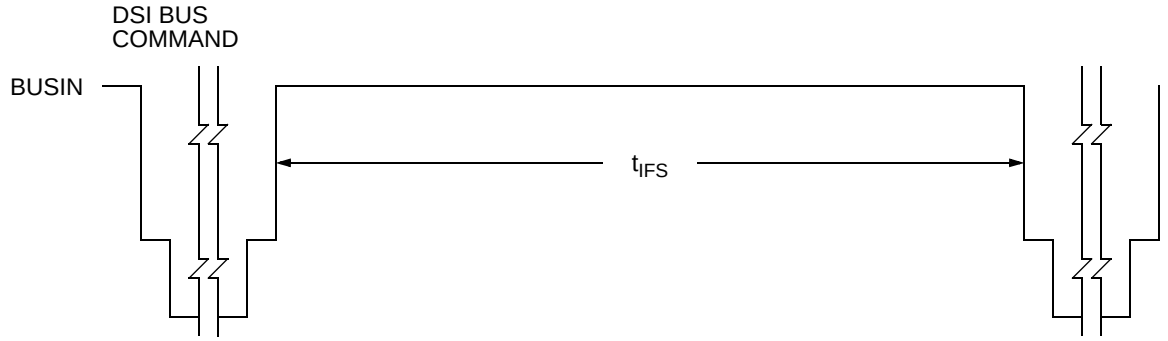


Figure 5-5. DSI Bus Interframe Timing

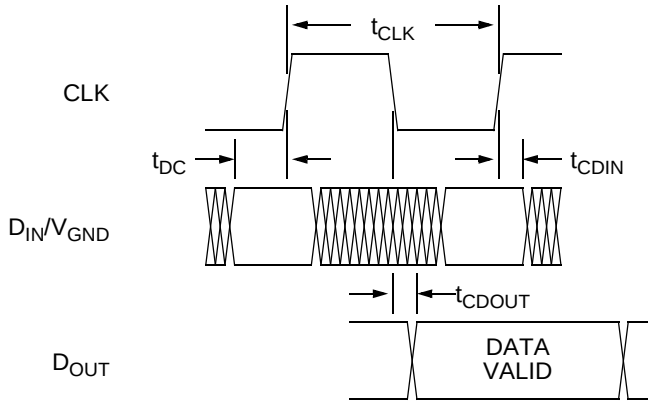


Figure 5-6. Serial Interface Timing

APPENDIX A TEST MODE OPERATION

Test mode is entered when certain conditions are satisfied after power is applied to the device. Communication with the device is conducted using the SPI when in test mode. Two test mode operations are of interest to the customer. These operations are described below. Test mode communication is conducted using the serial peripheral interface (SPI).

A.1 SPI DATA TRANSFER

A 16-bit SPI is available for data transfer when the voltage at V_{PP}/TEST is raised above V_{TEST}. Test mode is entered when the sequence of data values shown above are transferred following reset. See Figure A-4 for details of 16-bit SPI packet.

The state of D_{IN} is latched on the rising edge of CLK. D_{OUT} changes on the falling edge of CLK. The interface conforms to CPHA = 0, CPOL = 0 operation for conventional SPI devices.

A.2 ADC TEST MODE

A special device configuration useful for evaluating the performance of the analog-to-digital convertor block is available. When selected, internal buffers which drive the C_{FIL} pin and ADC input are disabled, and the input of the ADC is connected to the C_{FIL} pin, as illustrated in Figure A-1. The following sequence of operations must be performed to enter ADC Test Mode. Refer to Appendix A.4 for details regarding register read and write operations.

1. Apply V_{HCAP} to the H_{CAP} pin. This may be accomplished through BUSIN if desired.
2. Apply V_{TEST} to the V_{PP}/TEST pin.
3. Transfer the data value $AA to device register address $30 via the SPI.
4. Transfer the data value $55 to device register address $30 via the SPI.
5. Transfer the data value $1D to device register address $30 via the SPI.

Remove power or lower the voltage at V_{PP}/TEST to exit ADC Test Mode.

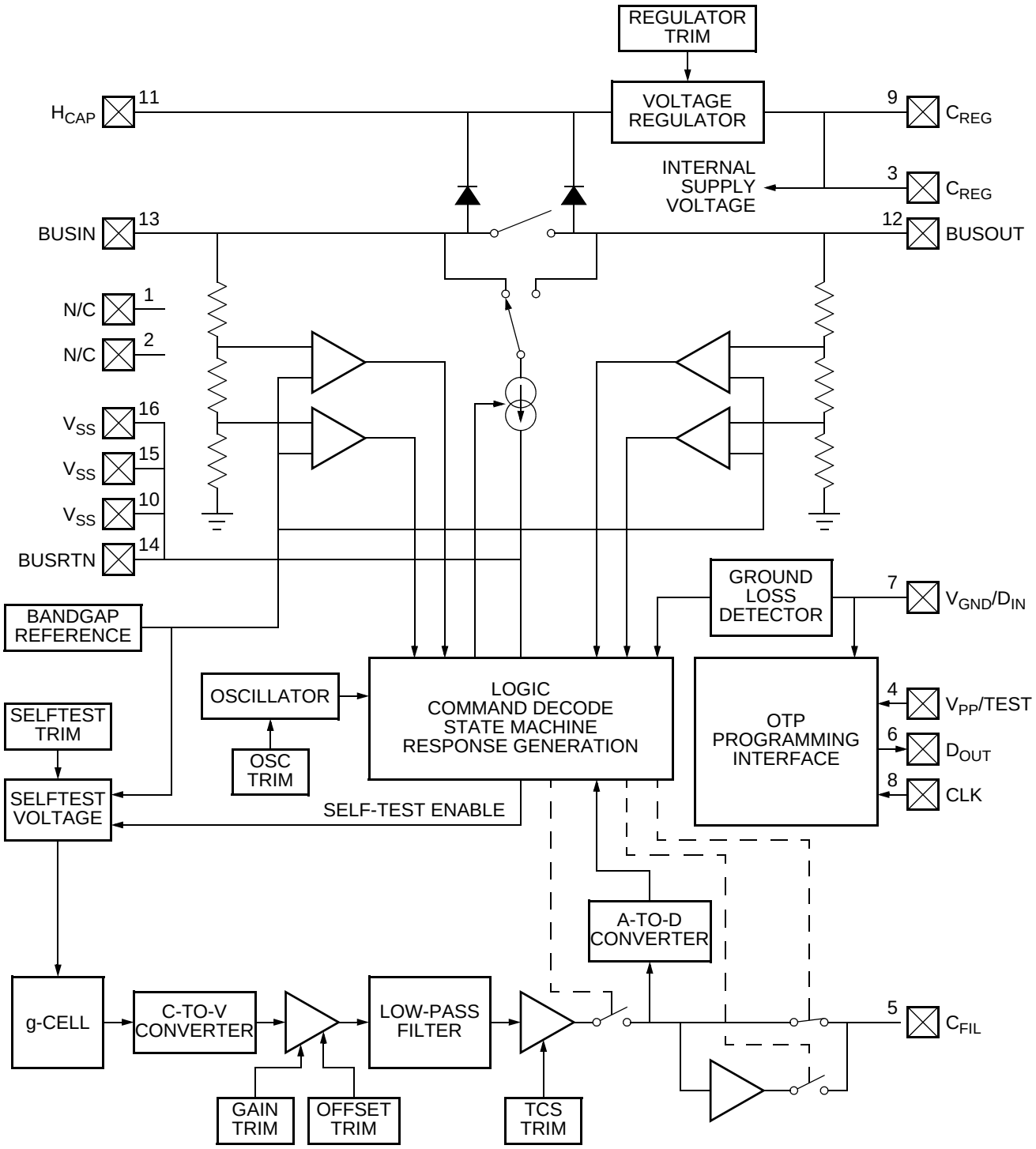


Figure A-1. ADC Test Mode Configuration

A.3 OTP PROGRAMMING OPERATIONS

The ten customer-programmed OTP locations (DEVCFG0, DEVCFG1 and REG-8 through REG-F) may be programmed when the device is in test mode if the following sequence of operations is performed. Register access operations required for OTP programming are described in Appendix A.4.

1. Apply V_{HCAP} to the H_{CAP} pin. This may be accomplished through BUSIN if desired.
2. Apply V_{TEST} to the V_{PP}/TEST pin.
3. Write the desired data values to the two registers via the SPI.
4. Transfer the data value $AA to device register address $30 via the SPI.
5. Transfer the data value $55 to device register address $30 via the SPI.
6. Transfer the data value $C6 to device register address $30 via the SPI.
7. Write the data value $00 to address $20 via the SPI. This will enable write access to the fuse mirror registers.
8. Write register data to be programmed into fuse array.
9. Write the data value $05 to address $20 via the SPI. The automatic programming sequence is initiated by this write operation.
10. Delay a minimum of 32 μs to allow the programming sequence to begin.
11. Read data value from address $29 until bit 5 is set.
12. If bit 4 of value read from address $29 is set, the programming operation did not complete successfully.

Bits which are unprogrammed may be programmed to a logic ‘1’ state. The device may be incrementally programmed if desired, however once a bit is programmed to a logic ‘1’ state, it may not be reset to logic ‘0’ in the OTP array. Once the LOCK2 bit has been set, no further changes to the OTP array are possible. Setting LOCK2 also enables parity detection when the device operates in normal mode.

A.4 INTERNAL REGISTER ACCESS

Using the DIN /VGND, CLK, and DOUT pins, each address location of MMA81XXEG/MMA82XXEG/MMA82XXTEG can be read and written from an external SPI interface shown in Figure A-2. The corresponding registers may be used to:

- Program the OTP memory
- Read the OTP memory
- Access various internal signals of the MMA81XXEG/MMA82XXEG/MMA82XXTEG in Test mode

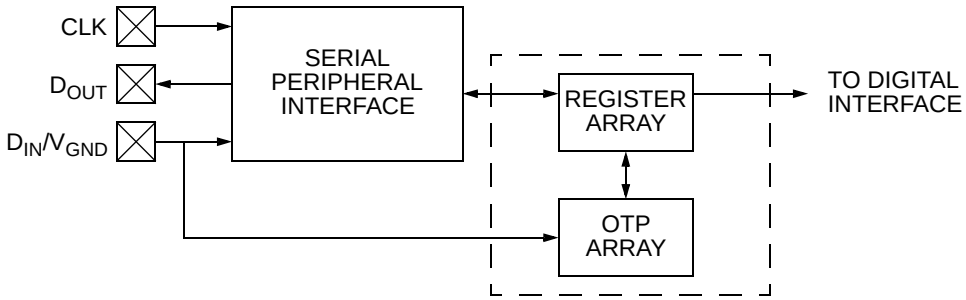


Figure A-2. OTP Interface Overview

A.4.1 Interface Data Bit Stream

The 16-bit SPI serial data consists of 6 bits for a data address, 1 bit for a data direction, and 8 bits for the data to be transferred as shown below.

	BIT															
	15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FUNCTION	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	RW	—	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]

Figure A-3. Serial Data Stream

A[5:0]

Register array location to be read or written.

D[7:0]

Register array data. This is the data to be transferred to the register array during write operations, or the data contained in the array at the associated address during read operations.

RW

Control of data direction during the clocking of D[7:0] data bits as follows:

RW = 1

Register array write. D[7:0] are transferred into the register array during subsequent transitions of the CLK input.

RW = 0

Register array read. Data are transferred from the register array during subsequent transitions of the CLK input.

A.4.2 Register Array Read Operation

Read operations are completed through16-bit transfers using the SPI as shown below. Data contained in the array at the associated address are presented at the D_{OUT} pin during the 8th through 15th falling edges at the CLK input.

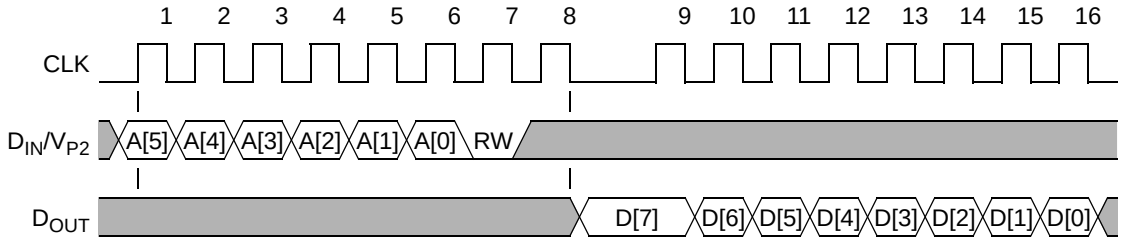


Figure A-4. Serial Data Timing, Register Array Read Operation

Should the data transfer be corrupted by e.g., noise on the clock line, a device reset is required to restore the state of internal logic.

A.4.3 Register Array Write Operation

A write operation is completed through the transfer of a 16-bit value using the SPI as shown in the diagram below. Data present at the D_{IN} pin are transferred to the register at the associated address during the 9th through 16th rising edges at the CLK input. Contents of the register at the time the write operation is initiated are presented at the D_{OUT} pin during the 8th through 15th falling edges of the CLK input.

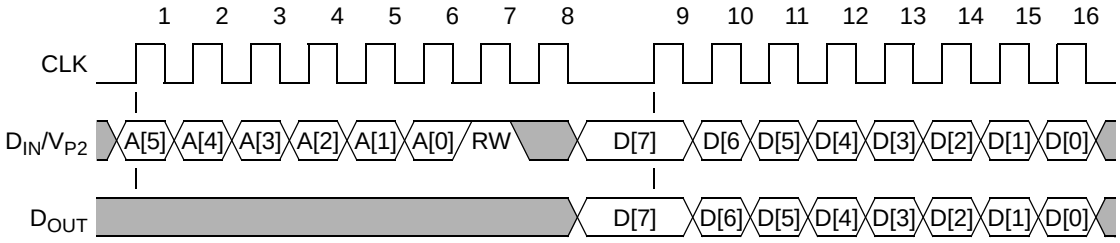


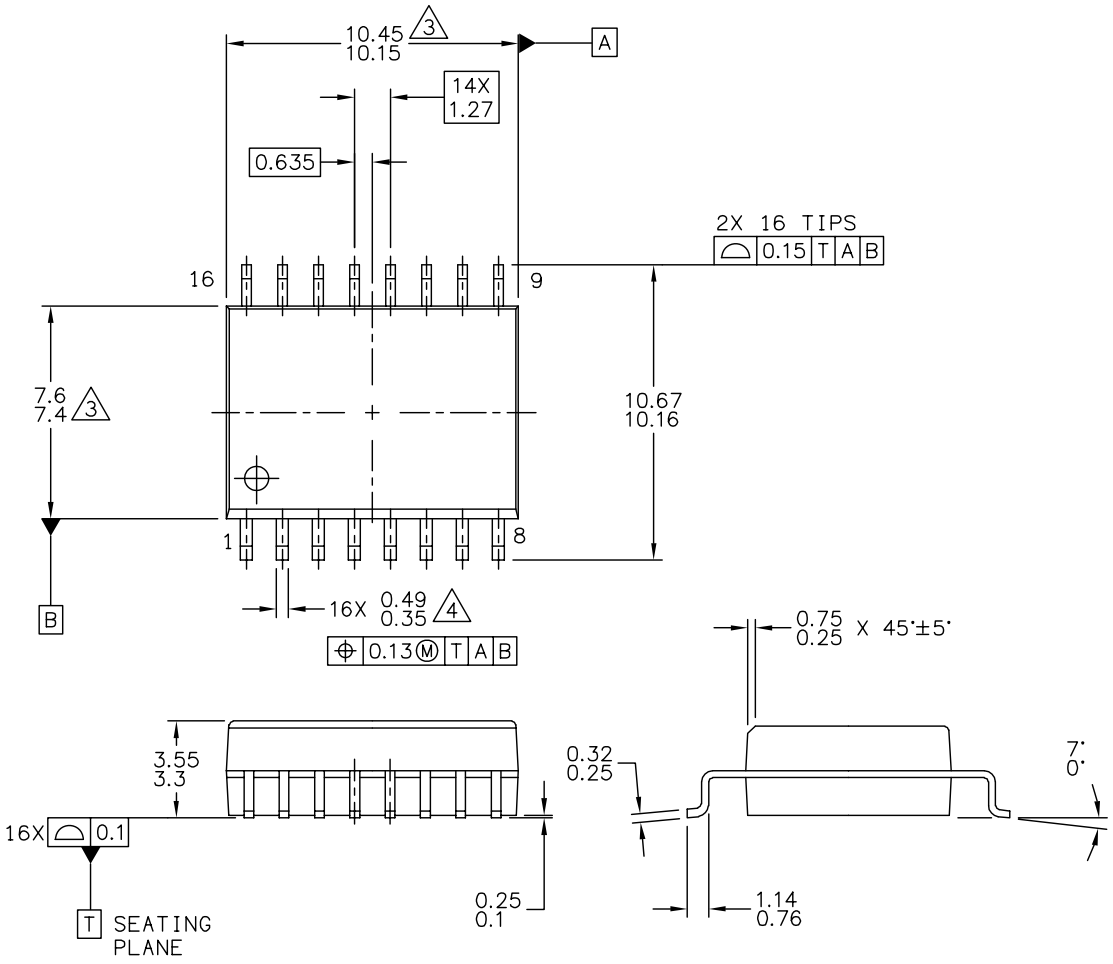
Figure A-5. Serial Data Timing, Register Array Write Operation

A.4.4 Internal Address Map Overview

OTP data is transferred to internal registers during the first sixteen clock cycles following oscillator startup and negation of internal reset. When the device operates in test mode, OTP data in the mirror registers may be overwritten. Mirror register writes must be enabled by setting the SPI_WRITE_ENABLE bit (address $29[5]). This bit may be set by writing the value $0 to address $20.

Internal register read and write operations are described in Section 3.

PACKAGE DIMENSIONS



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MMA81XXEG
Rev 5
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