GENERAL DESCRIPTION

The XRT75L04 is a four-channel fully integrated Line Interface Unit (LIU) with Jitter Attenuator for E3/DS3/STS-1 applications. It incorporates four independent Receivers, Transmitters and Jitter Attenuators in a single 176 pin LQFP package.

Each channel of the XRT75L04 can be configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz) rates that are independent of each other. Each transmitter can be turned off and tri-stated for redundancy support and for conserving power.

The XRT75L04's differential receivers provide high noise interference margin and are able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75L04 incorporates an advanced crystal-less jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Telcordia GR-499, GR-253 specifications.

The XRT75L04 provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The XRT75L04 supports local, remote and digital loop-backs. The XRT75L04 also contains an on-board Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error.

FEATURES

RECEIVER:

- On chip Clock and Data Recovery circuit for high input jitter tolerance.
- Meets the jitter tolerance requirements as specified in ITU-T G.823_1993 for E3 and Telcordia GR-499-CORE for DS3 applications.
- Detects and Clears LOS as per G.775.
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation.
- On chip B3ZS/HDB3 encoder and decoder that can either be enabled or disabled.
- On-chip clock synthesizer generates the appropriate rate clock from a single frequency XTAL.
- Provides low jitter clock outputs for either DS3,E3 or STS-1 rates.

TRANSMITTER:

- Compliant with Telcordia GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Transmitters can be turned on or off.

JITTER ATTENUATOR:

- On chip advanced crystal-less Jitter Attenuator.
- Jitter Attenuators can be selected in Receive or Transmit paths.
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755, GR-253 and GR-499-CORE,1995 standards.
- Meets ETSI TBR 24 Jitter Transfer Requirements.
- 16 or 32 bits selectable FIFO size.
- Meets the Wander specifications described in T1.105.03b.
- Jitter Attenuators can be disabled.

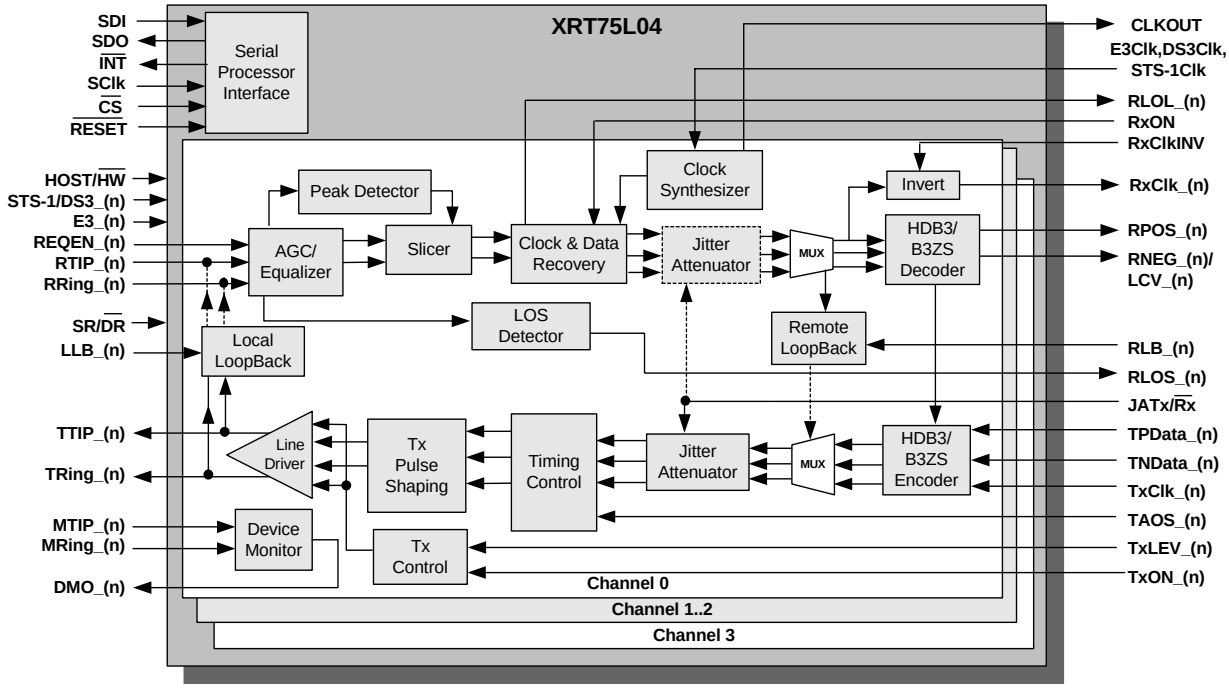
CONTROL AND DIAGNOSTICS:

- Serial Microprocessor Interface for control and configuration.
- Supports optional internal Transmit Driver Monitoring.
- PRBS error counter register to accumulate errors.
- Supports Local, Remote and Digital Loop-backs.
- Single 3.3 V ± 5% power supply.
- 5 V Tolerant I/O.
- Maximum Power Dissipation 1.5W.
- Available in 176 pin LQFP package
- - 40°C to 85°C Industrial Temperature Range.

APPLICATIONS

- E3/DS3 Access Equipment.
- STS1-SPE to DS3 Mapper.
- DSLAMs.
- Digital Cross Connect Systems.
- CSU/DSU Equipment.
- Routers.

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75L04



Notes: 1. (n) = 0, 1, 2 or 3 for respective Channels
2. Serial Processor Interface input pins are shared by the four Channels in "Host" Mode and redefined in the "Hardware" Mode.

TRANSMIT INTERFACE CHARACTERISTICS

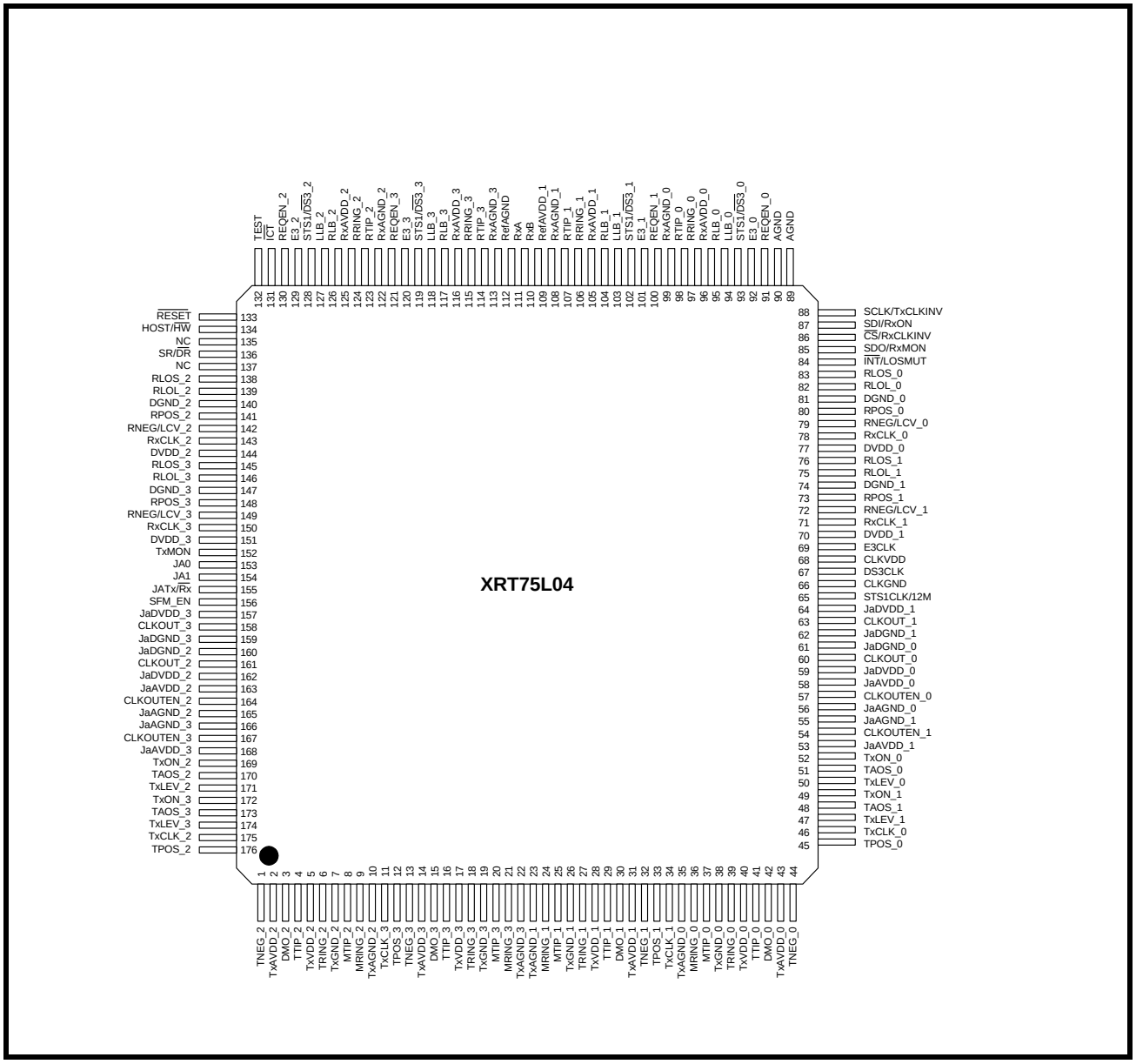
- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit.
- Built-in B3ZS/HDB3 Encoder (which can be disabled).
- Accepts Transmit Clock with duty cycle of 30%-70%.
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications.
- Generates pulses that comply with the DSX-3 pulse template, as specified in Telcordia GR-499-CORE and ANSI T1.102_1993.
- Generates pulses that comply with the STSX-1 pulse template, as specified in Telcordia GR-253-CORE.
- Transmitters can be turned off to support redundancy designs.

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization for optimal Clock and Data Recovery.
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications.
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications.
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms.
- Built-in B3ZS/HDB3 Decoder (which can be disabled).
- Recovered Data can be muted while the LOS Condition is declared.

- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment.

FIGURE 2. PIN OUT OF THE XRT75L04



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L04IV	176 Pin LQFP	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTIONS (BY FUNCTION)

TRANSMIT INTERFACE

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>52
49
169
172</td><td>TxON_0
TxON_1
TxON_2
TxON_3</td><td>I</td><td>Transmitter ON Input - Channel 0:
Transmitter ON Input - Channel 1:
Transmitter ON Input - Channel 2:
Transmitter ON Input - Channel 3:
These pins are active only when the corresponding TxON bit is set.
Table below shows the status of the transmitter based on theTxON bit and TxON pin settings.

<table>
<tr><th>Host/$\overline{HW}$</th><th>Bit</th><th>Pin</th><th>Transmitter Status</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>OFF</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>OFF</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>OFF</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>ON</td></tr>
<tr><td>0</td><td>x</td><td>0</td><td>OFF</td></tr>
<tr><td>0</td><td>x</td><td>1</td><td>ON</td></tr>
</table>

NOTES:
1. These pins will be active and can control the TTIP and TRING outputs only when the TxON_n bits in the channel register are set .
2. When Transmitters are turned off the TTIP and TRING outputs are Tri-stated.
3. These pins are internally pulled up.</td></tr>
<tr><td>46
34
175
11</td><td>TxCLK_0
TxCLK_1
TxCLK_2
TxCLK_3</td><td>I</td><td>Transmit Clock Input for TPOS and TNEG - Channel 0:
Transmit Clock Input for TPOS and TNEG - Channel 1:
Transmit Clock Input for TPOS and TNEG - Channel 2:
Transmit Clock Input for TPOS and TNEG - Channel 3:
The frequency accuracy of this input clock must be of nominal bit rate ± 20 ppm. The duty cycle can be 30%-70%.
By default, input data is sampled on the falling edge of TxCLK when input data is changing on the rising edge of TxCLK..</td></tr>
<tr><td>44
32
1
13</td><td>TNEG_0
TNEG_1
TNEG_2
TNEG_3</td><td>I</td><td>Transmit Negative Data Input - Channel 0:
Transmit Negative Data Input - Channel 1:
Transmit Negative Data Input - Channel 2:
Transmit Negative Data Input - Channel 3:
In Dual-rail mode, these pins are sampled on the falling or rising edge of TxCLK_n .
NOTES:
1. These input pins are ignored and must be grounded if the Transmitter Section is configured to accept Single-Rail data from the Terminal Equipment.</td></tr>
</table>

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
45 33 176 12	TPOS_0 TPOS_1 TPOS_2 TPOS_3	I	**Transmit Positive Data Input - Channel 0:** **Transmit Positive Data Input - Channel 1:** **Transmit Positive Data Input - Channel 2:** **Transmit Positive Data Input - Channel 3:** By default sampled on the falling edge of TxCLK
41 29 4 16	TTIP_0 TTIP_1 TTIP_2 TTIP_3	O	**Transmit TTIP Output - Channel 0:** **Transmit TTIP Output - Channel 1:** **Transmit TTIP Output - Channel 2:** **Transmit TTIP Output - Channel 3:** These pins along with TRING transmit bipolar signals to the line using a 1:1 transformer.
39 27 6 18	TRING_0 TRING_1 TRING_2 TRING_3	O	**Transmit Ring Output - Channel 0:** **Transmit Ring Output - Channel 1:** **Transmit Ring Output - Channel 2:** **Transmit Ring Output - Channel 3:** These pins along with TTIP transmit bipolar signals to the line using a 1:1 transformer.
50 47 171 174	TxLEV_0 TxLEV_1 TxLEV_2 TxLEV_3	I	**Transmit Line Build-Out Enable/Disable Select - Channel 0:** **Transmit Line Build-Out Enable/Disable Select - Channel 1:** **Transmit Line Build-Out Enable/Disable Select - Channel 2:** **Transmit Line Build-Out Enable/Disable Select - Channel 3:** These input pins are used to select the Transmit Line Build-Out circuit of Channel n. Setting these pins to "High" disables the Line Build-Out circuit of Channel n. In this mode, Channel n outputs partially-shaped pulses onto the line via the TTIP_n and TRing_n output pins. Setting these pins to "Low" enables the Line Build-Out circuit of Channel n. In this mode, Channel n outputs shaped pulses onto the line via the TTIP_n and TRing_n output pins. To comply with the Isolated DSX-3/STSX-1 Pulse Template Requirements per Bellcore GR-499-CORE or Bellcore GR-253-CORE: 1. Set these pins to "1" if the cable length between the Cross-Connect and the transmit output of Channel is greater than 225 feet. 2. Set these pins to "0" if the cable length between the Cross-Connect and the transmit output of Channel is less than 225 feet. These pins are active only if the following two conditions are true: a. The XRT75L04 is configured to operate in either the DS3 or SONET STS-1 Modes. b. The XRT75L04 is configured to operate in the Hardware Mode. ***NOTES:*** *1. These pins are internally pulled down.* *2. If the XRT75L04 is configured in HOST mode, these pins should be tied to GND.*

TRANSMIT INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
88	TxClkINV/ SClk	I	**Hardware Mode: Transmit Clock Invert** **Host Mode: Serial Clock Input:** Function of this pin depends on whether the XRT75L04 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" configures all three Transmitters to sample the TPOS_n and TNEG_n data on the rising edge of the TxCLK_n . ***NOTES:*** *1. If the XRT75L04 is configured in HOST mode, this pin functions as SClk input pin (please refer to the pin description for Microprocessor interface).*
152	TxMON	I	**Transmitter Monitor:** When this pin is pulled "High", MTIP and MRING are connected internally to TTIP and TRING and allows self monitoring of the transmitter.
51 48 170 173	TAOS_0 TAOS_1 TAOS_2 TAOS_3	I	**Transmit All Ones Select - Channel 0:** **Transmit All Ones Select - Channel 1:** **Transmit All Ones Select - Channel 2:** **Transmit All Ones Select - Channel 3:** A "High" on this pin causes the Transmitter Section of Channel_n to generate and transmit a continuous AMI all "1's" pattern onto the line. The frequency of this "1's" pattern is determined by TxClk_n. ***NOTES:*** *1. This input pin is ignored if the XRT75L04 is operating in the HOST Mode and should be tied to GND.* *2. Analog Loopback and Remote Loopback have priority over request.* *3. This pin is internally pulled down.*

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
78 71 143 150	RxCLK_0 RXCLK_1 RxCLK_2 RxCLK_3	O	**Receive Clock Output - Channel 0:** **Receive Clock Output - Channel 1:** **Receive Clock Output - Channel 2:** **Receive Clock Output - Channel 3:** By default, RPOS and RNEG data sampled on the rising edge RxCLK.. Set the RxCLKINV bit to sample RPOS/RNEG data on the falling edge of RxCLK
80 73 141 148	RPOS_0 RPOS_1 RPOS_2 RPOS_3	O	**Receive Positive Data Output - Channel 0:** **Receive Positive Data Output - Channel 1:** **Receive Positive Data Output - Channel 2:** **Receive Positive Data Output - Channel 3:** ***NOTE:*** *If the B3ZS/HDB3 Decoder is enabled in Single-rail mode, then the zero suppression patterns in the incoming line signal (such as: "00V", "000V", "B0V", "B00V") is removed and replaced with '0'.*
79 72 142 149	RNEG_0/LCV_0 RNEG_1/LCV_1 RNEG_2/LCV_2 RNEG_3/LCV_3	O	**Receive Negative Data Output/Line Code Violation Indicator - Channel 0:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 1:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 2:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 3:** In Dual Rail mode, a negative pulse is output through RNEG. **Line Code Violation Indicator - Channel n:** If configured in Single Rail mode then Line Code Violation will be output.
97 106 124 115	RRING_0 RRING_1 RRING_2 RRING_3	I	**Receive Ring Input - Channel 0:** **Receive Ring Input - Channel 1:** **Receive Ring Input - Channel 2:** **Receive Ring Input - Channel 3:** These pins along with RTIP receive the bipolar line signal from the remote DS3/E3/STS-1 Terminal.
98 107 123 114	RTIP_0 RTIP_1 RTIP_2 RTIP_3	I	**Receive TIP Input - Channel 0:** **Receive TIP Input - Channel 1:** **Receive TIP Input - Channel 2:** **Receive TIP Input - Channel 3:** These pins along with RRING receive the bipolar line signal from the Remote DS3/E3/STS-1 Terminal.

RECEIVE INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
91 100 130 121	REQEN_0 REQEN_1 REQEN_2 REQEN_3	I	**Receive Equalizer On/Off - Channel 0:** **Receive Equalizer On/Off- Channel 1:** **Receive Equalizer On/Off - Channel 2:** **Receive Equalier On/Off- Channel 3:** Tie these pins "High" to enable the receive equalizer. ***NOTES:*** *1. This input pin is ignored and should be connected to GND if the XRT75L04 is operating in the HOST Mode* *2. This pin is internally pulled down.*
87	RxON/ SDI	I	**Hardware Mode: Receiver Turn ON Input** **Host Mode: Serial Data Input:** Function of this pin depends on whether the XRT75L04 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" turns on and enables the Receivers of all three channels. ***NOTES:*** *1. If the XRT75L04 is configured in HOST mode, this pin functions as SDI input pin (please refer to the pin description for Microprocessor Interface)* *2. This pin is internally pulled down.*
86	RxClkINV/ $\overline{CS}$	I	**Hardware Mode: RxClk INVERT** **Host Mode: Chip Select**: Function of this pin depends on whether the XRT75L04 is configured to operate in Hardware mode or Host mode. In Hardware mode, setting this input pin "High" configures the Receiver Section of all channels to invert the RxClk_n output signals and outputs the recovered data via RPOS_n and RNEG_n on the falling edge of RxClk_n. ***NOTE:*** *If the XRT75L04 is configured in HOST mode, this pin functions as CS input pin (please refer to the pin description for Microprocessor Interface).*
85	RxMON/ SDO	I	**Hardware Mode: Receive Monitoring Mode** **Host Mode: Serial Data Output:** In Hardware mode, when this pin is tied "High" all 4 channels configure into monitoring channels. In the monitoring mode, the Receiver is capable of monitoring the signals with 20 dB flat loss plus 6 dB cable attenuation. This allows monitoring very weak signal before declaring LOS. In HOST Mode each channel can be independently configured to be a monitoring channel by setting the bits in the channel control registers. ***NOTE:*** *If the XRT75L04 is configured in HOST mode, this pin functions as SDO pin (please refer to the pin description for the Microprocessor Interface).*

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
69	E3CLK	I	**E3 Clock Input (34.368 MHz ± 20 ppm):** If any of the channels is configured in E3 mode, a reference clock 34.368 MHz is applied on this pin. ***NOTE:*** *In single frequency mode, this reference clock is not required.*
67	DS3CLK	I	**DS3 Clock Input (44.736 MHz ± 20 ppm):** If any of the channels is configured in DS3 mode, a reference clock 44.736 MHz. is applied on this pin. ***NOTE:*** *In single frequency mode, this reference clock is not required.*
65	STS-1CLK/ 12M	I	**STS-1 Clock Input (51.84 MHz ± 20 ppm):** If any of the channels is configured in STS-1 mode, a reference clock 51.84 MHz is applied on this pin.. In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the channels in E3, DS3 or STS-1.
156	SFM_EN	I	**Single Frequency Mode Enable:** Tie this pin "High" to enable the Single Frequency Mode. A reference clock of 12.288 MHz ± 20 ppm is applied. This offers the flexibility of using a low cost reference clock and configures the board for either E3 or DS3 or STS-1 without the need to change any components on the board. In the Single Frequency Mode (SFM) an output clock is provided for each channel if the CLK_EN bit is set thus eliminating the need for a separate clock source for the framer. Tie this pin "Low" if single frequency mode is not selected. In this case, the appropriate reference clocks must be provided. ***NOTE:*** *This pin is internally pulled down*
57 54 164 167	CLKOUTEN_0 CLKOUTEN_1 CLKOUTEN_2 CLKOUTEN_3	O	**Clock output enable for channel 0** **Clock output enable for channel 1** **Clock output enable for channel 2** **Clock output enable for channel 3** Pull this pin "High" to output low jitter clock on the CLKOUT_n pins. ***NOTES:*** *1. This clock output is only available in SFM mode.* *2. The maximum drive capability for the clockouts is 16 mA.*
60 63 161 158	CLKOUT_0 CLKOUT_1 CLKOUT_2 CLKOUT_3	O	**Clock output for channel 0** **Clock output for channel 1** **Clock output for channel 2** **Clock output for channel 3** If CLKOUTEN_n pin is "High", low jitter clock is output for each channel. Frequency of these clocks is based on the mode (E3,DS3 or STS-1) the channels are configured. This eliminates the need for a separate clock source for the framer. ***NOTES:*** *1. This clock output is only available in SFM mode.* *2. The maximum drive capability for the clockouts is 16 mA.*

CONTROL AND ALARM INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
36 24 9 21	MRING_0 MRING_1 MRING_2 MRING_3	I	**Monitor Ring Input - Channel 0:** **Monitor Ring Input - Channel 1:** **Monitor Ring Input - Channel 2:** **Monitor Ring Input - Channel 3:** The bipolar line output signal from TRING_n is connected to this pin via a 270 Ω resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled "Low".*
37 25 8 20	MTIP_0 MTIP_1 MTIP_2 MTIP_3	I	**Monitor Tip Input - Channel 0:** **Monitor Tip Input - Channel 1:** **Monitor Tip Input - Channel 2:** **Monitor Tip Input - Channel 3:** The bipolar line output signal from TTIP_n is connected to this pin via a 270-ohm resistor to check for line driver failure. ***NOTE:*** *This pin is internally pulled "Low".*
42 30 3 15	DMO_0 DMO_1 DMO_2 DMO_3	O	**Drive Monitor Output - Channel 0:** **Drive Monitor Output - Channel 1:** **Drive Monitor Output - Channel 2:** **Drive Monitor Output - Channel 3:** If MTIP_n and MRING_n has no transition pulse for 128 ± 32 TxCLK_n cycles, DMO_n goes “High” to indicate the driver failure. DMO_n output stays “High” until the next AMI signal is detected.
83 76 138 145	RLOS_0 RLOS_1 RLOS_2 RLOS_3	O	**Receive Loss of Signal Output Indicator - Channel 0:** **Receive Loss of Signal Output Indicator - Channel 1:** **Receive Loss of Signal Output Indicator - Channel 2:** **Receive Loss of Signal Output Indicator - Channel 3:** This output pin toggles "High" if the receiver has detected a Loss of Signal Condition. The criteria for declaring /clearing an LOS Condition depends upon whether it is operating in the E3 or STS-1/DS3 Mode.
82 75 139 146	RLOL_0 RLOL_1 RLOL_2 RLOL_3	O	**Receive Loss of Lock Output Indicator - Channel 0:** **Receive Loss of Lock Output Indicator - Channel 1:** **Receive Loss of Lock Output Indicator - Channel 2:** **Receive Loss of Lock Output Indicator - Channel 3:** This output pin toggles "High" if a Loss of Lock Condition is detected. LOL (Loss of Lock) condition occurs if the recovered clock frequency deviates from the Reference Clock frequency (available at either E3CLK or DS3CLK or STS-1CLK input pins) by more than 0.5%.
111	RXA	****	**External Resistor of 3 K Ω ± 1%.** Should be connected between RxA and RxB for internal bias.
110	RXB	****	**External Resistor of 3K Ω ±1%.** Should be connected between RxA and RxB for internal bias.

CONTROL AND ALARM INTERFACE

131	$\overline{\text{ICT}}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, tie this pin "High". ***NOTE:*** *This pin is internally pulled "High".*
132	TEST	****	**Factory Test Pin** ***NOTE:*** *This pin must be connected to GND for normal operation.*
84	LOSMUT/ $\overline{\text{INT}}$	I/O	**Hardware Mode: MUTE-upon-LOS Enable Input** **Host Mode: Interrupt Ouput:** In Hardware Mode, setting pin "High" configures all three channels to Mute the recovered data on the RPOS_n and RNEG_n whenever one of the channels declares an LOS condition. RPOS_n and RNEG_n outputs are pulled "Low". Muting of the output data can be configured/controlled on a per channel basis in Host Mode. ***NOTE:*** *If the XRT75L04 is configured in HOST mode, this pin functions as $\overline{\text{INT}}$ pin (please refer to the pin description for the Microprocessor Interface).*
94 103 127 118	LLB_0 LLB_1 LLB_2 LLB_3	I	**Local Loop-back - Channel 0:** **Local Loop-back - Channel 1:** **Local Loop-back - Channel 2:** **Local Loop-back - Channel 3:** This input pin along with RLB_n configures different Loop-Back modes. A "High" on this pin with RLB_n set to "Low" configures Channel_n to operate in the Analog Local Loop-back Mode. A "High" on this pin with RLB_n set to "High" configures Channel_n to operate in the Digital Local Loop-back Mode. ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT75L04 is operating in the HOST Mode.*
95 104 126 117	RLB_0 RLB_1 RLB_2 RLB_3	I	**Remote Loop-back - Channel 0:** **Remote Loop-back - Channel 1:** **Remote Loop-back - Channel 2:** **Remote Loop-back - Channel 3:** This input pin along with LLB_n configures different Loop-Back modes. A "High" on this pin with LLB_n set to "Low" configures Channel_n to operate in the Remote Loop-back Mode. A "High" on this pin with LLB_n set to "High" configures Channel_n to operate in the Digital Local Loop-back Mode. **RLB_n / LLB_n / Loopback Mode** **0 / 0 / Normal Operation** **0 / 1 / Analog Local** **1 / 0 / Remote** **1 / 1 / Digital** ***NOTE:*** *This input pin is ignored and should be connected to GND if the XRT75L04 is operating in the HOST Mode.*

OPERATING MODE SELECT

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
134	HOST/($\overline{HW}$)	I	**HOST/Hardware Mode Select:** Tie this pin "High" to configure in HOST mode. Tie this "Low" to configure in Hardware mode. When configured in HOST mode, the states of many of the discrete input pins are controlled by internal register bits. ***NOTE:*** *This pin is internally pulled up.*
92 101 129 120	E3_0 E3_1 E3_2 E3_3	I	**E3 Mode Select Input** A "High" on this pin configures Channel_n to operate in E3 mode. A "Low" on this pin configures Channel_n to operate in either STS-1 or DS3 mode depending on the settings on pins 93,102,128 and 119 pins. ***NOTES:*** *1. This pin is internally pulled down* *2. This pin is ignored and should be tied to GND if configured to operate in HOST mode.*
93 102 128 119	STS-1/$\overline{DS3}$_0 STS-1/$\overline{DS3}$_1 STS-1/$\overline{DS3}$_2 STS-1/$\overline{DS3}$_3	I	**STS-1/DS3 Select Input** A "High" on these pins configures the Channel_n to operate in STS-1 mode. A "Low" on these pins configures the Channel_n to operate in DS3 mode. These pins are ignored if the E3_n pins are set to "High". ***NOTES:*** *1. This pin is internally pulled down* *2. This pin is ignored and should be tied to GND if configured to operate in HOST mode.*
136	SR/$\overline{DR}$	I	**Single-Rail/Dual-Rail Select:** Setting this "High" configures both the Transmitter and Receiver to operate in Single-rail mode and also enables the B3ZS/HDB3 Encoder and Decoder. In Single-rail mode, TNEG_n pin should be grounded. Setting this "Low" configures both the Transmitter and Receiver to operate in Dual-rail mode and disables the B3ZS/HDB3 Encoder and Decoder. ***NOTE:*** *This pin is internally pulled down.*

SERIAL MICROPROCESSOR INTERFACE

86	$\overline{CS}$ RxCLKINV	I	**Microprocessor Serial Interface - Chip Select** Toggle this pin "Low" to enable the communication with the Microprocessor Serial Interface.(see figures 10 & 11) ***NOTE:*** *If configured in Hardware Mode, this pin functions as RxClkINV.*
88	SClk TxCLKINV	I	**Serial Interface Clock Input** The data on the SDI pin is sampled on the rising edge of this signal. Additionally, during Read operations the Microprocessor Serial Interface updates the SDO output on the falling edge of this signal. ***NOTE:*** *If configured in Hardware Mode, this pin functions as TxClkINV.*

SERIAL MICROPROCESSOR INTERFACE

87	SDI RxON	I	**Serial Data Input:** Data is serially input through this pin. The input data is sampled on the rising edge of the SClk pin (pin 88). ***NOTES:*** *1. This pin is internally pulled down* *2. If configured in Hardware Mode, this pin functions as RxON.*
85	SDO RxMON	I/O	**Serial Data Output:** This pin serially outputs the contents of the specified Command Register during Read Operations. The data is updated on the falling edge of the SClk and this pin is tri-stated upon completion of data transfer. ***NOTE:*** *If configured in Hardware Mode, this pin functions as RxMON.*
84	$\overline{\text{INT}}$ LOSMUT	I/O	**INTERRUPT Output:** This pin functions as Interrupt Output for Serial Interface. A transition to “Low” indicates that an interrupt has been generated by the Serial Interface. The interrupt function can be disabled by setting the interrupt enable bit to “0” in the Channel Control Register. ***NOTES:*** *1. In Hardware mode, this pin functions as LOSMUT.* *2. This pin will remain asserted “Low” until the interrupt is serviced.*
133	$\overline{\text{RESET}}$	I	**Register Reset:** Setting this input pin "Low" causes the XRT75L04 to reset the contents of the Command Registers to their default settings and default operating configuration ***NOTE:*** *This pin is internally pulled up.*

JITTER ATTENUATOR INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
154	JA1	I	**Jitter Attenuator Select 1:** In Hardware Mode, this pin along with the pin JA0 configures the Jitter Attenuator as shown in the table. **JA0 / JA1 / Mode** **0 / 0 / 16 bit FIFO** **0 / 1 / 32 bit FIFO** **1 / 0 / Disable Jitter Attenuator** **1 / 1 / Disable Jitter Attenuator** ***NOTE:*** *This pin is internally pulled down.*

JITTER ATTENUATOR INTERFACE

155	JATx/$\overline{Rx}$	I	**Jitter Attenuator Path Select** In Hardware Mode, tie this pin "High" to select the Jitter Attenuator in the Transmit Path . Connect this pin "Low" to select the Jitter Attenuator in the Receive Path. This applies to all4 channels. ***NOTE:*** *This pin is internally pulled down.*
153	JA0	I	**Jitter Attenuator Select 0:** In Hardware Mode, this pin along with pin 154 configures the Jitter Attenuator as shown in the above table for JA1 pin 154. ***NOTE:*** *This pin is internally pulled down.*

ANALOG POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
43	TxAVDD_0	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 0**
31	TxAVDD_1	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 1**
2	TxAVDD_2	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 2**
14	TxAVDD_3	****	**Transmitter Analog 3.3 V ± 5% VDD - Channel 3**
35	TxAGND_0	****	**Transmitter Analog GND - Channel 0**
23	TxAGND_1	****	**Transmitter Analog GND - Channel 1**
10	TxAGND_2	****	**Transmitter Analog GND - Channel 2**
22	TxAGND_3	****	**Transmitter Analog GND - Channel 3**
96	RxAVDD_0	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 0**
105	RxAVDD_1	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 1**
125	RxAVDD_2	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 2**
116	RxAVDD_3	****	**Receiver Analog 3.3 V ± 5% VDD - Channel 3**
99	RxAGND_0	****	**Receiver Analog GND - Channel_0**
108	RxAGND_1	****	**Receive Analog GND - Channel 1**
122	RxAGND_2	****	**Receive Analog GND - Channel 2**
113	RxAGND_3	****	**Receive Analog GND - Channel 3**
58	JaAVDD_0	****	**Analog 3.3 V ± 5% VDD - Channel 0**
53	JaAVDD_1	****	**Analog 3.3 V ± 5% VDD - Channel 1**
163	JaAVDD_2	****	**Analog 3.3 V ± 5% VDD - Channel 2**
168	JaAVDD_3	****	**Analog 3.3 V ± 5% VDD - Channel 3**
56	JaAGND_0	****	**Analog GND - Channel 0**
55	JaAGND_1	****	**Analog GND - Channel 1**
165	JaAGND_2	****	**Analog GND - Channel 2**

ANALOG POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
166	JaAGND_3	****	**Analog GND - Channel 3**
89	AGND	****	**Analog GND**
90	AGND	****	**Analog GND**
109	REFAVDD	****	**Analog 3.3 V ± 5% VDD - Reference**
112	REFAGND	****	**Reference GND**

DIGITAL POWER AND GROUND

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
40	TxVDD_0	****	**Transmitter 3.3 V ± 5% VDD Channel 0**
28	TxVDD_1	****	**Transmitter 3.3 V ± 5% VDD Channel 1**
5	TxVDD_2	****	**Transmitter 3.3 V ± 5% VDD Channel 2**
17	TxVDD_3	****	**Transmitter 3.3 V ± 5% VDD Channel 3**
38	TxGND_0	****	**Transmitter GND - Channel 0**
26	TxGND_1	****	**Transmitter GND - Channel 1**
7	TxGND_2	****	**Transmitter GND - Channel 2**
19	TxGND_3	****	**Transmitter GND - Channel 3**
77	DVDD_0	****	**Receiver 3.3 V ± 5% VDD - Channel 0**
70	DVDD_1	****	**Receiver 3.3 V ± 5% VDD - Channel 1**
144	DVDD_2	****	**Receiver 3.3 V ± 5% VDD - Channel 2**
151	DVDD_3	****	**Receiver 3.3 V ± 5% VDD - Channel 3**
81	DGND_0	****	**Receiver Digital GND - Channel 0**
74	DGND_1	****	**Receiver Digital GND - Channel 1**
140	DGND_2	****	**Receiver Digital GND - Channel 2**
147	DGND_3	****	**Receiver Digital GND - Channel 3**
59	JaDVDD_0	****	**VDD 3.3 V ± 5%**
64	JaDVDD_1	****	**VDD 3.3 V ± 5%**
162	JaDVDD_2	****	**VDD 3.3 V ± 5%**
157	JaDVDD_3	****	**VDD 3.3 V ± 5%**
61	JaDGND_0	****	**GND**
62	JaDGND_1	****	**Digital GND**
160	JaDGND_2	****	**Digital GND**
159	JaDGND_3	****	**Digital GND**
68	CLKVDD	****	**VDD 3.3 V± 5%**
66	CLKGND	****	**Digital GND**

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	5.0	V	Note 1
V_{IN}	Input Voltage at any Pin	-0.5	5+0.5	V	Note 1
I_{IN}	Input current at any pin		100	mA	Note 1
S_{TEMP}	Storage Temperature	-65	150	^0C	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	85	^0C	linear airflow 0 ft./min
ThetaJA	Thermal Resistance		26.6	$^0C/W$	linear air flow 0ft/min
ThetaJC			7.2	$^0C/W$	
M_{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating		2000	V	Note 2

NOTES:

1. *Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.*
2. *ESD testing method is per MIL-STD-883D,M-3015.7*

TABLE 2: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV_{DD}	Digital Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply current (Measured while transmitting and receiving all 1's)		450	520	mA
P_{DD}	Power Dissipation		1.3	1.5	W
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.0	V
V_{OL}	Output Low Voltage, I_{OUT} = - 4mA			0.4	V
V_{OH}	Output High Voltage, I_{OUT} = 4 mA	2.4			V
I_L	Input Leakage Current[1]			±10	µA
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

1. *Not applicable for pins with pull-up or pull-down resistors.*
2. *The Digital inputs and outputs are TTL 5V compliant.*

2.0 TIMING CHARACTERISTICS

FIGURE 3. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75L04 (DUAL-RAIL DATA)

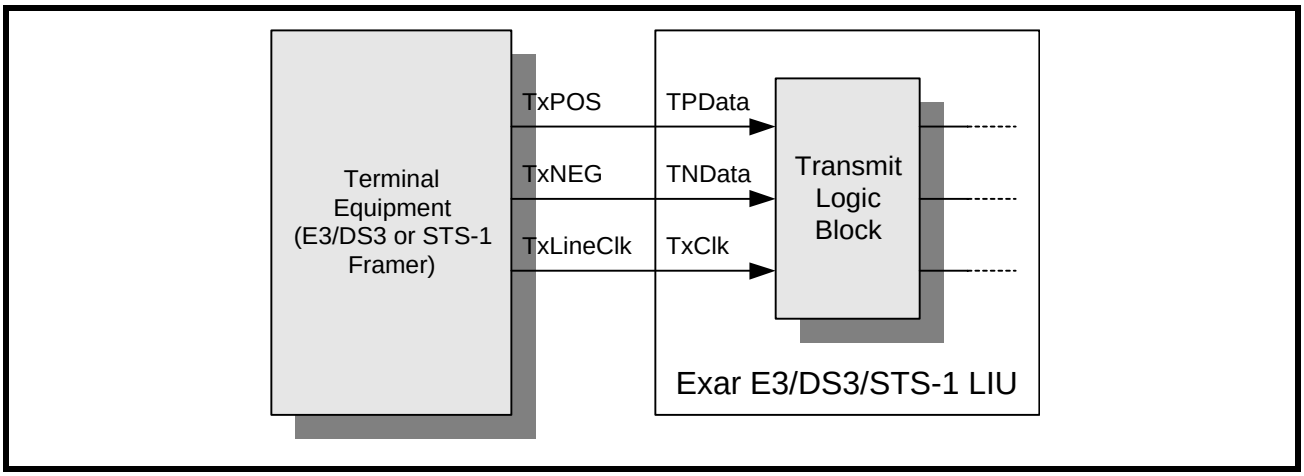
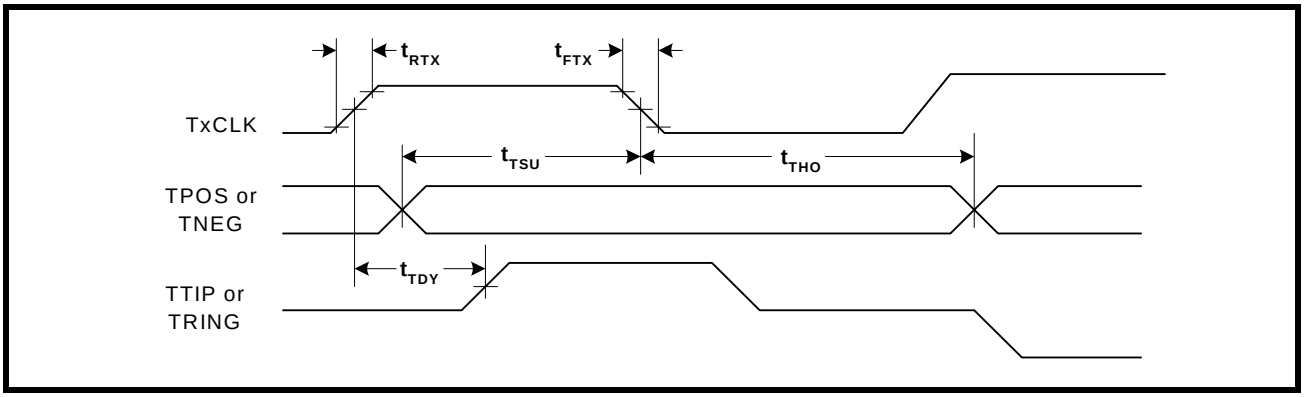
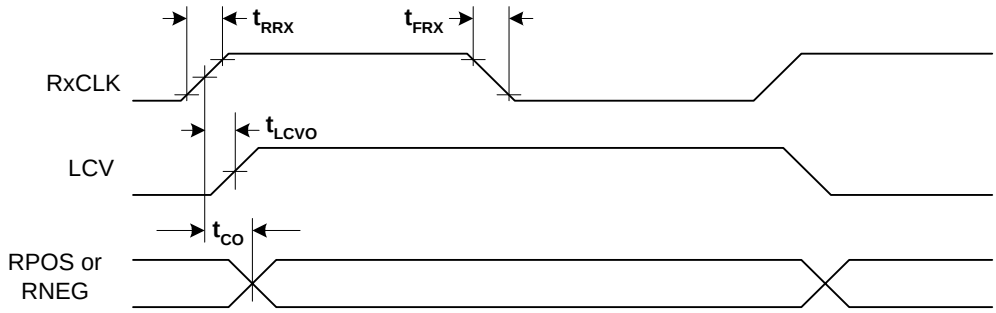


FIGURE 4. TRANSMITTER TERMINAL INPUT TIMING



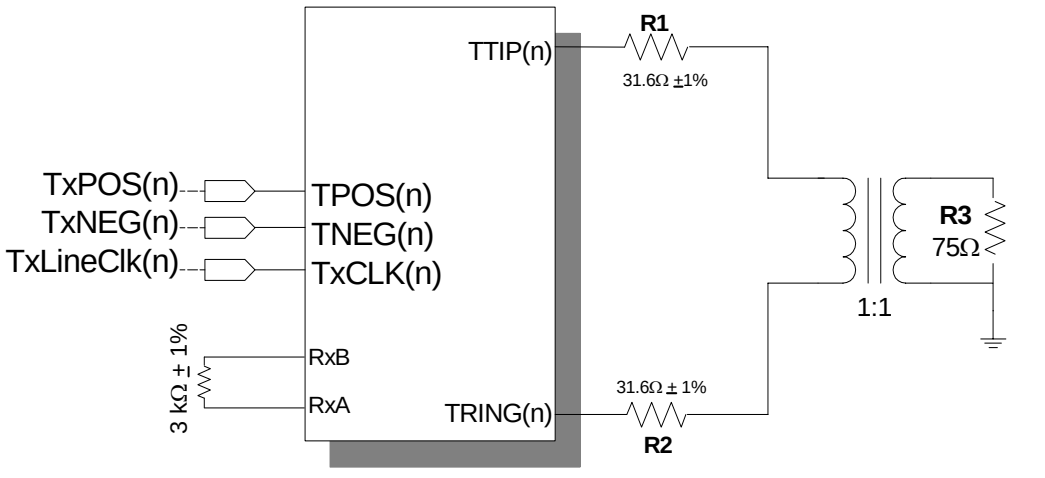
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle E3 DS3 STS-1	30	50 34.368 44.736 51.84	70	% MHz MHz MHz
t_{RTX}	TxCLK Rise Time (10% to 90%)			4	ns
t_{FTX}	TxCLKFall Time (10% to 90%)			4	ns
t_{TSU}	TPOS/TNEG to TxCLK falling set up time	3			ns
t_{THO}	TPOS/TNEG to TxCLK falling hold time	3			ns
t_{TDY}	TTIP/TRINGto TxCLK rising propagation delay time		8		ns

FIGURE 5. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
RxClk	Duty Cycle E3 DS3 STS-1	45	50 34.368 44.736 51.84	55	% MHz MHz MHz
t_{RRX}	RxCLK rise time (10% o 90%)		2	4	ns
t_{FRX}	RxCLKfalling time (10% to 90%)		2	4	ns
t_{CO}	RxCLKto RPOS/RNEG delay time			4	ns
t_{LCVO}	RxCLK to rising edge of LCV output delay		2.5		ns

FIGURE 6. TRANSMIT INTERFACE CIRCUIT FOR E3, DS3 AND STS-1 RATES



XRT75L04 (0nly one channel shown)

3.0 LINE SIDE CHARACTERISTICS:

3.1 E3 line side parameters:

The XRT75L04 line output at the transformer output meets the pulse shape specified in ITU-T G.703 for 34.368 Mbits/s operation. The pulse mask as specified in ITU-T G.703 for 34.368 Mbits/s is shown in Figure 7.

FIGURE 7. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

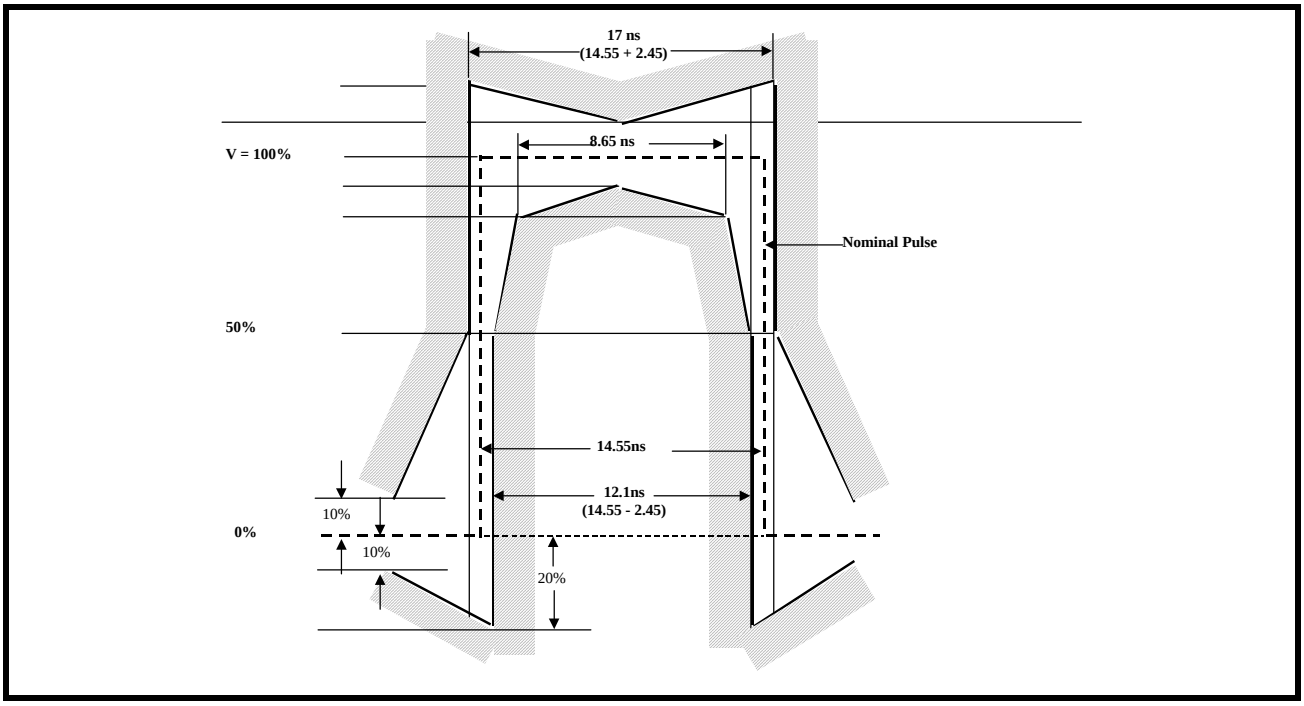


TABLE 3: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)		1200		feet
Interference Margin	-20	-16		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.30		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

NOTE: *The above values are at*

TA = 25^0C and V_{DD} = 3.3 V± 5%.

FIGURE 8. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

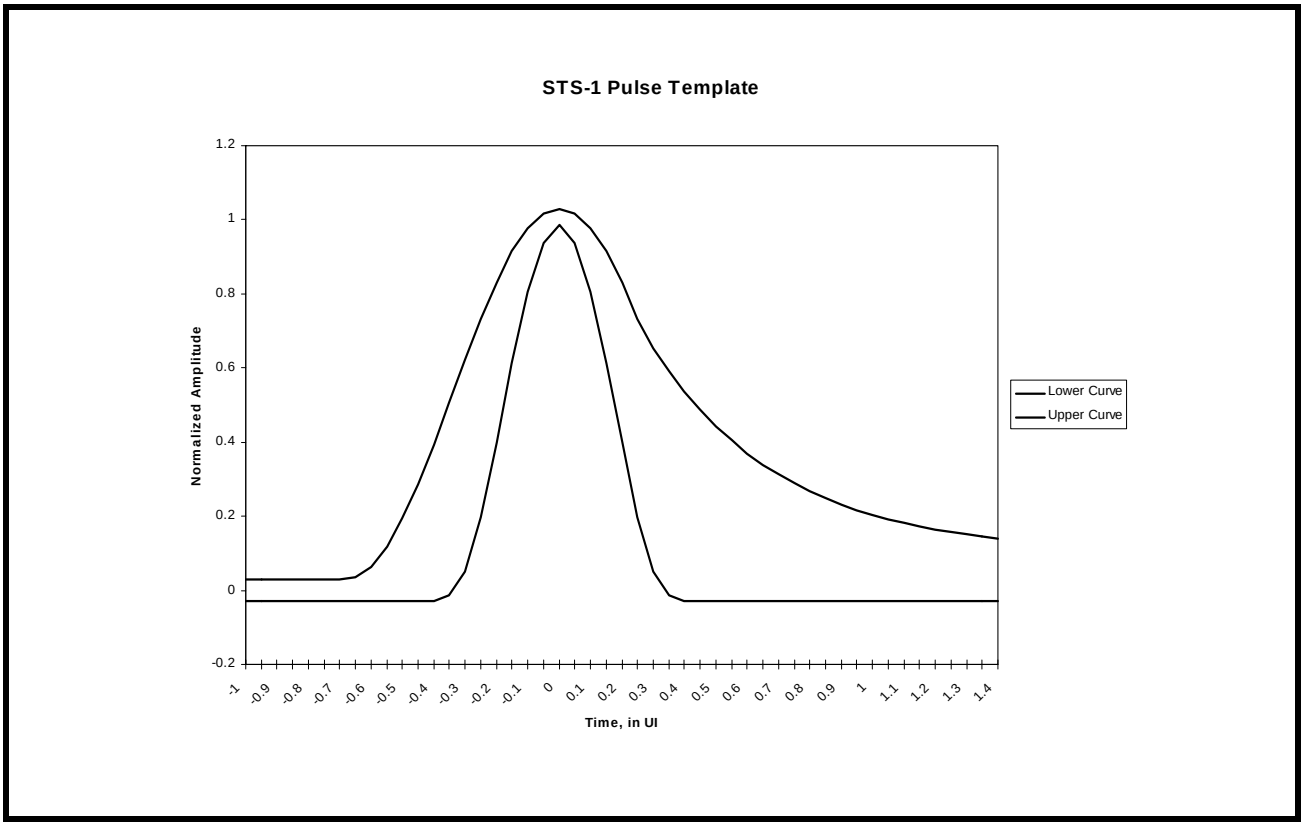


TABLE 4: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.38$	- 0.03
$-0.38 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 \times e^{-2.4[T-0.26]}$

TABLE 5: STS-1 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-253)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.90	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	8.6	9.65	10.6	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ Jitter Frequency 400 KHz	0.15	0.79		UI_{pp}

NOTE: *The above values are at*

TA = 25^0C and V_{DD} = 3.3 V ± 5%.

FIGURE 9. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

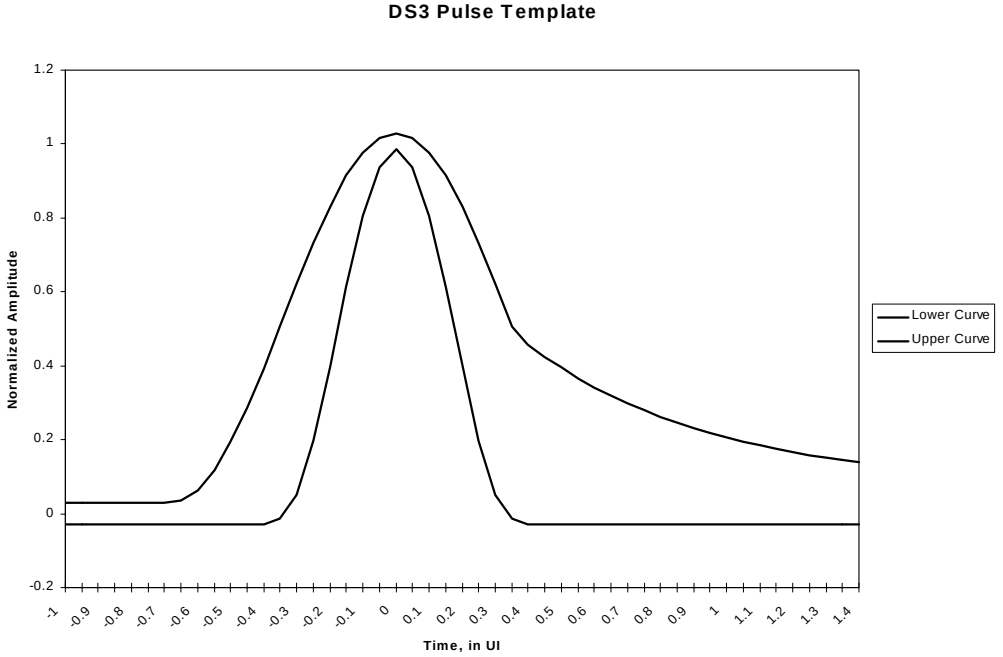


TABLE 6: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right] + 0.03$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 7: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10	
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)		0.60		UI_{pp}

NOTE: *The above values are at*

TA = 25^0C and V_{DD} = 3.3V ± 5%.

FIGURE 10. MICROPROCESSOR SERIAL INTERFACE STRUCTURE

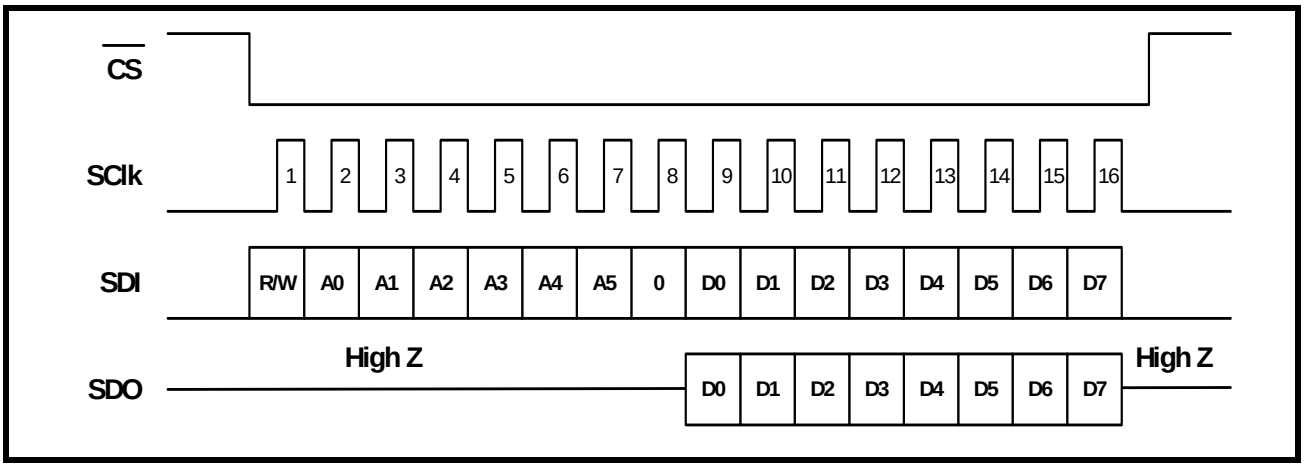


FIGURE 11. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

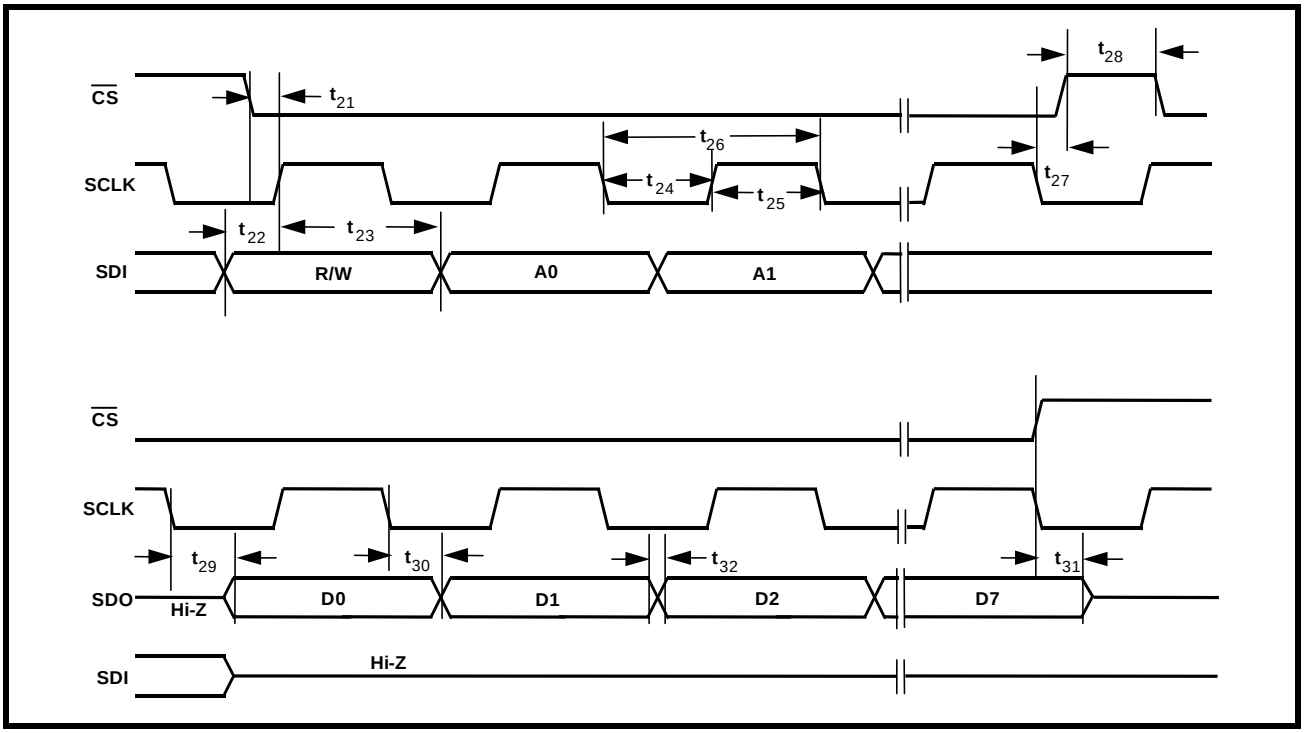


TABLE 8: MICROPROCESSOR SERIAL INTERFACE TIMINGS (T_A = 25^{0}C, V_{DD}=3.3V± 5% AND LOAD = 10PF)

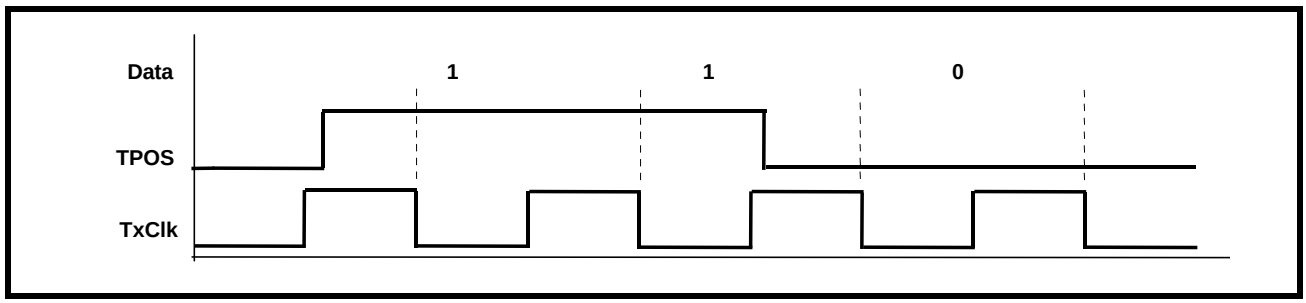
SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk	5			ns
t_{22}	SDI to Rising Edge of SClk	5			ns
t_{23}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{24}	SClk "Low" Time		25		ns
t_{25}	SClk "High" Time		25		ns
t_{26}	SClk Period		50		ns
t_{27}	Falling Edge of SClk to rising edge of $\overline{CS}$	0			ns
t_{28}	$\overline{CS}$ "Inactive" Time	50			ns
t_{29}	Falling Edge of SClk to SDO Valid Time			20	ns
t_{30}	Falling Edge of SClk to SDO Invalid Time			10	ns
t_{31}	Rising edge of $\overline{CS}$ to High Z		10		ns
t_{32}	Rise/Fall time of SDO Output			5	ns

4.0 THE TRANSMITTER SECTION:

The Transmitter Section, within each Channel, accepts TTL/CMOS level signals from the Terminal Equipment in selectable data formats.

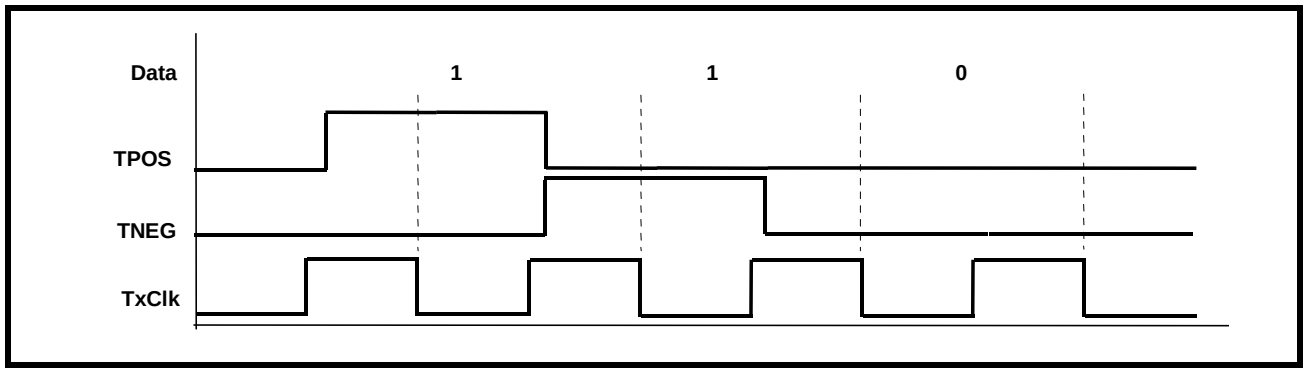
- Convert the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements. Figures 7, 8 and 9 illustrate the pulse template requirements.
- Encode the un-encoded NRZ data into either B3ZS format (for DS3 or STS-1) or HDB3 format (for E3) and convert to pulses with shapes and width that are compliant with industry standard pulse template requirements. Figures 7, 8 and 9 illustrate the pulse template requirements.
- In Single-Rail or un-encoded Non-Return-to-Zero (NRZ) mode, data is input via TPOS_n pins while TNEG_n pins must be grounded. The NRZ or Single-Rail mode is selected when the SR/DR input pin is "High" (in Hardware Mode) or bit 0 of channel control register is "1" (in Host Mode). Figure 12 illustrates the Single-Rail or NRZ format.

FIGURE 12. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)



- In Dual-Rail mode, data is input via TPOS_n and TNEG_n pins. TPOS_n contains positive data and TNEG_n contains negative data. The SR/DR input pin = "Low" (in Hardware Mode) or bit 0 of channel register = "0" (in Host Mode) enables the Dual-Rail mode. Figure 13 illustrates the Dual-Rail data format.

FIGURE 13. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED)



4.1 TRANSMIT CLOCK:

The Transmit Clock applied via TxClk_n pins, for the selected data rate (for E3 = 34.368 MHz, DS3 = 44.736 MHz or STS-1 = 51.84 MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle Transmit Clock to be supplied.

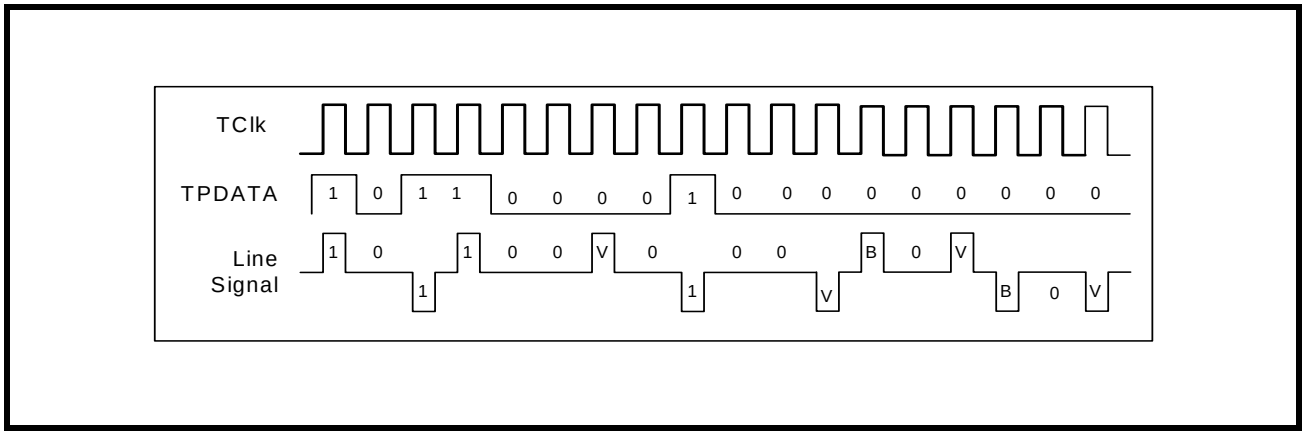
4.2 B3ZS/HDB3 ENCODER:

When the Single-Rail (NRZ) data format is selected, the Encoder Block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

4.2.1 B3ZS Encoding:

An example of B3ZS encoding is shown in Figure 14. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the Alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (e.g., a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of a DC component into the line signal.

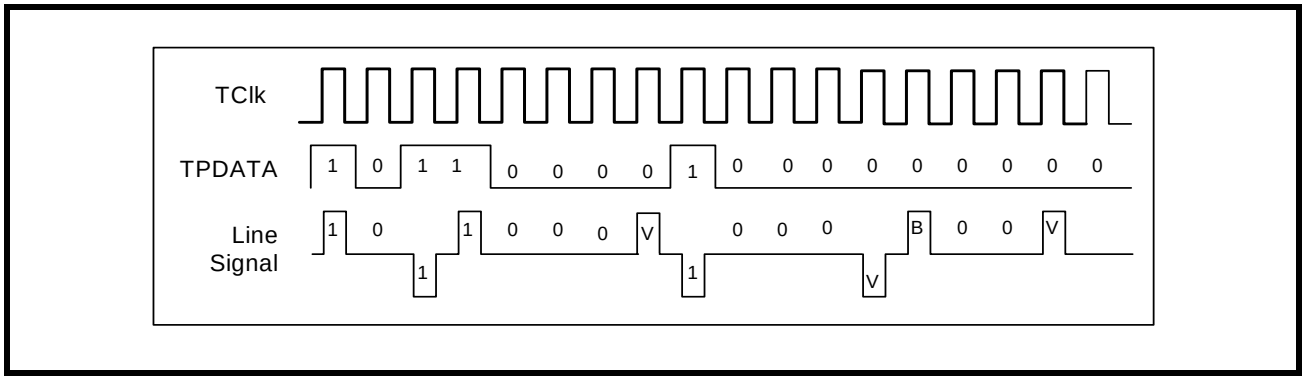
FIGURE 14. B3ZS ENCODING FORMAT



4.2.2 HDB3 Encoding:

An example of the HDB3 encoding is shown in Figure 15. If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either 000V or B00V pattern. The substitution code is made in such a way that an odd number of bipolar (B) pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.

FIGURE 15. HDB3 ENCODING FORMAT



NOTES:

1. *When Dual-Rail data format is selected, the B3ZS/HDB3 Encoder is automatically disabled.*
2. *In Dual-Rail format, the Bipolar Violations in the incoming data stream is converted to valid data pulses.*
3. *Encoder and Decoder is enabled only in Single-Rail mode.*

4.3 TRANSMIT PULSE SHAPER:

The Transmit Pulse Shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meet the industry standard mask template requirements for STS-1 and DS3. See Figures 8 and 9.

For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. This is illustrated in Figure 7.

The Pulse Shaper Block also includes a Transmit Build Out Circuit, which can either be disabled or enabled by setting the TxLEV_n input pin “High” or “Low” (in Hardware Mode) or setting the TxLEV_n bit to “1” or “0” in the control register (in Host Mode).

For DS3/STS-1 rates, the Transmit Build Out Circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet.

For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the Transmit Build Out Circuit is always disabled.

4.3.1 Guidelines for using Transmit Build Out Circuit:

If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system, is less than 225 feet, enable the Transmit Build Out Circuit by setting the TxLEV_n input pin “Low” (in Hardware Mode) or setting the TxLEV_n control bit to “0” (in Host Mode).

If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the Transmit Build Out Circuit.

4.3.2 Interfacing to the line:

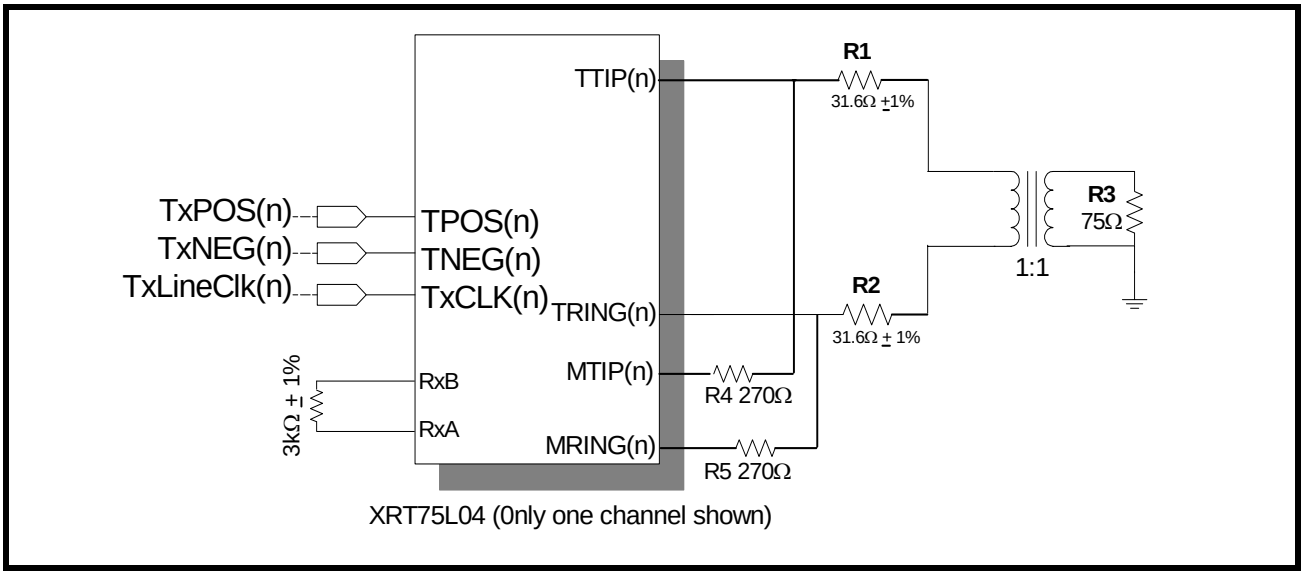
The differential line driver increases the transmit waveform to appropriate level and drives into the 75Ω load as shown in Figure 6.

4.4 Transmit Drive Monitor:

This feature is used for monitoring the transmit line for occurrence of fault conditions such as a short circuit on the line or a defective line driver.

To activate this function, connect MTIP_n pins to the TTIP_n lines via a 270 Ω resistor and MRing_n pins to TRing_n lines via 270 Ω resistor as shown in Figure 16.

FIGURE 16. TRANSMIT DRIVER MONITOR SET-UP.



Case 1:

MTIP_1 connected to TTIP_1

MRING_1 connected to TRING_1

TxMON_1 (bit) = 0

As shown in the figure 18, connect MTIP_1 to TTIP_1 and MRING_1 to TRING_1 via the 270 Ω resistors. When no transitions on the line are detected for 128 ± 32 TxClk_1 periods, the DMO_1 pin will toggle “High”.

The DMO_1 and the DMOIS_1 bits also will be set in the control register. When the transitions are detected, the DMO_1 pin will toggle back to normal state. The DMO_1 bit also will be cleared. However, the DMOIS_1 bit will remain set until read. If the DMOIE_1 bit has been set, an interrupt will be generated.

Case 2:

MTIP_1 connected to TTIP_1

MRING_1 connected to TRING_1

TxMON_1 (bit) = 1

This has the same effect as in Case 1. It is redundant to use the MTIP_1/MRING_1 pins in this case.

Case 3:

MTIP_1 not connected to TTIP_1

MRING_1 not connected to TRING_1

TxMON_1 (bit) = 1

When no transitions on the TTIP_1/TRING_1 are detected for 128 ± 32 TxClk_1 periods, the DMO_1 pin will toggle "High". The DMO_1 and the DMOIS_1 bits also will be set in the control register. When the transitions are detected, the DMO_1 pin will toggle back to normal state. The DMO_1 bit also will be cleared. However, the DMOIS_1 bit will remain set until read. If the DMOIE_1 bit has been set, an interrupt will be generated. Please note that the MTIP_1/MRING_1 pins cannot be used to monitor any other adjacent channels.

Case 4:

MTIP_m not connected to TTIP_m +n where m = 0,1...3 and n = 0,1...3

MRING_m not connected to TRING_m +n where m = 0,1...3 and n = 0,1...3

TxMON_n (bit) = 0

In this case, with external connection, any of the MTIP/MRING can be connected to any of the adjacent channel to be monitored.

Please note that if TxMON_n bit is set, then monitoring will be done for that channel n. By toggling the TxMON_n bit from 0 to 1, the monitoring can be switched between self-monitoring to monitoring any adajcent channels.

NOTE: *The Drive Monitor Circuit is only for diagnostic purpose and does not have to be used to operate the transmitter.*

4.5 Transmitter Section On/Off:

The transmitter section of each channel can either be turned on or off. To turn on the transmitter, set the input pin TxON_n to "High" (in Hardware Mode) or write a "1" to the TxON_n control bits (in Host Mode) with TxON_n pins tied "High".

When the transmitter is turned off, TTIP_n and TRing_n are tri-stated.

NOTES:

1. *This feature provides support for Redundancy.*
2. *If the XRT75L04 is configured in Host mode, to permit a system designed for redundancy to quickly shut-off the defective line card and turn on the back-up line card, writing a "1" to the TxON_n control bits transfers the control to TxON_n pins.*

5.0 THE RECEIVER SECTION:

This section describes the detailed operation of the various blocks in the receiver. The receiver recovers the TTL/CMOS level data from the incoming bipolar B3ZS or HDB3 encoded input pulses.

5.1 AGC/Equalizer:

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB.

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the

signal to reduce Inter-Symbol Interference (ISI) so that the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data.

The Equalizer can either be “IN” or “OUT” by setting the REQEN_n pin “High” or “Low” (in Hardware Mode) or setting the REQEN_n control bit to “1” or “0” (in Host Mode).

RECOMMENDATIONS FOR EQUALIZER SETTINGS:

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/ STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be left “IN” by setting the REQEN_n pin to “High” (in Hardware Mode) or setting the REQEN_n control bit to “1” (in Host Mode).

However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be left “OUT” for cable length less than 300 feet by setting the REQEN_n pin “Low” (in Hardware Mode) or by setting the REQEN_n control bit to “0” (in Host Mode).This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics.

NOTE: The results of extensive testing indicates that even when the Equalizer was left “IN” (REQEN_n = “HIGH”), regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.

The Equalizer also contain an additional 20 dB gain stage to provide the line monitoring capability of the resistively attenuated signals which may have 20dB flat loss. This capability can be turned on by writing a “1” to the RxMON_n bits in the control register or by setting the RxMON pin (pin 69) “High”.

5.1.1 Interference Tolerance:

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error-free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same recommendation is being used. Figure 17 shows the configuration to test the interference margin for DS3/ STS1. Figure 18 shows the set up for E3.

FIGURE 17. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1

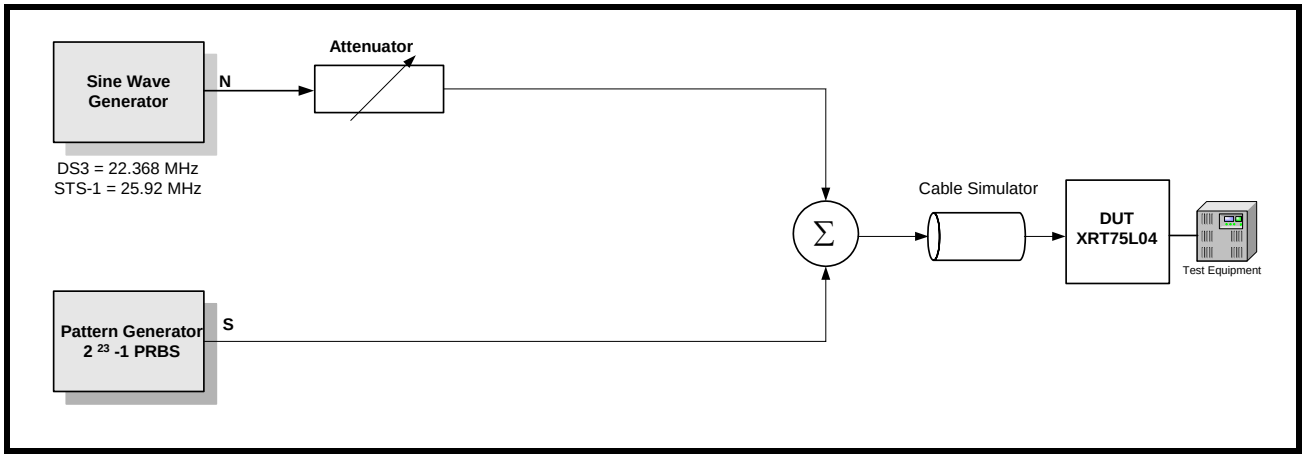


FIGURE 18. INTERFERENCE MARGIN TEST SET UP FOR E3.

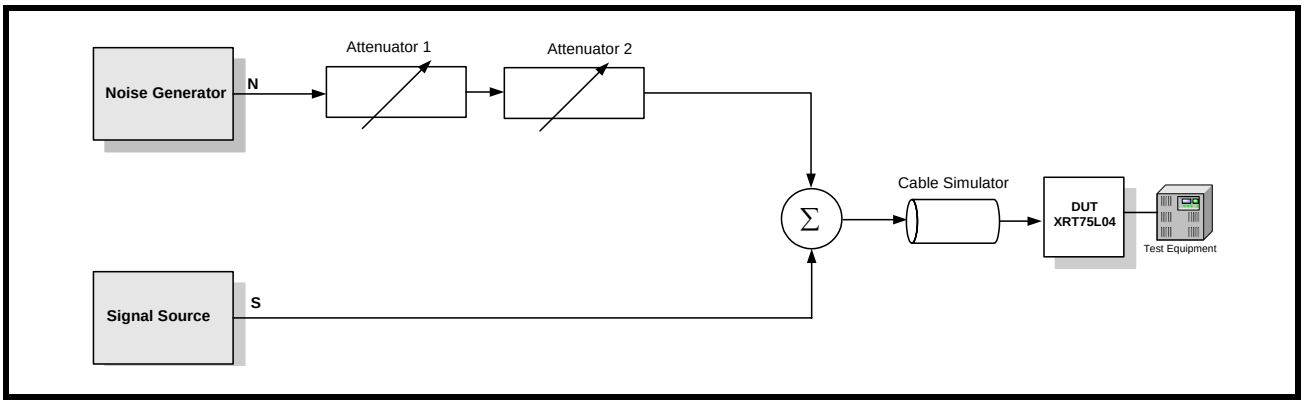


TABLE 9: INTERFERENCE MARGIN TEST RESULTS

MODE	CABLE LENGTH (ATTENUATION)	INTERFERENCE TOLERANCE
E3	0 dB	-14 dB
	12 dB	-18 dB
DS3	0 feet	-17 dB
	225 feet	-16 dB
	450 feet	-16dB
STS-1	0 feet	-16 dB
	225 feet	-15 dB
	450 feet	-15 dB

5.2 Clock and Data Recovery:

The Clock and Data Recovery Circuit extracts the embedded clock, RxClk_n from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder.

The Clock Recovery PLL can be in one of the following two modes:

TRAINING MODE:

In the absence of input signals at RTIP_n and RRing_n pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk_n input pins exceed 0.5%, a Loss of Lock condition is declared by toggling RLOL_n output pin “High” (in Hardware Mode) or setting the RLOL_n bit to “1” in the control registers (in Host Mode). Also, the clock output on the RxClk_n pins are the same as the reference clock applied on ExClk_n pins.

DATA/CLOCK RECOVERY MODE:

In the presence of input line signals on the RTIP_n and RRing_n input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk_n out pins is the Recovered Clock signal.

5.3 B3ZS/HDB3 Decoder:

The decoder block takes the output from clock and data recovery block and decodes the B3ZS (for DS3 or STS-1) or HDB3 (for E3) encoded line signal and detects any coding errors or excessive zeros in the data stream.

Whenever the input signal violates the B3ZS or HDB3 coding sequence for bipolar violation or contains three (for B3ZS) or four (for HDB3) or more consecutive zeros, an active “High” pulse is generated on the RLCV_n output pins to indicate line code violation.

NOTE: In Single- Rail (NRZ) mode, the decoder is bypassed.

5.4 LOS (Loss of Signal) Detector:

5.4.1 DS3/STS-1 LOS Condition:

A Digital Loss of SIgnal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS_n bit is set to “1” in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses.

Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 10.The status of the ALOS condition is reflected in the ALOS_n status control register.

RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS_n output pin is toggled “High” and the RLOS_n bit is set to “1” in the status control register.

TABLE 10: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF REQEN (DS3 AND STS-1 APPLICATIONS)

APPLICATION	REQEN SETTING	SIGNAL LEVEL TO DECLARE ALOS	SIGNAL LEVEL TO CLEAR ALOS
DS3	0	≤17 mV	≥70 mV
	1	≤20 mV	≥90 mV
STS-1	0	≤20 mV	≥90 mV
	1	≤25 mV	≥115 mV

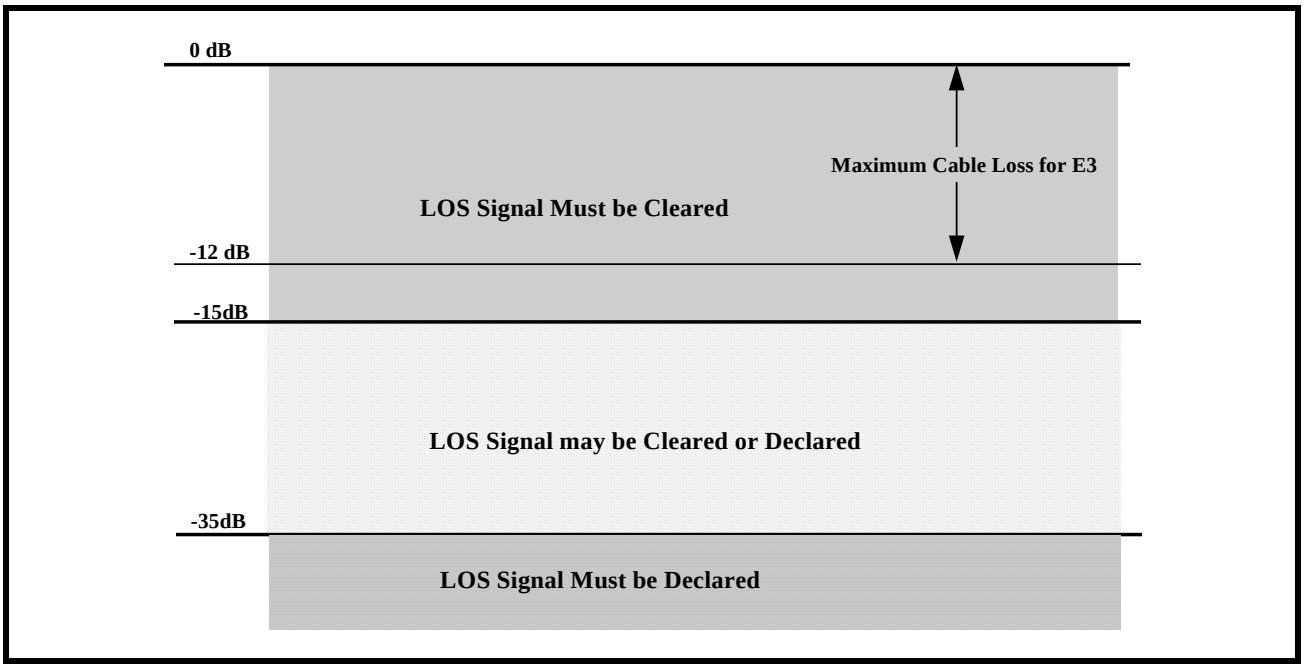
DISABLING ALOS/DLOS DETECTION:

For debugging purposes it is useful to disable the ALOS and/or DLOS detection. Writing a “1” to both ALOSDIS_n and DLOSDIS_n bits disables the LOS detection on a per channel basis.

5.4.2 E3 LOS Condition:

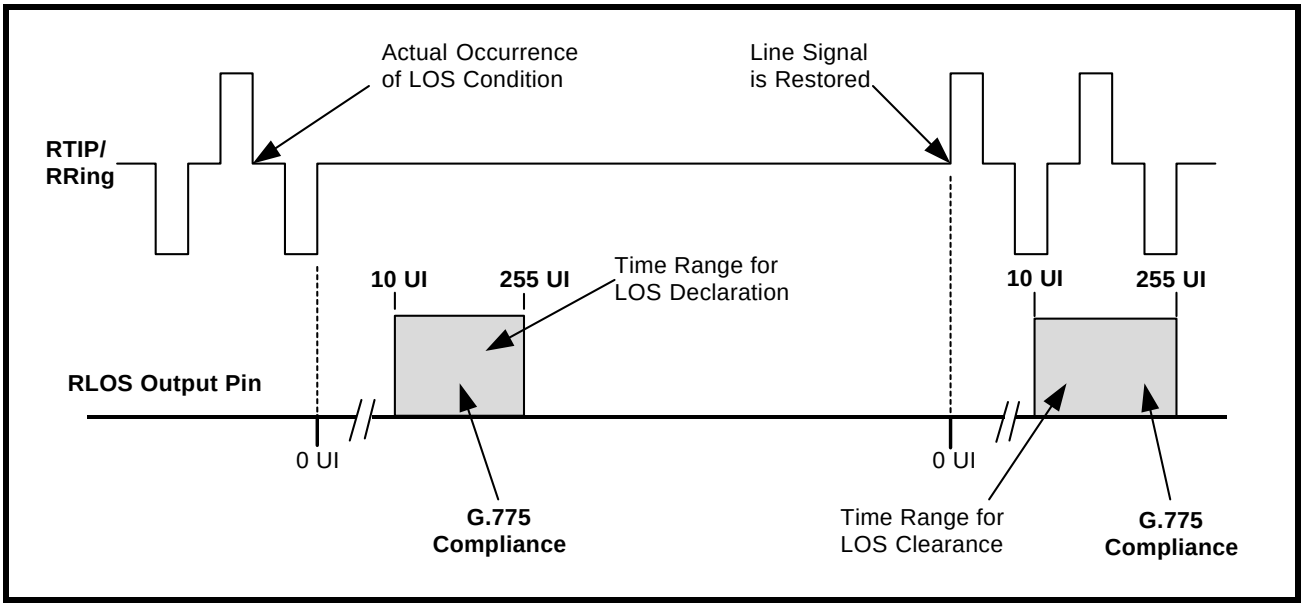
If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal level is defined to be between 15 and 35 dB below the normal level. If the signal drops below 35 dB for 175 ± 75 consecutive pulse periods, LOS condition is declared. This is illustrated in Figure 19.

FIGURE 19. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775



As defined in ITU-T G.775, an LOS condition is also declared between 10 and 255 UI (or E3 bit periods) after the actual time the LOS condition has occurred. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 20 shows the LOS declaration and clearance conditions.

FIGURE 20. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775.



5.4.3 Muting the Recovered Data with LOS condition:

When the LOS condition is declared, the clock recovery circuit locks into the reference clock applied to the ExClk_n pin and output this clock on the RxClk_n output.In Single Frequency Mode (SFM), the clock recovery locks into the rate clock generated and output this clock on the RxClk_n pins. The data on the RPOS_n and RNEG_n pins can be forced to zero by pulling the LOSMUT pin “High” (in Hardware Mode) or by setting the LOSMUT_n bits in the individual channel control register to “1” (in Host Mode).

NOTE: When the LOS condition is cleared, the recovered data is output on RPOS_n and RNEG_n pins.

6.0 JITTER:

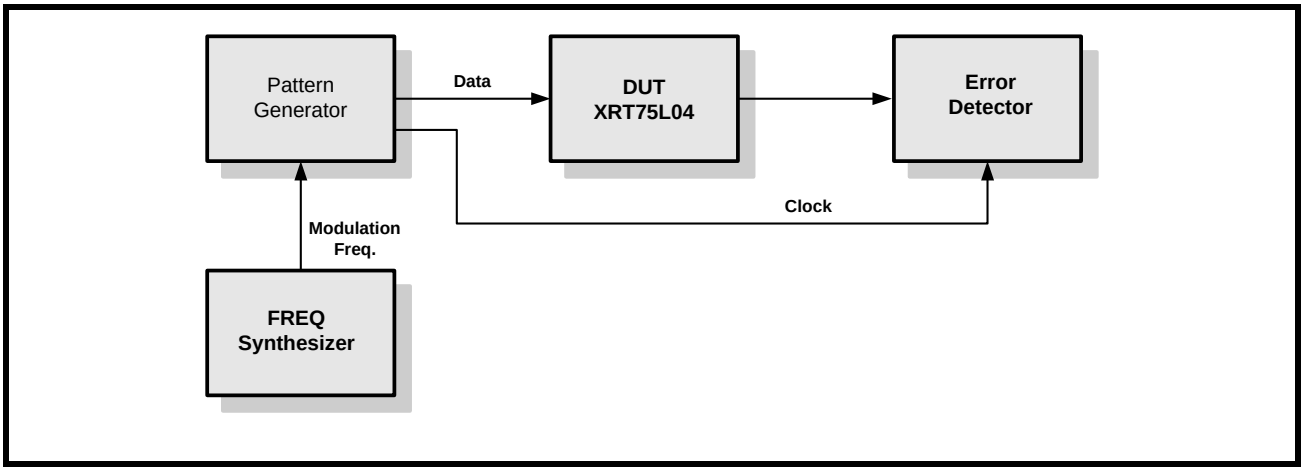
There are three fundamental parameters that describe circuit performance relative to jitter:

- **Jitter Tolerance (Receiver)**
- **Jitter Transfer (Receiver/Transmitter)**
- **Jitter Generation**

6.1 JITTER TOLERANCE - RECEIVER:

Jitter tolerance is a measure of how well a Clock and Data Recovery unit can successfully recover data in the presence of various forms of jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The tolerance depends on the frequency content of the jitter. Jitter Tolerance is measured as the jitter amplitude over a jitter spectrum for which the clock and data recovery unit achieves a specified bit error rate (BER). To measure the jitter tolerance as shown in Figure 21, jitter is introduced by the sinusoidal modulation of the serial data bit sequence.

FIGURE 21. JITTER TOLERANCE MEASUREMENTS

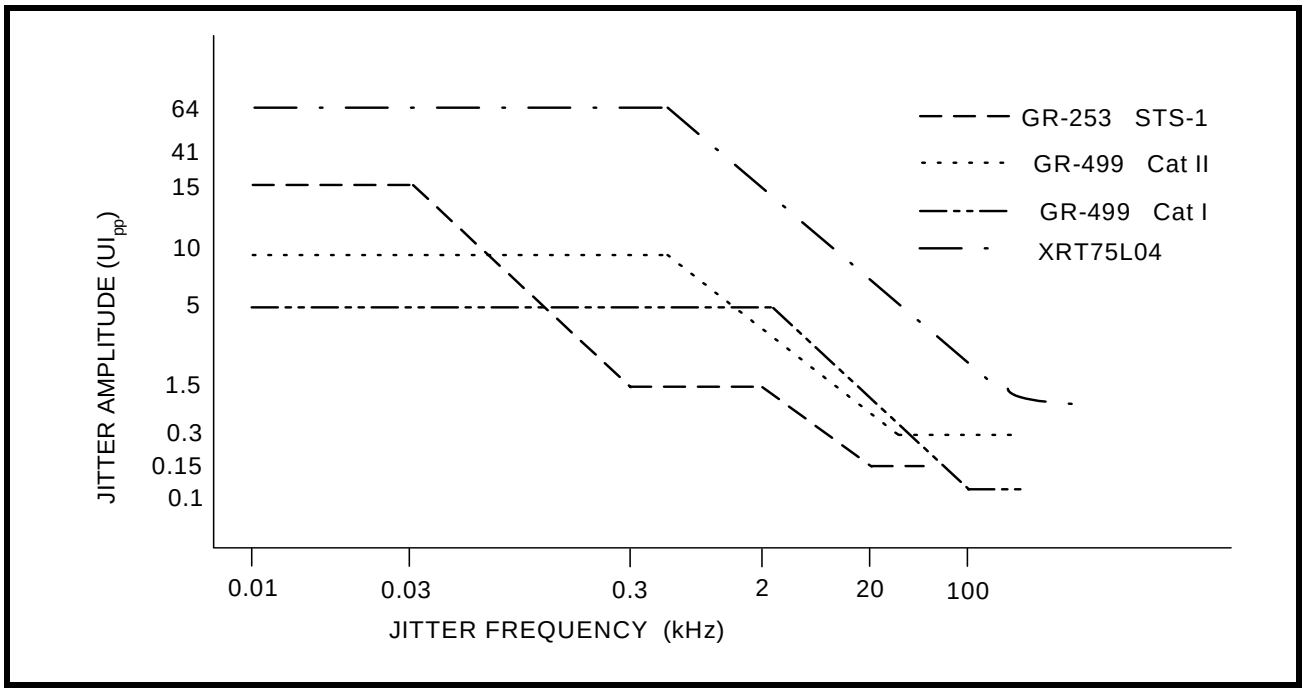


Input jitter tolerance requirements are specified in terms of compliance with jitter mask which is represented as a combination of points.Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency.

6.1.1 DS3/STS-1 Jitter Tolerance Requirements:

Bellcore GR-499 CORE, Issue 1, December 1995 specifies the minimum requirement of jitter tolerance for Category I and Category II. The jitter tolerance requirement for Category II is the most stringent. Figure 22 shows the jitter tolerance curve as per GR-499 specification.

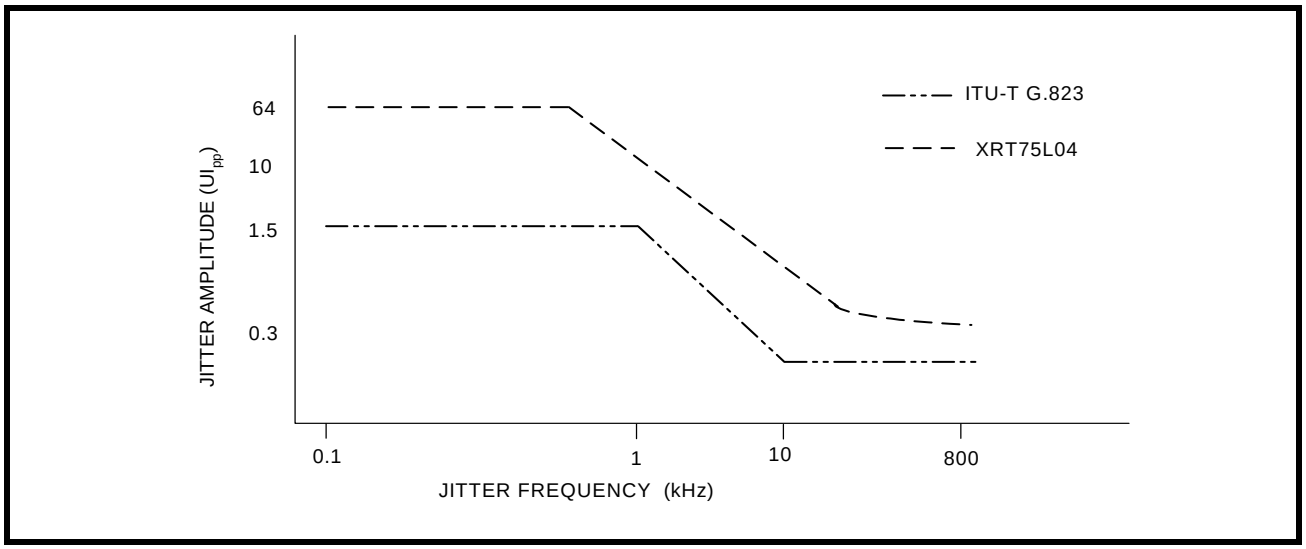
FIGURE 22. INPUT JITTER TOLERANCE FOR DS3/STS-1



6.1.2 E3 Jitter Tolerance Requirements:

ITU-T G.823 standard specifies that the clock and data recovery unit must be able to accommodate and tolerate jitter up to certain specified limits. Figure 23 shows the tolerance curve.

FIGURE 23. INPUT JITTER TOLERANCE FOR E3



As shown in the Figures 22 and 23 above, in the jitter tolerance measurement, the dark line indicates the minimum level of jitter that the E3/DS3/STS-1 compliant component must tolerate.

The Table 11 below shows the jitter amplitude versus the modulation frequency for various standards.

TABLE 11: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE)

BIT RATE (KB/S)	STANDARD	INPUT JITTER AMPLITUDE (UI_{P-P})			MODULATION FREQUENCY				
		A1	A2	A3	F1(HZ)	F2(HZ)	F3(KHZ)	F4(KHZ)	F5(KHZ)
34368	ITU-T G.823	1.5	0.15	-	100	1000	10	800	-
44736	GR-499 CORE Cat I	5	0.1	-	10	2.3k	60	300	-
44736	GR-499 CORE Cat II	10	0.3	-	10	669	22.3	300	-
51840	GR-253 CORE Cat II	15	1.5	0.15	10	30	300	2	20

6.2 JITTER TRANSFER - RECEIVER/TRANSMITTER:

Jitter Transfer function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency.

There are two distinct characteristics in jitter transfer: jitter gain (jitter peaking) defined as the highest ratio above 0dB; and jitter transfer bandwidth.The overall jitter transfer bandwidth is controlled by a low bandwidth loop, typically using a voltage-controller crystal oscillator (VCXO).

The jitter transfer function is a ratio between the jitter output and jitter input for a component, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter.A zero dB jitter transfer indicates the element had no effect on jitter.

Table 12 shows the jitter transfer characteristics and/or jitter attenuation specifications for various data rates:

TABLE 12: JITTER TRANSFER SPECIFICATION/REFERENCES

E3	DS3	STS-1
ETSI TBR-24	GR-499 CORE section 7.3.2 Category I and Category II	GR-253 CORE section 5.6.2.1

The above specifications can be met only with a jitter attenuator that supports E3/DS3/STS-1 rates.

6.3 JITTER GENERATION:

Jitter Generation is defined as the process whereby jitter appears at the output port of the digital equipment in the absence of applied input jitter. Jitter Generation is measured by sending jitter free data to the clock and data recovery circuit and measuring the amount of jitter on the output clock or the re-timed data. Since this is essentially a noise measurement, it requires a definition of bandwidth to be meaningful. The bandwidth is set according to the data rate. In general, the jitter is measured over a band of frequencies.

6.4 Jitter Attenuator:

An advanced crystal-less jitter attenuator per channel is included in the XRT75L04. The jitter attenuator requires no external crystal nor high-frequency reference clock.

In Host mode, by clearing or setting the JATx/$\overline{Rx}$_n bits in the channel control registers selects the jitter attenuator either in the Receive or Transmit path on per channel basis. In Hardware mode, JATx/$\overline{Rx}$ pin selects globally all three channels either in Receive or Transmit path.

The FIFO size can be either 16-bit or 32-bit. In HOST mode, the bits JA0_n and JA1_n can be set to appropriate combination to select the different FIFO sizes or to disable the Jitter Attenuator on a per channel basis. In Hardware mode, appropriate setting of the pins JA0 and JA1 selects the different FIFO sizes or disables the Jitter Attenuator for all three channels. Data is clocked into the FIFO with the associated clock

signal (TxClk or RxClk) and clocked out of the FIFO with the dejittered clock. When the FIFO is within two bits of overflowing or underflowing, the FIFO limit status bit, FL_n is set to “1” in the Alarm status register. Reading this bit clears the FIFO and resets the bit into default state.

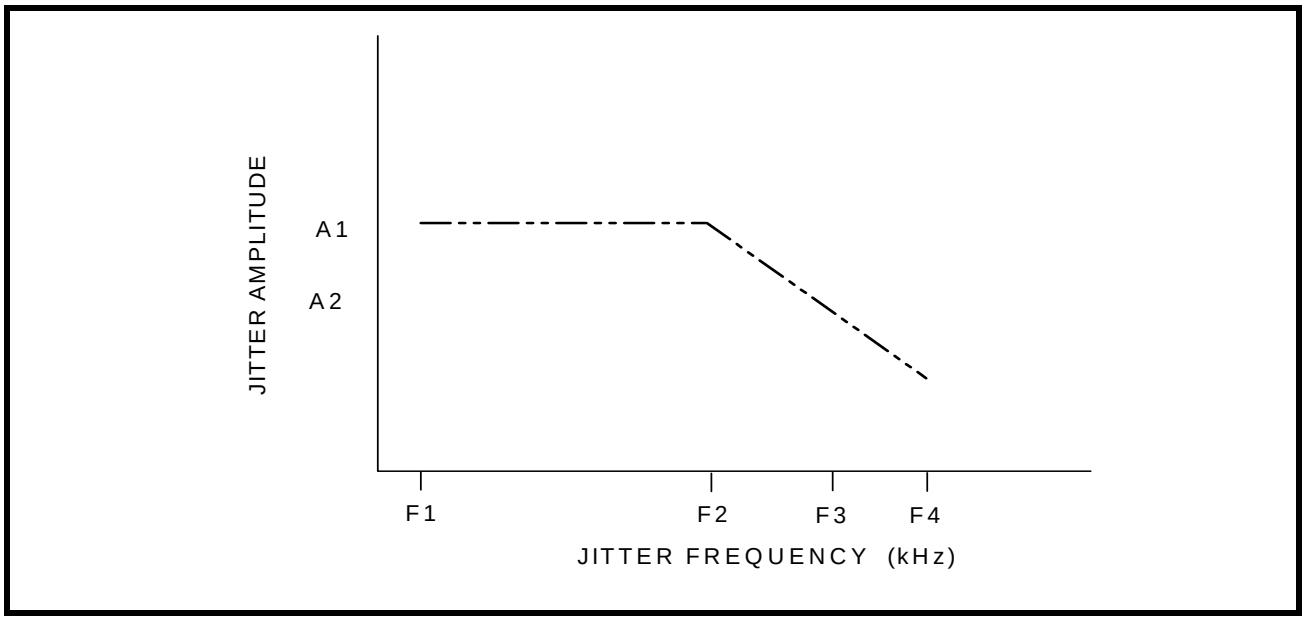
NOTE: *It is recommended to select the 16-bit FIFO for delay-sensitive applications as well as for removing smaller amounts of jitter. Table 13 specifies the jitter transfer mask requirements for various data rates:*

TABLE 13: JITTER TRANSFER PASS MASKS

RATE (KBITS)	MASK	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (KHZ)	A1(dB)	A2(dB)
34368	G.823 ETSI-TBR-24	100	300	3K	800K	0.5	-19.5
44736	GR-499, Cat I GR-499, Cat II GR-253 CORE	10 10 10	10k 56.6k 40	- - -	15k 300k 15k	0.1 0.1 0.1	- - -
51840	GR-253 CORE	10	40k	-	400k	0.1	-

The jitter attenuator in the XRT75L04 meets the latest jitter attenuation specifications and/or jitter transfer characteristics as shown in the Figure 24.

FIGURE 24. JITTER TRANSFER REQUIREMENTS AND JITTER ATTENUATOR PERFORMANCE



7.0 SERIAL HOST INTERFACE:

A serial microprocessor interface is included in the XRT75L04. The interface is generic and is designed to support the common microprocessors/microcontrollers. The XRT75L04 operates in Host mode when the HOST/$\overline{HW}$ pin is tied "High". The serial interface includes a serial clock (SClk), serial data input (SDI), serial data output (SDO), chip select (CS) and interrupt output (INT). The serial interface timing is shown in Figure 11.

The active low interrupt output signal ($\overline{INT}$ pin) indicates alarm conditions like LOS, DMO and FL to the processor.

When the XRT75L04 is configured in Host mode, the following input pins,TxLEV_n, TAOS_n, RLB_n, LLB_n, E3_n, STS-1/DS3_n, REQEN_n, JATx/Rx, JA0 and JA1 are disabled and must be connected to ground.

The Table 14 below illustrates the functions of the shared pins in either Host mode or in Hardware mode.

TABLE 14: FUNCTIONS OF SHARED PINS

PIN NUMBER	IN HOST MODE	IN HARDWARE MODE
86	$\overline{CS}$	RxClkINV
88	SClk	TxClkINV
87	SDI	RxON
85	SDO	RxMON
84	$\overline{INT}$	LOSMUT

NOTE: *While configured in Host mode, the TxON_n input pins will be active if the TxON_n bits in the control register are set to "1", and can be used to turn on and off the transmit output drivers. This permits a system designed for redundancy to quickly switch out a defective line card and switch-in the backup line card.*

TABLE 15: REGISTER MAP AND BIT NAMES

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x00	APS/Redundancy (read/write)	RxON-3	RxON-2	RxON-1	RxON_0	TxON_3	TxON_2	TxON_1	TxON_0
0x01-0x1F	Channel 0 - 3 Control Registers								
0x20	Interrupt Enable-Global (read/write)	Reserved				INTEN_3	INTEN_2	INTEN_1	INTEN_0
0x21	Interrupt Status (read only)	Reserved				INTST_3	INTST_2	INTST_1	INTST_0
0x22-0x2F	Reserved	Reserved							
0x30 - 0x37	PRBS Count Registers								
0x38	PRBS Holding Register								
0x39 - 0x3D	Reserved								

TABLE 15: REGISTER MAP AND BIT NAMES

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x3E	Chip_id (read only)	Device part number (7:0)							
0x3F	Chip_version (read only)	Chip revision number (7:0)							

TABLE 16: REGISTER MAP DESCRIPTION - GLOBAL

ADDRESS (HEX)	TYPE	REGISTER NAME	SYMBOL	DESCRIPTION	DEFAULT VALUE
0x00	R/W	APS/Redundancy	RxON_n	Bit 4 = RxON_0,Bit 5 = RxON_1,Bit 6 = RxON_2 and Bit 7 = RxON_3 Receiver Turn On. Writing a “1” to the bit field turns on the Receiver and a “0” turn off the Receiver.	0
			TxON_n	Bit 0 = TxON_0, Bit 1 = TxON_1, Bit 2 = TxON_2 and Bit 3 = TxON_3 Table below shows the status of the transmitter based on the bit and pin setting.	0
0x20	R/W	Interrupt Enable	INTEN_n	Bit 0 = INTEN_0, Bit 1 = INTEN_1, Bit 2 = INTEN_2 Bit 3 = INTEN_3. Writing a “1” to these bits enable the interrupts for the corresponding channels.	0
0x21	Read Only	Interrupt Status	INTST_n	Bit 0 = INTST_0, Bit 1 = INTST_1, Bit 2 = INTST_2 Bit 3 = INTST_3. Respective bits are set to “1” if an interrupt service is required. The respective source level interrupt status registers are read to determine the cause of interrupt.	0
0x22 - 0x2F	Reserved				
0x39 - 0x3D	Reserved				
0x3E	Read Only	Device Number	Chip_id	This read only register contains device id.	01110100
0x3F	Read Only	Version Number	Chip_version	This read only register contains chip version number	00000001

Bit	Pin	Transmitter Status
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

TABLE 17: REGISTER MAP AND BIT NAMES - CHANNEL 0 REGISTERS

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x01	Interrupt Enable (read/write)	Reserved		PRBSERCNTIE_0	PRBSERIE_0	FLIE_0	RLOLIE_0	RLOSIE_0	DMOIE_0
0x02	Interrupt Status (reset on read)	Reserved		PRBSERCNTIS_0	PRBSERIS_0	FLIS_0	RLOLIS_0	RLOSIS_0	DMOIS_0
0x03	Alarm Status (read only)	Reserved	PRBSLS_0	DLOS_0	ALOS_0	FL_0	RLOL_0	RLOS_0	DMO_0
0x04	Transmit Control (read/write)	Reserved		TxMON_0	INSPRBS_0	Reserved	TAOS_0	TxClkINV_0	TxLEV_0
0x05	Receive Control (read/write)	Reserved		DLOSDIS_0	ALOSDIS_0	RxClkINV_0	LOSMUT_0	RxMON_0	REQEN_0
0x06	Block Control (read/write)	Reserved		PRBSEN_0	RLB_0	LLB_0	E3_0	$\overline{\text{STS1}}$/$\overline{\text{DS3}}$_0	SR/$\overline{\text{DR}}$_0
0x07	Jitter Attenuator (read/write)	Reserved			DFLCK_0	PNTRST_0	JA1_0	JATx/$\overline{\text{Rx}}$_0	JA0_0
0x08	Reserved	Reserved							

TABLE 18: REGISTER MAP AND BIT NAMES - CHANNEL 1 REGISTERS

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x09	Interrupt Enable (read/write)	Reserved		PRBSERCNTIE_1	PRBSERIE_1	FLIE_1	RLOLIE_1	RLOSIE_1	DMOIE_1
0x0A	Interrupt Status (reset on read)	Reserved		PRBSERCNTIS_1	PRBSERIS_1	FLIS_1	RLOLIS_1	RLOSIS_1	DMOIS_1
0x0B	Alarm Status (read only)	Reserved	PRBSLS_1	DLOS_1	ALOS_1	FL_1	RLOL_1	RLOS_1	DMO_1
0x0C	Transmit Control (read/write)	Reserved		TxMON_1	INSPRBS_1	Reserved	TAOS_1	TxClkINV_1	TxLEV_1
0x0D	Receive Control (read/write)	Reserved		DLOSDIS_1	ALOSDIS_1	RxClkINV_1	LOSMUT_1	RxMON_1	REQEN_1
0x0E	Block Control (read/write)	Reserved		PRBSEN_1	RLB_1	LLB_1	E3_1	$\overline{\text{STS1}}$/$\overline{\text{DS3}}$_1	SR/$\overline{\text{DR}}$_1
0x0F	Jitter Attenuator (read/write)	Reserved			DFLCK_1	PNTRST_1	JA1_1	JATx/$\overline{\text{Rx}}$_1	JA0_1

TABLE 18: REGISTER MAP AND BIT NAMES - CHANNEL 1 REGISTERS

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x10	Reserved	Reserved							

TABLE 19: REGISTER MAP AND BIT NAMES - CHANNEL 2 REGISTERS

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x11	Interrupt Enable (read/write)	Reserved		PRBSERCNTIE_2	PRBSERIE_2	FLIE_2	RLOLIE_2	RLOSIE_2	DMOIE_2
0x12	Interrupt Status (reset on read)	Reserved		PRBSERCNTIS_2	PRBSERIS_2	FLIS_2	RLOLIS_2	RLOSIS_2	DMOIS_2
0x13	Alarm Status (read only)	Reserved	PRBSLS_2	DLOS_2	ALOS_2	FL_2	RLOL_2	RLOS_2	DMO_2
0x14	Transmit Control (read/write)	Reserved		TxMON_2	INSPRBS_2	Reserved	TAOS_2	TxClkINV_2	TxLEV_2
0x15	Receive Control (read/write)	Reserved		DLOSDIS_2	ALOSDIS_2	RxClkINV_2	LOSMUT_2	RxMON_2	REQEN_2
0x16	Block Control (read/write)	Reserved		PRBSEN_2	RLB_2	LLB_2	E3_2	$\overline{\text{STS1}}$/$\overline{\text{DS3}}$_2	SR/$\overline{\text{DR}}$_2
0x17	Jitter Attenuator (read/write)	Reserved			DFLCK_2	PNTRST_2	JA1_2	JATx/$\overline{\text{Rx}}$_2	JA0_2
0x18	Reserved	Reserved							

TABLE 20: REGISTER MAP AND BIT NAMES - CHANNEL 3 REGISTERS

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x19	Interrupt Enable (read/write)	Reserved		PRBSERCNTIE_3	PRBSERIE_3	FLIE_3	RLOLIE_3	RLOSIE_3	DMOIE_3
0x1A	Interrupt Status (reset on read)	Reserved		PRBSERCNTIS_3	PRBSERIS_3	FLIS_3	RLOLIS_3	RLOSIS_3	DMOIS_3
0x1B	Alarm Status (read only)	Reserved	PRBSLS_3	DLOS_3	ALOS_3	FL_3	RLOL_3	RLOS_3	DMO_3
0x1C	Transmit Control (read/write)	Reserved		TxMON_3	INSPRBS_3	Reserved	TAOS_3	TxClkINV_3	TxLEV_3

TABLE 20: REGISTER MAP AND BIT NAMES - CHANNEL 3 REGISTERS

ADDRESS (HEX)	PARAMETER NAME	DATA BITS							
		7	6	5	4	3	2	1	0
0x1D	Receive Control (read/write)	Reserved		DLOSDIS_3	ALOSDIS_3	RxClkINV_3	LOSMUT_3	RxMON_3	REQEN_3
0x1E	Block Control (read/write)	Reserved		PRBSEN_3	RLB_3	LLB_3	E3_3	$\overline{\text{STS1}}$/ $\overline{\text{DS3}}$_3	SR/$\overline{\text{DR}}$_3
0x1F	Jitter Attenuator (read/write)	Reserved			DFLCK_3	PNTRST_3	JA1_3	JATx/ $\overline{\text{Rx}}$_3	JA0_3

TABLE 21: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	REGISTER NAME	BIT#	SYMBOL	DESCRIPTION	DEFAULT VALUE
0x01 (ch 0) 0x09 (ch 1) 0x11 (ch 2) 0x19 (ch 3)	R/W	Interrupt Enable (source level)	D0	DMOIE_n	Set this bit to enable an interrupt when the no transmission detected on channel output.	0
			D1	RLOSIE_n	Writng a “1” to this bit enables an interrupt when Recieve Los of Signal is detected.	0
			D2	RLOLIE_n	Writing a “1” to this bit enables an interrupt when Receive Loss of Lock condition is detected	0
			D3	FLIE_n	Writing a “1” to this bit enables the interrupt when the FIFO Limit of the Jitter Attenuator is within 2 bits of overflow/underflow condition. ***NOTE:*** *This bit field is ignored when the Jitter Attenuator is disabled.*	0
			D4	PRBSERIE_n	Set this bit to enable the interrupt when the PRBS error is detected.	0
			D5	PRBSERCNTIE_n	Set this bit to enable the interrupt when the PRBS error count register saturates.	0
			D7-D6	Reserved		

TABLE 21: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	REGISTER NAME	BIT#	SYMBOL	DESCRIPTION	DEFAULT VALUE
0x02 (ch 0) 0x0A (ch 1) 0x12 (ch 2) 0x1A (ch 3)	Reset on Read	Interrupt Status (source level)	D0	DMOIS_n	This bit is set every time a DMO status change has occurred since the last cleared interrupt. This bit is cleared when the register bit is read.	0
			D1	RLOSIS_n	This bit is set every time a RLOS status change has occurred since the last cleared interrupt. This bit is cleared when the register bit is read.	0
			D2	RLOLIS_n	This bit is set every time a RLOL status change has occurred since the last cleared interrupt. This bit is cleared when the register bit is read.	0
			D3	FLIS_n	This bit is set every time a FIFO Limit status change has occurred since the last cleared interrupt. This bit is cleared when the register bit is read.	0
			D4	PRBSERIS_n	This bit is set when the PRBS error occurs.	0
			D5	PRBSERCNTIS_n	This bit is set when the PRBS error count register saturates.	0
			D7-D6	Reserved		
0x03 (ch 0) 0x0B (ch 1) 0x13 (ch 2) 0x1B (ch 3)	Read Only	Alarm Status	D0	DMO_n	This bit is set when no transitions on the TTIP/TRING have been detected for 128 ± 32 TxCLK periods.	0
			D1	RLOS_n	This bit is set every time the receiver declares an LOS condition.	0
			D2	RLOL_n	This bit is set every time when the receiver declares a Loss of Lock condition.	0
			D3	FL_n	This bit is set every time the FIFO in the Jitter Attenuator is within 2 bit of underflow/overflow condition.	0
			D4	ALOS_n	This bit is set every time the receiver declares Analog LOS condition.	0
			D5	DLOS_n	This bit is set every time the receiver declares Digital LOS condition.	0
			D6	PRBSLS_n	This bit is set every time the PRBS detector is not in sync.	0
			D7	Reserved		

TABLE 21: REGISTER MAP DESCRIPTION

ADDRESS (HEX)	TYPE	REGISTER NAME	BIT#	SYMBOL	DESCRIPTION	DEFAULT VALUE
0x04 (ch 0) 0x0C (ch 1) 0x14 (ch 2) 0x!C (ch 3)	R/W	Transmit Control	D0	TxLEV_n	Set this bit for cable length greater than 225 feet. ***NOTE:*** *See section 4.03 for detailed description.*	0
			D1	TxClkINV_n	Set this bit to sample the data on TPOS/TNEG pins on the rising edge of TxClk.	0
			D2	TAOS_n	Set this bit to send a continuous stream of marks (All Ones) out at the TTIP and TRing pins.	0
			D3	Reserved		
			D4	INSPRBS_n	Setting this bit causes the PRBS generator to insert a single-bit error onto the transmit PRBS data stream . ***NOTE:*** *PRBS Generator/Detector must be enabled for this bit to have any effect.*	0
			D5	TxMON_n	Setting this bit causes the driver monitor its own transmit driver. When the transmit failure is detected, DMO output pin goes "High" and DMOIS bit is set. When this bit is "0", MTIP and MRing are connected to other transmit channel for monitoring.	0
			D7-D6	Reserved		
0x05 (Ch 0) 0x0D (Ch 1) 0x15 (Ch 2) 0x1D (ch 3)	R/W	Receive Control	D0	REQEN_n	Set this bit to enable the Receive Equalizer. ***NOTE:*** *See section 5.01 for detailed description.*	0
			D1	RxMON_n	Set this bit to configure the Receiver in monitoring mode. In this mode, the Receiver can monitor a signal at the RTIP/RRing pins that has be attenuated up to 20dB flat loss.	0
			D2	LOSMUT_n	Setting this bit causes the RPOS/RNEG outputs to "0" while the LOS condition is declared. ***NOTE:*** *If this bit has been set, it will remain set even after the LOS condition is cleared.*	0
			D3	RxClkINV_n	Set this bit to configure the Receiver to output RPOS/RNEG data on the falling edge of RxClk_0.	0
			D4	ALOSDIS_n	Set this bit to disable the ALOS detector.	0
			D5	DLOSDIS_n	Set this bit to disable the DLOS detector.	0
			D7-D6	Reserved		

TABLE 21: REGISTER MAP DESCRIPTION

<table>
<tr><th>ADDRESS (HEX)</th><th>TYPE</th><th>REGISTER NAME</th><th>BIT#</th><th>SYMBOL</th><th>DESCRIPTION</th><th>DEFAULT VALUE</th></tr>
<tr><td rowspan="8">0x06 (Ch 0)
0x0E (Ch 1)
0x16 (Ch 2)
0x1E 9ch 3)</td><td rowspan="8">R/W</td><td rowspan="8">Block Control</td><td>D0</td><td>SR/$\overline{DR}$_n</td><td>Setting this bit configures the Receiver and Transmitter in Single-Rail (NRZ) mode.
NOTE: See section 4.0 for detailed description.</td><td>0</td></tr>
<tr><td>D1</td><td>$\overline{STS}$-1/ $\overline{DS3}$_n</td><td>Setting this bit configures the channel into STS-1 mode.
NOTE: This bit field is ignored if the channel is configured to operate in E3 mode.</td><td>0</td></tr>
<tr><td>D2</td><td>E3_n</td><td>Setting this bit configures the channel in E3 mode.</td><td>0</td></tr>
<tr><td>D3</td><td>LLB_n</td><td>Setting this bit configures the channel in Local Loopback mode.</td><td>0</td></tr>
<tr><td>D4</td><td>RLB_n</td><td>Setting this bit configures the channel in Remote Loopback mode.
<table>
<tr><th>RLB_n</th><th>LLB_n</th><th>Loopback Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal Operation</td></tr>
<tr><td>0</td><td>1</td><td>Analog Local</td></tr>
<tr><td>1</td><td>0</td><td>Remote</td></tr>
<tr><td>1</td><td>1</td><td>Digital</td></tr>
</table></td><td>0</td></tr>
<tr><td>D5</td><td>PRBSEN_n</td><td>Setting this bit enables the PRBS generator/detector. PRBS generator generate and detect either 2^{15}-1 (DS3 or STS-1) or 2^{23}-1 (for E3).
The pattern generated and detected are unframed pattern.</td><td>0</td></tr>
<tr><td>D7-D6</td><td colspan="3">Reserved</td></tr>
</table>

TABLE 21: REGISTER MAP DESCRIPTION

<table>
<tr><th>ADDRESS (HEX)</th><th>TYPE</th><th>REGISTER NAME</th><th>BIT#</th><th>SYMBOL</th><th>DESCRIPTION</th><th>DEFAULT VALUE</th></tr>
<tr><td rowspan="6">0x07 (Ch 0)
0x0F (Ch 1)
0x17 (Ch 2)
0x1F (ch 3)</td><td rowspan="6">R/W</td><td rowspan="6">Jitter Attenuator</td><td>D0</td><td>JA0_n</td><td>This bit along with JA1_n bit configures the Jitter Attenuator as shown in the table below.

<table><tr><th>JA0_n</th><th>JA1_n</th><th>Mode</th></tr><tr><td>0</td><td>0</td><td>16 bit FIFO</td></tr><tr><td>0</td><td>1</td><td>32 bit FIFO</td></tr><tr><td>1</td><td>0</td><td>Disable Jitter Attenuator</td></tr><tr><td>1</td><td>1</td><td>Disable Jitter Attenuator</td></tr></table></td><td>0</td></tr>
<tr><td>D1</td><td>JATx/$\overline{Rx}$_n</td><td>Setting this bit selects the Jitter Attenuator in the Transmit Path. A “0” selects in the Receive Path.</td><td>0</td></tr>
<tr><td>D2</td><td>JA1_n</td><td>This bit along with the JA0_n configures the Jitter Attenuator as shown in the table.</td><td>0</td></tr>
<tr><td>D3</td><td>PNTRST_n</td><td>Setting this bit resets the Read and Write pointers of the jitter attenuator FIFO.</td><td>0</td></tr>
<tr><td>D4</td><td>DFLCK_n</td><td>Set this bit to “1” to disable fast locking of the PLL. This helps to reduce the time for the PLL to lock to incoming frequeny when Jitter Attenuator switches to narrow band.</td><td>0</td></tr>
<tr><td>D7-D5</td><td colspan="2">Reserved</td></tr>
<tr><td>0x30 (Ch 0)
0x32 (Ch 1)
0x34 (Ch 2)
0x36 (ch 3)</td><td>RO</td><td>PRBS COUNT REG</td><td colspan="3">PRBS COUNT REGISTER MSB</td><td>0</td></tr>
<tr><td>0x31 (Ch 0)
0x33 (Ch 1)
0x35 (Ch 2)
0x37 (ch 3)</td><td>RO</td><td>PRBS COUNT REG</td><td colspan="3">PRBS COUNT REGISTER LSB</td><td>0</td></tr>
<tr><td>0x38</td><td>RO</td><td>PRBS HOLDING REG</td><td colspan="3">PRBS HOLDING REGISTER</td><td>0</td></tr>
<tr><td>0x08
0x10
0x18</td><td colspan="6">Reserved</td></tr>
</table>

8.0 DIAGNOSTIC FEATURES:

8.1 PRBS Generator and Detector:

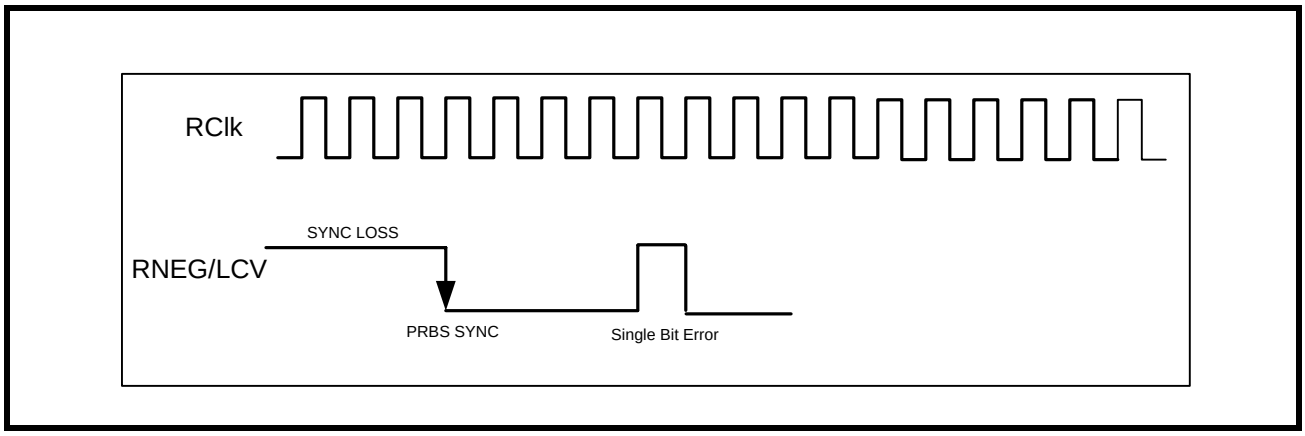
The XRT75L04 contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. This feature is only available in Host mode. With the PRBSEN_n bit = "1", the transmitter will send out PRBS of 2^{23}-1 in E3 rate or 2^{15}-1 in STS-1/DS3 rate. At the same time, the receiver PRBS detector is also enabled. When the correct PRBS pattern is detected by the receiver, the RNEG/LCV pin will go "Low" to indicate PRBS synchronization has been achieved. When the PRBS detector is not in sync the PRBSLS bit will be set to "1" and RNEG/LCV pin will go "High".

With the PRBS mode enabled, the user can also insert a single bit error by toggling "INSPRBS" bit. This is done by writing a "1" to INSPRBS bit. The receiver at RNEG/LCV pin will pulse "High" for one RxClk cycle for every bit error detected. Any subsequent single bit error insertion must be done by first writing a "0" to INSPRBS bit and followed by a "1".

Figure 25 shows the status of RNEG/LCV pin when the XRT75L04 is configured in PRBS mode.

NOTE: *In PRBS mode, the device is forced to operate in Single-Rail Mode.*

FIGURE 25. PRBS MODE



8.2 LOOPBACKS:

The XRT75L04 offers three loopback modes for diagnostic purposes. In Hardware mode, the loopback modes are selected via the RLB_n and LLB_n pins. In Host mode, the RLB_n and LLB_n bits n the Channel control registers select the loopback modes.

8.2.1 ANALOG LOOPBACK:

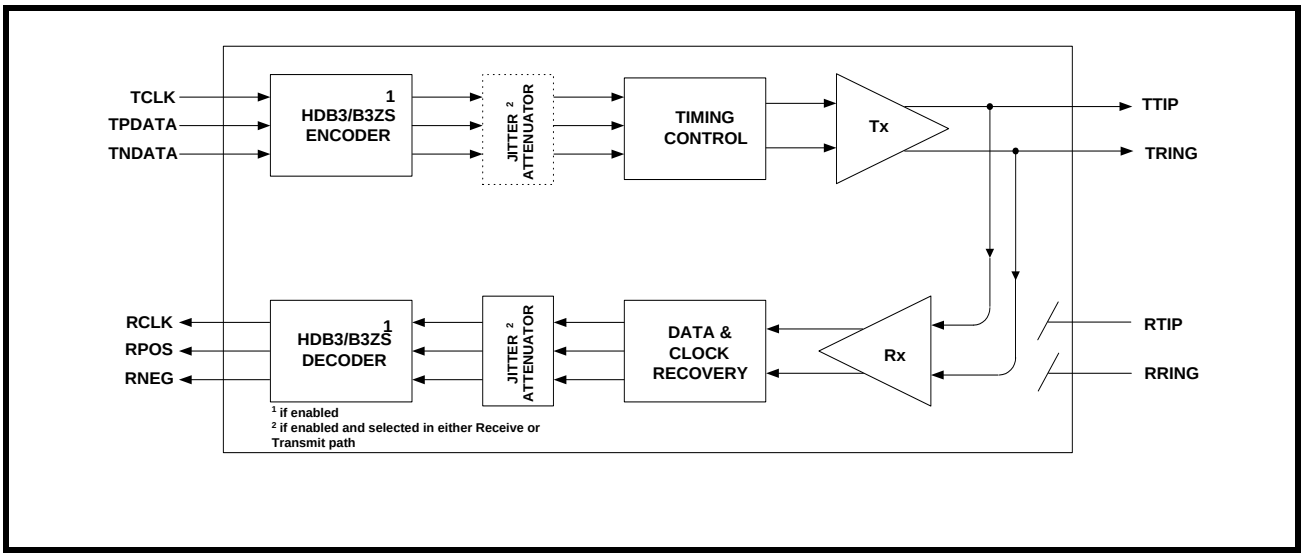
In this mode, the transmitter outputs (TTIP_n and TRING_n) are connected internally to the receiver inputs (RTIP_n and RRING_n) as shown in Figure 26. Data and clock are output at RCLK_n, RPOS_n and RNEG_n pins for the corresponding transceiver. Analog loopback exercises most of the functional blocks of the device including the jitter attenuator which can be selected in either the transmit or receive path.

XRT75L04 can be configured in Analog Loopback either in Hardware mode via the LLB_n and RLB_n pins or in Host mode via LLB_n and RLB_n bits in the channel control registers.

NOTES:

1. *In the Analog loopback mode, data is also output via TTIP_n and TRING_n pins.*
2. *Signals on the RTIP_n and RRING_n pins are ignored during analog loopback.*

FIGURE 26. ANALOG LOOPBACK

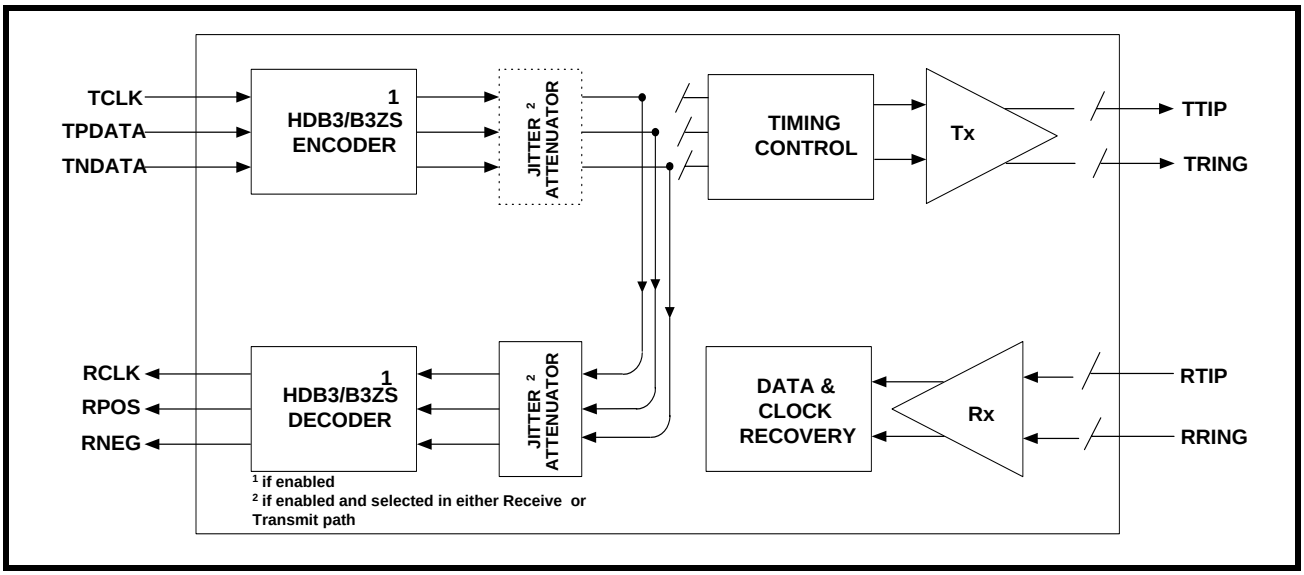


8.2.2 DIGITAL LOOPBACK:

The Digital Loopback function is available either in Hardware mode or Host mode. When the Digital Loopback is selected, the transmit clock (TxClk_n) and transmit data inputs (TPOS_n & TNEG_n) are looped back and output onto the RxClk_n, RPOS_n and RNEG_n pins as shown in Figure 27. The data presented on TxClk, TPOS and TNEG are not output on the TTIP and TRING pins.This provides the capability to configure the protection card (in redundancy applications) in Digital Loopback mode without affecting the traffic on the primary card.

NOTE: *Signals on the RTIP_n and RRING_n pins are ignored during digital loopback.*

FIGURE 27. DIGITAL LOOPBACK



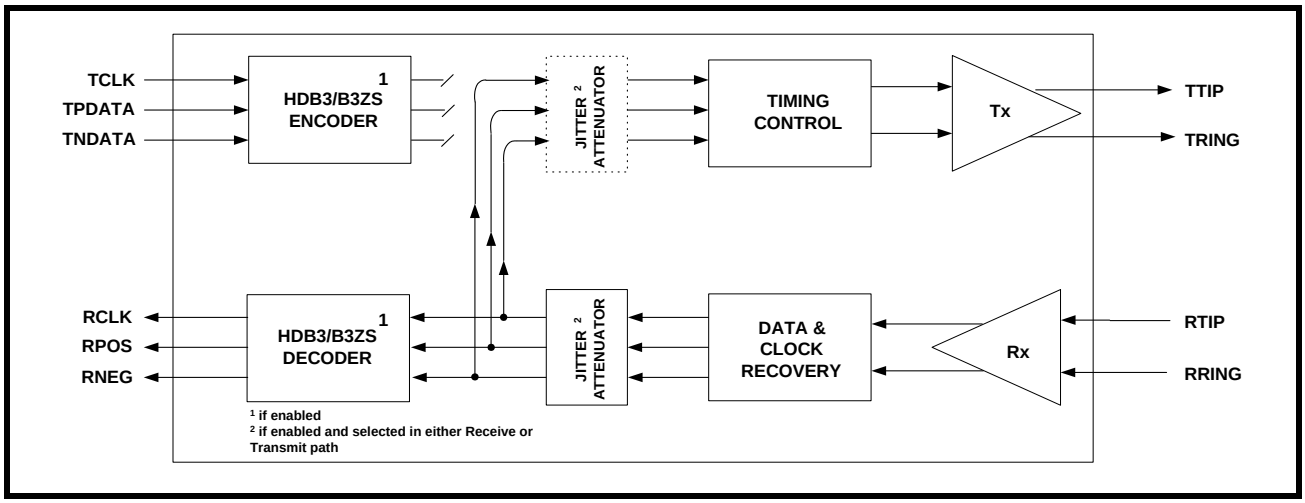
8.2.3 REMOTE LOOPBACK:

With Remote loopback activated as shown in Figure 28, the receive data on RTIP and RRING is looped back after the jitter attenuator (if selected in receive or transmit path) to the transmit path using RxClk as transmit timing. The receive data is also output via the RPOS and RNEG pins.

During the remote loopback mode, if the jitter attenuator is selected in the transmit path, the receive data after the Clock and Data Recovery Block is looped back to the transmit path and passed through the jitter attenuator using RxClk as the transmit timing.

NOTE: *Input signals on TxClk, TPOS and TNEG are ignored during Remote loopback.*

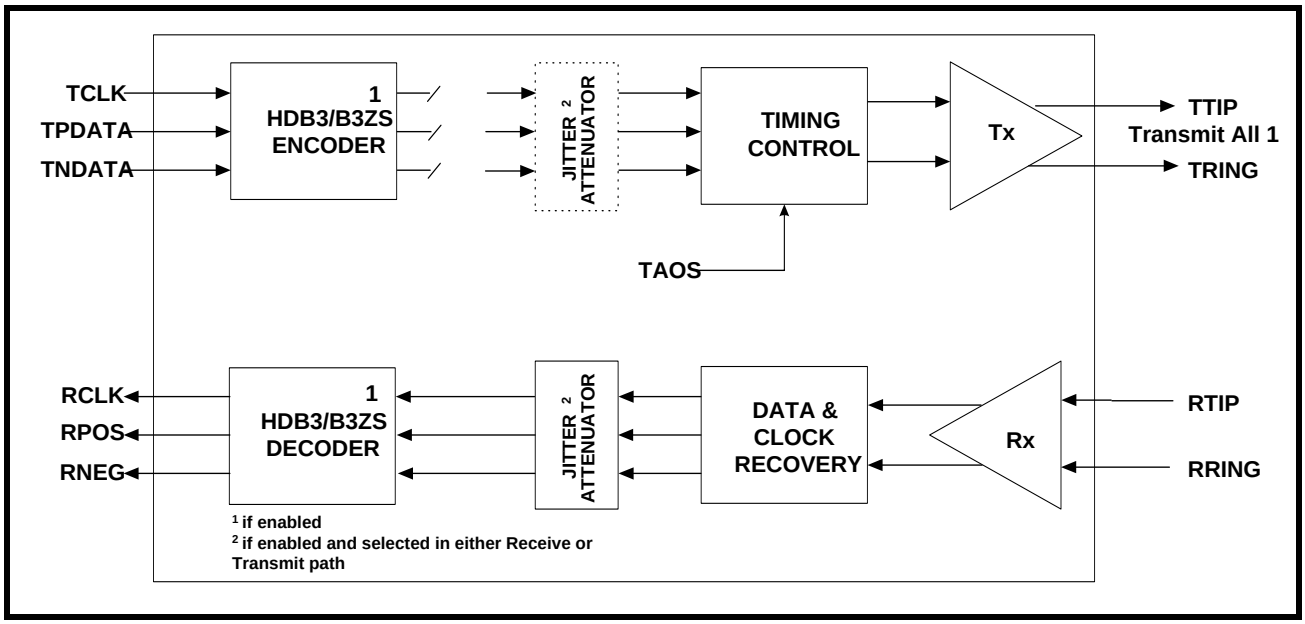
FIGURE 28. REMOTE LOOPBACK



8.3 TRANSMIT ALL ONES (TAOS):

Transmit All Ones (TAOS) can be set either in Hardware mode by pulling the TAOS_n pins “High” or in Host mode by setting the TAOS_n control bits to “1” in the Channel control registers. When the TAOS is set, the Transmit Section generates and transmits a continuous AMI all “1’s” pattern on TTIP_n and TRING_n pins. The frequency of this “1’s” pattern is determined by TClk_n.TAOS data path is shown in Figure 29.

FIGURE 29. TRANSMIT ALL ONES (TAOS)



APPENDIX B

TABLE 22: TRANSFORMER RECOMMENDATIONS

PARAMETER	VALUE
Turns Ratio	1:1
Primary Inductance	40 μH
Isolation Voltage	1500 Vrms
Leakage Inductance	0.6 μH

TABLE 23: TRANSFORMER DETAILS

PART NUMBER	VENDOR	INSULATION	PACKAGE TYPE
PE-68629	PULSE	3000 V	Large Thru-hole
PE-65966	PULSE	1500 V	Samll Thru-hole
PE-65967	PULSE	1500 V	SMT
T 3001	PULSE	1500 V	SMT
TG01-0406NS	HALO	1500 V	SMT
TTI 7601-SM	TransPower	1500 V	SMT

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FAX: 44-1483-401701

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Singapore 368324
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FAX: (650)568-6165
Email: info@haloelectronics.com
Website: http://www.haloelectronics.com
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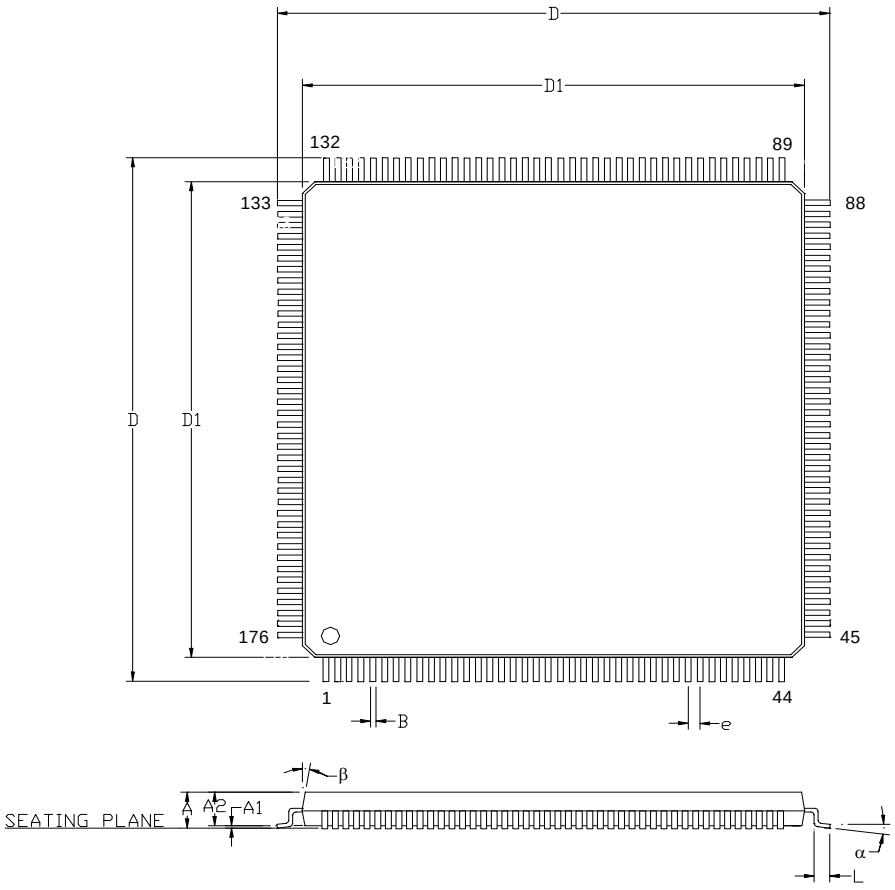
Park Center West Building
9805 Double R Blvd, Suite # 100
Reno, NV 89511
(800)500-5930 or (775)852-0140
Email: info@trans-power.com
Website: http://www.trans-power.com

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L04IV	24 x 24 x 1.4 mm 176 Pin LQFP	- 40°C to + 85°C

PACKAGE DIMENSIONS - 176 PIN PACKAGE



Note: The control dimension is in millimeters.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	1.016	1.031	25.80	26.20
D1	0.941	0.949	23.90	24.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°
β	7° typ		7° typ	

REVISIONS

REV. #	DATE	CHANGES
P1.0.0	2002	Oriiginal preliminary data sheet
P1.0.1	05/02	Cleaned up the Typo errors. Included the eval board schematics. Added some explanation in the register map.
1.0.0	07/03	Release to production, included electrical specs.
1.0.1	11/03	Changed ICC in the electrical characteristics. Removed the evaluation board schematic.
1.0.2	01/06	Changed power dissaption and package power ratings.
1.0.3	01/18/06	Changed package designation from QFP or TQFP to LQFP.
1.0.4	07/11/06	Removed reference to Jitter Attenuator 128 bit FIFO.

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Datasheet July 2006.

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