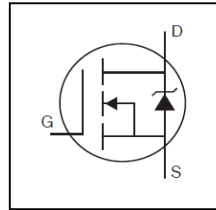


HEXFET® Power MOSFET

Features

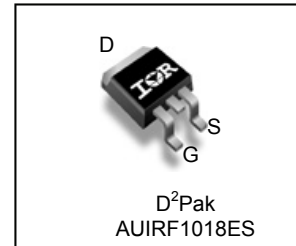
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}	60V
$R_{DS(on)}$ typ.	7.1mΩ
	8.4mΩ
max.	
I_D	79A

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF1018ES	D²-Pak	Tube	50	AUIRF1018ES
		Tape and Reel Left	800	AUIRF1018ESTRL

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	79	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	56	
I_{DM}	Pulsed Drain Current ①	315	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	110	W
	Linear Derating Factor	0.76	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	88	mJ
I_{AR}	Avalanche Current ①	47	A
E_{AR}	Repetitive Avalanche Energy ①	11	mJ
dv/dt	Peak Diode Recovery ③	21	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T_{STG}			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	1.32	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount), D² Pak ⑦	—	40	

HEXFET® is a registered trademark of Infineon.

*Qualification standards can be found at www.infineon.com

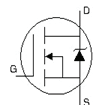
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.073	—	V/°C	Reference to 25°C, I _D = 5mA ①
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	7.1	8.4	mΩ	V _{GS} = 10V, I _D = 47A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 100μA
g _{fs}	Forward Trans conductance	110	—	—	S	V _{DS} = 50V, I _D = 47A
R _G	Internal Gate Resistance	—	0.73	—	Ω	
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 60V, V _{GS} = 0V
		—	—	250		V _{DS} = 48V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

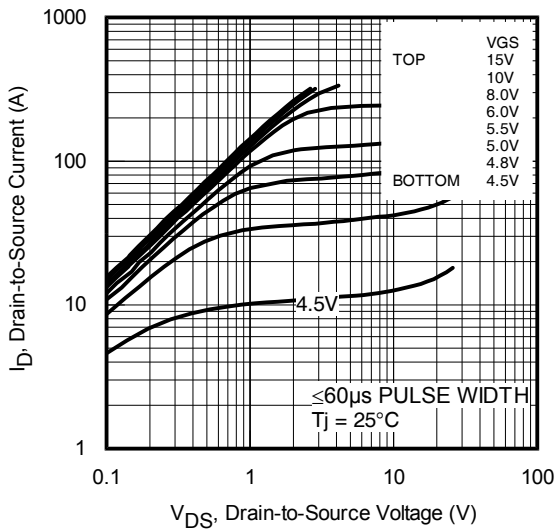
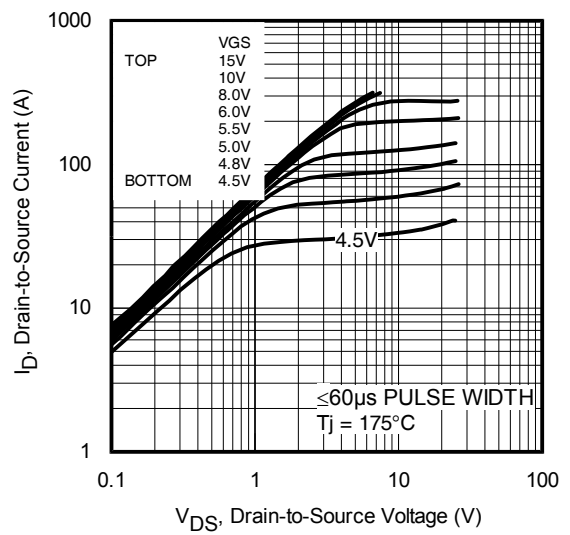
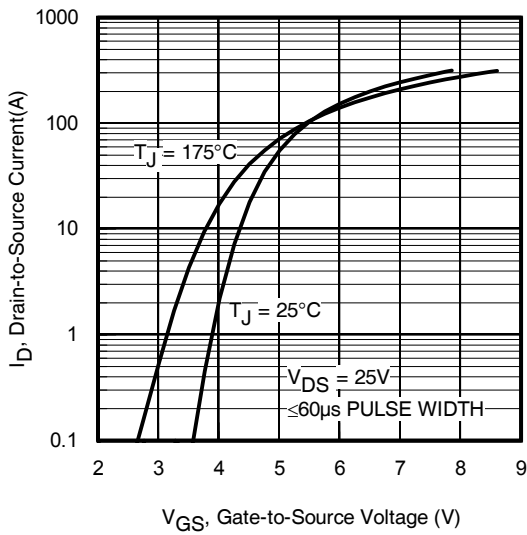
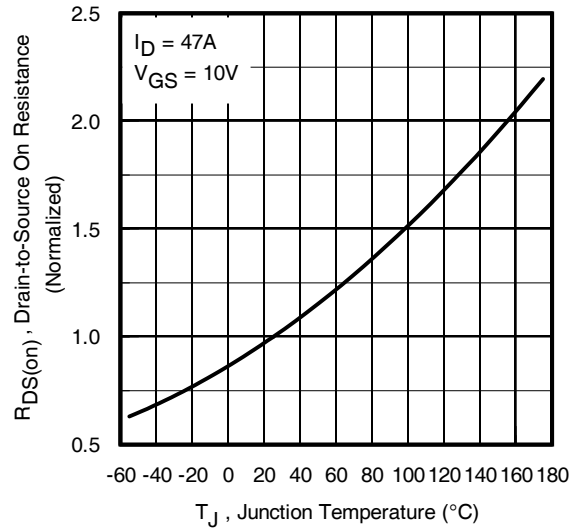
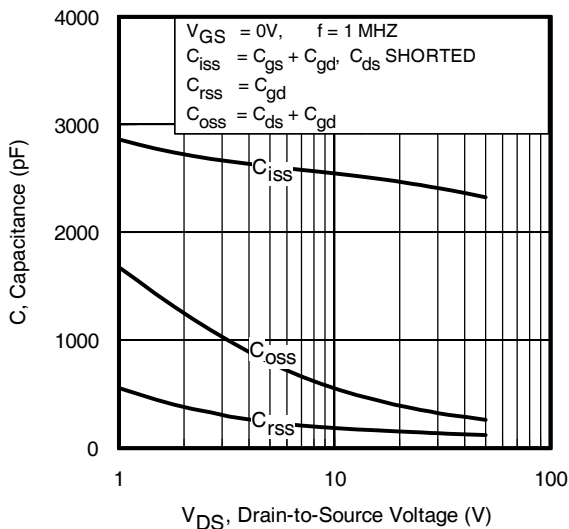
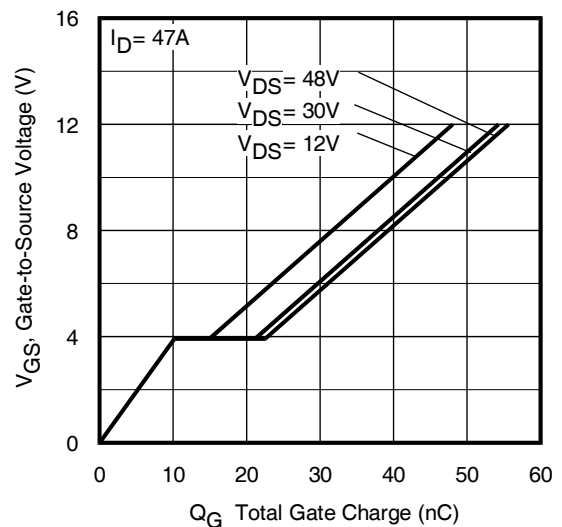
Q _g	Total Gate Charge	—	46	69	nC	I _D = 47A V _{DS} = 30V V _{GS} = 10V④
Q _{gs}	Gate-to-Source Charge	—	10	—		
Q _{gd}	Gate-to-Drain Charge	—	12	—		
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})	—	34	—		
t _{d(on)}	Turn-On Delay Time	—	13	—	ns	V _{DD} = 39V I _D = 47A R _G = 10Ω V _{GS} = 10V④
t _r	Rise Time	—	35	—		
t _{d(off)}	Turn-Off Delay Time	—	55	—		
t _f	Fall Time	—	46	—		
C _{iss}	Input Capacitance	—	2290	—	pF	V _{GS} = 0V V _{DS} = 50V f = 1.0MHz
C _{oss}	Output Capacitance	—	270	—		
C _{rss}	Reverse Transfer Capacitance	—	130	—		
C _{oss eff.(ER)}	Effective Output Capacitance (Energy Related)	—	390	—		
C _{oss eff.(TR)}	Effective Output Capacitance (Time Related)	—	630	—		

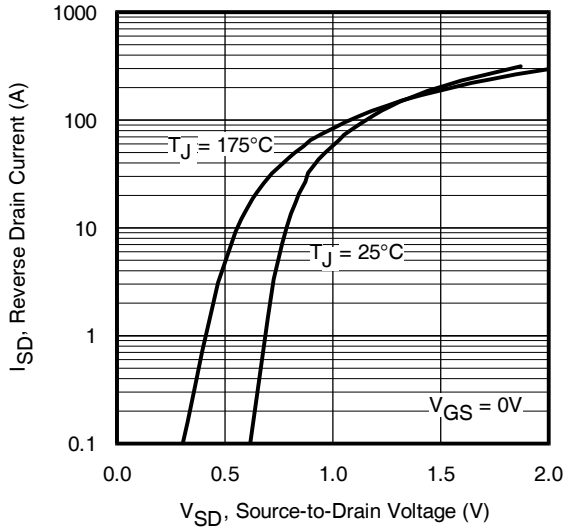
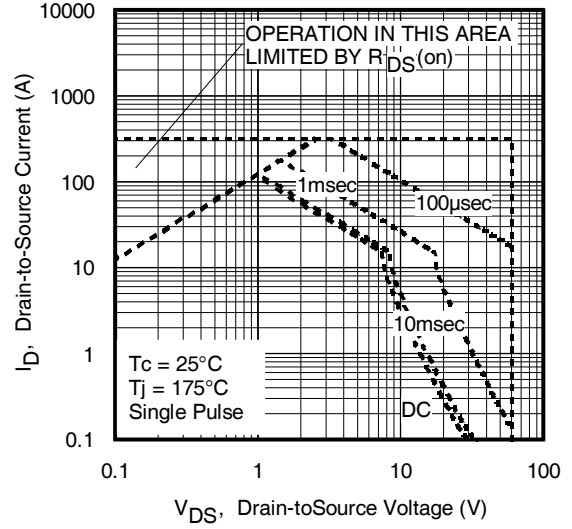
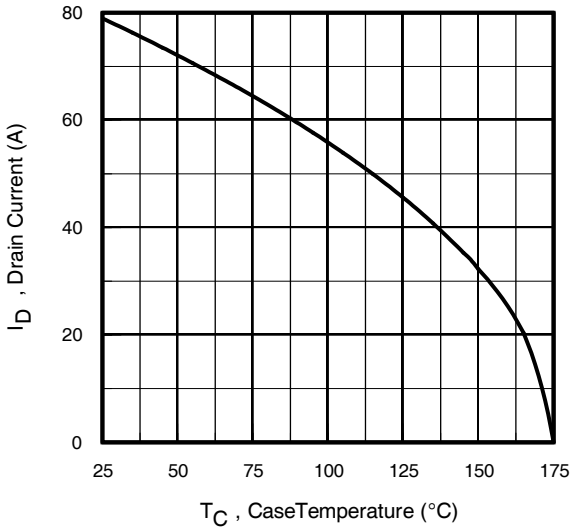
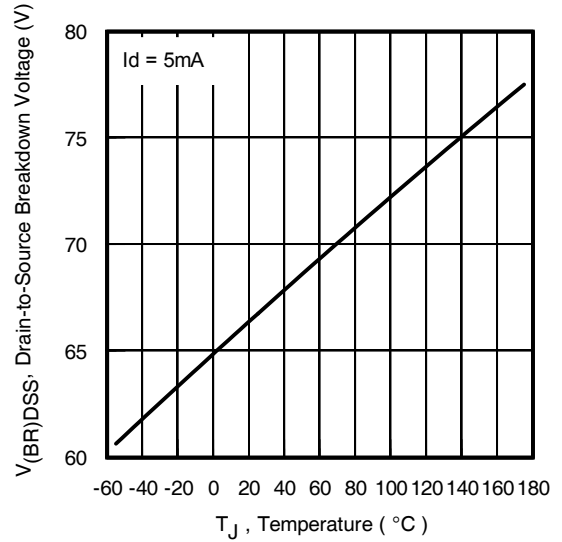
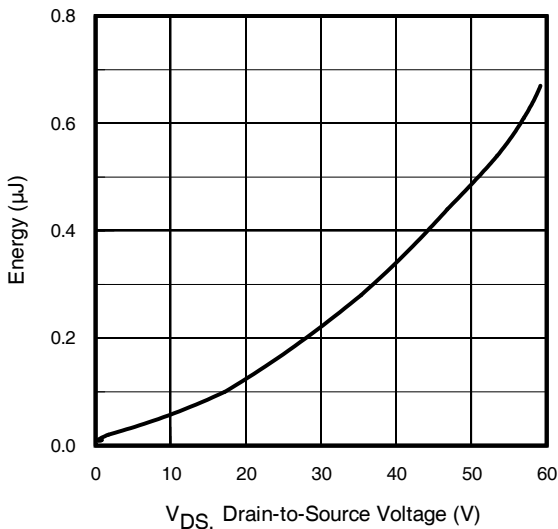
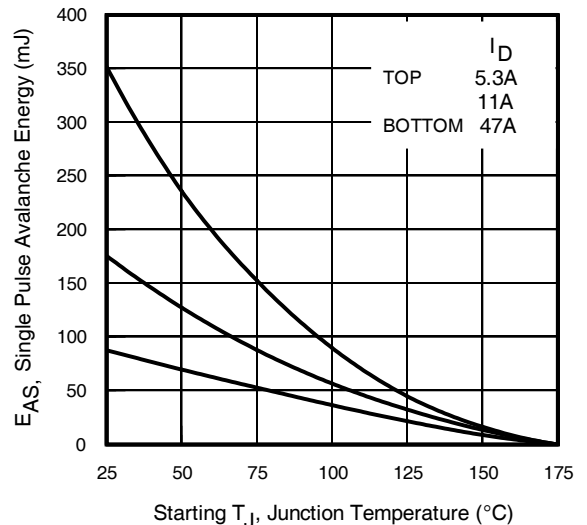
Diode Characteristics

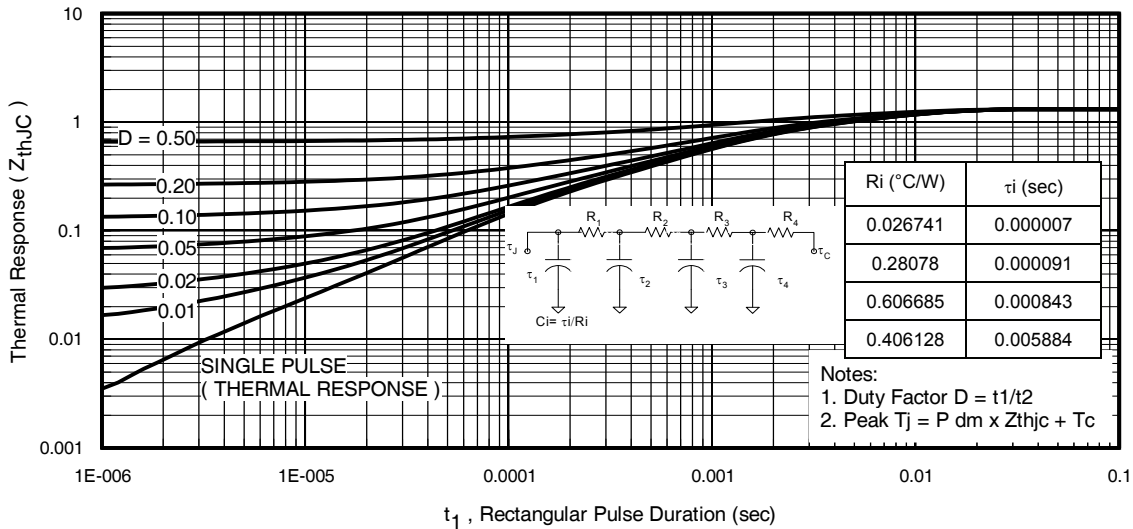
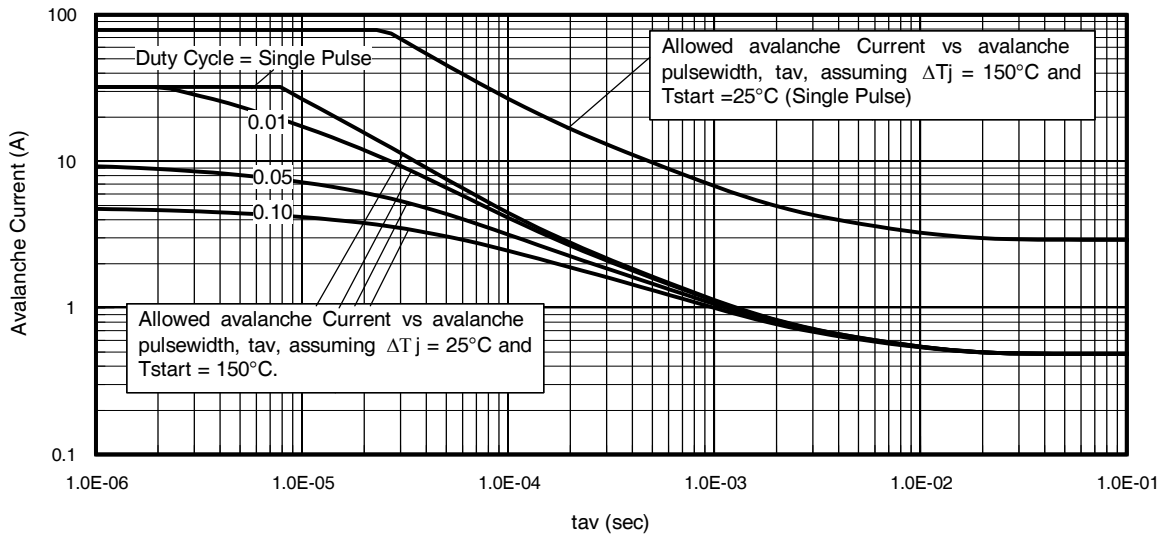
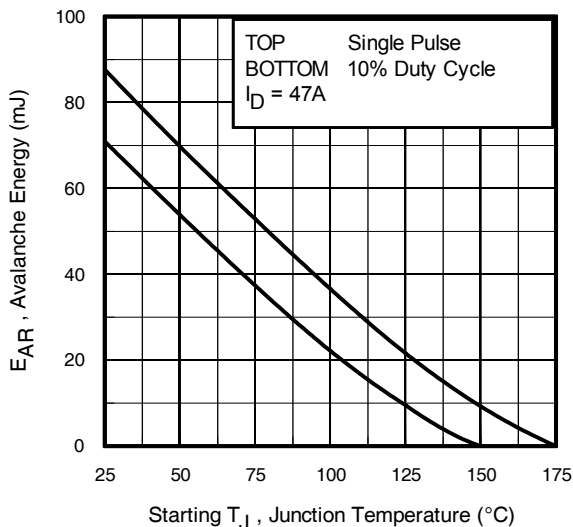
	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	79	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	315		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 47A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	26	39	ns	T _J = 25°C V _{DD} = 51V
		—	31	47		T _J = 125°C I _F = 47A,
Q _{rr}	Reverse Recovery Charge	—	24	36	nC	T _J = 25°C di/dt = 100A/μs ④
		—	35	53		T _J = 125°C
I _{RRM}	Reverse Recovery Current	—	1.8	—	A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.08mH, R_G = 25Ω, I_{AS} = 47A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ I_{SD} ≤ 47A, di/dt ≤ 1668A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff. (TR)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ C_{oss eff. (ER)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R_θ is measured at T_J approximately 90°C.
- ⑨ This is only applied to TO-220.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

Fig. 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig. 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

Fig. 8. Maximum Safe Operating Area

Fig. 9. Maximum Drain Current vs. Case Temperature

Fig. 10. Drain-to-Source Breakdown Voltage

Fig. 11. Typical C_{oss} Stored Energy

Fig. 12. Maximum Avalanche Energy vs. Drain Current


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Avalanche Current vs. Pulse width

**Notes on Repetitive Avalanche Curves , Figures 14, 15:
 (For further info, see AN-1005 at www.infineon.com)**

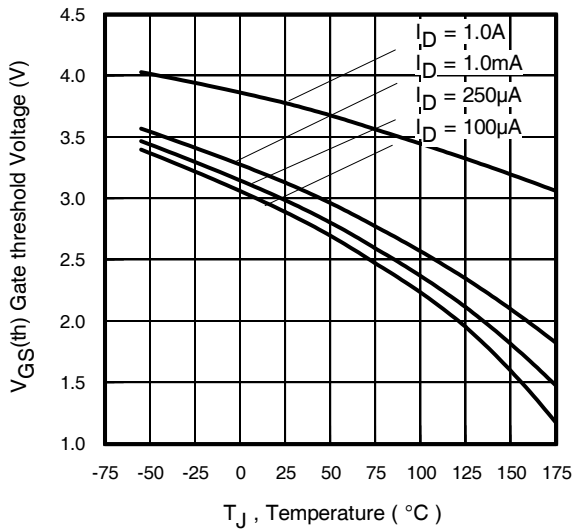
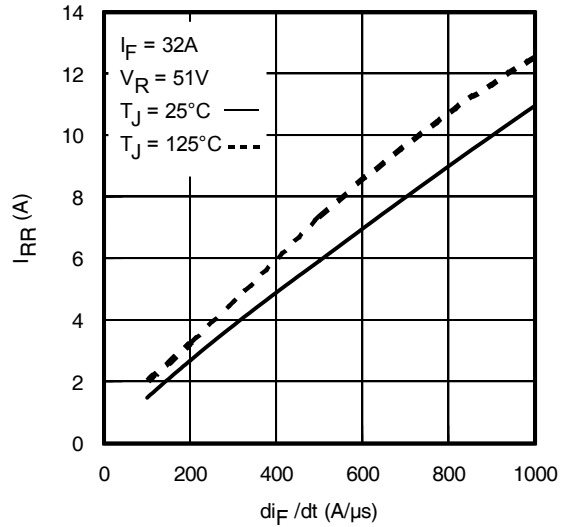
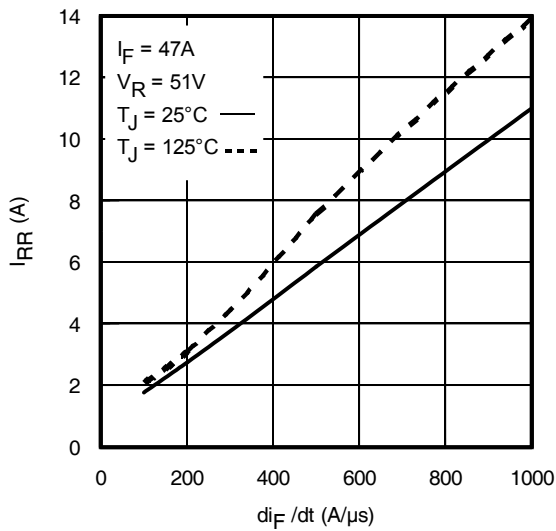
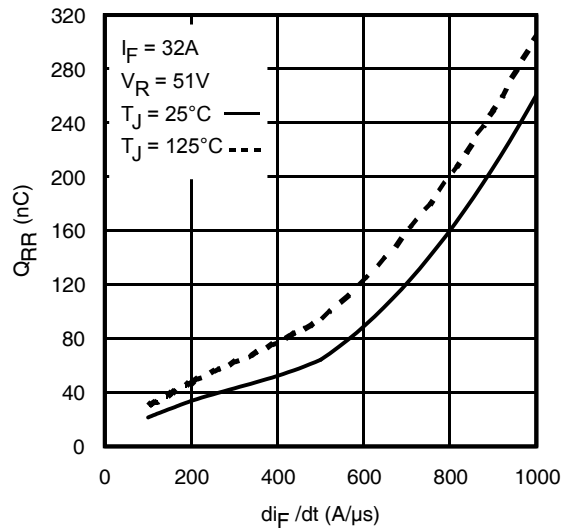
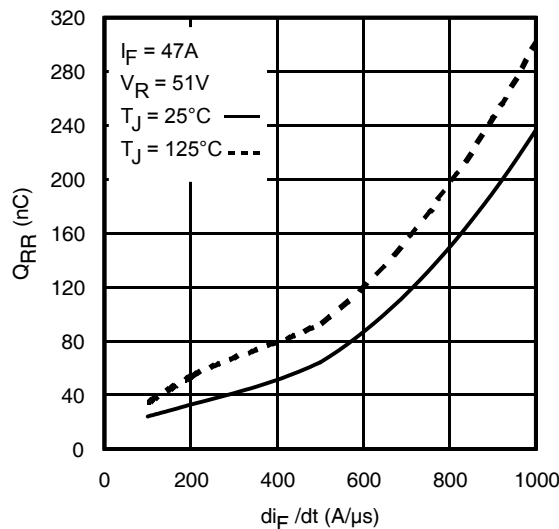
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 18a, 18b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 13, 14).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature


Fig. 16. Threshold Voltage vs. Temperature

Fig. 17 - Typical Recovery Current vs. di/dt

Fig. 18 - Typical Recovery Current vs. di/dt

Fig. 19 - Typical Stored Charge vs. di/dt

Fig. 20 - Typical Stored Charge vs. di/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



Fig 22a. Unclamped Inductive Test Circuit



Fig 22b. Unclamped Inductive Waveforms



Fig 23a. Switching Time Test Circuit

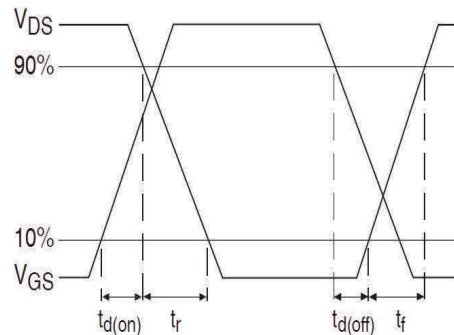


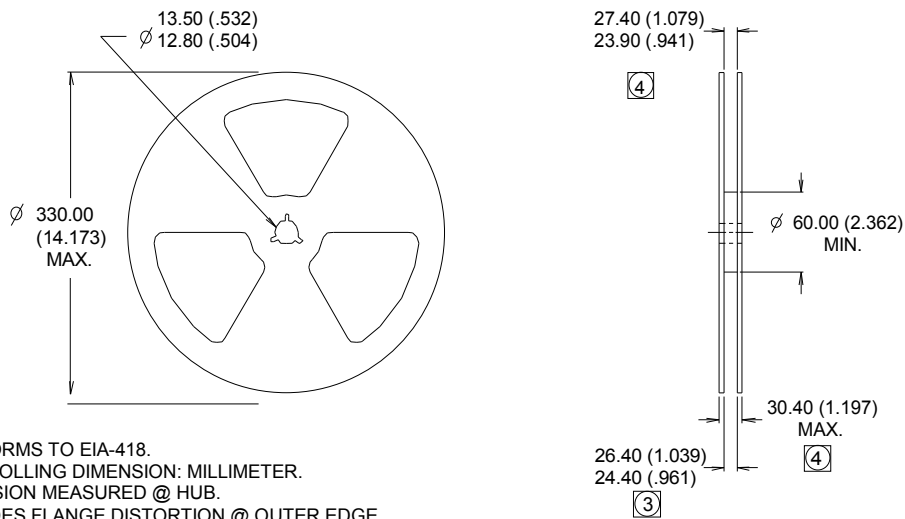
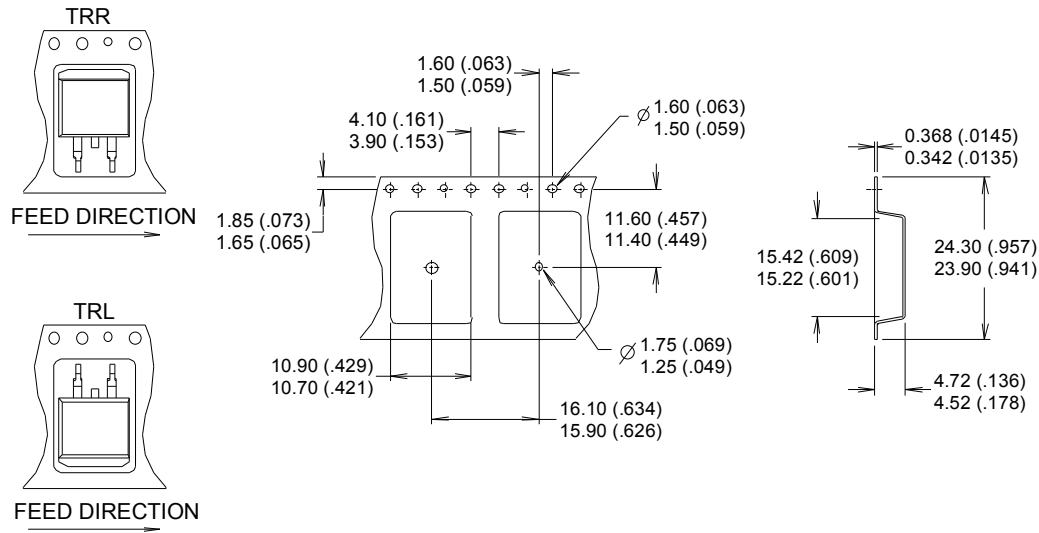
Fig 23b. Switching Time Waveforms



Fig 24a. Gate Charge Test Circuit



Fig 24b. Gate Charge Waveform

D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))


- NOTES :
1. COMFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D ² -Pak	MSL1
ESD	Human Body Model	Class H1B (+/- 1000V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

Revision History

Date	Comments
11/23/2015	<ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1. Added ESD table on page10

Published by
Infineon Technologies AG
81726 München, Germany
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<http://moschip.ru/get-element>

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