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June 2014 FDMC86139P

P-Channel PowerTrench[®] MOSFET -100 V, -15 A, 67 m Ω

Features

- \blacksquare Max $r_{DS(on)}$ = 67 m Ω at V_{GS} = -10 V, I_D = -4.4 A
- Max $r_{DS(on)}$ = 89 m Ω at V_{GS} = -6 V, I_D = -3.6 A
- Very low RDS-on mid voltage P channel silicon technology optimised for low Qg
- This product is optimised for fast switching applications as well as load switch applications
- 100% UIL Tested
- RoHS Compliant



General Description

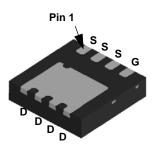
This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® technology. This very high density process is especially tailored to minimize on-state resistance and optimized for superior switching performance.

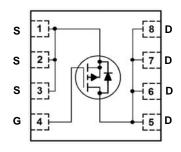
Applications

- Active Clamp Switch
- Load Switch

Top Bottom







MLP 3.3x3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-100	V
V_{GS}	Gate to Source Voltage			±25	V
	Drain Current -Continuous	T _C = 25 °C		-15	
I _D	-Continuous	T _A = 25 °C	(Note 1a)	-4.4	Α
	-Pulsed			-30	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	121	mJ
D	Power Dissipation	T _C = 25 °C		40	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.3	VV
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to + 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC86139P	FDMC86139P	Power 33	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25$ °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-100			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		-63		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -80 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

On Characteristics

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-2	-3	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μ A, referenced to 25 °C		7		mV/°C
		$V_{GS} = -10 \text{ V}, I_D = -4.4 \text{ A}$		56	67	
r _{DS(on)}	r _{DS(on)} Static Drain to Source On Resistance	$V_{GS} = -6 \text{ V}, I_D = -3.6 \text{ A}$		69	89	mΩ
, ,	$V_{GS} = -10 \text{ V}, I_D = -4.4 \text{ A}, T_J = 125 \text{ °C}$		87	104		
9 _{FS}	Forward Transconductance	V _{DS} = -10 V, I _D = -4.4 A		12		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 50 V V 0 V		1001	1335	pF
Coss	Output Capacitance	$V_{DS} = -50 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz		178	240	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 101112		10	15	pF
R _q	Gate Resistance		0.1	1.6	3.2	Ω

Switching Characteristics

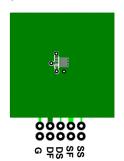
t _{d(on)}	Turn-On Delay Time		11	20	ns
t _r	Rise Time	V _{DD} = -50 V, I _D = -4.4 A,	2.5	10	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = -10 \text{ V}, R_{GEN} = 6 \Omega$	17	30	ns
t _f	Fall Time		4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V _{GS} = 0 V to -10 V	16	22	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to -6 V}$ $V_{DD} = -50 \text{ V},$ $I_{D} = -4.4 \text{ A}$	9.8	14	nC
Q_{gs}	Total Gate Charge	1 _D = -4.4 A	4.5		nC
Q _{qd}	Gate to Drain "Miller" Charge		3.2		nC

Drain-Source Diode Characteristics

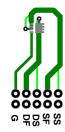
Type Source to Drain Diode Forward Voltage	Source to Drain Diode, Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = -4.4 \text{ A}$ (N	Note 2)	-0.84	-1.3	V
	$V_{GS} = 0 \text{ V}, I_S = -1.9 \text{ A}$ (N	Note 2)	-0.79	-1.2	V	
t _{rr}	Reverse Recovery Time			70	112	ns
Q _{rr}	Reverse Recovery Charge			141	225	nC

NOTES

^{1.} $R_{\theta,JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta,JC}$ is guaranteed by design while $R_{\theta,CA}$ is determined by the user's board design.



a) 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper

^{2.} Pulse Test: Pulse Width < 300 $\mu\text{s},$ Duty cycle < 2.0%.

^{3.} Starting $T_J = 25\,^{\circ}C$; P-ch: L = 3 mH, $I_{AS} = -9\,$ A, $V_{DD} = -100\,$ V, $V_{GS} = -10\,$ V. 100% test at L = 0.1 mH, $I_{AS} = -28\,$ A.

Typical Characteristics T_J = 25 °C unless otherwise noted

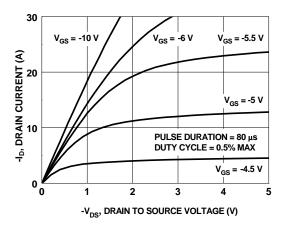


Figure 1. On Region Characteristics

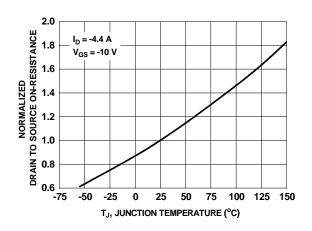


Figure 3. Normalized On Resistance vs Junction Temperature

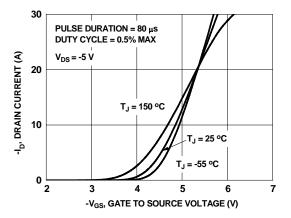


Figure 5. Transfer Characteristics

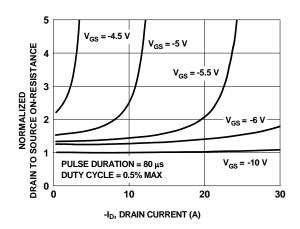


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

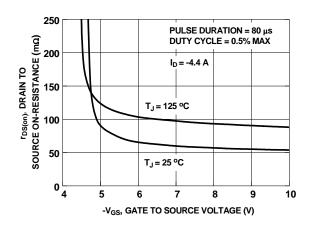


Figure 4. On-Resistance vs Gate to Source Voltage

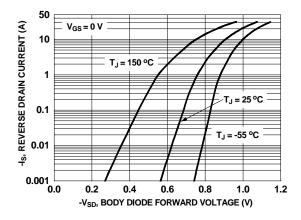


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

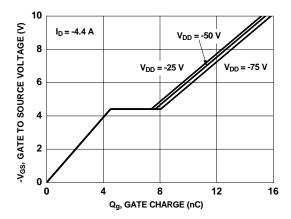


Figure 7. Gate Charge Characteristics

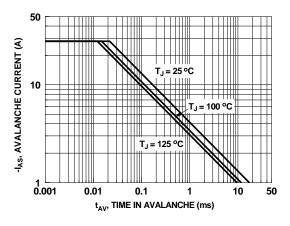


Figure 9. Unclamped Inductive Switching Capability

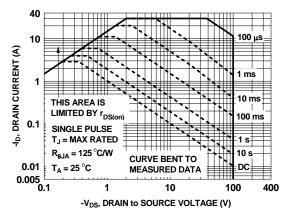


Figure 11. Forward Bias Safe Operating Area

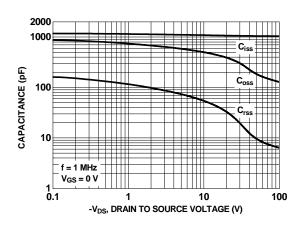


Figure 8. Capacitance vs Drain to Source Voltage

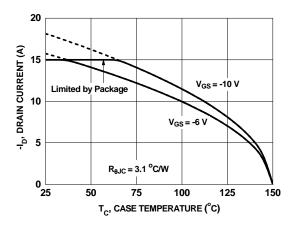


Figure 10. Maximum Continuous Drain Current vs Case Temperature

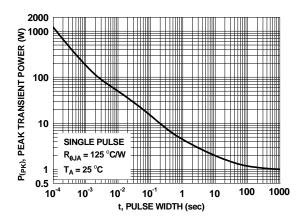


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

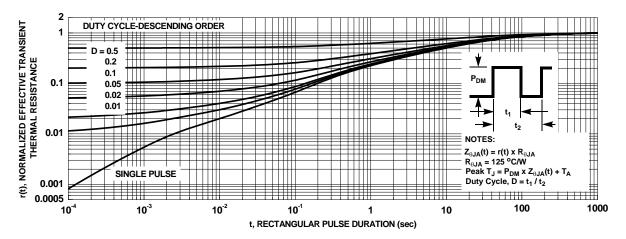
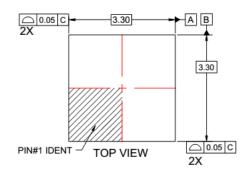
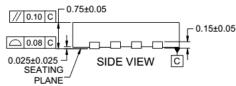
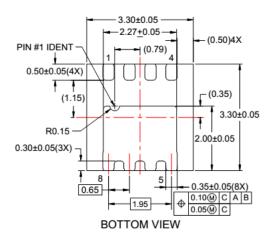


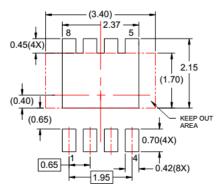
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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