

TOSHIBA Multi-chip Device

Silicon PNP Epitaxial Transistor , Field Effect Transistor Silicon N Channel MOS Type

TPCP8F01

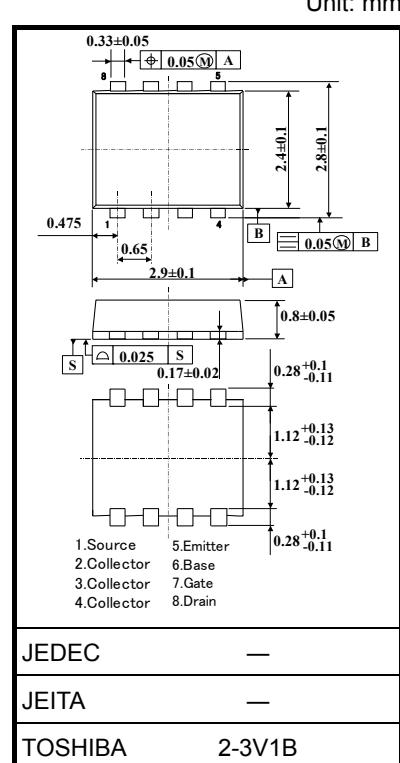
- Switching Applications
- Load Switch Applications
- Multi-chip discrete device; built-in PNP Transistor for main switch and N-ch MOS FET for drive

- High DC current gain: $hFE = 200$ to 500 ($I_C = -0.5$ A)
(PNP Transistor)
- Low collector-emitter saturation: $V_{CE}(\text{sat}) = -0.19$ V (max)
(PNP Transistor)
- High-speed switching: $t_f = 40$ ns (typ.) (PNP Transistor)

Absolute Maximum Ratings (Ta = 25°C)

Transistor

Characteristics	Symbol	Rating	Unit	
Collector-base voltage	V_{CBO}	-30	V	
Collector-emitter voltage	V_{CEO}	-20	V	
Emitter-base voltage	V_{EBO}	-7	V	
Collector current	DC	I_C	-3.0	A
	Pulse	I_{CP}	-5.0	
Base current	I_B	-250	mA	
Collector power dissipation	P_C (Note 1)	1.0	W	
Junction temperature	T_J	150	°C	



Weight : 0.017g (Typ.)

MOS FET

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V _{DSS}	20	V
Gate-source voltage	V _{GSS}	±10	V
Drain current	DC	I _D	100
	Pulse	I _{DP}	200
Channel temperature	T _j	150	°C

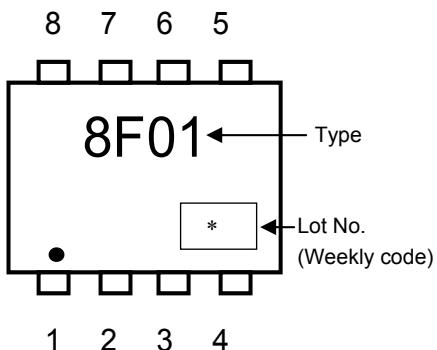
Note 1: Mounted on FR4 board (glass epoxy, 1.6mm thick, Cu area: 645mm²)

Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

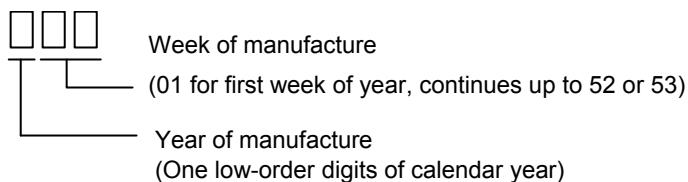
Common Absolute Maximum Rating (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Storage temperature range	T _{stg}	-55 to 150	°C

Figure 2 Marking (Note 3)

Note 3 : Black round marking " · " located on the left lower side of parts number marking "8F01" indicates terminal No.1

* Weekly code: (Three digits)

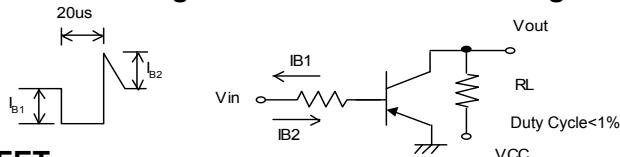


Electrical Characteristics (Ta = 25°C)

Transistor

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current	I _{CBO}	V _{CB} = -30 V, I _E = 0	—	—	-100	nA
Emitter cut-off current	I _{EBO}	V _{EB} = -7 V, I _C = 0	—	—	-100	nA
Collector-emitter breakdown voltage	V _{(BR) CEO}	I _C = -10 mA, I _B = 0	-20	—	—	V
DC current gain	h _{FE} (1)	V _{CE} = -2 V, I _C = -0.5 A	200	—	500	
	h _{FE} (2)	V _{CE} = -2 V, I _C = -1.6 A	100	—	—	
Collector-emitter saturation voltage	V _{CE (sat)}	I _C = -1.6 A, I _B = -53 mA	—	—	-0.19	V
Base-emitter saturation voltage	V _{BE (sat)}	I _C = -1.6 A, I _B = -53 mA	—	—	-1.10	V
Collector Output Capacitance	C _{ob}	V _{CB} = -10 V, I _E = 0, f = 1MHz	—	28	—	pF
Switching time	Rise time	t _r	See Figure 3 circuit diagram V _{CC} ≈ -12 V, R _L = 7.5 Ω -I _{B1} = I _{B2} = -53 mA	70	—	ns
	Storage time	t _{stg}		150	—	
	Fall time	t _f		40	—	

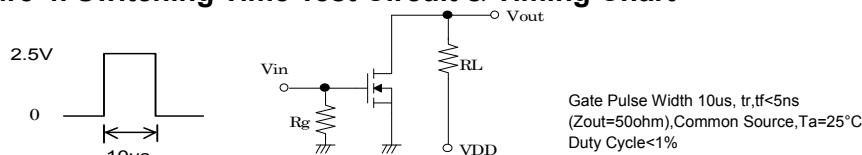
Figure 3. Switching Time Test Circuit & Timing Chart



MOS FET

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} = -10 V, V _{DS} = 0	—	—	±1	μA	
Drain-source breakdown voltage	V _{(BR) DSS}	I _D = 0.1 mA, V _{GS} = 0	20	—	—	V	
Drain cut-off current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0	—	—	1	μA	
Gate Threshold voltage	V _{th}	V _{DS} = 3 V, I _D = 0.1 mA	0.6	—	1.1	V	
Forward Transfer Admittance	Y _{fsl}	V _{DS} = 3 V, I _D = 10 mA	40	—	—	ms	
Drain-source ON resistance	R _{DSON}	I _D = 10 mA, V _{GS} = 4.0 V	—	1.5	3	Ω	
		I _D = 10 mA, V _{GS} = 2.5 V	—	2.2	4		
		I _D = 1 mA, V _{GS} = 1.5 V	—	5.2	15		
Input capacitance	C _{iss}	V _{DS} = 3 V, V _{GS} = 0, f = 1 MHz	—	9.3	—	pF	
Reverse transfer capacitance	C _{rss}		—	4.5	—		
Output capacitance	C _{oss}		—	9.8	—		
Switching time	Turn-on time	t _{on}	V _{DD} ≈ -3 V, R _L = 300 Ω V _{GS} = 0 to 2.5 V	—	70	—	ns
	Turn-off time	t _{off}		—	125	—	

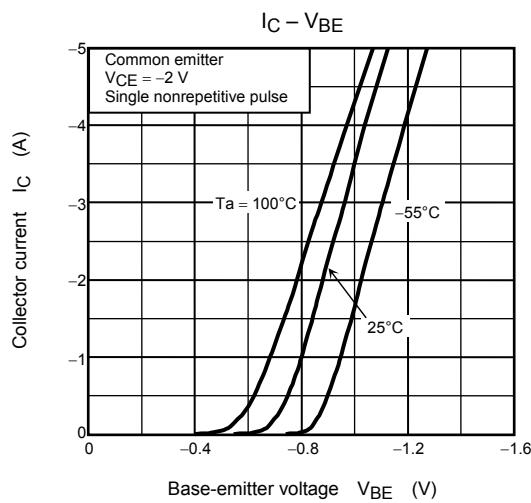
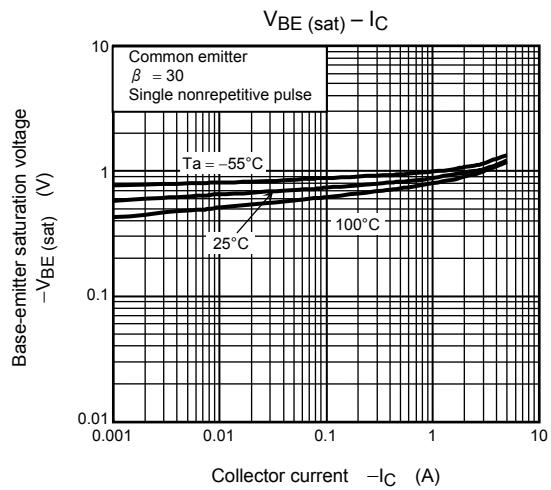
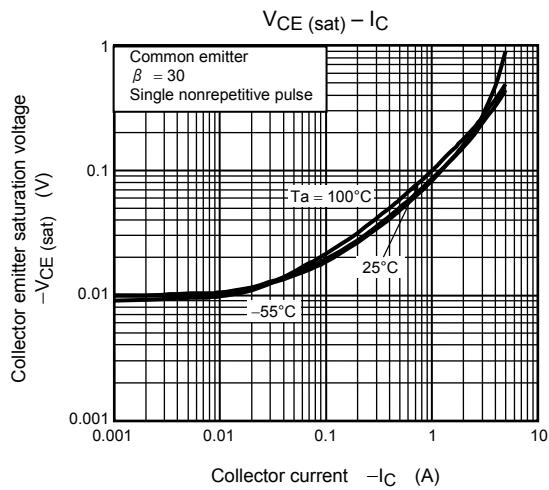
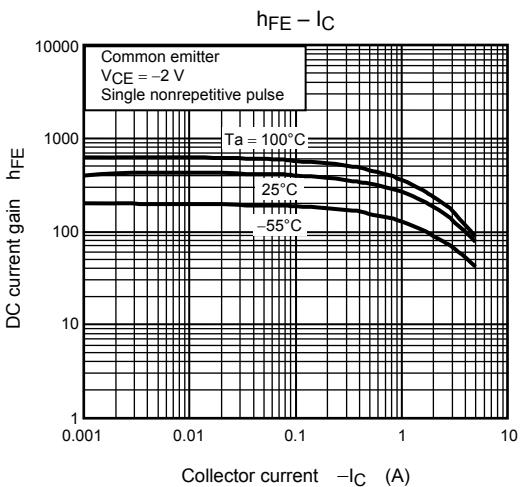
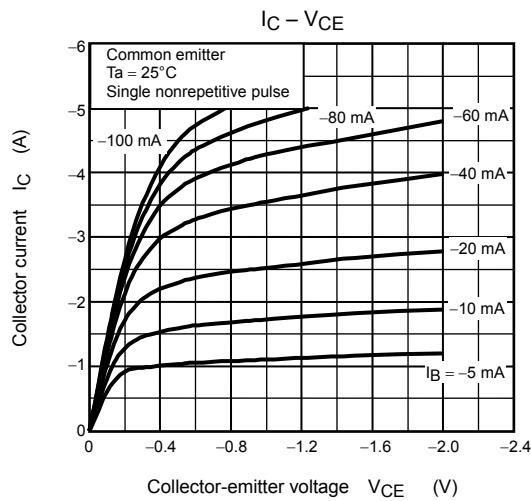
Figure 4. Switching Time Test Circuit & Timing Chart

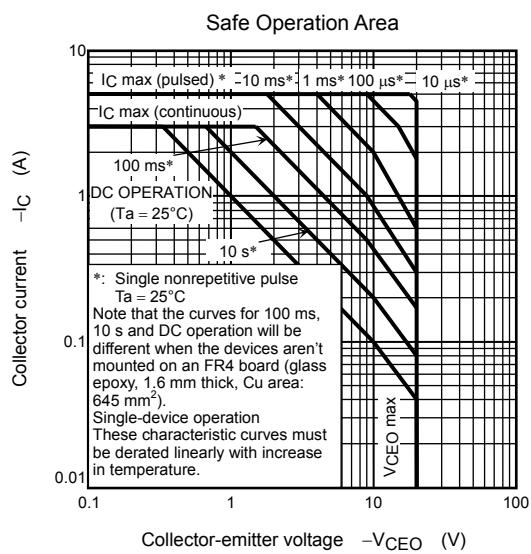
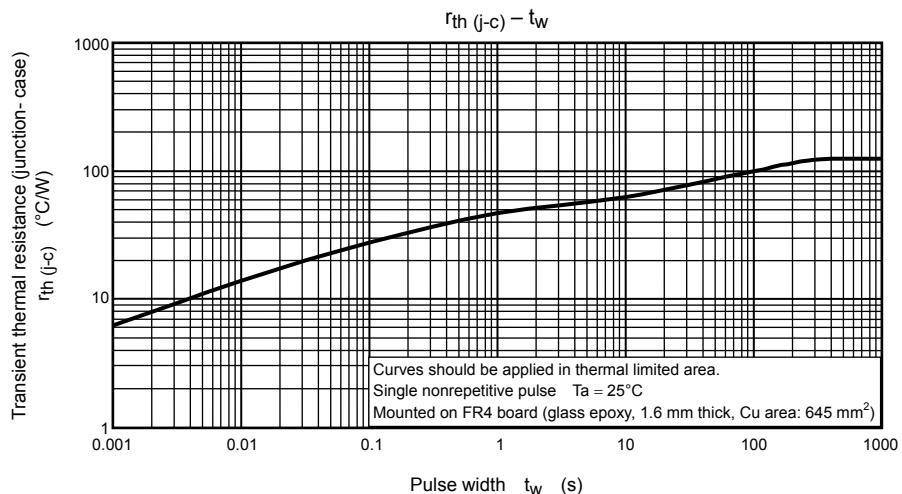


Precautions

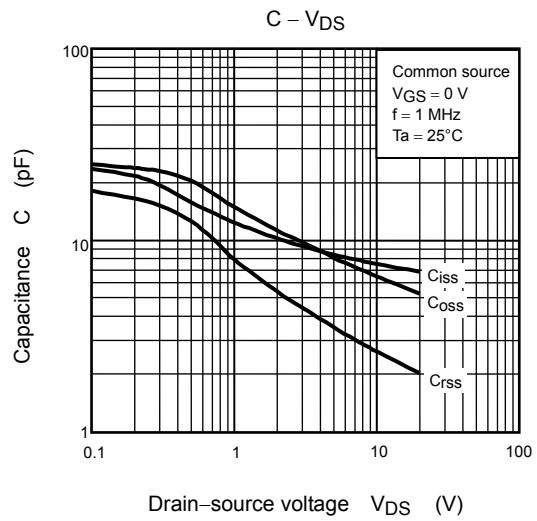
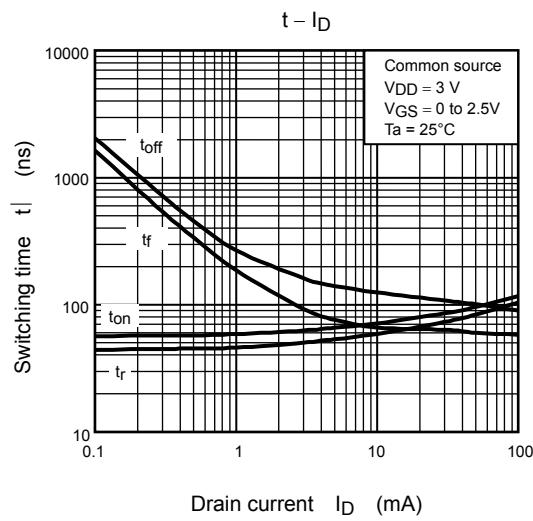
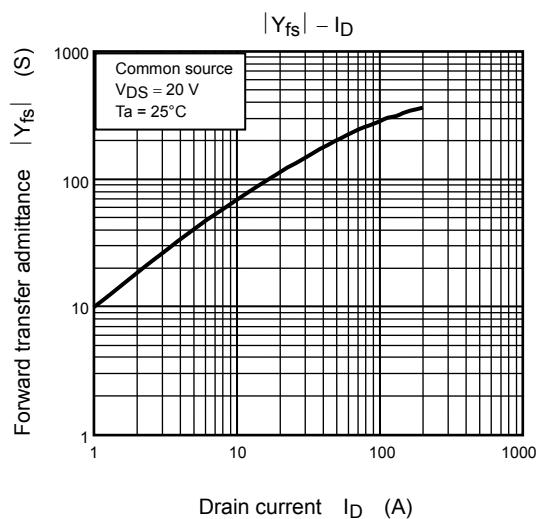
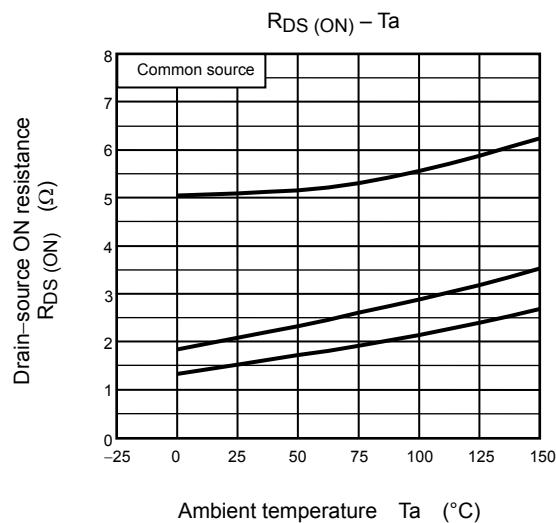
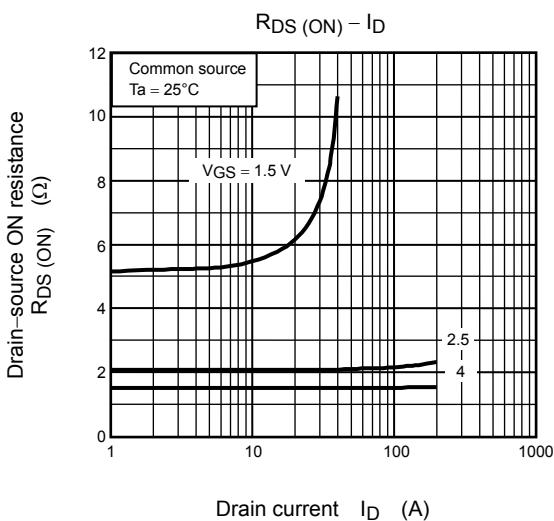
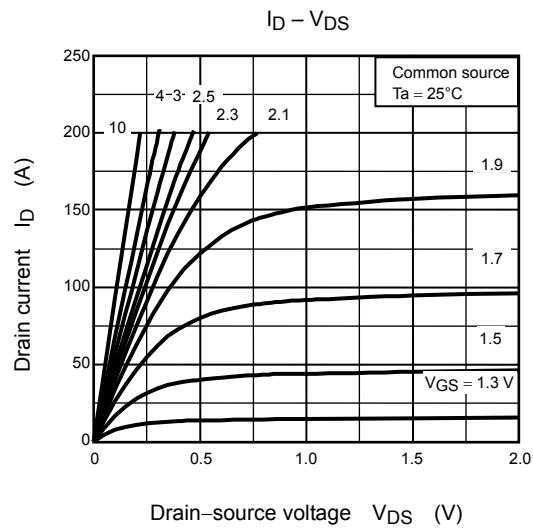
V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = 100 μA for this product. For normal switching operation, V_{GS(ON)} requires higher voltage than V_{th} and V_{GS(OFF)} requires lower voltage than V_{th}. (relationship can be established as follows: V_{GS(OFF)} < V_{th} < V_{GS(ON)}) Please take this into consideration for using the device.
VGS recommended voltage of 2.5V or higher to turn on this product.

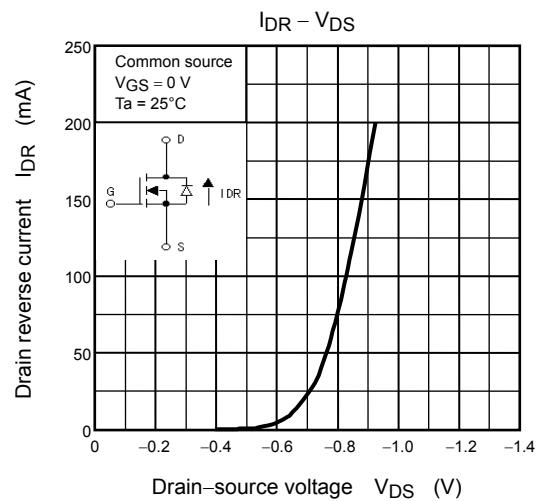
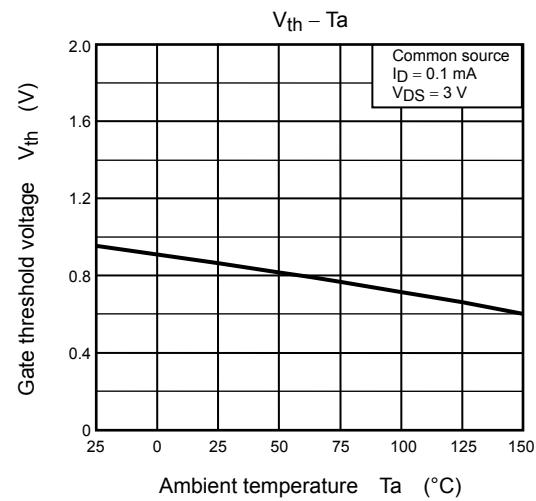
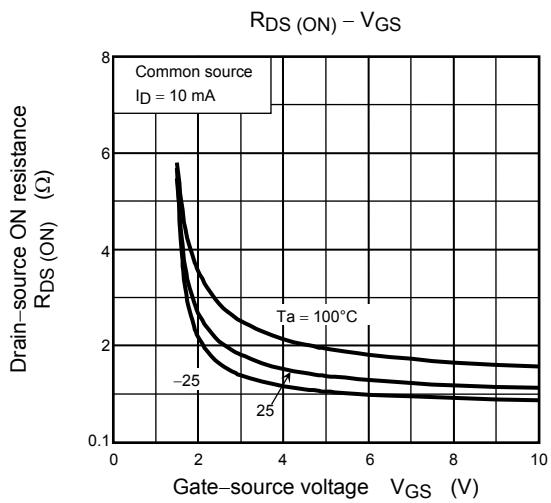
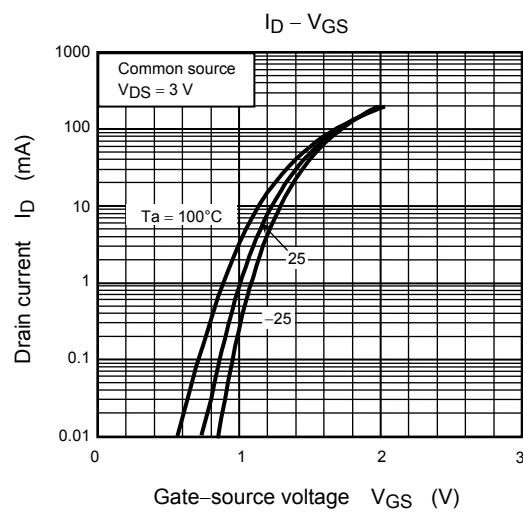
PNP





Nch-MOS





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