Integrated Device Technology, Inc.

VARIABLE WIDTH SUPERSYNC™ FIFO
8,192 x 18 or 16,384 x 9
16,384 x 18 or 32,768 x 9

IDT72264
IDT72274

FEATURES:

- Select 8192 x 18 or 16384x 9 organization (IDT72264)
- Select 16384 x 18 or 32678 x 9 organization (IDT72274)
- Flexible control of read and write clock frequencies
- Reduced dynamic power dissipation
- Auto power down minimizes power consumption
- 15 ns read/write cycle time (10 ns access time)
- Retransmit Capability
- Master Reset clears entire FIFO, Partial Reset clears data, but retains programmable settings
- Empty, full and half-full flags signal FIFO status
- Programmable almost empty and almost full flags, each flag can default to one of two preselected offsets
- Program partial flags by either serial or parallel means
- Select IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$ flags) or First Word Fall Through timing (using $\overline{OR}$ and $\overline{IR}$ flags)
- Easily expandable in depth and width
- Independent read and write clocks (permits simultaneous reading and writing with one clock signal)
- Available in the 64-pin Thin Quad Flat Pack (TQFP), 64-pin Slim Thin Quad Flat Pack (STQFP) and the 68-pin Pin Grid Array (PGA)
- Output enable puts data outputs into high impedance
- High-performance submicron CMOS technology
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

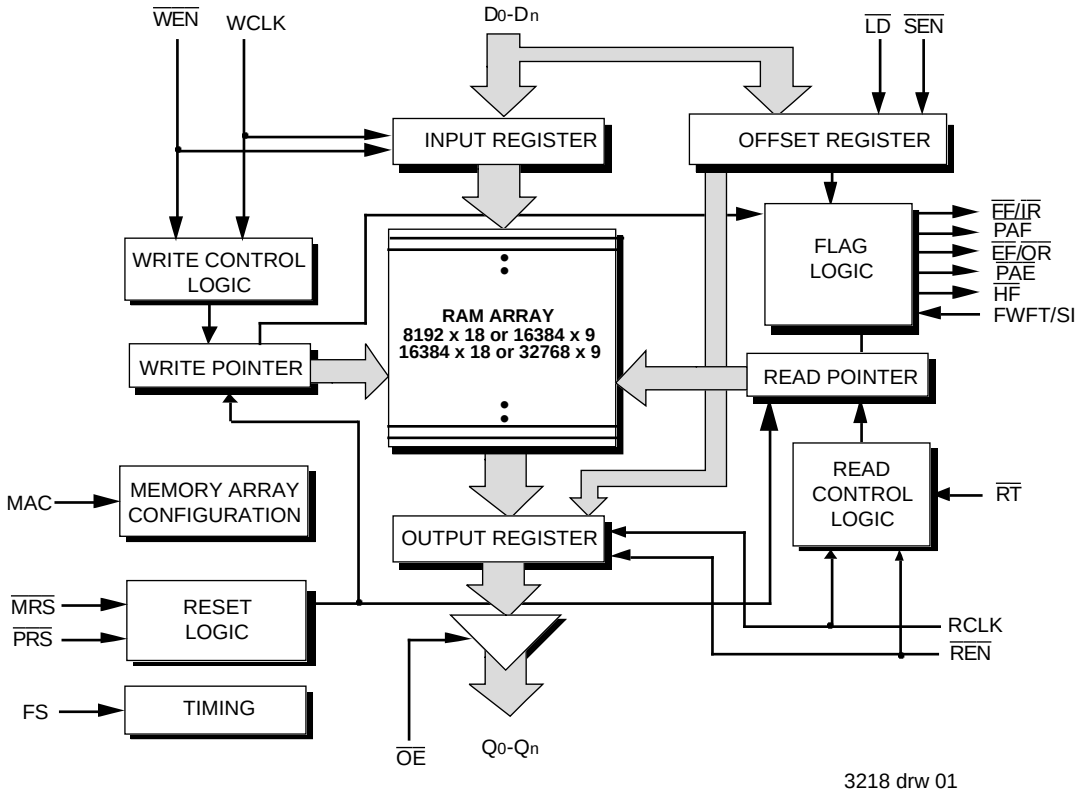
DESCRIPTION:

The IDT72264/72274 are monolithic, CMOS, high capacity, high speed, low power first-in, first-out (FIFO) memories with clocked read and write controls. These FIFOs have three main features that distinguish them among SuperSync FIFOs:

First, the data path width can be changed from 9-bits to 18-bits; as a result, halving the depth. A pin called Memory Array Select (MAC) chooses between the two options. This feature helps reduce the need for redesigns or multiple versions of PC cards, since a single layout can be used for both data bus widths.

Second, IDT72264/72274 offer the greatest flexibility for setting and varying the read and write clock (WCLK and RCLK) frequencies. For example, given that the two clock frequencies are unequal, the slower clock may exceed the faster by, at most, twice its frequency. This feature is especially useful for communications and network applications where clock frequencies are switched to permit different data rates.

FUNCTIONAL BLOCK DIAGRAM



3218 drw 01

SyncFIFO is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

©1997 Integrated Device Technology, Inc

Finally,of all SuperSync FIFOs, the IDT72264/72274 offer the lowest dynamic power dissipation.

These devices meet a wide variety of data buffering needs. In addition to those already mentioned, applications include such as optical disk controllers, Local Area Networks (LANs), and inter-processor communication.

Both FIFOs have an 18-bit input port (D_n) and an 18-bit output port (Q_n). The input port is controlled by a free-running clock (WCLK) and a data input enable pin ($\overline{WEN}$). Data is written into the synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronously for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the outputs.

The IDT72264/72274 have two modes of operation: In the *IDT Standard Mode*, the first word written to the FIFO is deposited into the memory array. A read operation is required to access that word. In the *First Word Fall Through Mode* (FWFT), the first word written to an empty FIFO appears automatically on the outputs, no read operation required. The state of the FWFT/SI pin during Master Reset determines the mode in use.

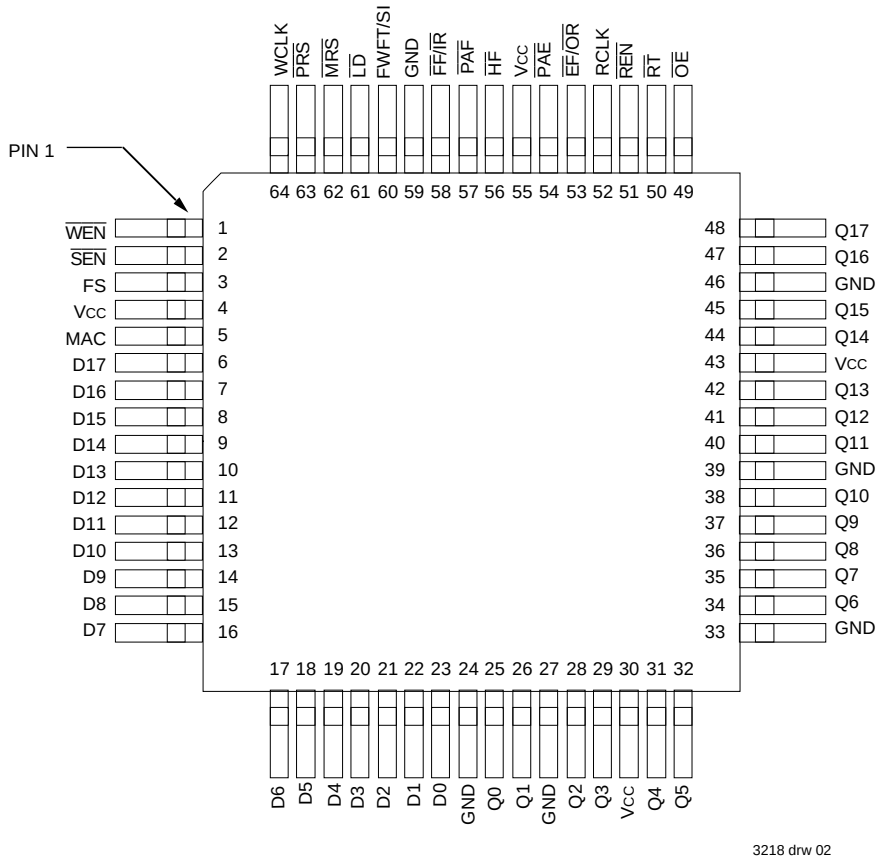
The IDT72264/72274 have five flag functions, $\overline{EF}/\overline{OR}$ (Empty Flag or Output Ready), $\overline{FF}/\overline{IR}$ (Full Flag or Input Ready), and $\overline{HF}$ (Half-full Flag). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the IDT Standard Mode.

The $\overline{IR}$ and $\overline{OR}$ functions are selected in the First Word Fall Through Mode. $\overline{IR}$ indicates that the FIFO has free space to receive data. $\overline{OR}$ indicates that data contained in the FIFO is available for reading.

$\overline{HF}$ is a flag whose threshold is fixed at the half-way point in memory. This flag can always be used irrespective of mode.

$\overline{PAE}$ and $\overline{PAF}$ can be programmed independantly to any point in memory. They, also, can be used irrespective of mode. Programmable offsets determine the flag threshold and can be loaded by two methods: parallel or serial. Two default offset settings are also provided, such that $\overline{PAE}$ can be set at 127 or 1023 locations from the empty boundary and the $\overline{PAF}$ threshold can be set at 127 or 1023 locations from the full boundary. All these choices are made with $\overline{LD}$ during Master Reset.

PIN CONFIGURATIONS



TQFP (PN64-1, order code: PF)
STQFP (PP64-1, order code: TF)
TOP VIEW

NOTES:

1. When the data path is selected to be 9 bits wide (MAC is HIGH), D_9 - D_{17} may either be tied to ground or left open, Q_9 - Q_{17} must be left open.

In the serial method, $\overline{SEN}$ together with $\overline{LD}$ are used to load the offset registers via the Serial Input (SI). In the parallel method, $\overline{WEN}$ together with $\overline{LD}$ can be used to load the offset registers via D_n. $\overline{REN}$ together with $\overline{LD}$ can be used to read the offsets in parallel from Q_n regardless of whether serial or parallel offset loading is selected.

During Master Reset ($\overline{MRS}$), the read and write pointers are set to the first location of the FIFO. The FWFT line selects IDT Standard Mode or FWFT Mode. The $\overline{LD}$ pin selects one of two partial flag default settings (127 or 1023) and, also, serial or parallel programming. The flags are updated accordingly.

The Partial Reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the mode setting, programming method, and partial flag offsets are not altered. The flags are updated accordingly. $\overline{PRS}$ is useful for resetting a device in mid-operation, when reprogramming offset registers may not be convenient.

The Retransmit function allows the read pointer to be reset to the first location in the RAM array. It is synchronized to RCLK when $\overline{RT}$ is LOW. This feature is convenient for sending the same data more than once.

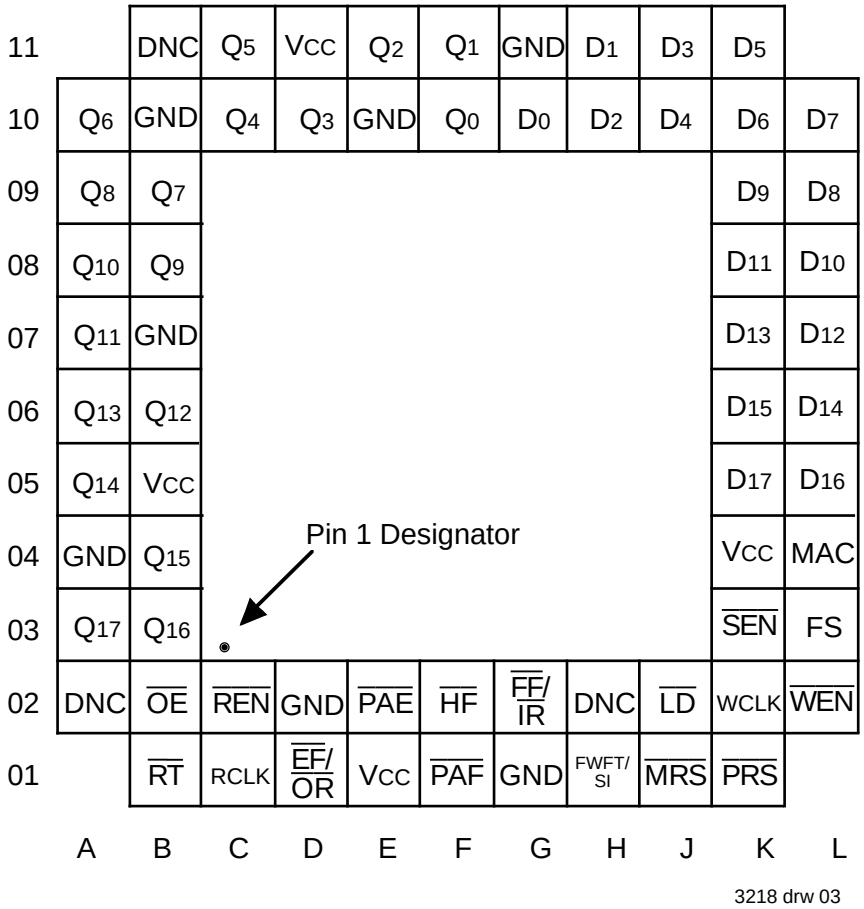
If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. This occurs if neither a read nor a write occurs within 10 cycles of the faster clock, RCLK or WCLK. During the Power Down state, supply current consumption (I_{CC2}) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the Power Down state.

The IDT72264/72274 are depth expandable. The addition of external components is unnecessary. The $\overline{IR}$ and $\overline{OR}$ functions, together with $\overline{REN}$ and $\overline{WEN}$, are used to extend the total FIFO memory capacity.

The FS line ensures optimal data flow through the FIFO. It is tied to GND if the RCLK frequency is higher than the WCLK frequency or to Vcc if the RCLK frequency is lower than the WCLK frequency

The IDT72264/72274 is fabricated using IDT's high speed submicron CMOS technology.

PIN CONFIGURATIONS (CONT.)



PGA (G68-1, order code: G)
TOP VIEW

NOTES:
1. When the data path is selected to be 9 bits wide (MAC is HIGH), D_9 - D_{17} may be tied to ground or left open, Q_9 - Q_{17} must be left open.
2. DNC = Do not connect

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_0–D_{17}	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{MRS}$	Master Reset	I	$\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the FIFO is configured for either FWFT or IDT Standard Mode, one of two programmable flag default settings, and serial or parallel programming of the offset settings.
$\overline{PRS}$	Partial Reset	I	$\overline{PRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Partial Reset,the existing mode (IDT or FWFT), programming method (serial or parallel), and programmable flag settings are all retained.
$\overline{RT}$	Retransmit	I	Allows data to be resent starting with the first location of FIFO memory.
FWFT/SI	First Word Fall Through/Serial In	I	During Master Reset, selects First Word Fall Through or IDT Standard mode. After Master Reset, this pin functions as a serial input for loading offset registers
WCLK	Write Clock	I	When enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO and offsets into the programmable registers.
$\overline{WEN}$	Write Enable	I	$\overline{WEN}$ enables WCLK for writing data into the FIFO memory and offset registers.
RCLK	Read Clock	I	When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers.
$\overline{REN}$	Read Enable	I	$\overline{REN}$ enables RCLK for reading data from the FIFO memory and offset registers.
$\overline{OE}$	Output Enable	I	$\overline{OE}$ controls the output impedance of Q_n.
$\overline{SEN}$	Serial Enable	I	$\overline{SEN}$ enables serial loading of programmable flag offsets.
$\overline{LD}$	Load	I	During Master Reset, $\overline{LD}$ selects one of two partial flag default offsets (127 and 1023) and determines programming method, serial or parallel. After Master Reset, this pin enables writing to and reading from the offset registers.
MAC	Memory Array Configuration	I	MAC selects 8192 x 18 or 16384x 9 memory array organization for the IDT72264. It selects 16384 x 18 or 32678 x 9 memory array organization for the IDT72274.
FS	Frequency Select	I	FS selects selects WCLK or RCLK, whichever is running at a higher frequency, to synchronize the FIFO's internal state machine.
$\overline{FF}$/$\overline{IR}$	Full Flag/ Input Ready	O	In the IDT Standard Mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is full. In the FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether or not there is space available for writing to the FIFO memory.
$\overline{EF}$/$\overline{OR}$	Empty Flag/ Output Ready	O	In the IDT Standard Mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether or not there is valid data available at the outputs.
$\overline{PAF}$	Programmable Almost Full Flag	O	$\overline{PAF}$ goes HIGH if the number of free locations in the FIFO memory is more than offset m which is stored in the Full Offset register. $\overline{PAF}$goes LOW if the number of free locations in the FIFO memory is less than m.
$\overline{PAE}$	Programmable Almost Empty Flag	O	$\overline{PAE}$ goes LOW if the number of words in the FIFO memory is less than offset n which is stored in the Empty Offset register. $\overline{PAE}$ goes HIGH if the number of words in the FIFO memory is greater than offset n.
$\overline{HF}$	Half-full Flag	O	$\overline{HF}$ indicates whether the FIFO memory is more or less than half-full.
Q_0–Q_{17}	Data Outputs	O	Data outputs for a 18-bit bus.
V_{CC}	Power		+5 volt power supply pins.
GND	Ground		Ground pins.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IL} (1,2)	Input Low Voltage Commercial	—	—	0.8	V

NOTE:

1. Does not apply to MAC which can only be tied to Vcc or GND.
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter		IDT72264L IDT72274L Commercial t_{CLK} = 15, 20ns Min.	Type	Max	Unit
I_{LI} (1)	Input Leakage Current (any input except MAC)		-1	—	1	µA
I_{LO} (2)	Output Leakage Current		-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2mA		2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8mA		—	—	0.4	V
I_{CC1} (3)	Active Power Supply Current	MAS = V_{CC}	—	—	115	mA
		MAS = GND	—	—	135	mA
I_{CC2} (3,4)	Power Down Current (All inputs = V_{CC} - 0.2V or GND + 0.2V, RCLK and WCLK are free-running)		—	—	115	mA

NOTES:
1. Measurements with $0.4 \le V_{IN} \le V_{CC}$.
2. $\overline{OE}$ + V_{IH}
3. Tested at f = 20 MHz with outputs uploaded.
4. No data written or read for more than 10 cycles.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:

1. With output deselected, ($\overline{OE}$=HIGH).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial 72264L15 72274L15 Min.	Commercial 72264L15 72274L15 Max.	Commercial 72264L20 72274L20 Min.	Commercial 72264L20 72274L20 Max.	Unit
f_S	Clock Cycle Frequency	—	66.7	—	50	MHz
t_A	Data Access Time	2	10	2	12	ns
t_{CLK}	Clock Cycle Time	15	—	20	—	ns
t_{CLKH}	Clock High Time	6	—	8	—	ns
t_{CLKL}	Clock Low Time	6[2]	—	8	—	ns
t_{DS}	Data Set-up Time	4	—	5	—	ns
t_{DH}	Data Hold Time	1	—	1	—	ns
t_{ENS}	Enable Set-up Time	4	—	5	—	ns
t_{ENH}	Enable Hold Time	1	—	1	—	ns
t_{LDS}	Load Set-up Time	4	—	5	—	ns
t_{LDH}	Load Hold Time	10	—	10	—	ns
t_{RS}	Reset Pulse Width[3]	15	—	20	—	ns
t_{RSS}	Reset Set-up Time	15	—	20	—	ns
t_{RSR}	Reset Recovery Time	15	—	20	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	—	20	ns
t_{FWFT}	Mode Select Time	0	—	0	—	ns
t_{RTS}	Retransmit Set-Up Time	4	—	5	—	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	3	8	3	10	ns
t_{OHZ}	Output Enable to Output in High Z[4]	3	8	3	10	ns
t_{WFF}	Write Clock to $\overline{FF}$ or $\overline{IR}$	—	10	—	12	ns
t_{REF}	Read Clock to $\overline{EF}$ or $\overline{OR}$	—	10	—	12	ns
t_{PAF}	Write Clock to $\overline{PAF}$	—	10	—	12	ns
t_{PAE}	Read Clock to $\overline{PAE}$	—	10	—	12	ns
t_{HF}	Clock to $\overline{HF}$	—	20	—	22	ns
t_{SKEW1}	Skew time between RCLK and WCLK for $\overline{FF}$ and $\overline{IR}$	12	—	15	—	ns
t_{SKEW2}	Skew time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	21	—	25	—	ns

NOTES:

1. All AC timings apply to both Standard IDT Mode and First Word Fall Through Mode.
2. For the RCLK line: t_{CLKL} (min.) = 7 ns only when reading the offsets from the programmable flag registers; otherwise, use the table value. For the WCLK line, use the t_{CLKL} (min.) value given in the table.
3. Pulse widths less than minimum values are not allowed.
4. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3037 tbl 08

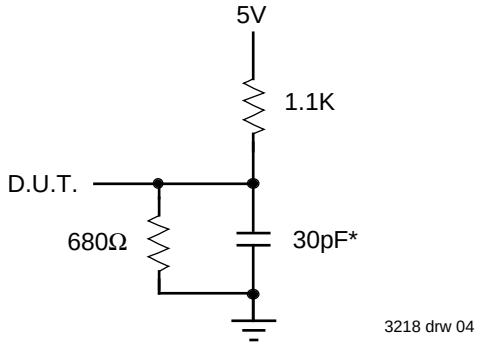


Figure 1. Output Load
* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_{17})

All 18 data inputs (D_0 - D_{17}) function when the Memory Array Configuration input (MAC) is tied to ground. Only 9-data inputs (D_0 - D_8) function when MAC is connected to Vcc. The other data inputs (D_9 - D_{17}) do not function and may either be tied to ground or left open.

CONTROLS:

MEMORY ARRAY CONFIGURATION (MAC)

The MAC line determines whether the FIFO will operate with a nine-bit-wide data bus or an 18-bit wide data bus. A FIFO is configured for 18-bit wide operation has half the memory depth of the same FIFO configured for 9-bit wide operation. MAC must be tied to either GND or Vcc. Connecting MAC to Vcc will configure the FIFO's input and output data buses to be 9 bits wide. In this case, the IDT72264 will have a 16384x 9 organization, and the IDT72274 will have a 32678 x 9 organization.

Connecting MAC to GND will configure the FIFO's input and output data buses to be 18 bits wide. In this case, the IDT72264 will have a 8192 x 18 organization, and the IDT72274 will have a 16384 x 18 organization. MAC must be set before Master Reset; afterwards, it cannot be dynamically varied.

MASTER RESET ($\overline{MRS}$)

A Master Reset is accomplished whenever the $\overline{MRS}$ input is taken to a LOW state. This operation sets the internal read and write pointers to the first location of the RAM array. $\overline{PAE}$ will go LOW, $\overline{PAF}$ will go HIGH, and $\overline{HF}$ will go HIGH.

If FWFT is LOW during Master Reset then the IDT Standard Mode, along with $\overline{EF}$ and $\overline{FF}$ are selected. $\overline{EF}$ will go LOW and $\overline{FF}$ will go HIGH. If FWFT is HIGH, then the First Word Fall through Mode (FWFT), along with $\overline{IR}$ and $\overline{OR}$, are selected. $\overline{OR}$ will go HIGH and $\overline{IR}$ will go LOW.

If $\overline{LD}$ is LOW during Master Reset, then $\overline{PAE}$ is assigned a threshold 127 words from the empty boundary and $\overline{PAF}$ is assigned a threshold 127 words from the full boundary; 127 words corresponds to an offset value of 07FH. Following Master Reset, parallel loading of the offsets is permitted, but not serial loading.

If $\overline{LD}$ is HIGH during Master Reset, then $\overline{PAE}$ is assigned a threshold 1023 words from the empty boundary and $\overline{PAF}$ is assigned a threshold 1023 words from the full boundary; 1023 words corresponds to an offset value of 3FFH. Following Master Reset, serial loading of the offsets is permitted, but not parallel loading.

Regardless of whether serial or parallel offset loading has been selected, parallel reading of the registers is always permitted. (See section describing the $\overline{LD}$ line for further details).

During a Master Reset, the output register is initialized to all zeroes. A Master Reset is required after power up, before a write operation can take place. $\overline{MRS}$ is asynchronous

PARTIAL RESET ($\overline{PRS}$)

A Partial Reset is accomplished whenever the $\overline{PRS}$ input is taken to a LOW state. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array, $\overline{PAE}$ goes LOW, $\overline{PAF}$ goes HIGH, and $\overline{HF}$ goes HIGH.

Whichever mode is active at the time of partial reset, IDT Standard Mode or First Word Fall-through, that mode will remain selected. If the IDT Standard Mode is active, then $\overline{FF}$ will go HIGH and $\overline{EF}$ will go LOW. If the First word Fall-through Mode is active, then $\overline{OR}$ will go HIGH, and $\overline{IR}$ will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The programming method (parallel or serial) currently active at the time of Partial Reset is also retained. The output register is initialized to all zeroes. $\overline{PRS}$ is asynchronous.

A Partial Reset is useful for resetting the device during the course of operation, when reprogramming flag settings may not be convenient.

RETRANSMIT ($\overline{RT}$)

The Retransmit operation allows data that has already been read to be accessed again. There are two stages: first, a setup procedure that resets the read pointer to the first location of memory, then the actual retransmit, which consists of reading out the memory contents, starting at the beginning of memory.

Retransmit Setup is initiated by holding $\overline{RT}$ LOW during a rising RCLK edge. $\overline{REN}$ and $\overline{WEN}$ must be HIGH before bringing $\overline{RT}$ LOW. At least one word, but no more than Full - 2 words should have been written into the FIFO between Reset (Master or Partial) and the time of Retransmit Setup. (For the IDT72264, 8,192 when MAC is LOW, 16,384 when MAC is HIGH; For the IDT72274, Full = 16,384 words when MAC is LOW, 32,768 when MAC is LOW).

If IDT Standard mode is selected, the FIFO will mark the beginning of the Retransmit Setup by setting $\overline{EF}$ LOW. The change in level will only be noticeable if $\overline{EF}$ was HIGH before setup. During this period, the internal read pointer is initialized to the first location of the RAM array.

When $\overline{EF}$ goes HIGH, Retransmit Setup is complete and read operations may begin starting with the first location in memory. Since IDT Standard Mode is selected, every word read including the first word following Retransmit Setup requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. Writing operations can begin after one of two conditions have been met: $\overline{EF}$ is HIGH or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.

The deassertion time of $\overline{EF}$ during Retransmit Setup is variable. The parameter t_{RTF1}, which is measured from the rising RCLK edge enabled by $\overline{RT}$ to the rising edge of $\overline{EF}$ is described by the following equation:

$$t_{RTF1} \text{ max.} = 14*T_f + 3*T_{RCLK} \text{ (in ns)}$$

where Tf is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.

Regarding $\overline{FF}$: Note that since no more than Full - 2 writes are allowed between a Reset and a Retransmit Setup, FF will remain HIGH throughout the setup procedure.

For IDT Standard mode, updating the $\overline{PAE}$, $\overline{HF}$, and $\overline{PAF}$ flags begins with the "first" $\overline{REN}$-enabled rising RCLK edge following the end of Retransmit Setup (the point at which $\overline{EF}$ goes HIGH). This same RCLK rising edge is used to access the "first" memory location. $\overline{HF}$ is updated on the first RCLK rising edge. $\overline{PAE}$ is updated after two more rising RCLK edges. $\overline{PAF}$ is updated after the "first" rising RCLK edge, followed by the next two rising WCLK edges. (If the tskew2 specification is not met, add one more WCLK cycle.)

If FWFT mode is selected, the FIFO will mark the beginning of the Retransmit Setup by setting $\overline{OR}$ HIGH. The change in level will only be noticeable if $\overline{OR}$ was LOW before setup. During this period, the internal read pointer is set to the first location of the RAM array.

When $\overline{OR}$ goes LOW, Retransmit Setup is complete; at the same time, the contents of the first location are automatically displayed on the outputs. Since FWFT Mode is selected, the first word appears on the outputs, no read request necessary. Reading all subsequent words requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. Writing operations can begin after one of two conditions have been met: $\overline{OR}$ is LOW or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.

The assertion time of OR during Retransmit Setup is variable. The parameter t_{RTF2}, which is measured from the rising RCLK edge enabled by $\overline{RT}$ to the falling edge of $\overline{OR}$ is described by the following equation:

$$t_{RTF2} \text{ max.} = 14*T_f + 4*T_{RCLK} \text{ (in ns)}$$

where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period. Note that a Retransmit Setup in FWFT mode requires one more RCLK cycle than in IDT Standard mode.

Regarding $\overline{IR}$: Note that since no more than Full - 2 writes are allowed between a Reset and a Retransmit Setup, $\overline{IR}$ will remain LOW throughout the setup procedure.

For FWFT mode, updating the $\overline{PAE}$, $\overline{HF}$, and $\overline{PAF}$ flags begins with the "last" rising edge of RCLK before the end of Retransmit Setup. This is the same edge that asserts $\overline{OR}$ and automatically accesses the first memory location. Note that, in this case, $\overline{REN}$ is not required to initiate flag updating. $\overline{HF}$ is updated on the "last" RCLK rising edge. $\overline{PAE}$ is updated after two more rising RCLK edges. $\overline{PAF}$ is updated after the "last" rising RCLK edge, followed by the next two rising WCLK edges. (If the t_{SKEW2} specification is not met, add one more WCLK cycle.)

$\overline{RT}$ is synchronized to RCLK. The Retransmit operation is useful in the event of a transmission error on a network, since it allows a data packet to be resent.

FIRST WORD FALL THROUGH/SERIAL IN (FWFT/SI)

This is a dual purpose pin. During Master Reset, the state of the FWFT/SI input helps determine whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the FIFO memory. It also uses the Full Flag function ($\overline{FF}$) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$) line.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the data outputs (Q_n). It also uses Input Ready ($\overline{IR}$) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Q_n, no read request necessary. Subsequent words must be accessed using the Read Enable ($\overline{REN}$) line.

After Master Reset, FWFT/SI acts as a serial input for loading $\overline{PAE}$ and $\overline{PAF}$ offsets into the programmable registers. The serial input function can only be used when the serial loading method has been selected during Master Reset. FWFT/SI functions the same way in both IDT Standard and FWFT modes.

WRITE CLOCK (WCLK)

A write cycle is initiated on the rising edge of the WCLK input. Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. The write and read clocks can either be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)

When the $\overline{WEN}$ input is LOW, data can be loaded into the input register on the rising edge of every WCLK cycle. Data is stored in the RAM array sequentially and independently of any on-going read operation.

When $\overline{WEN}$ is HIGH, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow in the IDT Standard Mode, $\overline{FF}$ will go LOW , inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FF}$ will go HIGH allowing a write to occur. $\overline{WEN}$ is ignored when the FIFO is full.

To prevent data overflow in the FWFT mode, $\overline{IR}$ will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{IR}$ will go LOW allowing a write to occur.

$\overline{WEN}$ is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs, on the rising edge of the RCLK input, when Output Enable ($\overline{OE}$) is set LOW. The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)

When Read Enable is LOW, data is loaded from the RAM array into the output register on the rising edge of the RCLK.

When the $\overline{REN}$ input is HIGH, the output register holds the previous data and no new data is loaded into the output register.

In the IDT Standard Mode, every word accessed at Q_n, including the first word written to an empty FIFO, must be requested using $\overline{REN}$. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}$ will go HIGH after $t_{FWL1} + t_{REF}$ and a read is permitted.

In the FWFT Mode, the first word written to an empty FIFO automatically goes to the outputs Q_n, no need for any read request. In order to access all other words, a read must be executed using $\overline{REN}$. When all the data has been read from the FIFO, Output Ready ($\overline{OR}$) will go HIGH, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{OR}$ will go LOW after $t_{FWL2} + t_{REF}$, when the first word appears at Q_n ; if a second word is written into the FIFO, then $\overline{REN}$ can be used to read it out.

SERIAL ENABLE ($\overline{SEN}$)

The $\overline{SEN}$ input is an enable used only for serial programming of the offset registers. The serial programming method must be selected during Master Reset. $\overline{SEN}$ is always used in conjunction with $\overline{LD}$. When these lines are both LOW, data at the SI input can be loaded into the input register one bit for each LOW-to-HIGH transition of WCLK.

When $\overline{SEN}$ is HIGH, the programmable registers retains the previous settings and no offsets are loaded.

$\overline{SEN}$ functions the same way in both IDT Standard and FWFT modes.

$\overline{LD}$	$\overline{WEN}$	$\overline{REN}$	$\overline{SEN}$	WCLK	RCLK	Selection	
						MAC = Vcc	MAC = GND
0	0	1	1	↑	X	Parallel write to registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)	Parallel write to registers: Empty Offset Full Offset
0	1	0	1	X	↑	Parallel read from registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)	Parallel read from registers: Empty Offset Full Offset
0	1	1	0	↑	X	Serial shift into registers: 28 bits for the 72264 30 bits for the 72274 1 bit for each rising WCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)	Serial shift into registers: 26 bits for the 72264 28 bits for the 72274 1 bit for each rising WCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)
X	1	1	1	X	X	No Operation	No Operation
1	0	X	X	↑	X	Write Memory	Write Memory
1	X	0	X	X	↑	Read Memory	Read Memory
1	1	1	X	X	X	No Operation	No Operation

3218 tbl 01

NOTES:
1. Only one of the two offset programming methods, serial or parallel, is available for use at any given time.
2. The programming method can only be selected at Master Reset.
3. Parallel reading of the offset registers is always permitted regardless of which programming method has been selected.
4. The programming sequence applies to both IDT Standard and FWFT modes.

Figure 2. Partial Flag Programming Sequence

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is HIGH, the output data bus (Q_n) goes into a high impedance state.

LOAD ($\overline{LD}$)

This is a dual purpose pin. During Master Reset, the state of the $\overline{LD}$ input determines one of two default values (127 or 1023) for the $\overline{PAE}$ and $\overline{PAF}$ flags, along with the method by which these flags can be programmed, parallel or serial. After Master Reset, $\overline{LD}$ enables write operations to and read operations from the registers. Only the offset loading method currently selected can be used to write to the registers. Aside from Master Reset, there is no other way change the loading method. Registers can be read only in parallel; this can be accomplished regardless of whether serial or the parallel loading has been selected.

Associated with each of the programmable flags, $\overline{PAE}$ and $\overline{PAF}$, is one register which can either be written to or read from. Offset values contained in these registers determine how many words need to be in the FIFO memory to switch a partial flag. A LOW on $\overline{LD}$ during Master Reset selects a default $\overline{PAE}$ offset value of 07FH (a threshold 127 words from the empty boundary), a default $\overline{PAF}$ offset value of 07FH (a threshold 127 words from the full boundary), and parallel loading of other offset values. A HIGH on $\overline{LD}$ during Master Reset selects a default $\overline{PAE}$ offset value of 3FFH (a threshold 1023 words from the empty boundary), a default $\overline{PAF}$ offset value of 3FFH (a threshold 1023 words form the full boundary), and serial loading of other offset values.

The act of writing offsets (in parallel or serial) employs a dedicated write offset register pointer. The act of reading offsets employs a dedicated read offset register pointer. The two pointers operate independently; however, a read and a write should not be performed simultaneously to the offset registers. A Master Reset initializes both pointers to the Empty Offset (LSB) register. A Partial Reset has no effect on the position of these pointers.

It is important to note that the MAC setting configures the offset register architecture to suit the memory array dimensions being selected. Therefore, the way offsets are programmed will vary according to whether MAS is tied to Vcc or GND.

Consider the case where serial offset loading has been selected. If MAC = GND (18-bit operation), then programming $\overline{PAE}$ and $\overline{PAF}$ proceeds as follows: When $\overline{LD}$ and $\overline{SEN}$ are set LOW, data on the SI input are written, one bit for each WCLK rising edge, starting with the Empty Offset (13 bits for the 72264, 14 bits for the 72274) and ending with the Full Offset (13 bits for the 72264, 14 bits for the 72274). A total of 26 bits are necessary to program the 72264; a total of 28 bits are necessary to program the 72274.

If serial offset loading has been selected and MAC = Vcc (9-bit operation), then programming $\overline{PAE}$ and $\overline{PAF}$ proceeds as follows: When $\overline{LD}$ and $\overline{SEN}$ are set LOW, data on the SI input are written, one bit for each WCLK rising edge, starting with the Empty Offset LSB (8 bits for both the 72264 and 72274), then the Empty Offset MSB (6 bits for the 72264, 7 bits for the 72274) , then the Full Offset LSB (8 bits for both the 72264 and 72274), ending with the Full Offset MSB (6 bits for the 72264, 7 bits for the 72274). A total of 28 bits are necessary to program the 72264; a total of 30 bits are necessary to program the 72274.

For either MAC setting, individual registers cannot be loaded serially; rather, all offsets must be programmed in sequence, no padding allowed. $\overline{PAE}$ and $\overline{PAF}$ can show a valid status only after the full set of bits have been entered. The registers can be re-programmed as long as all offsets are loaded. When $\overline{LD}$ is LOW and $\overline{SEN}$ is HIGH, no serial write to the registers can occur.

Consider the case where parallel offset loading has been selected. If MAC = GND (18-bit operation), then programming $\overline{PAE}$ and $\overline{PAF}$ proceeds as follows: When $\overline{LD}$ and $\overline{WEN}$ are set LOW, data on the inputs D_n are written into the Empty Offset Register on the first LOW-to-HIGH transition of WCLK. Upon the second LOW-to-HIGH transition of WCLK, data at the inputs are written into the Full Register. The third transition of WCLK writes, once again, to the Empty Offset Register.

If parallel offset loading has been selected and MAC = Vcc (9-bit operation), then programming $\overline{PAE}$ and $\overline{PAF}$ proceeds as follows: When $\overline{LD}$ and $\overline{WEN}$ are set LOW, data on the inputs D_n are written into the LSB Empty Offset Register on the first LOW-to-HIGH transition of WCLK. Upon the second LOW-to-HIGH transition of WCLK, data at the inputs are written into the MSB Empty Offset Register. Upon the third LOW-to-HIGH transition of WCLK, data at the inputs are written into the LSB Full Offset Register. Upon the fourth LOW-to-HIGH transition of WCLK, data at the inputs are written into the MSB Full Offset Register. The fifth transition of WCLK writes, once again, to the LSB Empty Offset Register.

To ensure proper programming (serial or parallel) of the offset registers, no read operation is permitted from the time of reset (master or partial) to the time of programming. (During this period, the read pointer must be pointing to the first location of the memory array.) After the programming has been accomplished, read operations may begin.

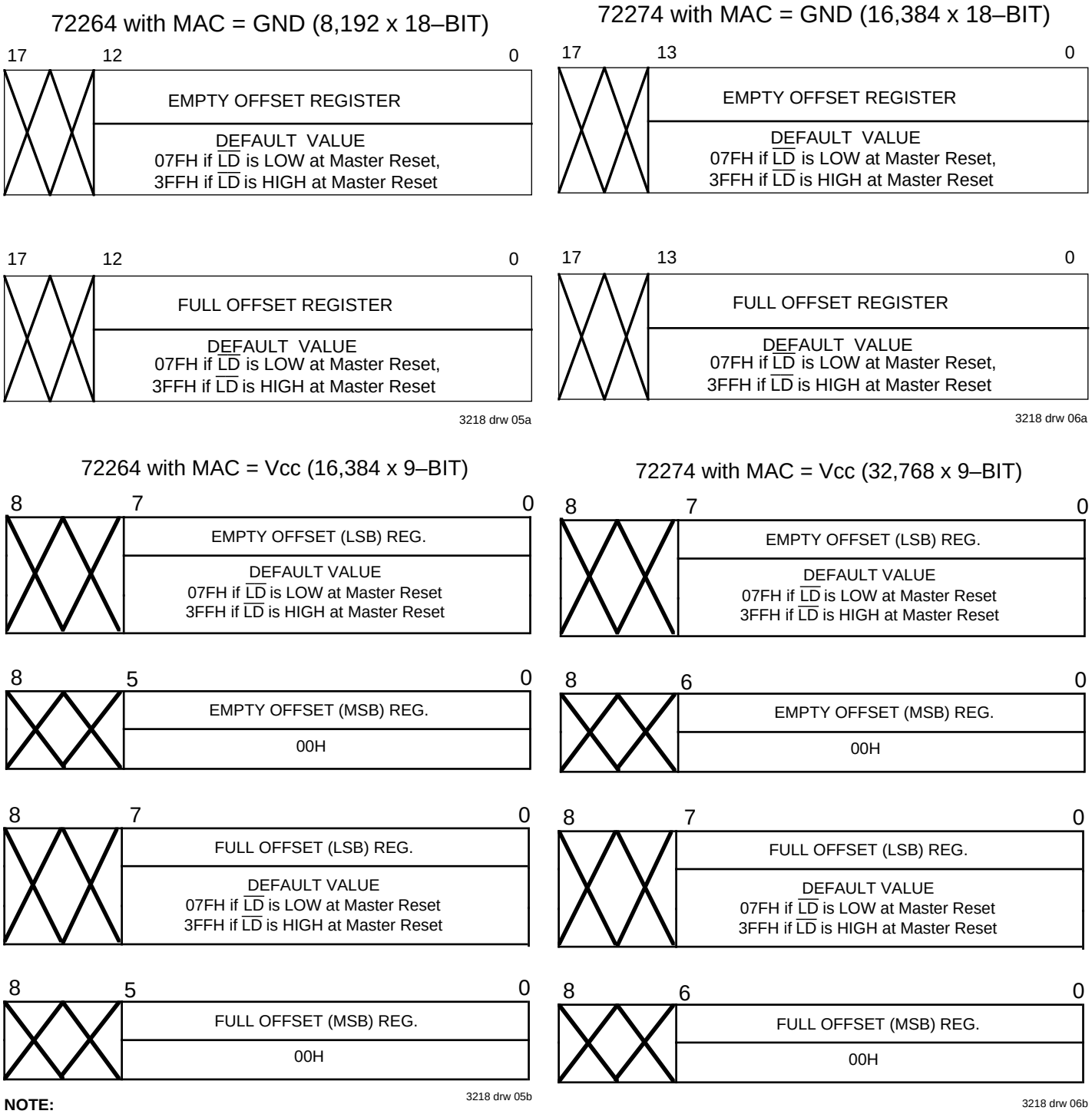
Write operations to memory are allowed before and during the parallel programming sequence. In this case, the programming of all offset registers does not have to occur at one time. One or two offset registers can be written to and then, by bringing $\overline{LD}$ HIGH, write operations can be redirected to the FIFO memory. When $\overline{LD}$ is set LOW again, and $\overline{WEN}$ is LOW, the next offset register in sequence is written to. As an alternative to holding $\overline{WEN}$ LOW and toggling $\overline{LD}$, parallel programming can also be interrupted by setting $\overline{LD}$ LOW and toggling $\overline{WEN}$.

Write operations to memory are allowed before and during the serial programming sequence. In this case, the programming of all offset bits does not have to occur at once. A select number of bits can be written to the SI input and then, by bringing $\overline{LD}$ and $\overline{SEN}$ HIGH, data can be written to FIFO memory via D_n by toggling $\overline{WEN}$. When $\overline{WEN}$ is brought HIGH with $\overline{LD}$ and $\overline{SEN}$ restored to a LOW, the next offset bit in sequence is written to the registers via SI. If a mere interruption of serial programming is desired, it is sufficient either to set

$\overline{LD}$ LOW and deactivate $\overline{SEN}$ or to set $\overline{SEN}$ LOW and deactivate $\overline{LD}$. Once $\overline{LD}$ and $\overline{SEN}$ are both restored to a LOW level, serial offset programming continues from where it left off.

Note that the status of a partial flag ($\overline{PAE}$ or $\overline{PAF}$) output is invalid during the programming process. From the time parallel programming has begun, a partial flag output will not be valid until the appropriate offset word has been written to the register(s) pertaining to that flag. From the time serial programming has begun, neither partial flag will be valid until the full set of bits required to fill all the offset registers has been written. Measuring from the rising WCLK edge that achieves either of the above criteria; $\overline{PAF}$ will be valid after two more rising WCLK edges plus t_{PAF}, $\overline{PAE}$ will be valid after the next two rising RCLK edges plus t_{PAE} (Add one more RCLK cycle if t_{SKEW2} is not met.)

The act of reading the offset registers employs a dedicated read offset register pointer. The contents of the offset registers can be read on the output lines when $\overline{LD}$ is set LOW and



NOTE:
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

$\overline{REN}$ is set LOW. If MAC = GND (18-bit operation), then data are read via Q_n from the Empty Offset Register on the first LOW-to-HIGH transition of RCLK. Upon the second LOW-to-HIGH transition of RCLK, data are read from the Full Offset Register. The third transition of RCLK reads, once again, from the Empty Offset Register.

If MAC = Vcc (9-bit operation) when reading the offset registers, then data are read via Q_n from the LSB Empty Offset Register on the first LOW-to-HIGH transition of RCLK. Upon the second LOW-to-HIGH transition of RCLK, data are read from the MSB Empty Offset Register. Upon the third LOW-to-HIGH transition of RCLK, data are read from the LSB Full Offset Register. Upon the fourth LOW-to-HIGH transition of RCLK, data are read from the MSB Full Offset Register. The fifth transition of RCLK reads, once again, from the LSB Empty Offset Register.

It is permissible to interrupt the offset register access sequence with reads or writes to memory . The interruption is accomplished by deasserting $\overline{REN}$, $\overline{LD}$, or both together. When $\overline{REN}$ and $\overline{LD}$ are restored to a LOW level, access of the registers continues where it left off.

$\overline{LD}$ functions the same way in both IDT Standard and FWFT modes.

FREQUENCY SELECT INPUT (FS)

An internal state machine manages the movement of data through the SuperSync FIFO. The FS line determines whether RCLK or WCLK will synchronize the state machine. The clock tied to the state machine is referred to as the "selected clock". The clock that is not tied to the state machine is referred to as the "non-selected clock". To set FS, follow the guidelines presented in Figure 3; this ensures efficient handling of the data within the FIFO. Once having determined the FS setting, it is permissible to vary the WCLK and RCLK frequencies, as long as the inequalities corresponding to the chosen FS level hold true. (See Figure 3.)

For example, if FS is set LOW, then the selected clock is RCLK, whose frequency, f_{RCLK}, may vary anywhere from $f_{WCLK}/2$ to the maximum allowable clock frequency a speed grade permits (f_s max. from AC Electrical Characteristics table). The non-selected clock is WCLK, whose frequency, f_{WCLK}, may vary anywhere from 0 to 2 f_{RCLK} (as long f_s max. as is not exceeded).

If FS is set HIGH, then the selected clock is WCLK, whose frequency, f_{WCLK}, may vary anywhere from $f_{RCLK}/2$ to the maximum allowable clock frequency a speed grade permits (f_s max.). The non-selected clock is RCLK, whose frequency, f_{RCLK}, may vary anywhere from 0 to 2 f_{WCLK} (as long f_s max. as is not exceeded).

The selected clock must be continuous. It is, however, permissible to stop the non-selected clock. Note, as long as RCLK is idle, $\overline{EF}/\overline{OR}$ and $\overline{PAE}$ will not be updated. Likewise, as long as WCLK is idle, $\overline{FF}/\overline{IR}$ and $\overline{PAF}$ will not be updated.

Changing the FS setting during FIFO operation (i.e. reading or writing) is not permitted; however, such a change at the time of Master Reset or Partial Reset is all right. FS is an asynchronous input.

OUTPUTS:

FULL FLAG ($\overline{FF}/\overline{IR}$)

This is a dual purpose pin. In IDT Standard Mode, the Full Flag ($\overline{FF}$) function is selected. When the FIFO is full (i.e. the write pointer catches up to the read pointer), $\overline{FF}$ will go LOW, inhibiting further write operation. When $\overline{FF}$ is HIGH, the FIFO is not full. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{FF}$ will go LOW after 8,192 writes for the IDT72264 and 16,384 writes to the IDT72274 when MAC = GND. If MAC = Vcc, $\overline{FF}$ will go LOW after 16,384 writes for the IDT72264 and 32,768 writes to the IDT72274.

In FWFT Mode, the Input Ready (IR) function is selected. IR goes LOW when memory space is available for writing in data. When there is no longer any free space left, IR goes HIGH, inhibiting further write operation. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), IR will go HIGH after 8,193 writes for the IDT72264 and 16,385 writes for the IDT72274 when MAC = GND. If MAC = Vcc, IR will go HIGH after 16,385 writes for the IDT72264 and 32,769 writes to the IDT72274.

The IR status not only measures the contents of the FIFO memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to deassert IR is one greater than needed to assert FF in IDT Standard mode.

FF/IR is synchronized to WCLK. It is double-registered to enhance metastable immunity.

FS	Clock Identity	Clock Frequency Range
LOW	Selected Clock = RCLK	$f_{WCLK}/2 < f_{RCLK} \le f_s$ max.
	Non-selected Clock = WCLK	$0 \le f_{WCLK} < 2f_{RCLK}$
HIGH	Selected Clock = WCLK	$f_{RCLK}/2 < f_{WCLK} \le f_s$ max.
	Non-selected Clock = RCLK	$0 \le f_{RCLK} < 2f_{WCLK}$

Figure 3. Guidelines for Determining the FS Setting and the Range of Allowable Clock Frequency Variation

EMPTY FLAG ($\overline{EF}$/$\overline{OR}$)

This is a dual purpose pin. In the IDT Standard Mode, the Empty Flag ($\overline{EF}$) function is selected. When the FIFO is empty (i.e. the read pointer catches up to the write pointer), $\overline{EF}$ will go LOW, inhibiting further read operations. When $\overline{EF}$ is HIGH, the FIFO is not empty.

When writing the first word to an empty FIFO, the deassertion time of $\overline{EF}$ is variable, and can be represent by the First Word Latency parameter, t_{FWL1}, which is measured from the rising WCLK edge that writes the first word to the rising RCLK edge that updates the flag. t_{FWL1} includes any delays due to clock skew and can be expressed as follows:

$$t_{FWL1} \text{ max.} = 10*T_f + 2*T_{RCLK} \text{ (in ns)}$$

where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period. Since no read can take place until $\overline{EF}$ goes HIGH, the t_{FWL1} delay determines how early the first word can be available at Q_n. This delay has no effect on the reading of subsequent words.

In FWFT Mode, the Output Ready ($\overline{OR}$) function is selected. $\overline{OR}$ goes LOW at the same time that the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}$ goes HIGH one cycle after RCLK shifts the last word from the FIFO memory to the outputs. Then further data reads are inhibited until $\overline{OR}$ goes LOW again.

When writing the first word to an empty FIFO, the assertion time of $\overline{OR}$ is variable, and can be represented by the First Word Latency parameter, t_{FWL2}, which is measured from the rising WCLK edge that writes the first word to the rising RCLK edge that updates the flag. t_{FWL2} includes any delay due to clock skew and can be expressed as follows:

$$t_{FWL2} \text{ max.} = 10*T_f + 3*T_{RCLK} \text{ (in ns)}$$

where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period. Note that the First Word Latency in FWFT mode is one RCLK cycle longer than in IDT Standard mode. The t_{FWL2} delay determines how early the first word can be available at Q_n. This delay has no effect on the reading of subsequent words.

$\overline{EF}$/$\overline{OR}$ is sychronized to the RCLK. It is double-registered to enhance metastable immunity.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW when the FIFO reaches the Almost-Full condition as specified by the offset m stored in the Full Offset register.

At the time of Master Reset, depending on the state of $\overline{LD}$, one of two possible default offset values are chosen. If $\overline{LD}$ is LOW, then m = 07FH and the $\overline{PAF}$ switching threshold is 127 words from the Full boundary, if $\overline{LD}$ is HIGH, then m = 3FFH and the $\overline{PAF}$ switching threshold is 1023 words away from the Full boundary.

Any integral value of m from 0 to the maximum FIFO depth minus 1 (8,191 words for the 72264 and 16,383 words for the 72274 when MAC = GND; 16,383 words for the 72264 and 32,767 words for the 72274 when MAC = Vcc) can be programmed into the Full Offset register.

In IDT Standard Mode with MAC = GND, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{PAF}$ will go LOW after (8,192-m) writes to the IDT72264, and (16,384-m) writes to the IDT72274. If MAC = Vcc, $\overline{PAF}$ will go LOW after (16,384-m) writes to the IDT72264, and (32,768-m) writes to the IDT72274.

In FWFT Mode with MAC = GND, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{PAF}$ will go LOW after (8,193-m) writes to the IDT72264, and (16,385-m) writes to the IDT72274. If MAC = Vcc, $\overline{PAF}$ will go LOW after (16,385-m) writes to the IDT72264, and (32,679-m) writes to the IDT72274. In FWFT Mode, the first word written to an empty FIFO does not stay in memory, but goes unrequested to the output register; therefore, it has no effect on determining the state of $\overline{PAF}$.

Note that even though $\overline{PAF}$ is programmed to switch LOW during the first word latency period (t_{FWL}), attempts to read data will be ignored until $\overline{EF}$ goes HIGH indicating that data is available at the output port. This is true for both timing modes.

$\overline{PAF}$ is synchronous and updated on the rising edge of WCLK. It is double-registered to enhance metastable immunity.

TABLE I –– STATUS FLAGS FOR IDT STANDARD MODE

Number of Words in FIFO Memory[1]								
72264		72274						
MAC =GND	MAC = Vcc	MAC = GND	MAC = Vcc	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	0	H	H	H	L	L
1 to n[2]	1 to n[2]	1 to n[2]	1 to n [2]	H	H	H	L	H
(n+1) to 4,096	(n+1) to 8,192	(n+1) to 8,192	(n+1) to 16,384	H	H	H	H	H
4,097 to (8,192-(m+1))	8,193 to (16,384-(m+1))	8,193 to (16,384-(m+1))	16,385 to (32,768-(m+1))	H	H	L	H	H
(8,192-m)[3] to 8,191	(16,384-m)[3] to 16,383	(16,384-m)[3] to 16,383	(32,768-m)[3] to 32,767	H	L	L	H	H
8,192	16,384	16,384	32,768	L	L	L	H	H

NOTES:
1. Data in the output register does not count as a 'word in FIFO memory". Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
2. n = Empty Offset, Default Values: n = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.
3. m = Full Offset, Default Values: m = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW when the FIFO reaches the Almost-Empty condition as specified by the offset n stored in the Empty Offset register.

At the time of Master Reset, depending on the state of $\overline{LD}$, one of two possible default offset values are chosen. If $\overline{LD}$ is LOW, then n = 07FH and the $\overline{PAE}$ switching threshold is 127 words from the Empty boundary, if $\overline{LD}$ is HIGH, then n = 3FFH and the $\overline{PAE}$ switching threshold is 1023 words away from the Empty boundary.

Any integral value of n from 0 to the maximum FIFO depth minus 1 (8,191 words for the 72264 and 16,383 words for the 72274 when MAC = GND; 16,383 words for the 72264 and 32,767 words for the 72274 when MAC = Vcc) can be programmed into the Empty Offset register.

In IDT Standard Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), the $\overline{PAE}$ will go HIGH after (n + 1) writes to the IDT72264/72274.

In FWFT Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), the $\overline{PAE}$ will go HIGH after (n+2) writes to the IDT72264/72274. In this case, the first word written to an empty FIFO does not stay in memory, but goes unrequested to the output register; therefore, it has no effect on determining the state of $\overline{PAE}$.

Note that even though $\overline{PAE}$ is programmed to switch HIGH during the first word latency period (t_{FWL}), attempts to read data will be ignored until $\overline{EF}$ goes HIGH indicating that data is available at the output port. This is true for both timing modes.

$\overline{PAE}$ is synchronous and updated on the rising edge of RCLK. It is double-registered to enhance metastable immunity.

HALF-FULL FLAG ($\overline{HF}$)

This output indicates a half-full memory. The rising WCLK edge that fills the memory beyond half-full sets $\overline{HF}$ LOW. The flag remains LOW until the difference between the write and read pointers becomes less than or equal to half of the total depth of the device; the rising RCLK edge that accomplishes this condition also sets $\overline{HF}$ HIGH.

In IDT Standard Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ will go LOW after (D/2 + 1) writes, where D is the maximum FIFO depth (8,192 words for the 72264 and 16,384 words for the 72274 when MAC = GND; 16,384 words for the 72264 and 32,768 words for the 72274 when MAC = Vcc).

In FWFT Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ will go LOW after (D/2+2) writes to the IDT72264/72274. In this case, the first word written to an empty FIFO does not stay in memory, but goes unrequested to the output register; therefore, it has no effect on determining the state of $\overline{HF}$.

Because $\overline{HF}$ uses both RCLK and WCLK for synchronization purposes, it is asynchronous.

DATA OUTPUTS (Q_0-Q_{17})

All 18 data outputs (Q_0 - Q_{17}) function when the Memory Array Configuration input (MAC) is tied to ground. Only 9-data inputs (Q_0 - Q_8) function when MAC is connected to Vcc. The other data inputs (Q_9 - Q_{17}), though they do not function, are nevertheless active and should be left open.

TABLE II –– STATUS FLAGS FOR FWFT MODE

Number of Words in FIFO Memory[1]								
72264		72274						
MAC = GND	MAC = Vcc	MAC = GND	MAC = Vcc	$\overline{IR}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{OR}$
0	0	0	0	L	H	H	L	H[4]
1 to n[2]	1 to n[2]	1 to n[2]	1 to n [2]	L	H	H	L	L
(n+1) to 4,096)	(n+1) to 8,192	(n+1) to 8,192	(n+1) to 16,384	L	H	H	H	L
4,097 to (8,192-(m+1))	8,193 to (16,384-(m+1))	8,193 to (16,384-(m+1))	16,385 to (32,768-(m+1))	L	H	L	H	L
(8,192-m)[3] to 8,191	(16,384-m)[3] to 16,383	(16,384-m)[3] to 16,383	(32,768-m)[3] to 32,767	L	L	L	H	L
8,192	16,384	16,384	32,768	H	L	L	H	L

NOTES:
1. Data in the output register does not count as a 'word in FIFO memory". Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
2. n = Empty Offset, Default Values: n = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.
3. m = Full Offset, Default Values: m = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.
4. Following a reset (Master or Partial), the FIFO memory is empty and $\overline{OR}$ = HIGH. After writing the first word, the FIFO memory remains empty, the data is placed into the output register, and $\overline{OR}$ goes LOW. In this case, or any time the last word in the FIFO memory has been read into the output register; a rising RCLK edge, enabled by $\overline{REN}$, will set $\overline{OR}$ HIGH.

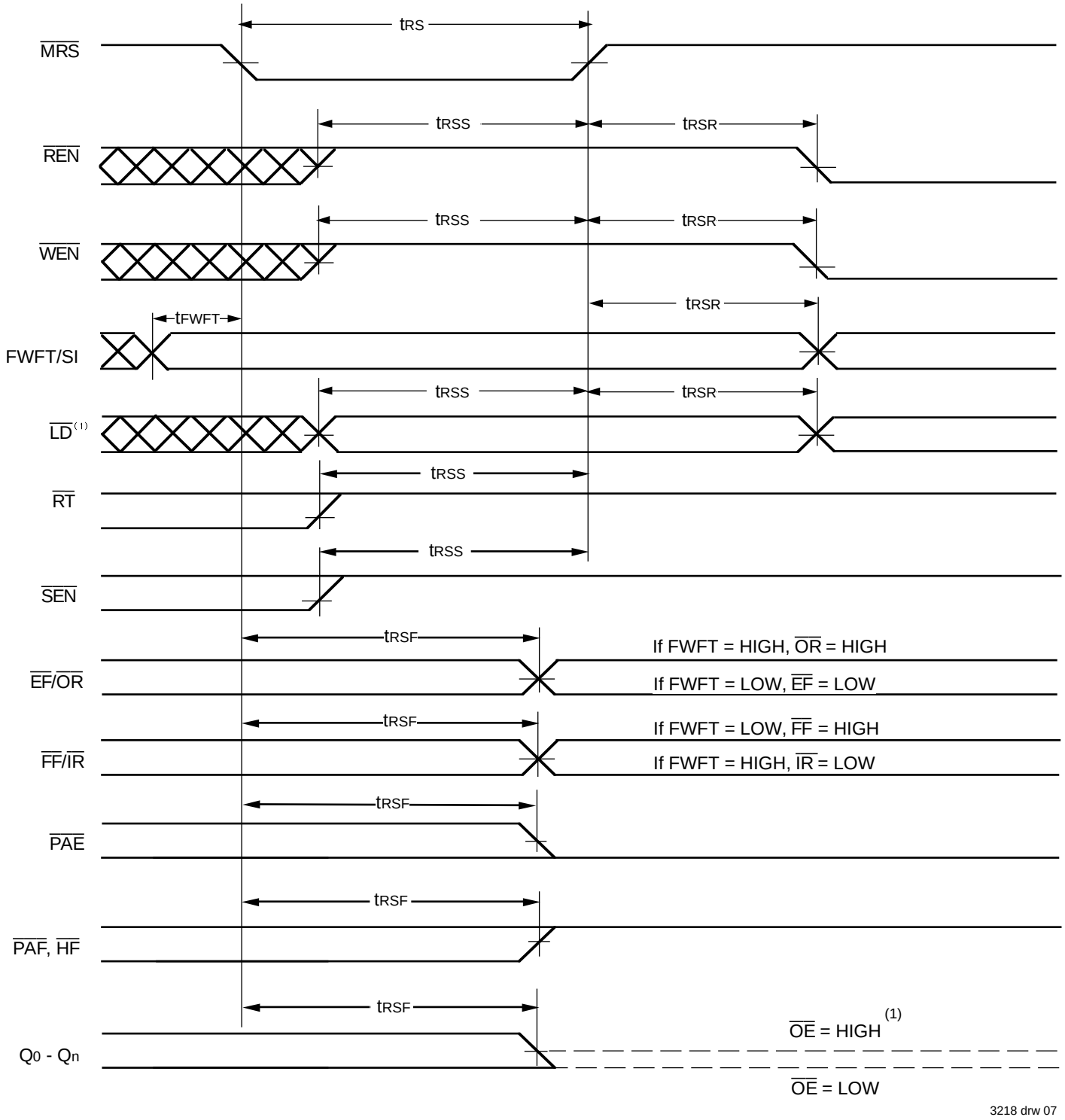


Figure 4. Master Reset Timing

NOTE:
1. Use MAC to select the memory array configuration by connecting it to either GND (18-bit operation) or Vcc (9-bit operation) before Master Reset

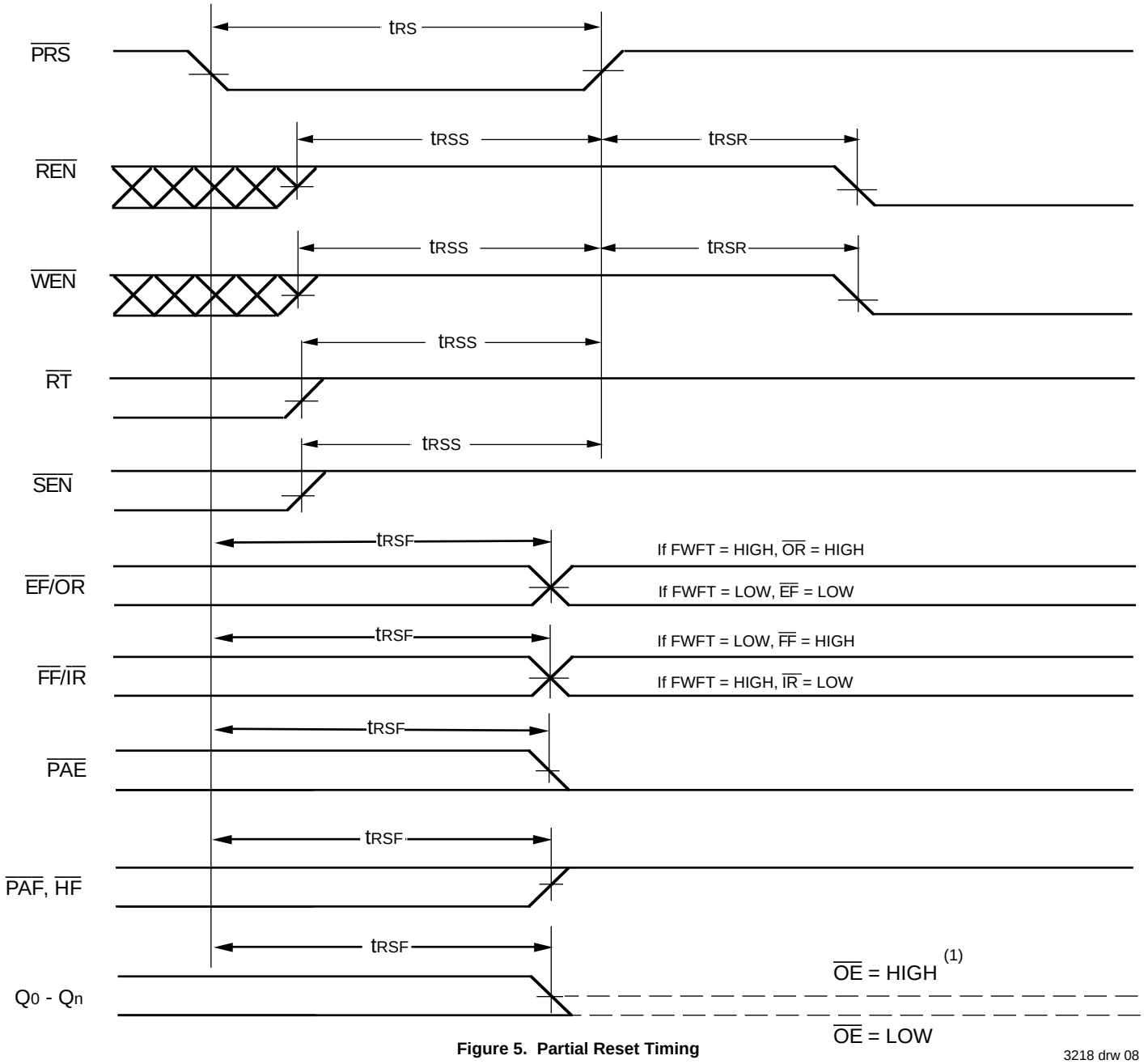
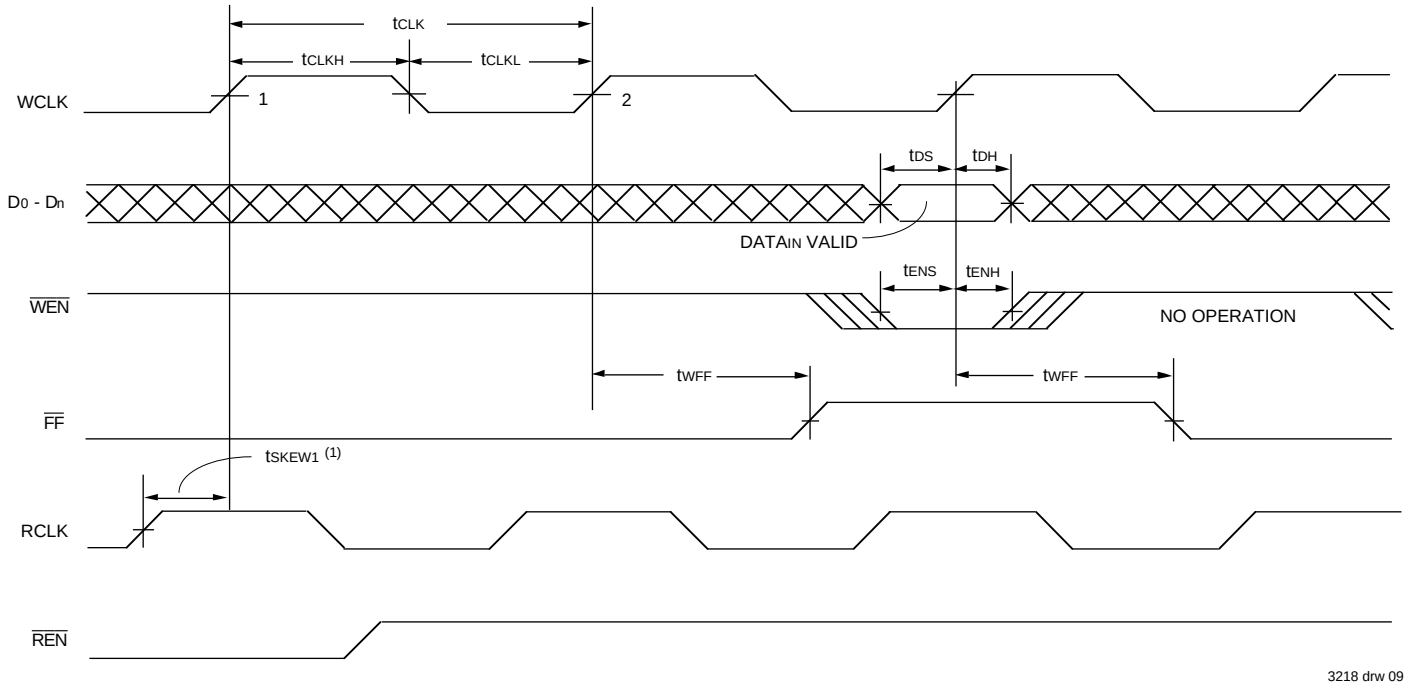


Figure 5. Partial Reset Timing

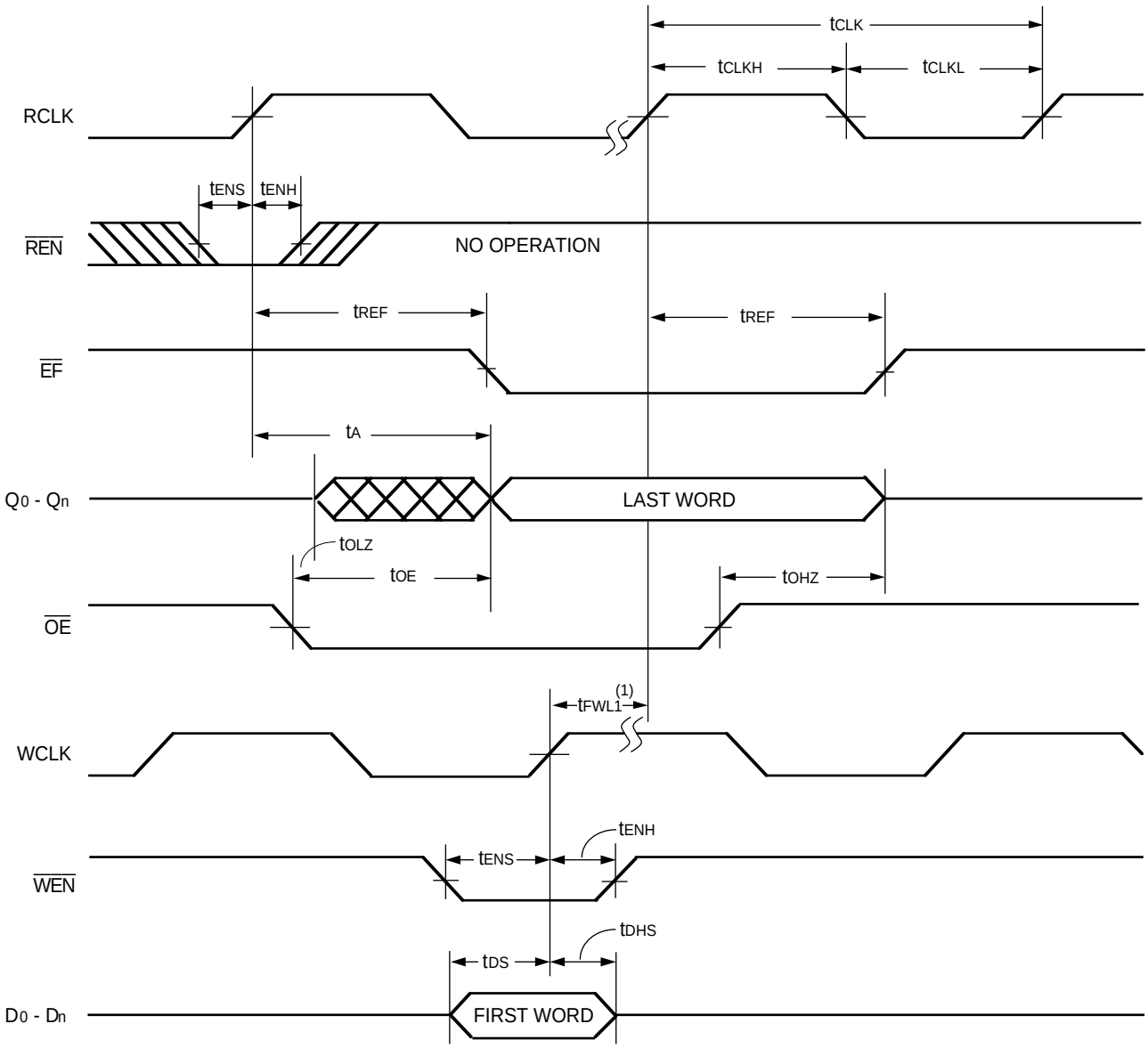
3218 drw 08



NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle plus t_{WFF}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then the $\overline{FF}$ deassertion may be delayed an extra WCLK cycle.
2. $\overline{LD}$ = HIGH

Figure 6. Write Cycle Timing (IDT Standard Mode)

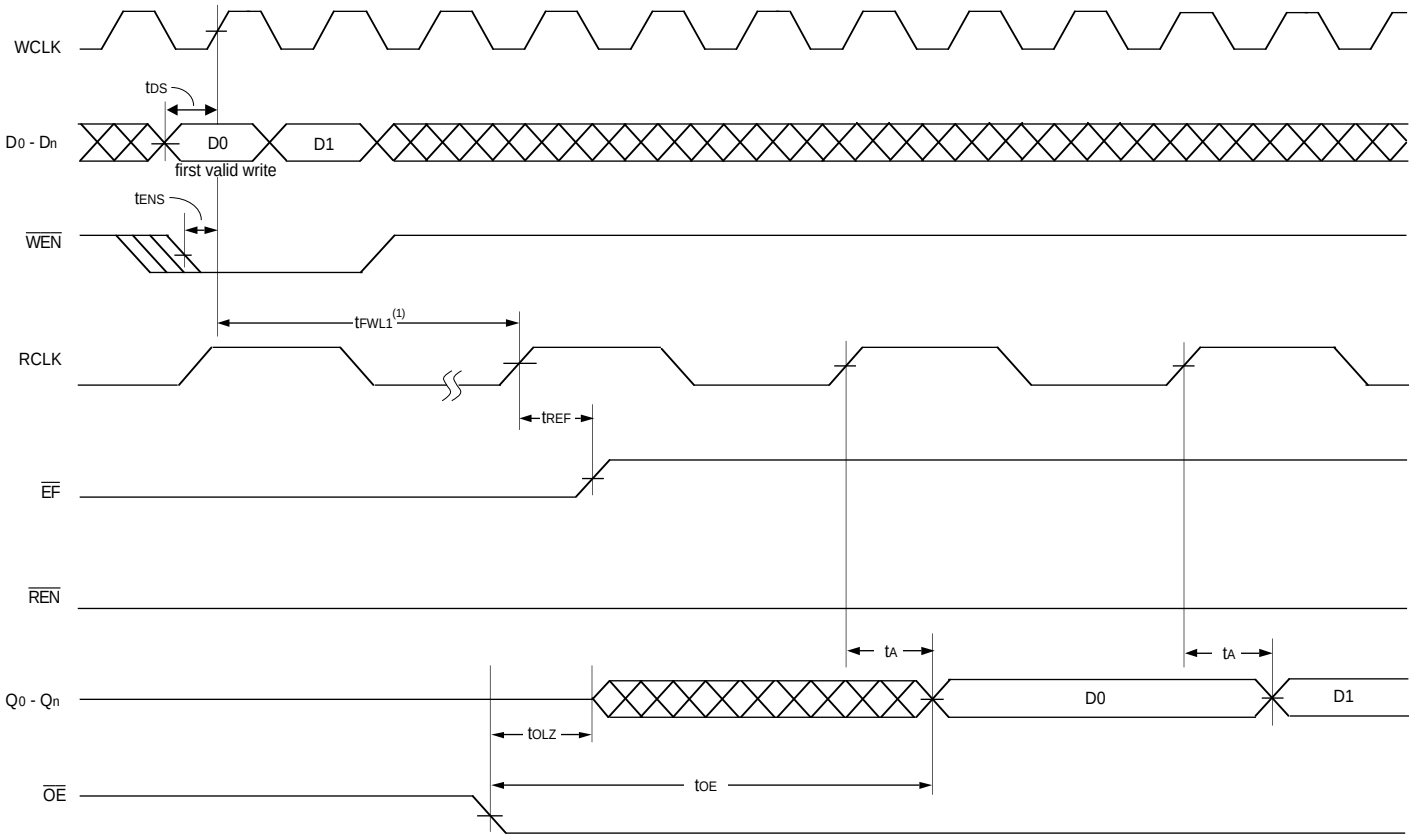


3218 drw 10

NOTES:

1. t_{FWL1} contributes a variable delay to the overall first word latency (this parameter includes delays due to skew):
   t_{FWL1} max. (in ns) = $10*T_f + 2*T_{RCLK}$
   where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period
2. $\overline{LD}$ = HIGH

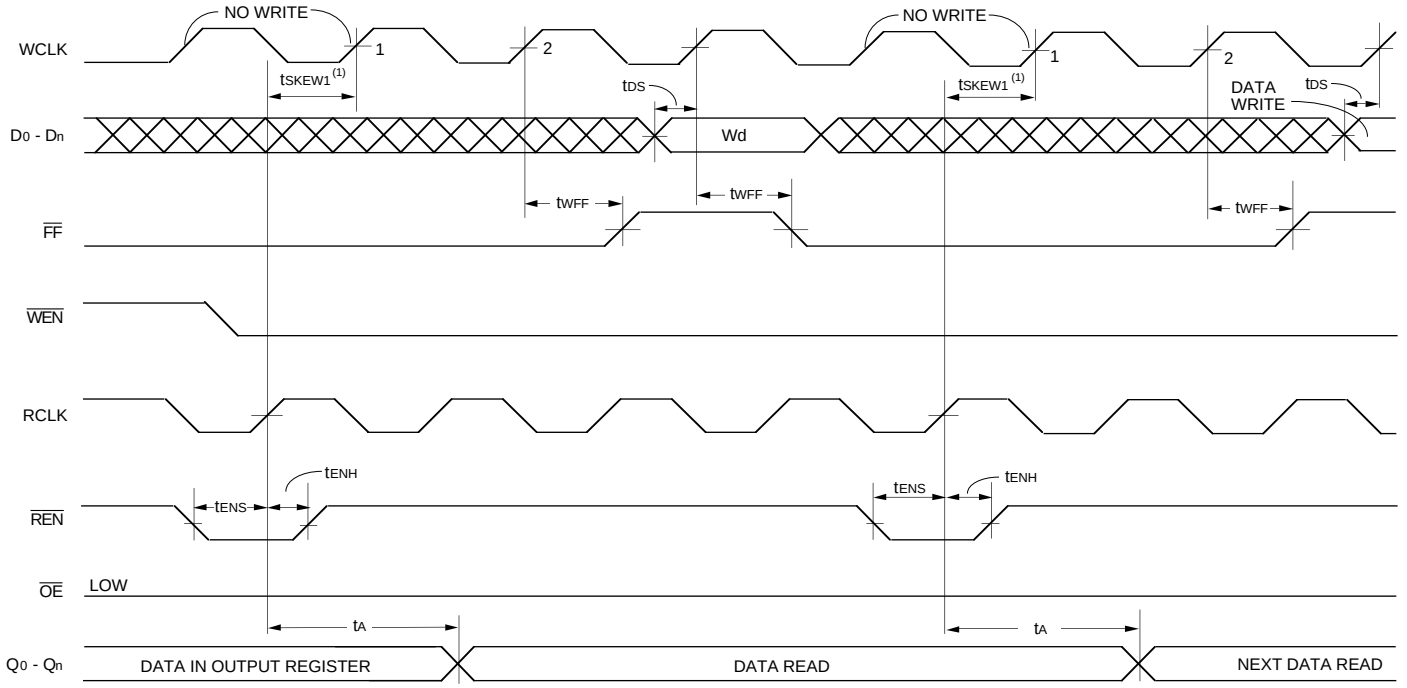
Figure 7. Read Cycle Timing (IDT Standard Mode)



3218 drw 11

NOTES:
1. t_{FWL1} max. (in ns) = 10* T_f + 2* T_{RCLK}
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period
2. $\overline{LD}$ = HIGH

Figure 8. First Data Word Latency (IDT Standard Mode)

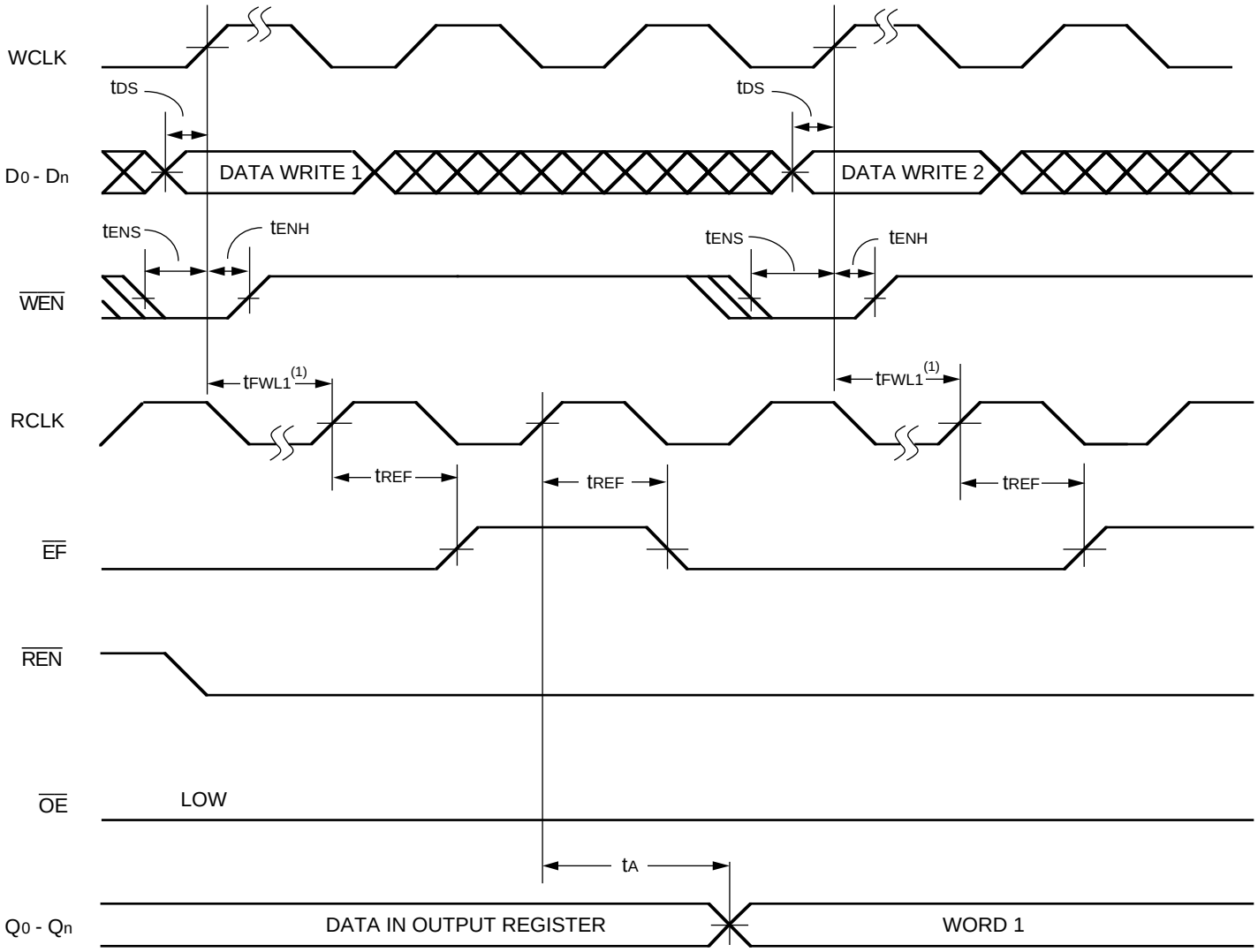


3218 drw 12

NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go high (after one WCLK cycle pus t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{SKEW1}, then the $\overline{FF}$ deassertion may be delayed an extra WCLK cycle.
2. $\overline{LD}$ = HIGH

Figure 9. Full Flag Timing (IDT Standard Mode)



3218 drw 13

NOTES:
1. t_{FWL1} max. (in ns) = 10*T_f + 2*T_{RCLK}
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the period.
2. $\overline{LD}$ = HIGH

Figure 10. Empty Flag Timing (IDT Standard Mode)

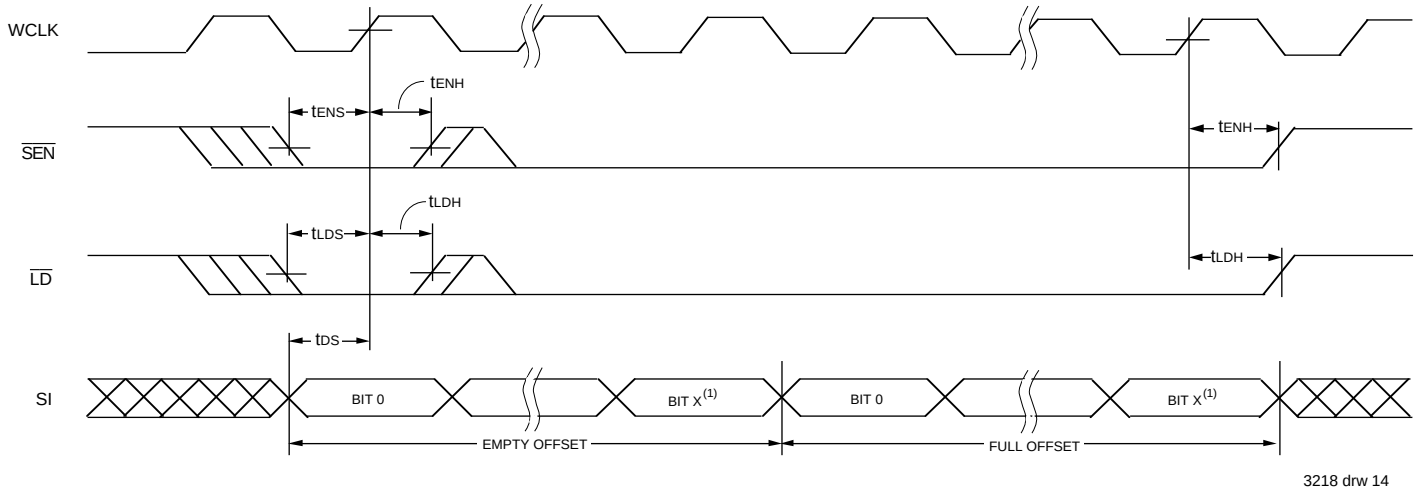


Figure 11. Serial Loading of Programmable Flag Registers (IDT Standard and FWFT modes)

NOTE:
1. If MAC is tied to GND, X = 12 for the 72264 and X = 13 for the 72274. If MAC is tied to Vcc, X = 5 for the 72264 and X = 6 for the 72274.

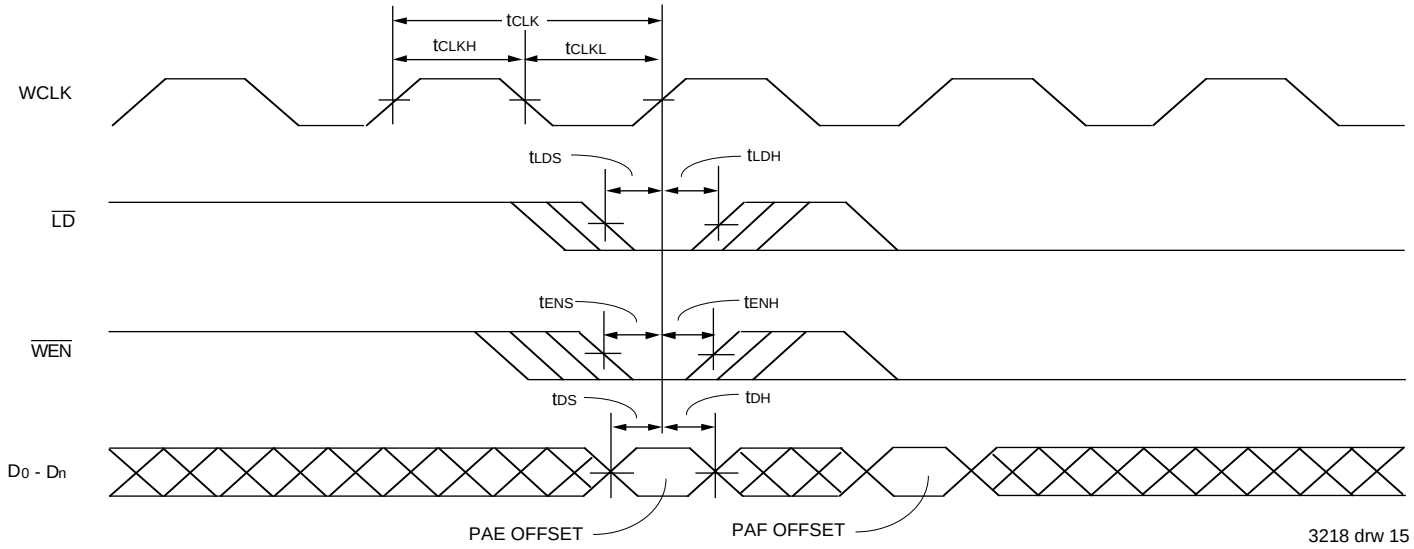


Figure 12. Parallel Loading of Programmable Flag Registers (IDT Standard and FWFT modes)

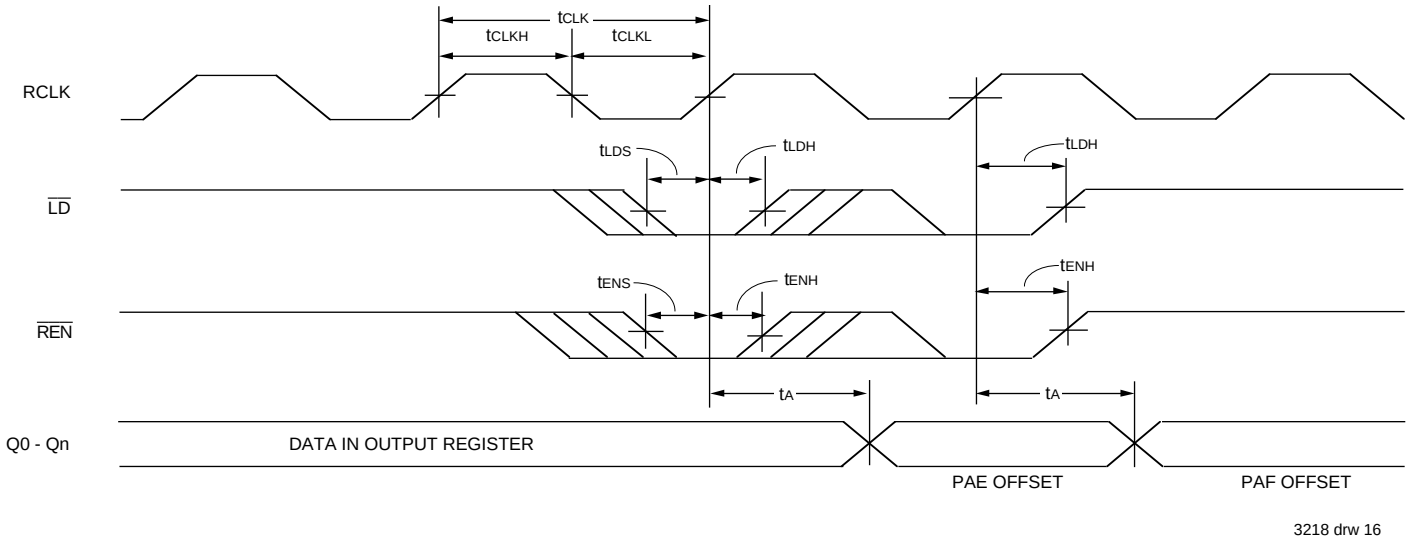
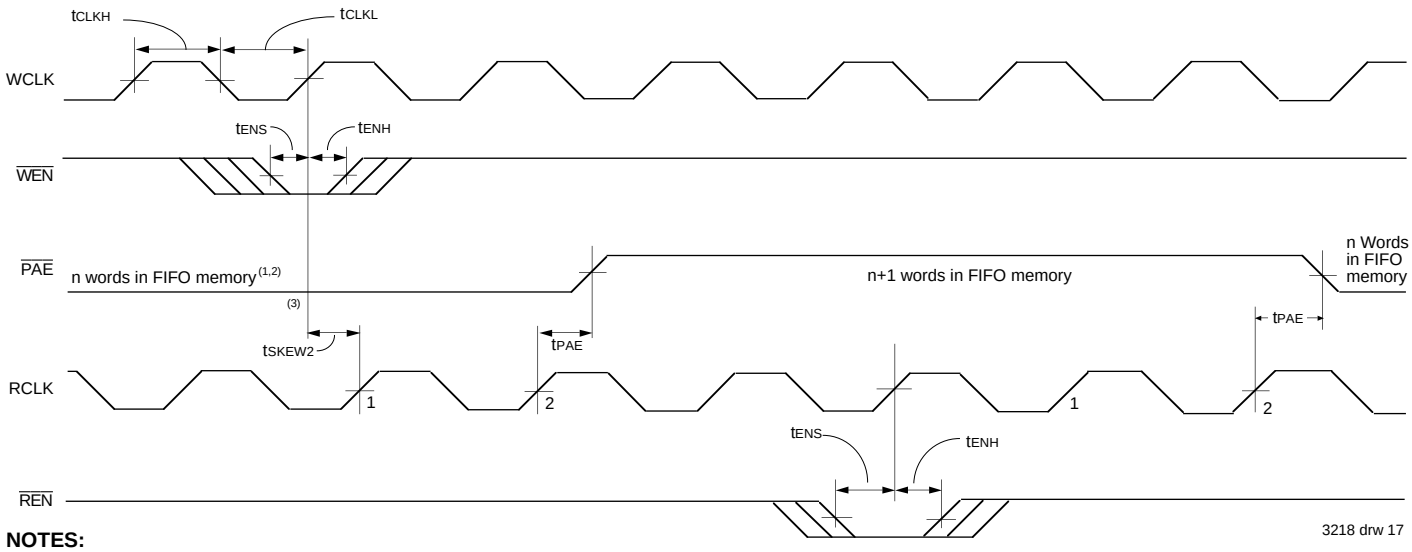


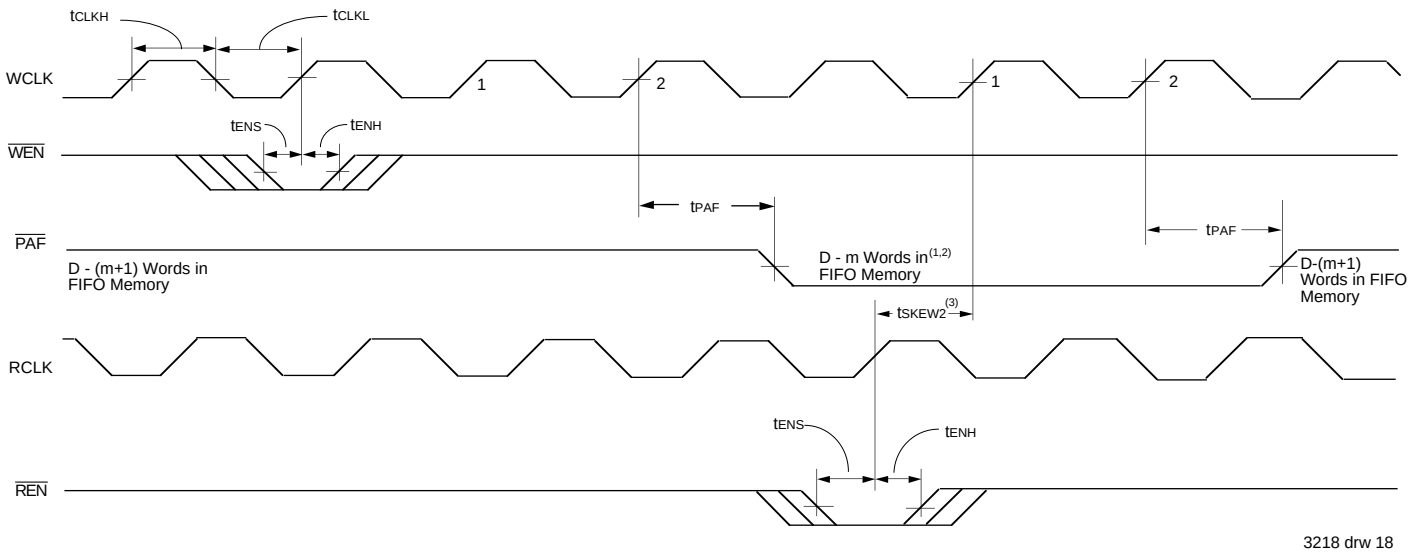
Figure 13. Parallel Read of Programmable Flag Registers (IDT Standard and FWFT modes)

NOTE:
1. $\overline{OE}$=LOW



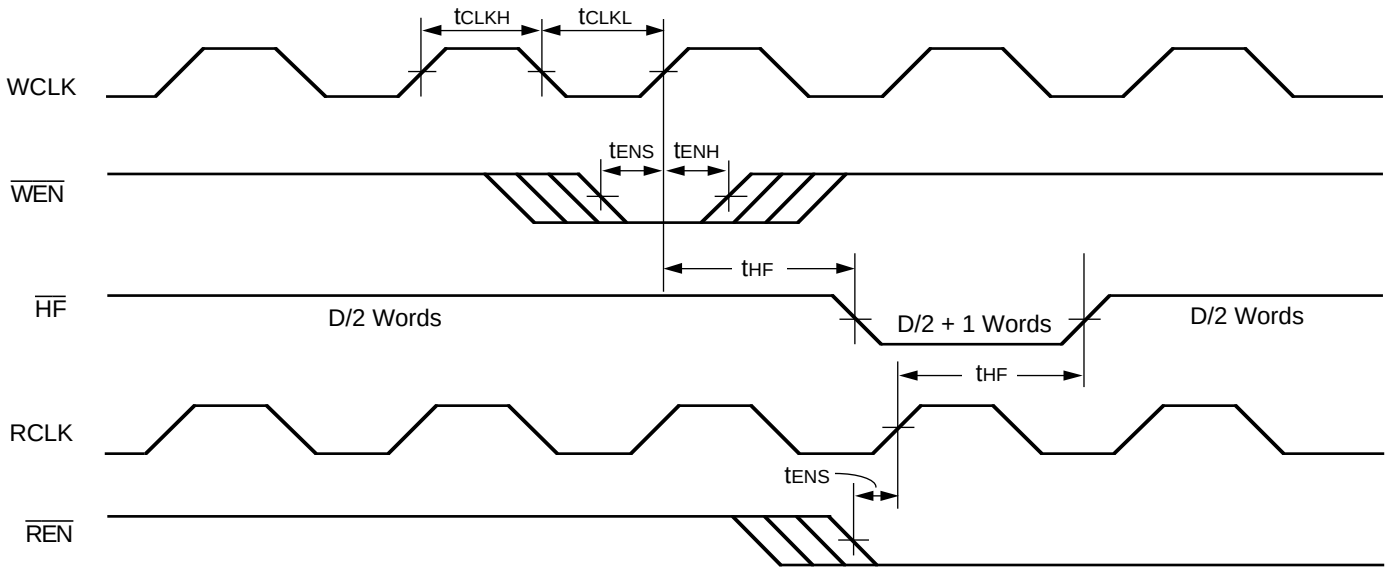
NOTES:
1. $\overline{PAE}$ offset = n
2. Data in the output register does not count as a "word in FIFO memory". Since, in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to go HIGH (after one RCLK cycle plus t_{PAE}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.

Figure 14. Programmable Almost Empty Flag Timing (IDT Standard and FWFT modes)



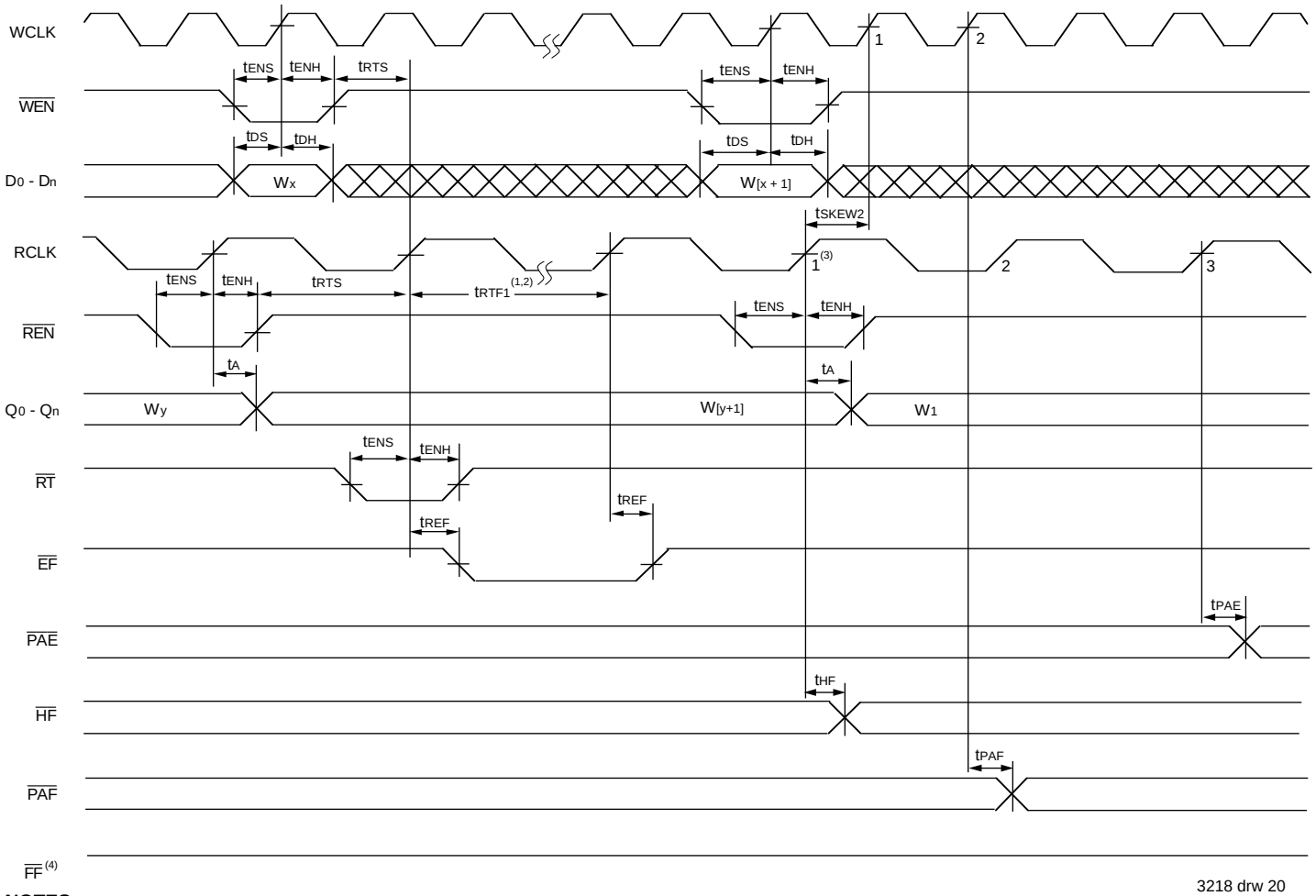
NOTES:
1. $\overline{PAF}$ offset = m; maximum FIFO depth = D = 8,192 for IDT 72264 with MAC = GND; D = 16,384 for IDT 72274 with MAC = GND; D = 16,384 for IDT 72264 with MAC = Vcc; D = 32,768 for IDT 72274 with MAC = Vcc.
2. Data in the output register does not count as a "word in FIFO memory". Since, in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to go HIGH (after one WCLK cycle plus t_{PAF}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}$ deassertion time may be delayed an extra WCLK cycle.

Figure 15. Programmable Almost Full Flag Timing (IDT Standard and FWFT modes)



NOTE:
1. D = 8,192 for IDT 72264 with MAC = GND; D = 16,384 for IDT 72274 with MAC = GND; D = 16,384 for IDT 72264 with MAC = Vcc; D = 32,768 for IDT 72274 with MAC = Vcc.

Figure 16. Half - Full Flag Timing (IDT Standard and FWFT modes)

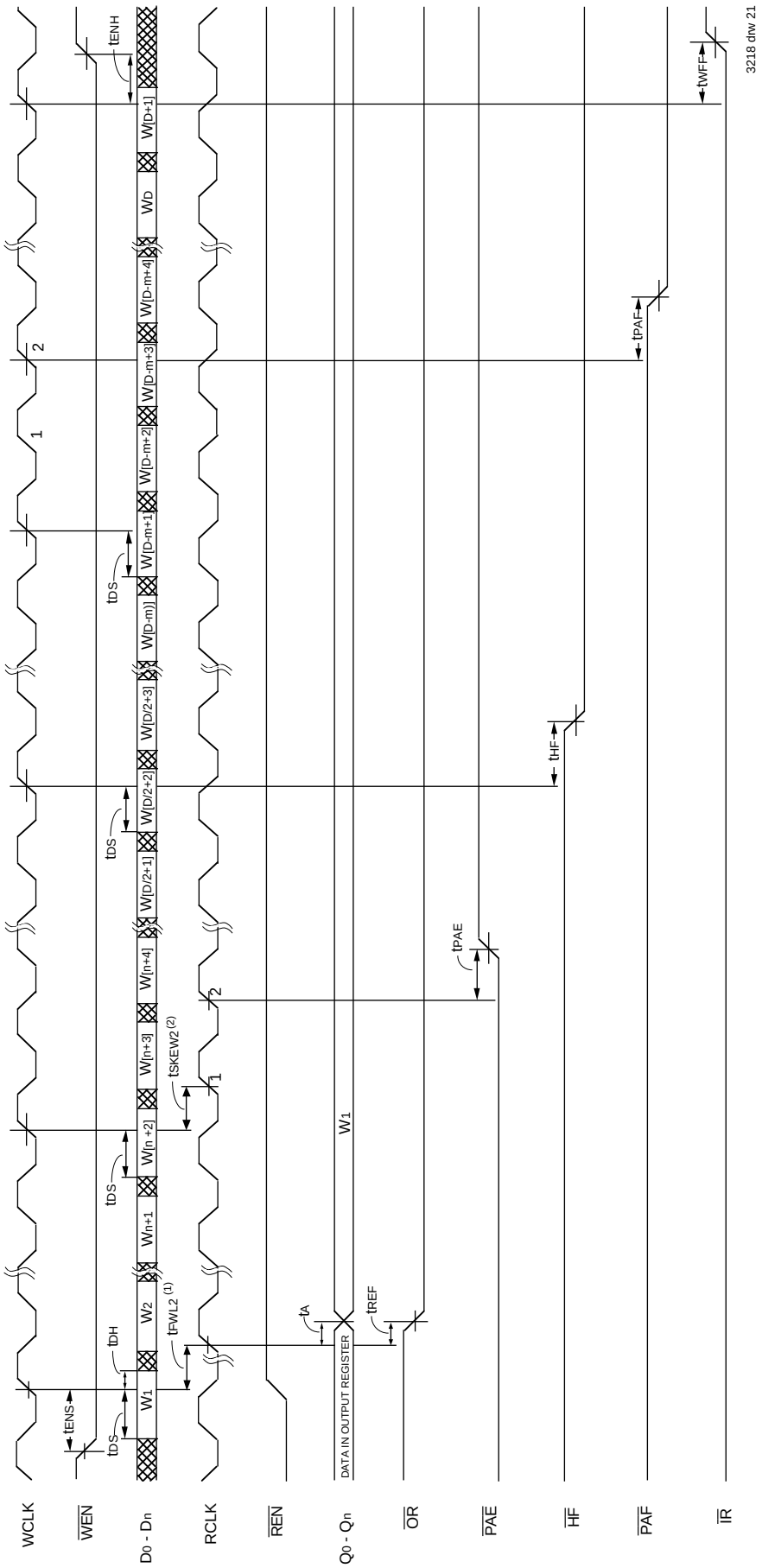


3218 drw 20

NOTES:

1. t_{RTF1} contributes a variable delay to the overall retransmit recovery time:
   t_{RFTF1} max = 14*T_f + 3*T_{RCLK} (in ns)
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.
2. Retransmit set up is complete after $\overline{EF}$ returns HIGH, only then can a read operation begin. Write operations are permitted after one of two conditions have been met: $\overline{EF}$ is HIGH or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.
3. Following Retransmit Setup, the rising edge of RCLK that accesses the first memory location also initiates the updating of $\overline{HF}$, $\overline{PAE}$, and $\overline{PAF}$.
4. No more than D-2 words should have been written to the FIFO between Reset (Master or Partial) and Retransmit Setup. Therefore, $\overline{FF}$ will be HIGH throughout the Restransmit Setup procedure. (D = 8,192 for IDT 72264 with MAC = GND; D = 16,384 for IDT 72274 with MAC = GND; D = 16,384 for IDT 72264 with MAC = Vcc; D = 32,768 for IDT 72274 with MAC = Vcc.)
5. $\overline{OE}$=LOW

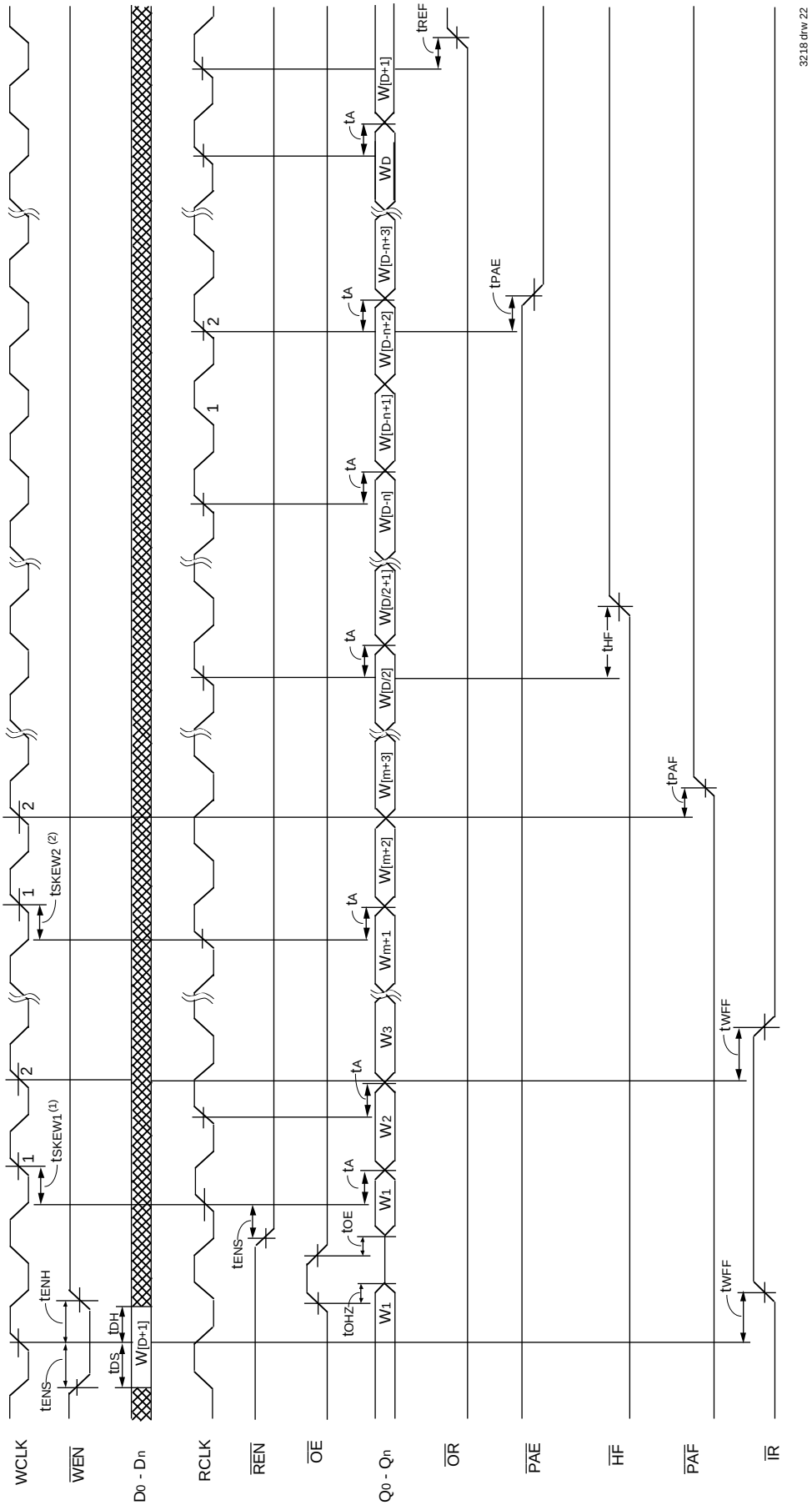
Figure 17. Retransmit Timing (IDT Standard mode)



NOTES:

1. t_{FWL2} max. (in ns) = 10*Tf + 3*T_{RCLK}
   where Tf is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to go HIGH (after one RCLK cycle plus t_{PAE}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
3. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW
4. $\overline{PAE}$ offset = n; $\overline{PAF}$ offset = m; D = 8,192 for IDT 72264 with MAC = GND; D = 16,384 for IDT 72274 with MAC = GND; D = 16,384 for IDT 72264 with MAC = Vcc; D = 32,768 for IDT 72274 with MAC = Vcc.

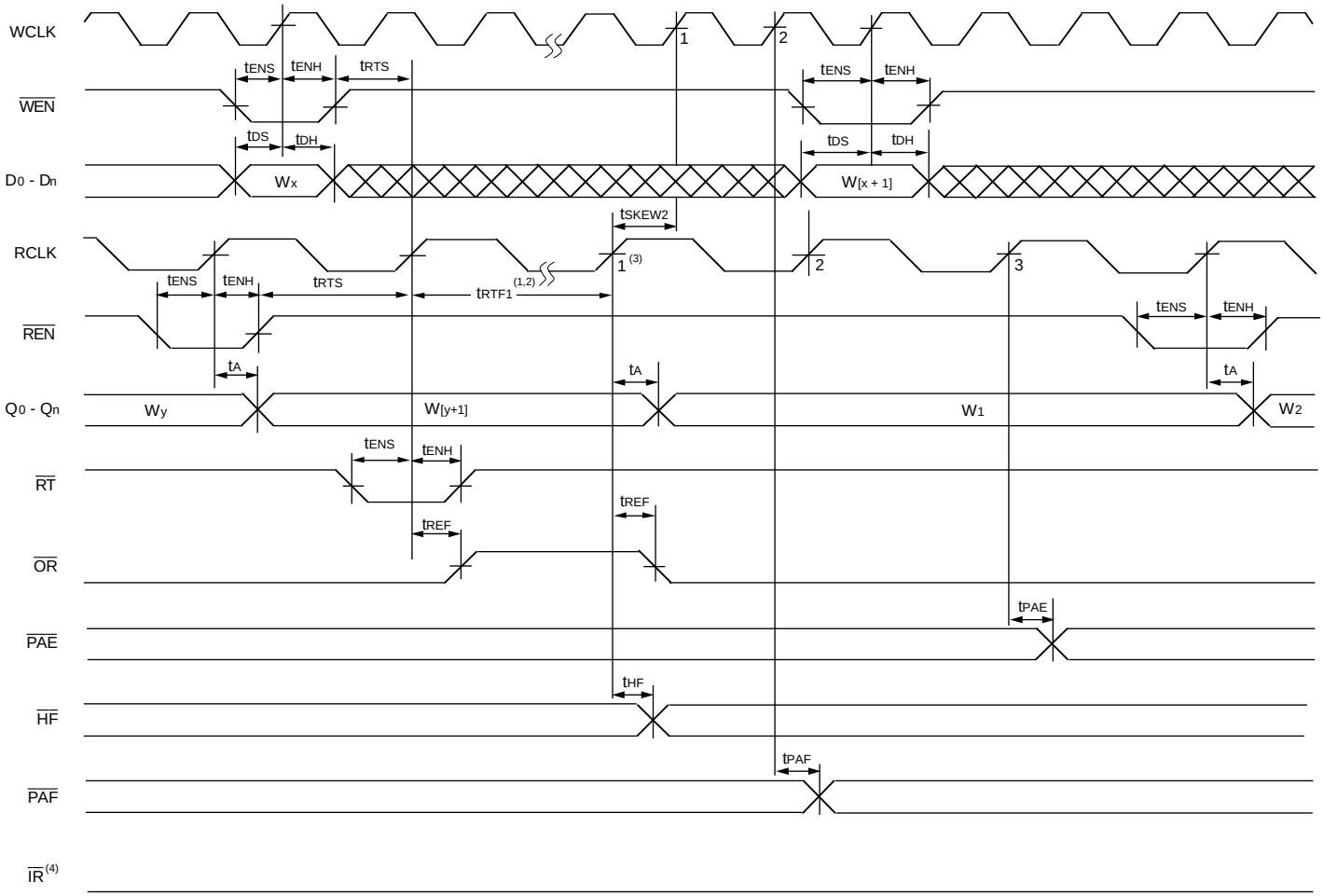
Figure 18. Write Timing (First Word Fall Through Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{IR}$ will go LOW (after one WCLK cycle plus t_{WFF}). If the time between the rising ege of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then the $\overline{IR}$ assertion may be delayed an extra WCLK cycle.
2. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to go HIGH (after one WCLK cycle plus t_{PAF}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}$ deassertion may be delayed an extra WCLK cycle.
3. $\overline{LD}$ = HIGH
4. $\overline{PAE}$ Offset = n; $\overline{PAF}$ offset = m; D = 8,192 for IDT 72264 with MAC = GND; D = 16,384 for IDT 72274 with MAC = Vcc; D = 16,384 for IDT 72264 with MAC = GND; D = 32,768 for IDT 72274 with MAC = Vcc.

Figure 19. Read Timing (First Word Fall Through Mode)



3218 drw 23

NOTES:

1. t_{RTF2} contribute a variable delay to the overall retransmit time:
   t_{RTF2} max = 14*T_f + 4*T_{RCLK} (in ns)
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.
2. Retransmit set up is complete after $\overline{OR}$ returns LOW, only then can a read operation begin. Write operations are permitted after one of two conditions have been met: $\overline{OR}$ is LOW or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.
3. Following Retransmit Setup, the rising edge of RCLK that accesses the first memory location also initiates the updating of $\overline{HF}$, $\overline{PAE}$, and $\overline{PAF}$.
4. No more than D-2 words should have been written to the FIFO between Reset (Master or Partial) and Retransmit Setup. Therefore, $\overline{IR}$ will be LOW throughout the Retransmit Setup procedure. (D = 8,192 for IDT 72264 with MAC = GND; D = 16,384 for IDT 72274 with MAC = GND; D = 16,384 for IDT 72264 with MAC = Vcc; D = 32,768 for IDT 72274 with MAC = Vcc.)
5. $\overline{OE}$=LOW

Figure 20. Retransmit Timing (FWFT mode)

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72264/72274 may be used when the application requires depths up to 8,192/16,384 for an 18-bit data path (MAC = GND) or 16,384/32,768 for a 9-bit data path (MAC = Vcc). The IDT72264/72274 can always be used in Single Device Configuration, whether IDT Standard Mode or FWFT Mode has been selected. No special set up procedure is necessary.

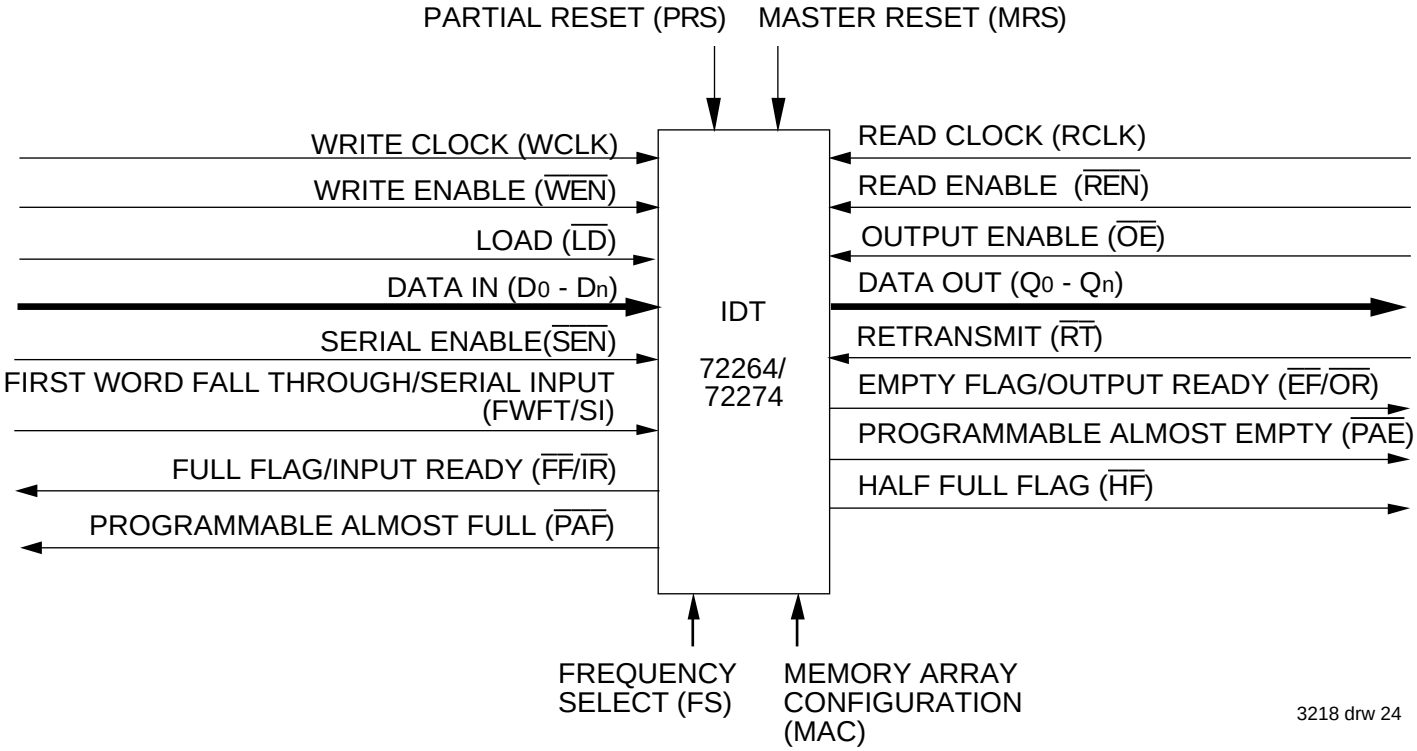
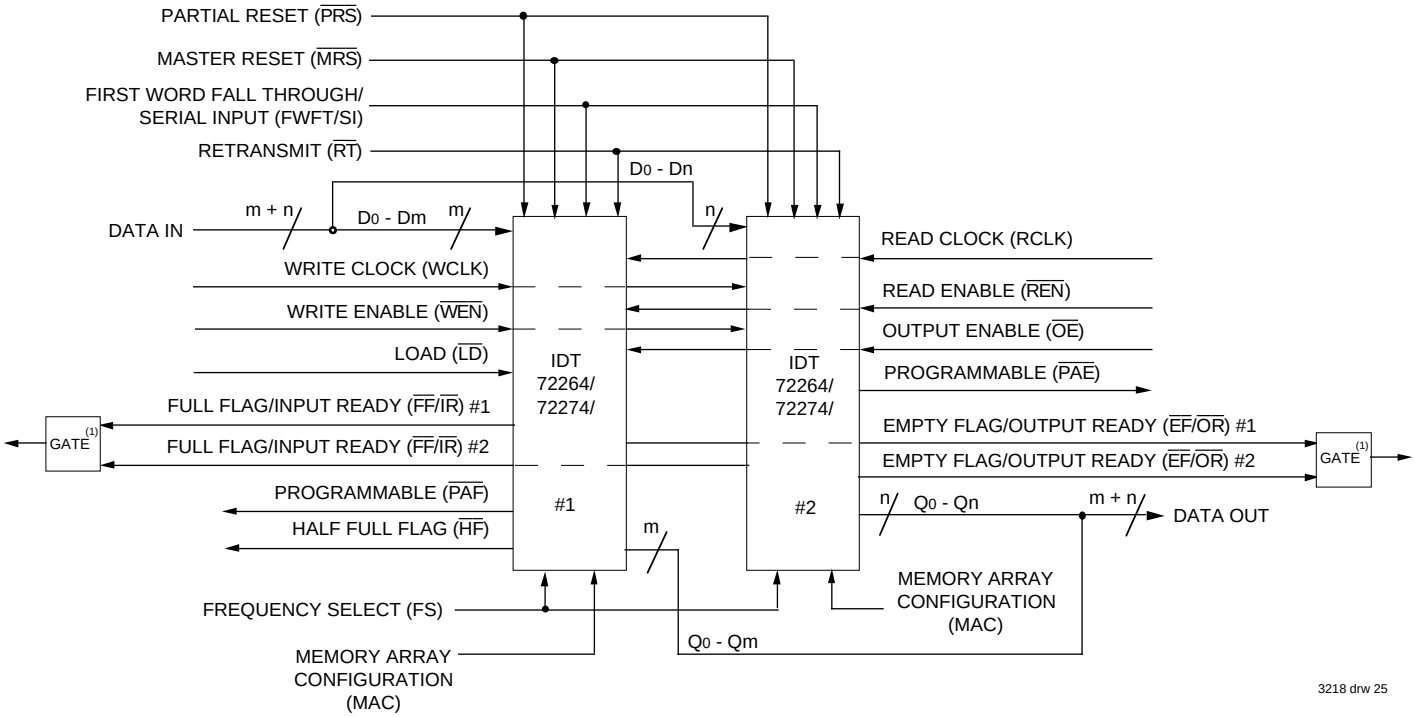


Figure 21. Block Diagram of IDT72264/74 FIFO in single device configuration: 8,192 x 18 or 16,384 x 18 if MAC = GND; 16,384 x 9 or 32,678 x 9 if MAC = Vcc

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the $\overline{EF}$ and $\overline{FF}$ functions in IDT Standard mode and the $\overline{IR}$ and $\overline{OR}$ functions in FWFT mode. Because of variations in skew between RCLK and WCLK, it is possible for $\overline{EF}$/$\overline{FF}$ deassertion and $\overline{IR}$/$\overline{OR}$ assertion to vary by one cycle between FIFOs. In IDT Standard mode, such problems can be avoided by creating composite flags, that is, ANDing $\overline{EF}$ of every FIFO, and separately ANDing $\overline{FF}$ of every FIFO. In FWFT mode, composite flags can be created by ORing $\overline{OR}$ of every FIFO, and separately ORing $\overline{IR}$ of every FIFO.

Figure 22 demonstrates a width expansion using two IDT72264/72274s. If MAC = GND for both FIFOs, then D_0 - D_{17} from each device, taken together, form a 36-bit wide input bus and Q_0 - Q_{17} from each device, taken together, form a 36-bit wide output bus. If MAC = Vcc for both FIFOs, then D_0 - D_8 from each device, taken together, form an 18-bit wide input bus and Q_0 - Q_8 from each device, taken together, form an 18-bit wide output bus. (In this case, both FIFOs' D_9 - D_{17} and Q_9 - Q_{17} do not function.) Any word width can be attained by adding additional IDT72264/72274s.



NOTE:
1. Use an AND gate in IDT Standard mode, an OR gate in FWFT mode.
2. Do not connect any output control signals directly together.

Figure 22. Block Diagram of IDT72264/74 Width Expansion: 8,192 x 36 or 16,384 x 36 if MAC = GND; 16,384 x 18 or 32,768 x 18 if MAC = Vcc

DEPTH EXPANSION CONFIGURATION

The IDT72264/72274 can easily be adapted to applications requiring depths greater than 8,192/16,384 with an18- bit bus width (MAC = GND) or 16,384/32,768 words with a 9-bit bus width (MAC = Vcc). In FWFT mode, the FIFOs can be connected in series (the data outputs of one FIFO connected to the data inputs of the next)–no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. Figure 23 shows a depth expansion using two IDT72264/ 72274s.

Care should be taken to select FWFT mode during Master Reset for all FIFOs in the depth expansion configuration. The first word written to an empty configuration will pass from one FIFO to the next ("ripple down") until it finally appears at the outputs of the last FIFO in the chain–no read operation is necessary. Each time the data word appears at the outputs of one FIFO, that device's OR line goes LOW, enabling a write to the next FIFO in line.

The OR assertion time is variable and is described with the help of the t_{FWL2} parameter, which includes including delay caused by clock skew:

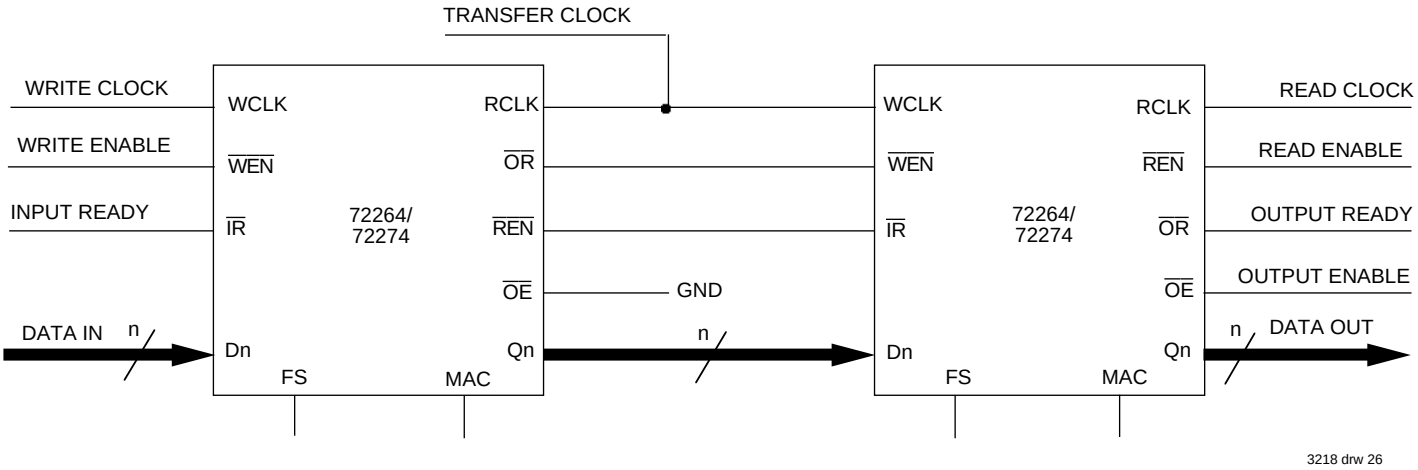


Figure 23. Block Diagram of IDT72264/74 Depth Expansion: 16,384 x 18 or 32,768 x 18 if MAC = GND; 32,768 x 9, 65,536 x 9 if MAC = Vcc

$$t_{FWL2}\ \text{max.} = 10*T_f + 3*T_{RCLK}$$

where T_{RCLK} is the RCLK period and T_f is either the RCLK or the WCLK period, whichever is shorter.

The maximum amount of time it takes for a word to pass from the inputs of the first FIFO to the outputs of the last FIFO in the chain is the sum of the delays for each individual FIFO:

$$t_{FWL2(1)} + t_{FWL2(2)} + \ldots + t_{FWL2(N)} + N*T_{RCLK}$$

where N is the number of FIFOs in the expansion.

Note that the additional RCLK term accounts for the time it takes to pass data between FIFOs.

The ripple down delay is only noticeable for the first word written to an empty depth expansion configuration. There will be no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full depth expansion configuration will "bubble up" from the last FIFO to the previous one until it finally moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's $\overline{IR}$ line goes LOW, enabling the preceding FIFO to write a word to fill it.

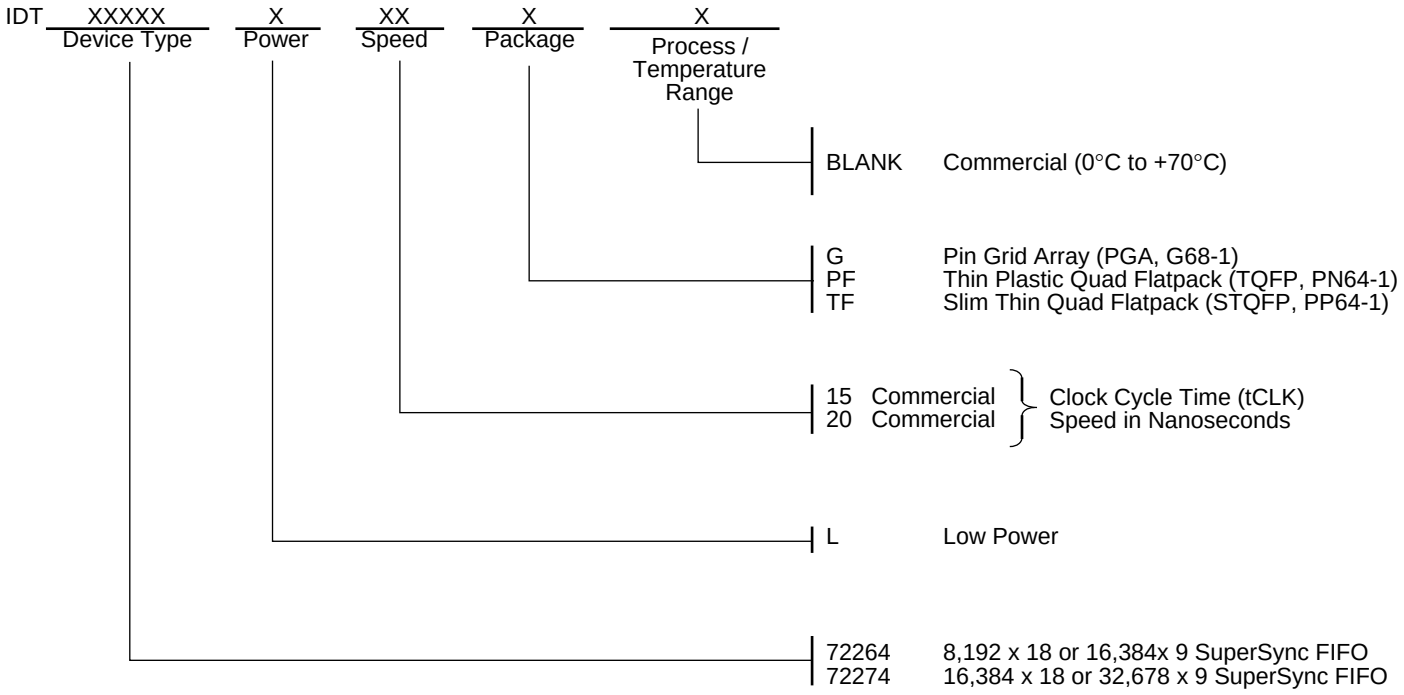
The amount of time it takes for $\overline{IR}$ of the first FIFO in the chain to assert after a word is read from the last FIFO is the sum of the delays for each individual FIFO:

$$N*(3*T_{WCLK})$$

where N is the number of FIFOs in the expansion and T_{WCLK} is the WCLK period. Note that one of the three WCLK cycle accounts for T_{SKEW1} delays.

In a SuperSync depth expansion, set FS individually for each FIFO in the chain. The Transfer Clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in moving, as quickly as possible, data to the end of the chain and free locations to the beginning of the chain.

ORDERING INFORMATION



3218 drw 27

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9