

DMT3020LDV

DUAL 30V N-CHANNEL ENHANCEMENT MODE MOSFET PowerDI3333-8 (Type UXC)

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _C = +25°C		
00)/	$20m\Omega$ @ $V_{GS} = 10V$	32A		
30V	$32m\Omega @ V_{GS} = 4.5V$	25A		

Features

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

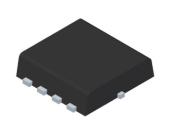
Applications

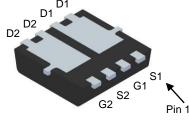
- Power Management Functions
- Analog Switch

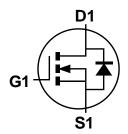
Mechanical Data

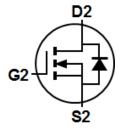
- Case: PowerDI[®]3333-8 (Type UXC)
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe.
 Solderable per MIL-STD-202, Method 208 (2)
- Weight: 0.072 grams (Approximate)

PowerDI3333-8 (Type UXC)









Top View

Bottom View

Equivalent Circuit

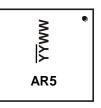
Ordering Information (Note 4)

Part Number	Case	Packaging
DMT3020LDV-7	PowerDI3333-8 (Type UXC)	2,000/Tape & Reel
DMT3020LDV-13	PowerDI3333-8 (Type UXC)	3,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



AR5 = Product Type Marking Code

YYWW = Date Code Marking

YY = Last Two Digits of Year (ex: 18 for 2018)

WW = Week Code (01 to 53)



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current, $V_{GS} = 10V$ (Note 7) Steady State $T_C = +25^{\circ}C$ $T_C = +70^{\circ}C$			I _D	32 25	А
Maximum Body Diode Forward Current (Note 7)	I _S	25	Α		
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)	I _{DM}	50	Α		
Pulsed Drain Body Diode Forward Current (10µs Pul	I _{SM}	50	Α		
Avalanche Current (L = 0.1mH) (Note 8)			I _{AS}	13	Α
Avalanche Energy (L = 0.1mH) (Note 8)			E _{AS}	8.5	mJ

Thermal Characteristics ($@T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	
Total Power Dissipation (Note 5)	P_{D}	0.9	W	
Thermal Resistance, Junction to Ambient (Note 5) Steady State		$R_{ heta JA}$	138	°C/W
Total Power Dissipation (Note 6)		P _D	1.9	W
Thermal Resistance, Junction to Ambient (Note 6) Steady State		$R_{ heta JA}$	67	°C/W
Thermal Resistance, Junction to Case (Note 7)		$R_{ heta JC}$	4.8	C/VV
Operating and Storage Temperature Range		$T_{J_i}T_{STG}$	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 9)							
Drain-Source Breakdown Voltage	BV _{DSS}	30.0	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	_	_	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 9)							
Gate Threshold Voltage	V _{GS(TH)}	1.0	_	2.5	٧	$V_{DS} = V_{GS}, I_D = 250 \mu A$	
Static Drain-Source On-Resistance	0		14	20	mΩ	$V_{GS} = 10V, I_D = 9.0A$	
Static Diain-Source On-Resistance	R _{DS(ON)}	_	22	32	mΩ	$V_{GS} = 4.5V, I_D = 7.0A$	
Diode Forward Voltage	V_{SD}	_	8.0	1.2	V	$V_{GS} = 0V, I_{S} = 2A$	
DYNAMIC CHARACTERISTICS (Note 10)							
Input Capacitance	C _{iss}	l	393	_	pF	151/1/ 01/	
Output Capacitance	Coss	-	173	_	pF	$V_{DS} = 15V, V_{GS} = 0V,$ - f = 1.0MHz	
Reverse Transfer Capacitance	C _{rss}	_	27	_	pF	7 = 1.0WH IZ	
Gate Resistance	Rg	_	1.1	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	
Total Gate Charge (V _{GS} = 10V)	Qg	_	7.0	_	nC		
Total Gate Charge (V _{GS} = 4.5V)	Qg	_	3.6	_	nC	\\\\ 45\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	
Gate-Source Charge	Q _{gs}	_	0.9	_	nC	$V_{DD} = 15V, I_{D} = 9A$	
Gate-Drain Charge	Q_{gd}	_	1.5	_	nC		
Turn-On Delay Time	t _{D(ON)}	_	1.8	_	ns		
Turn-On Rise Time	t _R	_	1.9	_	ns	$V_{DD} = 15V, V_{GS} = 10V,$ $R_{G} = 6\Omega, I_{D} = 9A$	
Turn-Off Delay Time	t _{D(OFF)}	_	7.5	_	ns		
Turn-Off Fall Time	t _F	_	2.4	_	ns		
Reverse Recovery Time	t _{RR}		10	_	ns	1 00 41/44 4000/	
Reverse Recovery Charge	Q _{RR}		2.6	_	nC	$I_F = 9A$, $dI/dt = 100A/\mu s$	

5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

^{6.} Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).

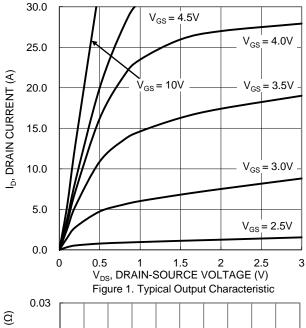
^{8.} I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25$ °C.

^{9.} Short duration pulse test used to minimize self-heating effect.

^{10.} Guaranteed by design. Not subject to product testing.







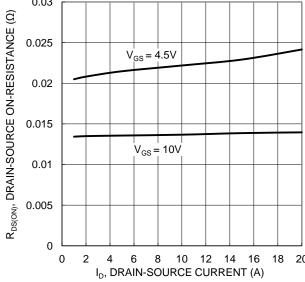


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

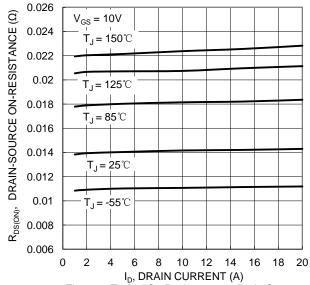
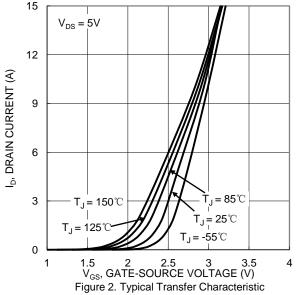
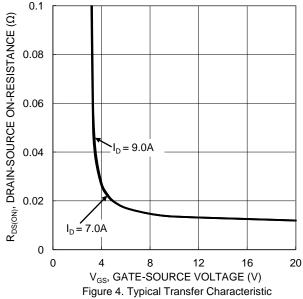


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature





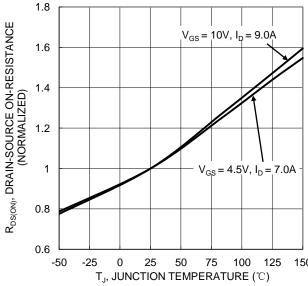


Figure 6. On-Resistance Variation with Junction Temperature





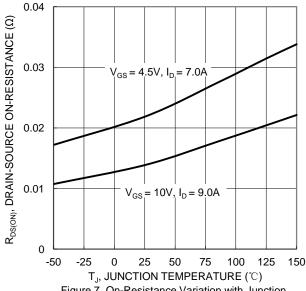
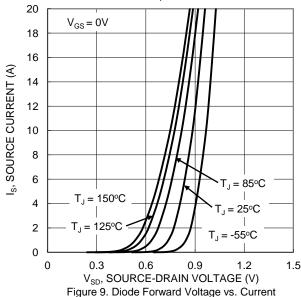
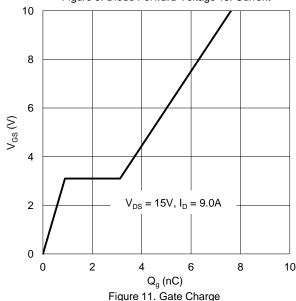


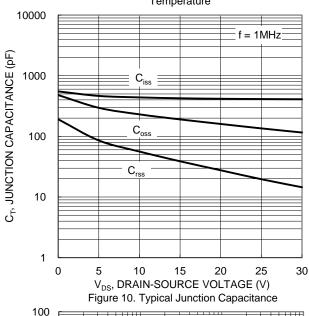
Figure 7. On-Resistance Variation with Junction Temperature





2 $V_{GS(TH)},$ GATE THRESHOLD VOLTAGE (V) 1.8 $I_D = 1 \text{mA}$ 1.6 1.4 I_D= 250μA 1.2 1 8.0 0.6 50 -50 -25 25 75 100 125 150 T_J , JUNCTION TEMPERATURE (°C)

Figure 8. Gate Threshold Variation vs. Junction Temperature



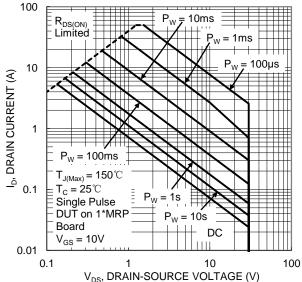


Figure 12. SOA, Safe Operation Area



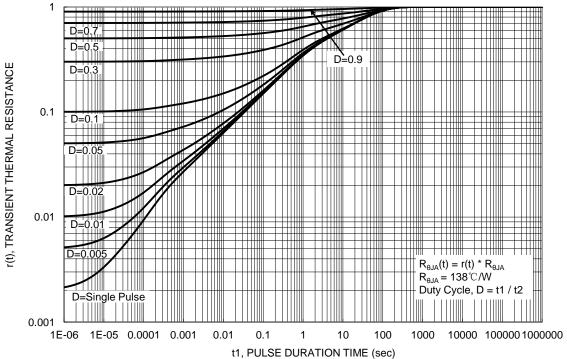


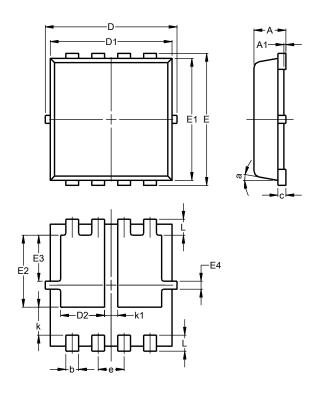
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8 (Type UXC)

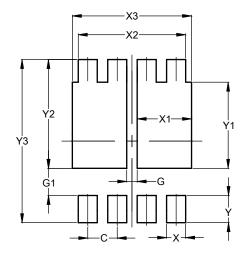


PowerDI3333-8					
(Type UXC)					
Dim	Min	Max	Тур		
Α	0.75	0.85	0.80		
A 1	0.00	0.05			
b	0.25	0.40	0.32		
С	0.10	0.25	0.15		
D	3.20	3.40	3.30		
D1	2.95	3.15	3.05		
D2	0.90	1.30	1.10		
Е	3.20	3.40	3.30		
E1	2.95	3.15	3.05		
E2	1.60	2.00	1.80		
E3	0.95	1.35	1.15		
E4	0.10	0.30	0.20		
е	_	_	0.65		
L	0.30	0.50	0.40		
k	0.50	0.90	0.70		
k1	0.13	0.53	0.33		
а	0°	12°	10°		
All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI3333-8 (Type UXC)



Dimensions	Value (in mm)		
С	0.650		
G	0.230		
G1	0.600		
Х	0.420		
X1	1.200		
X2	2.370		
Х3	2.630		
Υ	0.600		
Y1	1.900		
Y2	2.400		
Y3	3.600		

May 2018

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