

AD565A/AD566A

FEATURES

- Single Chip Construction**
- Very High Speed Settling to 1/2 LSB**
 - AD565A: 250 ns max
 - AD566A: 350 ns max
- Full-Scale Switching Time: 30 ns**
- Guaranteed for Operation with ± 12 V (565A) Supplies, with -12 V Supply (AD566A)**
- Linearity Guaranteed Overtemperature**
1/2 LSB max (K, T Grades)
- Monotonicity Guaranteed Overtemperature**
- Low Power: AD566A = 180 mW max;**
AD565A = 225 mW max
- Use with On-Board High Stability Reference (AD565A) or with External Reference (AD566A)**
- Low Cost**
- MIL-STD-883-Compliant Versions Available**

PRODUCT DESCRIPTION

The AD565A and AD566A are fast 12-bit digital-to-analog converters that incorporate the latest advances in analog circuit design to achieve high speeds at low cost.

The AD565A and AD566A use 12 precision, high speed bipolar current-steering switches, a control amplifier, and a laser-trimmed thin-film resistor network to produce a very fast, high accuracy analog output current. The AD565A also includes a buried Zener reference that features low noise, long-term stability, and temperature drift characteristics comparable to the best discrete reference diodes.

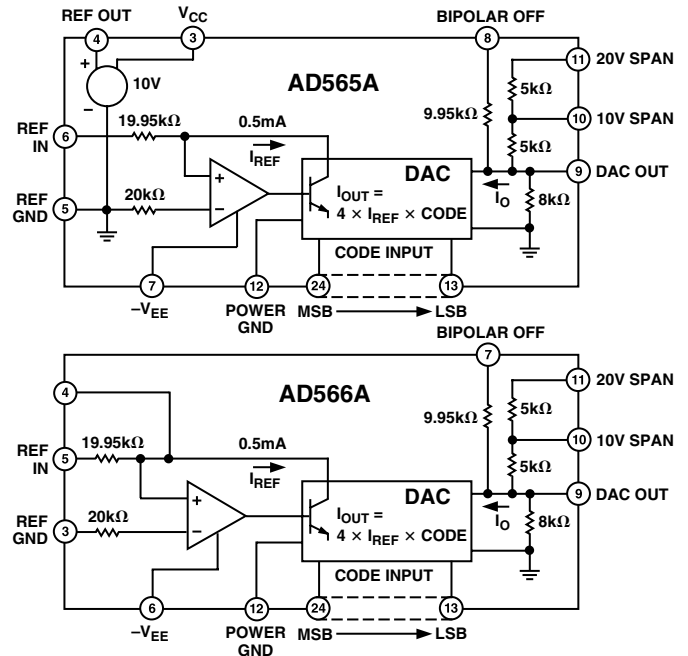
The combination of performance and flexibility in the AD565A and AD566A has resulted from major innovations in circuit design, an important new high speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD565A and AD566A have a 10%–90% full-scale transition time less than 35 ns and settle to within $\pm 1/2$ LSB in 250 ns max (350 ns for AD566A). Both are laser-trimmed at the wafer level to $\pm 1/8$ LSB typical linearity and are specified to $\pm 1/4$ LSB max error (K and T grades) at $+25^\circ\text{C}$. High speed and accuracy make the AD565A and AD566A the ideal choice for high speed display drivers as well as for fast analog-to-digital converters.

The laser trimming process that provides the excellent linearity is also used to trim both the absolute value and the temperature coefficient of the reference of the AD565A, resulting in a typical full-scale gain TC of 10 ppm/ $^\circ\text{C}$. When tighter TC performance is required or when a system reference is available, the AD566A may be used with an external reference.

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FUNCTIONAL BLOCK DIAGRAMS



AD565A and AD566A are available in four performance grades. The J and K grades are specified for use over the 0°C to $+70^\circ\text{C}$ temperature range while the S and T grades are specified for the -55°C to $+125^\circ\text{C}$ range. The D grades are all packaged in a 24-lead, hermetically sealed, ceramic, dual-in-line package. The JR grade is packaged in a 28-lead plastic SOIC.

PRODUCT HIGHLIGHTS

1. The wide output compliance range of the AD565A and AD566A are ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The devices incorporate a newly developed, fully differential, nonsaturating precision current switching cell structure that combines the dc accuracy and stability first developed in the AD562/AD563 with very fast switching times and an optimally damped settling characteristic.
3. The devices also contain SiCr thin-film application resistors that can be used with an external op amp to provide a precision voltage output or as input resistors for a successive-approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full-scale and bipolar offset errors.
4. The AD565A and AD566A are available in versions compliant with MIL-STD-883. Refer to the Analog Devices *Military Products Databook* or current /883B data sheet for detailed specifications.

AD565A—SPECIFICATIONS (T_A = 25°C, V_{CC} = 15 V, V_{EE} = 15 V, unless otherwise noted.)

| Parameter | AD565AJ | | | AD565AK | | | Unit |
|---|---------|---|-----------------|---------|---|-------------------|------------------------|
| | Min | Typ | Max | Min | Typ | Max | |
| DATA INPUTS¹ (Pins 13 to 24) | | | | | | | |
| TTL or 5 V CMOS | | | | | | | |
| Input Voltage | | | | | | | |
| Bit ON Logic "1" | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Bit OFF Logic "0" | | | 0.8 | | | 0.8 | V |
| Logic Current (Each Bit) | | | | | | | |
| Bit ON Logic "1" | | 120 | 300 | | 120 | 300 | μA |
| Bit OFF Logic "0" | | 35 | 100 | | 35 | 100 | μA |
| RESOLUTION | | | 12 | | | 12 | Bits |
| OUTPUT | | | | | | | |
| Current | | | | | | | |
| Unipolar (All Bits On) | -1.6 | -2.0 | -2.4 | -1.6 | -2.0 | -2.4 | mA |
| Bipolar (All Bits On or Off) | ±0.8 | ±1.0 | ±1.2 | ±0.8 | ±1.0 | ±1.2 | mA |
| Resistance (Exclusive of Span Resistors) | 6 | 8 | 10 | 6 | 8 | 10 | kΩ |
| Offset | | | | | | | |
| Unipolar | | 0.01 | 0.05 | | 0.01 | 0.05 | % of F.S. Range |
| Bipolar (Figure 3, R2 = 50 Ω Fixed) | | 0.05 | 0.15 | | 0.05 | 0.1 | % of F.S. Range |
| Capacitance | | 25 | | | 25 | | pF |
| Compliance Voltage | | | | | | | |
| T _{MIN} to T _{MAX} | -1.5 | | +10 | -1.5 | | +10 | V |
| ACCURACY (Error Relative to Full Scale) 25°C | | ±1/4 (0.006) | ±1/2 (0.012) | | ±1/8 (0.003) | ±0.35 (0.0084) | LSB % of F.S. Range |
| T _{MIN} to T _{MAX} | | ±1/2 (0.012) | ±3/4 (0.018) | | ±1/4 (0.006) | ±1/2 (0.012) | LSB % of F.S. Range |
| DIFFERENTIAL NONLINEARITY 25°C | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | LSB |
| T _{MIN} to T _{MAX} | | MONOTONICITY GUARANTEED | | | MONOTONICITY GUARANTEED | | |
| TEMPERATURE COEFFICIENTS With Internal Reference | | | | | | | |
| Unipolar Zero | | 1 | 2 | | 1 | 2 | ppm/°C |
| Bipolar Zero | | 5 | 10 | | 5 | 10 | ppm/°C |
| Gain (Full Scale) | | 15 | 50 | | 10 | 20 | ppm/°C |
| Differential Nonlinearity | | 2 | | | 2 | | ppm/°C |
| SETTLING TIME TO 1/2 LSB All Bits ON-to-OFF or OFF-to-ON | | 250 | 400 | | 250 | 400 | ns |
| FULL-SCALE TRANSITION | | | | | | | |
| 10% to 90% Delay plus Rise Time | | 15 | 30 | | 15 | 30 | ns |
| 90% to 10% Delay plus Fall Time | | 30 | 50 | | 30 | 50 | ns |
| TEMPERATURE RANGE | | | | | | | |
| Operating | 0 | | +70 | 0 | | +70 | °C |
| Storage | -65 | | +150 | -65 | | +150 | °C |
| POWER REQUIREMENTS | | | | | | | |
| V _{CC} , +11.4 to +16.5 V dc | | 3 | 5 | | 3 | 5 | mA |
| V _{EE} , -11.4 to -16.5 V dc | | -12 | -18 | | -12 | -18 | mA |
| POWER SUPPLY GAIN SENSITIVITY ² | | | | | | | |
| V _{CC} = +11.4 to +16.5 V dc | | 3 | 10 | | 3 | 10 | ppm of F.S./% |
| V _{EE} = -11.4 to -16.5 V dc | | 15 | 25 | | 15 | 25 | ppm of F.S./% |
| PROGRAMMABLE OUTPUT RANGES (See Figures 2, 3, 4) | | 0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10 | | | 0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10 | | V V V V V |
| EXTERNAL ADJUSTMENTS | | | | | | | |
| Gain Error with Fixed 50 Ω Resistor for R2 (Figure 2) | | ±0.1 | ±0.25 | | ±0.1 | ±0.25 | % of F.S. Range |
| Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 3) | | ±0.05 | ±0.15 | | ±0.05 | ±0.1 | % of F.S. Range |
| Gain Adjustment Range (Figure 2) | ±0.25 | | | ±0.25 | | | % of F.S. Range |
| Bipolar Zero Adjustment Range | ±0.15 | | | ±0.15 | | | % of F.S. Range |
| REFERENCE INPUT | | | | | | | |
| Input Impedance | 15 | 20 | 25 | 15 | 20 | 25 | kΩ |
| REFERENCE OUTPUT | | | | | | | |
| Voltage | 9.90 | 10.00 | 10.10 | 9.90 | 10.00 | 10.10 | V |
| Current (Available for External Loads) ³ | 1.5 | 2.5 | | 1.5 | 2.5 | | mA |
| POWER DISSIPATION | | 225 | 345 | | 225 | 345 | mW |

NOTES

¹The digital inputs are guaranteed but not tested over the operating temperature range.

²The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15 V dc.

³For operation at elevated temperatures, the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied.

Specifications subject to change without notice.

AD565A/AD566A

| Parameter | AD565AS | | | AD565AT | | | Unit |
|---|-------------|--------------------------------|-------------------------------|-------------|--------------------------------|---------------------------------|------------------------|
| | Min | Typ | Max | Min | Typ | Max | |
| DATA INPUTS ¹ (Pins 13 to 24) | | | | | | | |
| TTL or 5 V CMOS | | | | | | | |
| Input Voltage | | | | | | | |
| Bit ON Logic "1" | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Bit OFF Logic "0" | | | 0.8 | | | 0.8 | V |
| Logic Current (Each Bit) | | | | | | | |
| Bit ON Logic "1" | | 120 | 300 | | 120 | 300 | μA |
| Bit OFF Logic "0" | | 35 | 100 | | 35 | 100 | μA |
| RESOLUTION | | | 12 | | | 12 | Bits |
| OUTPUT | | | | | | | |
| Current | | | | | | | |
| Unipolar (All Bits On) | -1.6 | -2.0 | -2.4 | -1.6 | -2.0 | -2.4 | mA |
| Bipolar (All Bits On or Off) | ±0.8 | ±1.0 | ±1.2 | ±0.8 | ±1.0 | ±1.2 | mA |
| Resistance (Exclusive of Span Resistors) | 6 | 8 | 10 | 6 | 8 | 10 | kΩ |
| Offset | | | | | | | |
| Unipolar | | 0.01 | 0.05 | | 0.01 | 0.05 | % of F.S. Range |
| Bipolar (Figure 3, R2 = 50 Ω Fixed) | | 0.05 | 0.15 | | 0.05 | 0.1 | % of F.S. Range |
| Capacitance | | 25 | | | 25 | | pF |
| Compliance Voltage | | | | | | | |
| T _{MIN} to T _{MAX} | -1.5 | | +10 | -1.5 | | +10 | V |
| ACCURACY (Error Relative to Full Scale) 25°C | | ±1/4 (0.006) | ±1/2 (0.012) | | ±1/8 (0.003) | ±0.35 (0.0084) | LSB % of F.S. Range |
| T _{MIN} to T _{MAX} | | ±1/2 (0.012) | ±3/4 (0.018) | | ±1/4 (0.006) | ±1/2 (0.012) | LSB % of F.S. Range |
| DIFFERENTIAL NONLINEARITY 25°C | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | LSB |
| T _{MIN} to T _{MAX} | | MONOTONICITY GUARANTEED | | | MONOTONICITY GUARANTEED | | |
| TEMPERATURE COEFFICIENTS | | | | | | | |
| With Internal Reference | | | | | | | |
| Unipolar Zero | | 1 | 2 | | 1 | 2 | ppm/°C |
| Bipolar Zero | | 5 | 10 | | 5 | 10 | ppm/°C |
| Gain (Full Scale) | | 15 | 30 | | 10 | 15 | ppm/°C |
| Differential Nonlinearity | | 2 | | | 2 | | ppm/°C |
| SETTLING TIME TO 1/2 LSB | | | | | | | |
| All Bits ON-to-OFF or OFF-to-ON | | 250 | 400 | | 250 | 400 | ns |
| FULL-SCALE TRANSITION | | | | | | | |
| 10% to 90% Delay plus Rise Time | | 15 | 30 | | 15 | 30 | ns |
| 90% to 10% Delay plus Fall Time | | 30 | 50 | | 30 | 50 | ns |
| TEMPERATURE RANGE | | | | | | | |
| Operating | -55 | | +125 | -55 | | +125 | °C |
| Storage | -65 | | +150 | -65 | | +150 | °C |
| POWER REQUIREMENTS | | | | | | | |
| V _{CC} , +11.4 to +16.5 V dc | | 3 | 5 | | 3 | 5 | mA |
| V _{EE} , -11.4 to -16.5 V dc | | -12 | -18 | | -12 | -18 | mA |
| POWER SUPPLY GAIN SENSITIVITY ² | | | | | | | |
| V _{CC} = +11.4 to +16.5 V dc | | 3 | 10 | | 3 | 10 | ppm of F.S./% |
| V _{EE} = -11.4 to -16.5 V dc | | 15 | 25 | | 15 | 25 | ppm of F.S./% |
| PROGRAMMABLE OUTPUT RANGES | | | | | | | |
| (See Figures 2, 3, 4) | | 0 to +5 | | | 0 to +5 | | V |
| | | -2.5 to +2.5 | | | -2.5 to +2.5 | | V |
| | | 0 to +10 | | | 0 to +10 | | V |
| | | -5 to +5 | | | -5 to +5 | | V |
| | | -10 to +10 | | | -10 to +10 | | V |
| EXTERNAL ADJUSTMENTS | | | | | | | |
| Gain Error with Fixed 50 Ω Resistor for R2 (Figure 2) | | ±0.1 | ±0.25 | | ±0.1 | ±0.25 | % of F.S. Range |
| Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 3) | | ±0.05 | ±0.15 | | ±0.05 | ±0.1 | % of F.S. Range |
| Gain Adjustment Range (Figure 2) | ±0.25 | | | ±0.25 | | | % of F.S. Range |
| Bipolar Zero Adjustment Range | ±0.15 | | | ±0.15 | | | % of F.S. Range |
| REFERENCE INPUT | | | | | | | |
| Input Impedance | 15 | 20 | 25 | 15 | 20 | 25 | kΩ |
| REFERENCE OUTPUT | | | | | | | |
| Voltage | 9.90 | 10.00 | 10.10 | 9.90 | 10.00 | 10.10 | V |
| Current (Available for External Loads) ³ | 1.5 | 2.5 | | 1.5 | 2.5 | | mA |
| POWER DISSIPATION | | 225 | 345 | | 225 | 345 | mW |

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specification subject to change without notice.

AD566A—SPECIFICATIONS (T_A = 25°C, V_{EE} = -15 V, unless otherwise noted)

| Parameter | AD566AJ | | | AD566AK | | | Unit |
|---|---------|--|-----------------|---------|---|-------------------|------------------------|
| | Min | Typ | Max | Min | Typ | Max | |
| DATA INPUTS ¹ (Pins 13 to 24) TTL or 5 V CMOS | | | | | | | |
| Input Voltage | | | | | | | |
| Bit ON Logic "1" | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Bit OFF Logic "0" | 0 | | 0.8 | 0 | | 0.8 | V |
| Logic Current (Each Bit) | | | | | | | |
| Bit ON Logic "1" | | 120 | 300 | | 120 | 300 | μA |
| Bit OFF Logic "0" | | 35 | 100 | | 35 | 100 | μA |
| RESOLUTION | | | 12 | | | 12 | Bits |
| OUTPUT | | | | | | | |
| Current | | | | | | | |
| Unipolar (All Bits On) | -1.6 | -2.0 | -2.4 | -1.6 | -2.0 | -2.4 | mA |
| Bipolar (All Bits On or Off) | ±0.8 | ±1.0 | ±1.2 | ±0.8 | ±1.0 | ±1.2 | mA |
| Resistance (Exclusive of Span Resistors) | 6 | 8 | 10 | 6 | 8 | 10 | kΩ |
| Offset | | | | | | | |
| Unipolar (Adjustable to Zero per Figure 3) | | 0.01 | 0.05 | | 0.01 | 0.05 | % of F.S. Range |
| Bipolar (Figure 4, R1 and R2 = 50 Ω Fixed) | | 0.05 | 0.15 | | 0.05 | 0.1 | % of F.S. Range |
| Capacitance | | 25 | | | 25 | | pF |
| Compliance Voltage T _{MIN} to T _{MAX} | -1.5 | | +10 | -1.5 | | +10 | V |
| ACCURACY (Error Relative to Full Scale) 25°C | | | | | | | |
| T _{MIN} to T _{MAX} | | ±1/4 (0.006) | ±1/2 (0.012) | | ±1/8 (0.003) | ±0.35 (0.0084) | LSB % of F.S. Range |
| | | ±1/2 (0.012) | ±3/4 (0.018) | | ±1/4 (0.006) | ±1/2 (0.012) | LSB % of F.S. Range |
| DIFFERENTIAL NONLINEARITY 25°C T _{MIN} to T _{MAX} | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | LSB |
| | | MONOTONICITY GUARANTEED | | | MONOTONICITY GUARANTEED | | |
| TEMPERATURE COEFFICIENTS | | | | | | | |
| Unipolar Zero | | 1 | 2 | | 1 | 2 | ppm/°C |
| Bipolar Zero | | 5 | 10 | | 5 | 10 | ppm/°C |
| Gain (Full Scale) | | 7 | 10 | | 3 | 5 | ppm/°C |
| Differential Nonlinearity | | 2 | | | 2 | | ppm/°C |
| SETTLING TIME TO 1/2 LSB All Bits ON-to-OFF or OFF-to-ON | | 250 | 350 | | 250 | 350 | ns |
| FULL-SCALE TRANSITION | | | | | | | |
| 10% to 90% Delay plus Rise Time | | 15 | 30 | | 15 | 30 | ns |
| 90% to 10% Delay plus Fall Time | | 30 | 50 | | 30 | 50 | ns |
| POWER REQUIREMENTS | | | | | | | |
| V _{EE} , -11.4 to -16.5 V dc | | -12 | -18 | | -12 | -18 | mA |
| POWER SUPPLY GAIN SENSITIVITY ² V _{EE} = -11.4 to -16.5 V dc | | 15 | 25 | | 15 | 25 | ppm of F.S./% |
| PROGRAMMABLE OUTPUT RANGES (see Figures 3, 4, 5) | | 0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10 | | | 0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10 | | V V V V V |
| EXTERNAL ADJUSTMENTS | | | | | | | |
| Gain Error with Fixed 50 Ω Resistor for R2 (Figure 3) | | ±0.1 | ±0.25 | | ±0.1 | ±0.25 | % of F.S. Range |
| Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 4) | | ±0.05 | ±0.15 | | ±0.05 | ±0.1 | % of F.S. Range |
| Gain Adjustment Range (Figure 3) | ±0.25 | | | ±0.25 | | | % of F.S. Range |
| Bipolar Zero Adjustment Range | ±0.15 | | | ±0.15 | | | % of F.S. Range |
| REFERENCE INPUT | | | | | | | |
| Input Impedance | 15 | 20 | 25 | 15 | 20 | 25 | kΩ |
| POWER DISSIPATION | | 180 | 300 | | 180 | 300 | mW |
| MULTIPLYING MODE PERFORMANCE (All Models) | | Two (2): Bipolar Operation at Digital Input Only 1 V to 10 V, Unipolar 10 Bits (±0.05% of Reduced F.S.) for 1 V dc Reference Voltage | | | | | |
| Quadrants | | | | | | | |
| Reference Voltage | | | | | | | |
| Accuracy | | | | | | | |
| Reference Feedthrough (Unipolar Mode, All Bits OFF, and 1 V to 10 V [p-p], Sine Wave Frequency for 1/2 LSB [p-p] Feedthrough) | | 40 | | | | | kHz typ |
| Output Slew Rate 10%–90% | | 5 | | | | | mA/μs |
| 90%–10% | | 1 | | | | | mA/μs |
| Output Settling Time (All Bits ON and a 0 V–10 V Step Change in Reference Voltage) | | 1.5 μs to 0.01% F.S. | | | | | |
| CONTROL AMPLIFIER | | | | | | | |
| Full Power Bandwidth | | 300 | | | | | kHz |
| Small-Signal Closed-Loop Bandwidth | | 1.8 | | | | | MHz |

NOTES

¹The digital input levels are guaranteed but not tested over the temperature range.

²The power supply gain sensitivity is tested in reference to a V_{EE} of -1.5 V dc.

Specifications subject to change without notice.

AD565A/AD566A

| Parameter | AD566AS | | | AD566AT | | | Unit |
|---|-------------|---|---------------------------------|-------------|--------------------------------|-----------------------------------|------------------------|
| | Min | Typ | Max | Min | Typ | Max | |
| DATA INPUTS ¹ (Pins 13 to 24) TTL or 5 V CMOS | | | | | | | |
| Input Voltage | | | | | | | |
| Bit ON Logic "1" | 2.0 | | 5.5 | 2.0 | | 5.5 | V |
| Bit OFF Logic "0" | 0 | | 0.8 | 0 | | 0.8 | V |
| Logic Current (Each Bit) | | | | | | | |
| Bit ON Logic "1" | | 120 | 300 | | +120 | 300 | μA |
| Bit OFF Logic "0" | | 35 | 100 | | +35 | 100 | μA |
| RESOLUTION | | | 12 | | | 12 | Bits |
| OUTPUT | | | | | | | |
| Current | | | | | | | |
| Unipolar (All Bits On) | -1.6 | -2.0 | -2.4 | -1.6 | -2.0 | -2.4 | mA |
| Bipolar (All Bits On or Off) | ±0.8 | ±1.0 | ±1.2 | ±0.8 | ±1.0 | ±1.2 | mA |
| Resistance (Exclusive of Span Resistors) | 6 | 8 | 10 | 6 | 8 | 10 | kΩ |
| Offset | | | | | | | |
| Unipolar (Adjustable to Zero per Figure 3) | | 0.01 | 0.05 | | 0.01 | 0.05 | % of F.S. Range |
| Bipolar (Figure 4, R1 and R2 = 50 Ω Fixed) | | 0.05 | 0.15 | | 0.05 | 0.1 | % of F.S. Range |
| Capacitance | | 25 | | | 25 | | pF |
| Compliance Voltage | | | | | | | |
| T _{MIN} to T _{MAX} | -1.5 | | +10 | -1.5 | | +10 | V |
| ACCURACY (Error Relative to Full Scale) 25°C | | | | | | | |
| T _{MIN} to T _{MAX} | | ±1/4 (0.006) | ±1/2 (0.012) | | ±1/8 (0.003) | ±0.35 (0.0084) | LSB % of F.S. Range |
| | | ±1/2 (0.012) | ±3/4 (0.018) | | ±1/4 (0.006) | ±1/2 (0.012) | LSB % of F.S. Range |
| DIFFERENTIAL NONLINEARITY 25°C | | | | | | | |
| T _{MIN} to T _{MAX} | | ±1/2 | ±3/4 | | ±1/4 | ±1/2 | LSB |
| | | MONOTONICITY GUARANTEED | | | MONOTONICITY GUARANTEED | | |
| TEMPERATURE COEFFICIENTS | | | | | | | |
| Unipolar Zero | | 1 | 2 | | 1 | 2 | ppm/°C |
| Bipolar Zero | | 5 | 10 | | 5 | 10 | ppm/°C |
| Gain (Full Scale) | | 7 | 10 | | 3 | 5 | ppm/°C |
| Differential Nonlinearity | | 2 | | | 2 | | ppm/°C |
| SETTLING TIME TO 1/2 LSB | | | | | | | |
| All Bits ON-to-OFF or OFF-to-ON | | 250 | 350 | | 250 | 350 | ns |
| FULL-SCALE TRANSITION | | | | | | | |
| 10% to 90% Delay plus Rise Time | | 15 | 30 | | 15 | 30 | ns |
| 90% to 10% Delay plus Fall Time | | 30 | 50 | | 30 | 50 | ns |
| POWER REQUIREMENTS | | | | | | | |
| V _{EE} -11.4 to -16.5 V dc | | -12 | -18 | | -12 | -18 | mA |
| POWER SUPPLY GAIN SENSITIVITY ² | | | | | | | |
| V _{EE} = -11.4 to -16.5 V dc | | 15 | 25 | | 15 | 25 | ppm of F.S./% |
| PROGRAMMABLE OUTPUT RANGES (see Figures 3, 4, 5) | | | | | | | |
| | | 0 to +5 | | | 0 to +5 | | V |
| | | -2.5 to +2.5 | | | -2.5 to +2.5 | | V |
| | | 0 to +10 | | | 0 to +10 | | V |
| | | -5 to +5 | | | -5 to +5 | | V |
| | | -10 to +10 | | | -10 to +10 | | V |
| EXTERNAL ADJUSTMENTS | | | | | | | |
| Gain Error with Fixed 50 Ω Resistor for R2 (Figure 3) | | ±0.1 | ±0.25 | | ±0.1 | ±0.25 | % of F.S. Range |
| Bipolar Zero Error with Fixed 50 Ω Resistor for R1 (Figure 4) | | ±0.05 | ±0.15 | | ±0.05 | ±0.1 | % of F.S. Range |
| Gain Adjustment Range (Figure 3) | ±0.25 | | | ±0.25 | | | % of F.S. Range |
| Bipolar Zero Adjustment Range | ±0.15 | | | ±0.15 | | | % of F.S. Range |
| REFERENCE INPUT | | | | | | | |
| Input Impedance | 15 | 20 | 25 | 15 | 20 | 25 | kΩ |
| POWER DISSIPATION | | 180 | 300 | | 180 | 300 | mW |
| MULTIPLYING MODE PERFORMANCE (All Models) | | | | | | | |
| Quadrants | | Two (2): Bipolar Operation at Digital Input Only | | | | | |
| Reference Voltage | | 1 V to 10 V, Unipolar | | | | | |
| Accuracy | | 10 Bits (±0.05% of Reduced F.S.) for 1 V dc Reference Voltage | | | | | |
| Reference Feedthrough (Unipolar Mode, All Bits OFF, and 1 V to 10 V [p-p], Sine Wave Frequency for 1/2 LSB [p-p] Feedthrough) | | 40 | | | | | kHz typ |
| Output Slew Rate 10%–90% | | 5 | | | | | mA/μs |
| 90%–10% | | 1 | | | | | mA/μs |
| Output Settling Time (All Bits ON and a 0 V–10 V Step Change in Reference Voltage) | | 1.5 μs to 0.01% F.S. | | | | | |
| CONTROL AMPLIFIER | | | | | | | |
| Full Power Bandwidth | | 300 | | | | | kHz |
| Small-Signal Closed-Loop Bandwidth | | 1.8 | | | | | MHz |

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specification subject to change without notice.

AD565A/AD566A

ABSOLUTE MAXIMUM RATINGS

| | |
|--|--|
| V _{CC} to Power Ground | 0 V to +18 V |
| V _{EE} to Power Ground (AD565A) | 0 V to -18 V |
| Voltage on DAC Output (Pin 9) | -3 V to +12 V |
| Digital Inputs (Pins 13 to 24) to Power Ground | -1.0 V to +7.0 V |
| REF IN to Reference Ground | ±12 V |
| Bipolar Offset to Reference Ground | ±12 V |
| 10 V Span R to Reference Ground | ±12 V |
| 20 V Span R to Reference Ground | ±24 V |
| REF OUT (AD565A) | Indefinite Short to Power Ground Momentary Short to V _{CC} |
| Power Dissipation | 1000 mW |

GROUNDING RULES

The AD565A and AD566A use separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns minimize current flow in low level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

AD565A ORDERING GUIDE

| Model ¹ | Max Gain T.C. (ppm of F.S./°C) | Temperature Range | Linearity Error Max @ +25°C | Package Options ² |
|--------------------|--------------------------------|-------------------|-----------------------------|------------------------------|
| AD565AJD | 50 | 0°C to +70°C | ±1/2 LSB | Ceramic (D-24) |
| AD565AJR | 50 | 0°C to +70°C | ±1/2 LSB | SOIC (RW-28) |
| AD565AKD | 20 | 0°C to +70°C | ±1/4 LSB | Ceramic (D-24) |
| AD565ASD | 30 | -55°C to +125°C | ±1/2 LSB | Ceramic (D-24) |
| AD565ATD | 15 | -55°C to +125°C | ±1/4 LSB | Ceramic (D-24) |

NOTES

¹For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices *Military Products Databook* or current/883B data sheet.

²D = Ceramic DIP, R = SOIC.

AD566A ORDERING GUIDE

| Model ¹ | Max Gain T.C. (ppm of F.S./°C) | Linearity Temperature Range | Error Max @ +25°C | Package Option ² |
|--------------------|--------------------------------|-----------------------------|-------------------|-----------------------------|
| AD566AJD | 10 | 0°C to +70°C | ±1/2 LSB | Ceramic (D-24) |
| AD566AKD | 3 | 0°C to +70°C | ±1/4 LSB | Ceramic (D-24) |
| AD566ASD | 10 | -55°C to +125°C | ±1/2 LSB | Ceramic (D-24) |
| AD566ATD | 3 | -55°C to +125°C | ±1/4 LSB | Ceramic (D-24) |

NOTES

¹For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices *Military Products Databook* or current/883B data sheet.

²D = Ceramic DIP.

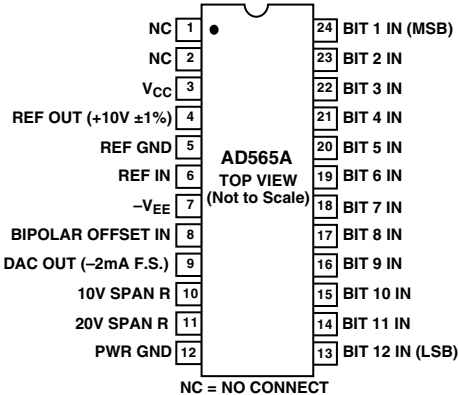
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD565A/AD566A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

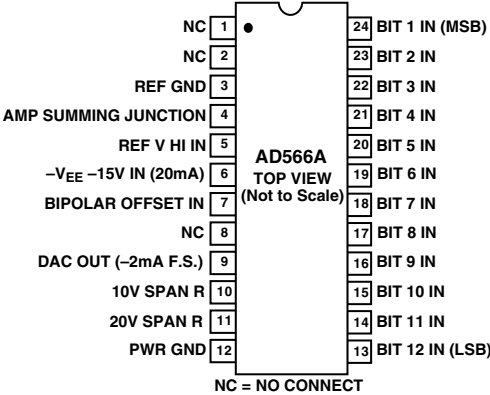


PIN CONFIGURATIONS

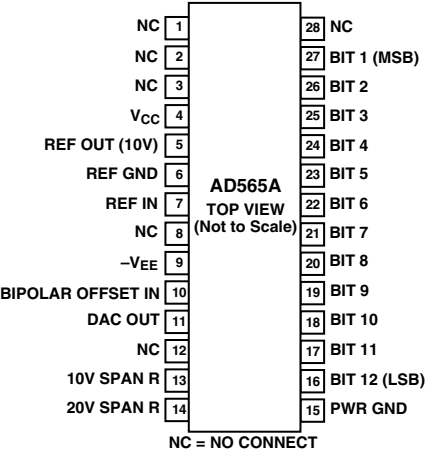
24-Lead DIP



24-Lead DIP



28-Lead SOIC



AD565A/AD566A

CONNECTING THE AD565A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown in Figures 1, 2, and 3 with the preferred trimming techniques. If a low offset operational amplifier (OP77, AD741L, OP07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV max offset voltage should be used to keep offset errors below 1/2 LSB). If a 50 Ω fixed resistor is substituted for the 100 Ω trimmer, unipolar zero is typically within $\pm 1/2$ LSB (plus op amp offset) and full-scale accuracy is within 0.1% (0.25% max). Substituting a 50 Ω resistor for the 100 Ω bipolar offset trimmer gives a bipolar zero error typically within ± 2 LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications that require a settling time to $\pm 1/2$ LSB of 1 μ s. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 pF DAC output capacitance.

FIGURE 1. UNIPOLAR CONFIGURATION

This configuration provides a unipolar 0 V to 10 V output range. In this mode, the bipolar terminal, Pin 8, should be grounded if not used for trimming.

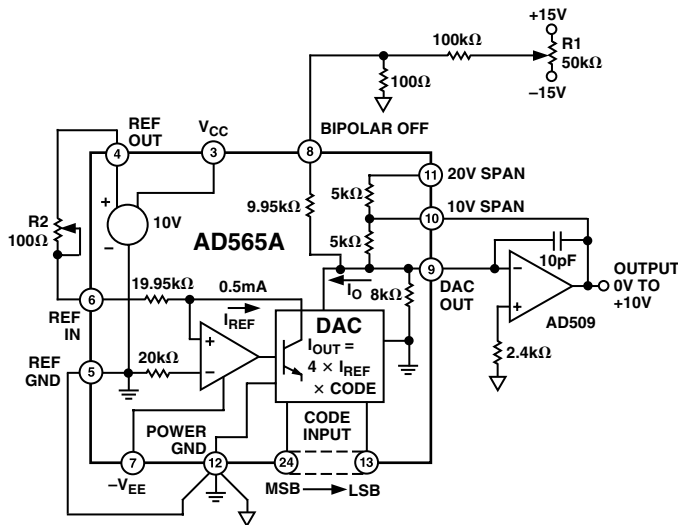


Figure 1. 0 V to 10 V Unipolar Voltage Output

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1 until the output reads 0.000 V (1 LSB = 2.44 mV). In most cases, this trim is not needed, but Pin 8 should then be connected to Pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100 Ω gain trimmer R2 until the output is 9.9976 V. (Full scale is adjusted to 1 LSB less than nominal full scale of 10.000 V.) If a 10.2375 V full scale is desired (exactly 2.5 mV/bit), insert a 120 Ω resistor in series with the gain resistor at Pin 10 to the op amp output.

FIGURE 2. BIPOLAR CONFIGURATION

This configuration provides a bipolar output voltage from -5.000 V to +4.9976 V, with positive full scale occurring with all bits ON (all 1s).

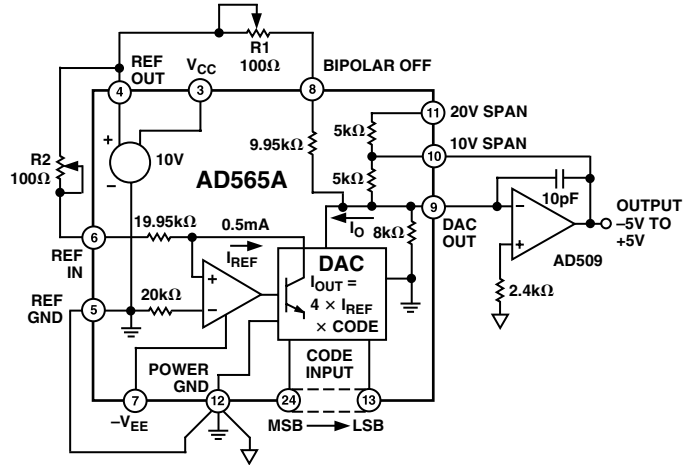


Figure 2. ± 5 V Bipolar Voltage Output

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100 Ω gain trimmer R1 to give -5.000 V output.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100 Ω gain trimmer R2 to give a reading of +4.9976 V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 3. OTHER VOLTAGE RANGES

The AD565A can also be easily configured for a unipolar 0 V to +5 V range or ± 2.5 V and ± 10 V bipolar ranges by using the additional 5 kΩ application resistor provided at the 20 V span R terminal, Pin 11. For a 5 V span (0 V to +5 V, or ± 2.5 V), the two 5 kΩ resistors are used in parallel by shorting Pin 11 to Pin 10 and connecting Pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ± 10 V range (20 V span) use the 5 kΩ resistors in series by connecting only Pin 11 to the op amp output and the bipolar offset connected as shown. The ± 10 V option is shown in Figure 3.

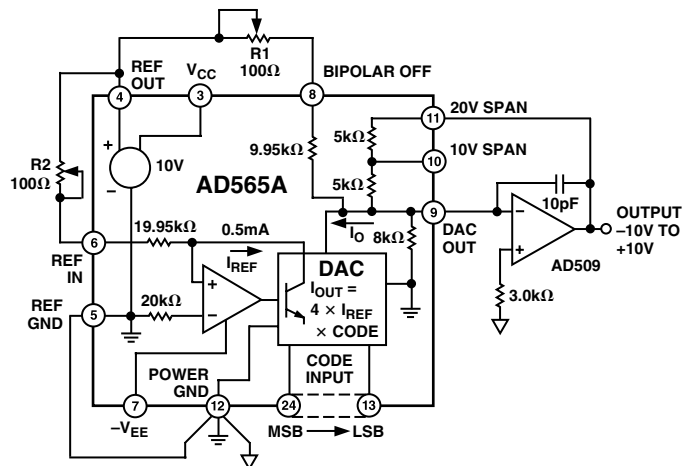


Figure 3. ± 10 V Voltage Output

CONNECTING THE AD566A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown in Figures 4, 5, and 6 with the preferred trimming techniques. If a low offset operational amplifier (OP77, AD741L, OP07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5 mV max offset voltage should be used to keep offset errors below 1/2 LSB). If a 50 Ω fixed resistor is substituted for the 100 Ω trimmer, unipolar zero typically is within ±1/2 LSB (plus op amp offset), and full-scale accuracy is within 0.1% (0.25% max). Substituting a 50 Ω resistor for the 100 Ω bipolar offset trimmer gives a bipolar zero error typically within ±2 LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications that require a settling time to ±1/2 LSB of 1 μs. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 pF DAC output capacitance.

FIGURE 4. UNIPOLAR CONFIGURATION

This configuration provides a unipolar 0 V to 10 V output range. In this mode, the bipolar terminal, Pin 7, should be grounded if not used for trimming.

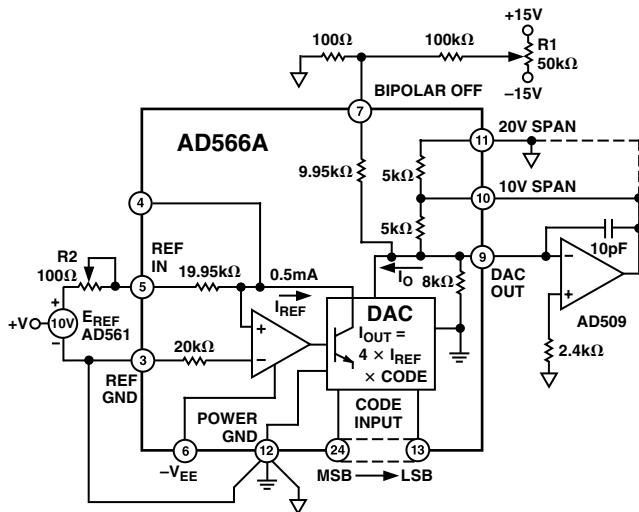


Figure 4. 0 V to 10 V Unipolar Voltage Output

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 V (1 LSB = 2.44 mV). In most cases, this trim is not needed, but Pin 7 should then be connected to Pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100 Ω gain trimmer, R2, until the output is 9.9976 V. (Full scale is adjusted to 1 LSB less than nominal full scale of 10.000 V.) If a 10.2375 V full scale is desired (exactly 2.5 mV/bit), insert a 120 Ω resistor in series with the gain resistor at Pin 10 to the op amp output.

FIGURE 5. BIPOLAR CONFIGURATION

This configuration provides a bipolar output voltage from -5.000 V to +4.9976 V, with positive full scale occurring with all bits ON (all 1s).

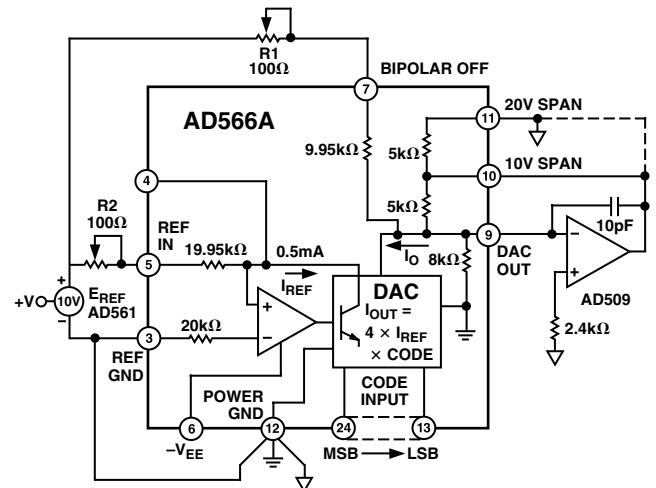


Figure 5. ±5 V Bipolar Voltage Output

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100 Ω trimmer R1 to give -5.000 output V.

STEP II . . . GAIN ADJUST

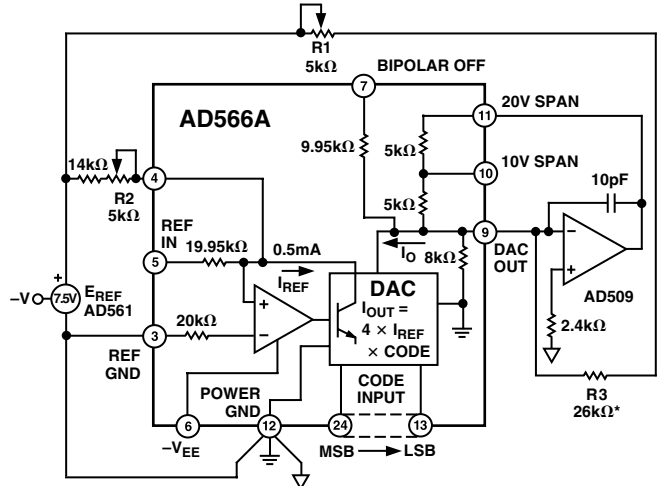
Turn ON all bits. Adjust 100 Ω gain trimmer R2 to give a reading of +4.9976 V.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

AD565A/AD566A

FIGURE 6. OTHER VOLTAGE RANGES

The AD566A can also be easily configured for a unipolar 0 V to +5 V range or ± 2.5 V and ± 10 V bipolar ranges by using the additional 5 k Ω application resistor provided at the 20 V span R terminal, Pin 11. For a 5 V span (0 V to +5 V or ± 2.5 V), the two 5 k Ω resistors are used in parallel by shorting Pin 11 to Pin 9 and connecting Pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF} for the bipolar range. For the ± 10 V range (20 V span), use the 5 k Ω resistors in series by connecting only Pin 11 to the op amp output and the bipolar offset connected as shown. The ± 10 V option is shown in Figure 6.



* THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISHES A CURRENT TO BALANCE THE MSB CURRENT. THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPANDED ON PREVIOUS PAGE.

Figure 6. ± 10 V Voltage Output

Table I. Digital Input Codes

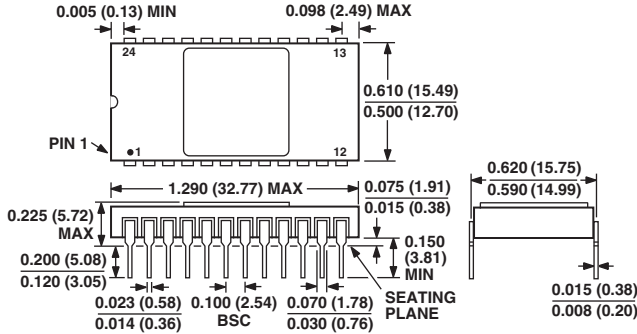
| DIGITAL INPUT | | Straight Binary | ANALOG OUTPUT Offset Binary | Twos Complement* |
|---------------|-----|-------------------|--------------------------------|------------------|
| MSB | LSB | | | |
| 0 | 0 | Zero | -FS | Zero |
| 0 | 1 | Mid Scale - 1 LSB | Zero - 1 LSB | +FS - 1 LSB |
| 1 | 0 | +1/2 FS | Zero | -FS |
| 1 | 1 | +FS - 1 LSB | +FS - 1 LSB | Zero - 1 LSB |

*Inverts the MSB of the offset binary code with an external inverter to obtain twos complement.

OUTLINE DIMENSIONS

24-Lead Side-Brazed Solder Lid Ceramic DIP [DIP/SB]
(D-24)

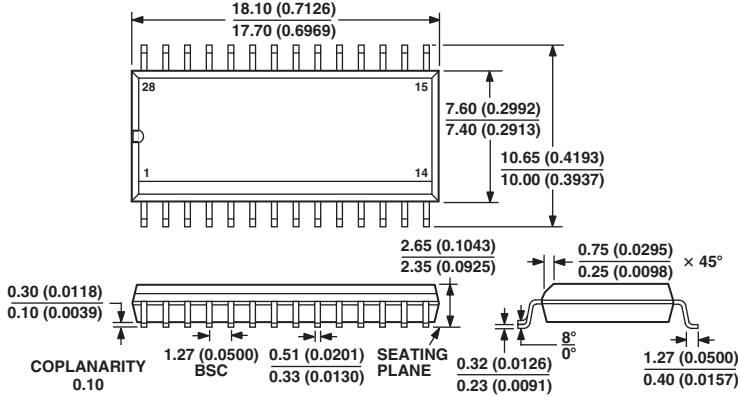
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

28-Lead Standard Small Outline Package [SOIC]
Wide Body
(RW-28)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AE
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

| Location | Page |
|---|------|
| 10/02—Data Sheet changed from REV. D to REV. E. | |
| Edits to SPECIFICATIONS | 2 |
| OUTLINE DIMENSIONS updated | 11 |

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