Low Power, 16-Bit Buffered Sigma-Delta ADC

Data Sheet **AD7790**

FEATURES

Power
- **Supply: 2.5 V to 5.25 V operation**
- **Normal: 75 µA maximum**
- **Power-down: 1 µA maximum**

RMS noise: 1.1 µV at 9.5 Hz update rate
16-bit p-p resolution
Integral nonlinearity: 3.5 ppm typical
Simultaneous 50 Hz and 60 Hz rejection
Internal clock oscillator
Programmable gain amplifier
Rail-to-rail input buffer
V_{DD} monitor channel
Temperature range: –40°C to +105°C
10-lead MSOP

INTERFACE

3-wire serial
SPI®, QSPI™, MICROWIRE™, and DSP compatible
Schmitt trigger on SCLK

APPLICATIONS

Smart transmitters
Battery applications
Portable instrumentation
Sensor measurement
Temperature measurement
Pressure measurement
Weigh scales
4 to 20 mA loops

FUNCTIONAL BLOCK DIAGRAM

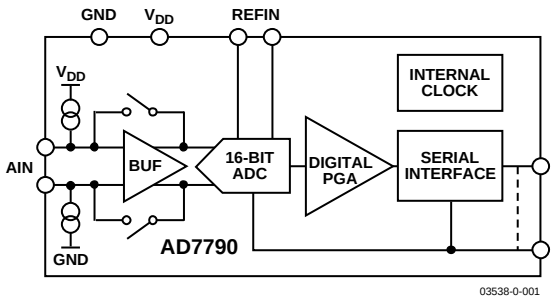


Figure 1.

GENERAL DESCRIPTION

The AD7790 is a low power, complete analog front end for low frequency measurement applications. It contains a low noise 16-bit ∑-Δ ADC with one differential input that can be buffered or unbuffered along with a digital PGA, which allows gains of 1, 2, 4, and 8.

The device operates from an internal clock. Therefore, the user does not have to supply a clock source to the device. The output data rate from the part is software programmable and can be varied from 9.5 Hz to 120 Hz, with the rms noise equal to 1.1 µV at the lower update rate. The internal clock frequency can be divided by a factor of 2, 4, or 8, which leads to a reduction in the current consumption. The update rate, cutoff frequency, and settling time will scale with the clock frequency.

The part operates with a power supply from 2.5 V to 5.25 V. When operating from a 3 V supply, the power dissipation for the part is 225 µW maximum. It is housed in a 10-lead MSOP.

Rev. A **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

3/13—Rev. 0 to Rev. A

Added ESD Caution Section 7
Changes to Figure 10 15
Change to Reference Input Section 17
Updated Outline Dimensions 19
Changes to Ordering Guide 19

8/03—Revision 0: Initial Version

AD7790—SPECIFICATIONS[1]

Table 1. (V_{DD} = 2.5 V to 5.25 V; REFIN(+) = 2.5 V; REFIN(–) = GND; CDIV1 = CDIV0 = 0; GND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD7790B	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATION			
Output Update Rate	9.5	Hz min nom	
	120	Hz max nom	
ADC CHANNEL			
No Missing Codes[2]	16	Bits min	$\pm V_{REF}$ Range, Update Rate $\leq$ 20 Hz
Resolution	16	Bits p-p	9.5 Hz Update Rate
Output Noise	1.1	µV rms typ	
Integral Nonlinearity	±15	ppm of FSR max	3.5 ppm typ
Offset Error	±3	µV typ	
Offset Error Drift vs. Temperature	±10	nV/°C typ	
Full-Scale Error[3]	±10	µV typ	
Gain Drift vs. Temperature	±0.5	ppm/°C typ	
Power Supply Rejection	90	dB min	Input Range = ±REFIN, 100 dB typ
ANALOG INPUTS			
Differential Input Voltage Ranges	±REFIN/GAIN	V nom	REFIN = REFIN(+) – REFIN(–); GAIN = 1, 2, 4, or 8
Absolute AIN Voltage Limits[2]	GND + 100 mV	V min	Buffered Mode of Operation
	V_{DD} – 100 mV	V max	
Analog Input Current			Buffered Mode of Operation
Average Input Current[2]	±1	nA max	
Average Input Current Drift	±5	pA/°C typ	
Absolute AIN Voltage Limits[2]	GND – 30 mV	V min	Unbuffered Mode of Operation
	V_{DD} + 30 mV	V max	
Analog Input Current			Unbuffered Mode of Operation Input current varies with input voltage.
Average Input Current	±400	nA/V typ	
Average Input Current Drift	±50	pA/V/°C typ	
Normal Mode Rejection[2]			
@ 50 Hz, 60 Hz	65	dB min	73 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[2:0] = 100[4]
@ 50 Hz	80	dB min	90 dB typ, 50 ± 1 Hz, FS[2:0] = 101[4]
@ 60 Hz	80	dB min	90 dB typ, 60 ± 1 Hz, FS[2:0] = 011[4]
Common Mode Rejection			Input Range = ±REFIN, AIN = 1 V
@ DC	90	dB min	100 dB typ (FS[2:0] = 100[4])
@ 50 Hz, 60 Hz[2]	100	dB min	50 ± 1 Hz (FS[2:0] = 101[4]), 60 ± 1 Hz (FS[2:0] = 011[4])
REFERENCE INPUT			REFIN = REFIN(+) – REFIN(–)
REFIN Voltage	2.5	V nom	
Reference Voltage Range[2]	0.1	V min	
	V_{DD}	V max	
Absolute REFIN Voltage Limits[2]	GND – 30 mV	V min	
	V_{DD} + 30 mV	V max	
Average Reference Input Current	0.5	µA/V typ	
Average Reference Input Current Drift	±0.03	nA/V/°C typ	

[1] Temperature Range –40°C to +105°C.
[2] Specification is not production tested, but is supported by characterization data at initial product release.
[3] Full-scale error applies to both positive and negative full-scale and applies at the factory calibration conditions (V_{DD} = 4 V).
[4] FS[2:0] are the three bits used in the filter register to select the output word rate.

SPECIFICATIONS (continued)[1]

Parameter	AD7790B	Unit	Test Conditions/Comments
REFERENCE INPUT (continued)			
Normal Mode Rejection[2]			
@ 50 Hz, 60 Hz	65	dB min	73 dB typ, 50 ± 1 Hz, 60 ± 1 Hz, FS[2:0] = 100[4]
@ 50 Hz	80	dB min	90 dB typ, 50 ± 1 Hz, FS[2:0] = 101[4]
@ 60 Hz	80	dB min	90 dB typ, 60 ± 1 Hz, FS[2:0] = 011[4]
Common Mode Rejection			Input Range = ±2.5 V, AIN = 1 V
@ DC	100	dB typ	FS[2:0] = 100[4]
@ 50 Hz, 60 Hz	110	dB typ	50 ± 1 Hz (FS[2:0] = 101[4]), 60 ± 1 Hz (FS[2:0] = 011[4])
LOGIC INPUTS			
All Inputs Except SCLK[2]			
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V min	V_{DD} = 3 V or 5 V
SCLK Only (Schmitt-Triggered Input)[2]			
$V_T(+)$	1.4/2	V min/V max	V_{DD} = 5 V
$V_T(-)$	0.8/1.4	V min/V max	V_{DD} = 5 V
$V_T(+) - V_T(-)$	0.3/0.85	V min/V max	V_{DD} = 5 V
$V_T(+)$	0.9/2	V min/V max	V_{DD} = 3 V
$V_T(-)$	0.4/1.1	V min/V max	V_{DD} = 3 V
$V_T(+) - V_T(-)$	0.3/0.85	V min/V max	V_{DD} = 3 V
Input Currents	±1	µA max	$V_{IN} = V_{DD}$ or GND
Input Capacitance	10	pF typ	All Digital Inputs
LOGIC OUTPUTS			
V_{OH}, Output High Voltage[2]	V_{DD} – 0.6	V min	V_{DD} = 3 V, I_{SOURCE} = 100 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 3 V, I_{SINK} = 100 µA
V_{OH}, Output High Voltage[2]	4	V min	V_{DD} = 5 V, I_{SOURCE} = 200 µA
V_{OL}, Output Low Voltage[2]	0.4	V max	V_{DD} = 5 V, I_{SINK} = 1.6 mA
Floating-State Leakage Current	±1	µA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset Binary		
POWER REQUIREMENTS[5]			
Power Supply Voltage			
V_{DD} – GND	2.5/5.25	V min/max	
Power Supply Currents			
I_{DD} Current[6]	75	µA max	65 µA typ, V_{DD} = 3.6 V, Unbuffered Mode
	145	µA max	130 µA typ, V_{DD} = 3.6 V, Buffered Mode
	80	µA max	73 µA typ, V_{DD} = 5.25 V, Unbuffered Mode
	160	µA max	145 µA typ, V_{DD} = 5.25 V, Buffered Mode
I_{DD} (Power-Down Mode)	1	µA max	

[5] Digital inputs equal to V_{DD} or GND.
[6] The current consumption can be further reduced by using the ADC in one of the low power modes (see Table 15).

TIMING CHARACTERISTICS[1, 2]

Table 2. (V_{DD} = 2.5 V to 5.25 V; GND = 0 V, REFIN(+) = 2.5 V, REFIN(–) = GND, CDIV1 = CDIV0 = 0, Input Logic 0 = 0 V, Input Logic 1 = V_{DD}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
t_3	100	ns min	SCLK High Pulsewidth
t_4	100	ns min	SCLK Low Pulsewidth
Read Operation			
t_1	0	ns min	$\overline{CS}$ Falling Edge to DOUT/$\overline{RDY}$ Active Time
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.5 V to 3.6 V
t_2[3]	0	ns min	SCLK Active Edge to Data Valid Delay[4]
	60	ns max	V_{DD} = 4.75 V to 5.25 V
	80	ns max	V_{DD} = 2.5 V to 3.6 V
t_5[5, 6]	10	ns min	Bus Relinquish Time after $\overline{CS}$ Inactive Edge
	80	ns max	
t_6	100	ns max	SCLK Inactive Edge to $\overline{CS}$ Inactive Edge
t_7	10	ns min	SCLK Inactive Edge to DOUT/$\overline{RDY}$ High
Write Operation			
t_8	0	ns min	$\overline{CS}$ Falling Edge to SCLK Active Edge Setup Time[4]
t_9	30	ns min	Data Valid to SCLK Edge Setup Time
t_{10}	25	ns min	Data Valid to SCLK Edge Hold Time
t_{11}	0	ns min	$\overline{CS}$ Rising Edge to SCLK Edge Hold Time

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 3 and Figure 4.
[3] These numbers are measured with the load circuit of Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[4] SCLK active edge is falling edge of SCLK.
[5] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.
[6] $\overline{RDY}$ returns high after a read of the ADC. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. In continuous read mode, the digital word can be read only once.

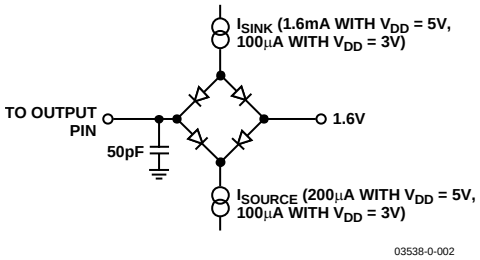


Figure 2. Load Circuit for Timing Characterization

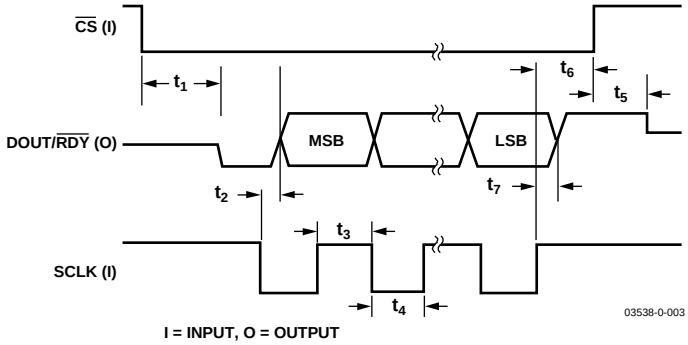


Figure 3. Read Cycle Timing Diagram

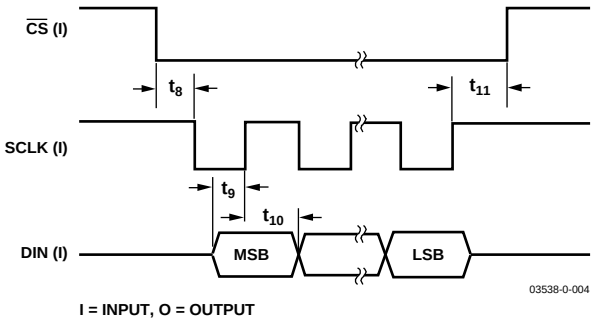


Figure 4. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3. (T_A= 25°C, unless otherwise noted.)

Parameter	Rating
V_{DD} to GND	–0.3 V to +7 V
Analog Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Total AIN/REFIN Current (Indefinite)	30 mA
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature	150°C
MSOP	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

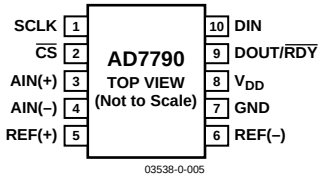


Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	SCLK	Serial Clock Input for Data Transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to or from the ADC in smaller batches of data.
2	$\overline{CS}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{CS}$ can be used to select the ADC in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the device. $\overline{CS}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device.
3	AIN(+)	Analog Input. AIN(+) is the positive terminal of the fully differential analog input.
4	AIN(–)	Analog Input. AIN(–) is the negative terminal of the fully differential analog input.
5	REFIN(+)	Positive Reference Input. REFIN(+) can lie anywhere between V_{DD} and GND + 0.1 V. The nominal reference voltage (REFIN(+) – REFIN(–)) is 2.5 V, but the part functions with a reference from 0.1 V to V_{DD}.
6	REFIN(–)	Negative Reference Input. This reference input can lie anywhere between GND and V_{DD} – 0.1 V.
7	GND	Ground Reference Point.
8	V_{DD}	Supply Voltage, 2.5 V to 5.25 V.
9	DOUT/$\overline{RDY}$	Serial Data Output/Data Ready Output. DOUT/$\overline{RDY}$ serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. In addition, DOUT/$\overline{RDY}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin will go high before the next update occurs. The DOUT/$\overline{RDY}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/$\overline{RDY}$ pin. With $\overline{CS}$ low, the data/control word information is placed on the DOUT/$\overline{RDY}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. The end of a conversion is also indicated by the $\overline{RDY}$ bit in the status register. When $\overline{CS}$ is high, the DOUT/$\overline{RDY}$ pin is three-stated but the $\overline{RDY}$ bit remains active.
10	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers within the ADC, the register selection bits of the communications register identifying the appropriate register.

TYPICAL PERFORMANCE CHARACTERISTICS

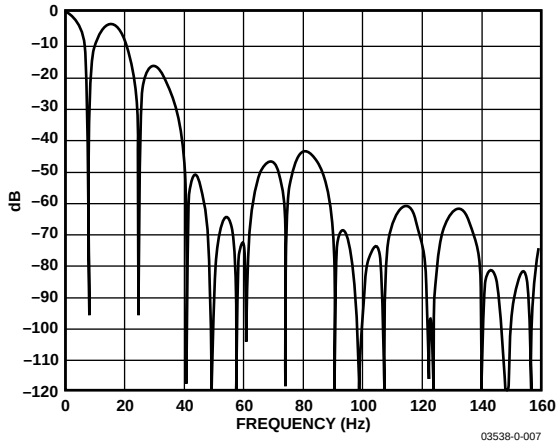


Figure 6. Frequency Response for a 16.6 Hz Update Rate

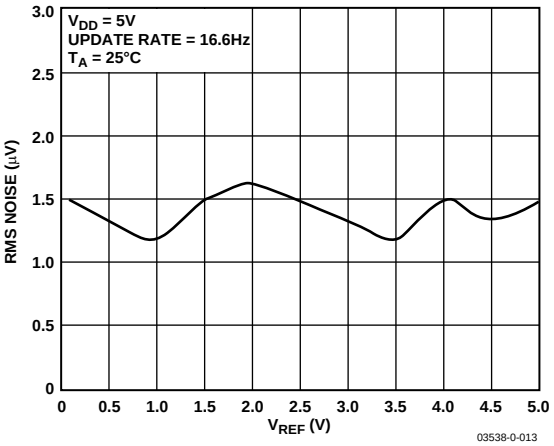


Figure 7. RMS Noise vs. Reference Voltage

ON-CHIP REGISTERS

The ADC is controlled and configured via a number of on-chip registers, which are described on the following pages. In the following descriptions, *set* implies a Logic 1 state and *cleared* implies a Logic 0 state, unless otherwise stated.

COMMUNICATIONS REGISTER (RS1, RS0 = 0, 0)

The communications register is an 8-bit write-only register. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation, and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface and, on power-up or after a reset, the ADC is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high returns the ADC to this default state by resetting the entire part. Table 5 outlines the bit designations for the communications register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the communications register. CR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}$(0)	0(0)	RS1(0)	RS0(0)	R/$\overline{\text{W}}$(0)	CREAD(0)	CH1(0)	CH0(0)

Table 5. Communications Register Bit Designations

Bit Location	Bit Name	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so that the write to the communications register actually occurs. If a 1 is the first bit written, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the communications register.
CR6	0	This bit must be programmed to Logic 0 for correct operation.
CR5–CR4	RS1–RS0	Register Address Bits. These address bits are used to select which of the ADC's registers are being selected during this serial interface communication. See Table 6.
CR3	R/$\overline{\text{W}}$	A 0 in this bit location indicates that the next operation will be a write to a specified register. A 1 in this position indicates that the next operation will be a read from the designated register.
CR2	CREAD	Continuous Read of the Data Register. When this bit is set to 1 (and the data register is selected), the serial interface is configured so that the data register can be continuously read, i.e., the contents of the data register are placed on the DOUT pin automatically when the SCLK pulses are applied. The communications register does not have to be written to for data reads. To enable continuous read mode, the instruction 001111XX must be written to the communications register. To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit continuous read mode. Additionally, a reset will occur if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.
CR1–CR0	CH1–CH0	These bits are used to select the analog input channel. The differential channel can be selected (AIN(+)/AIN(–)) or an internal short (AIN(–)/AIN(–)) can be selected. Alternatively, the power supply can be selected, i.e., the ADC can measure the voltage on the power supply, which is useful for monitoring power supply variation. The power supply voltage is divided by 5 and then applied to the modulator for conversion. The ADC uses a 1.17 V ± 5% on-chip reference as the reference source for the analog to digital conversion. Any change in channel resets the filter and a new conversion is started.

Table 6. Register Selection

RS1	RS0	Register	Register Size
0	0	Communications Register during a Write Operation	8-Bit
0	0	Status Register during a Read Operation	8-Bit
0	1	Mode Register	8-Bit
1	0	Filter Register	8-Bit
1	1	Data Register	16-Bit

Table 7. Channel Selection

CH1	CH0	Channel
0	0	AIN(+) – AIN(–)
0	1	Reserved
1	0	AIN(–) – AIN(–)
1	1	V_{DD} Monitor

STATUS REGISTER (RS1, RS0 = 0, 0; POWER-ON/RESET = 0x88)

The status register is an 8-bit read-only register. To access the ADC status register, the user must write to the communications register, select the next operation to be a read, and load bits RS1 and RS0 with 0. Table 8 outlines the bit designations for the status register. SR0 through SR7 indicate the bit locations, SR denoting the bits are in the status register. SR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
$\overline{\text{RDY}}$(1)	ERR(0)	0(0)	0(0)	1(1)	WL(0)	CH1(0)	CH0(0)

Table 8. Status Register Bit Designations

Bit Location	Bit Name	Description
SR7	$\overline{\text{RDY}}$	Ready bit for ADC. *Cleared* when data is written to the ADC data register. The $\overline{\text{RDY}}$ bit is *set* automatically after the ADC data register has been read or a period of time before the data register is updated with a new conversion result to indicate to the user not to read the conversion data. It is also *set* when the part is placed in powe-down mode. The end of a conversion is indicated by the DOUT/$\overline{\text{RDY}}$ pin also. This pin can be used as an alternative to the status register for monitoring the ADC for conversion data.
SR6	ERR	ADC Error Bit. This bit is written to at the same time as the $\overline{\text{RDY}}$ bit. *Set* to indicate that the result written to the ADC data register has been clamped to all 0s or all 1s. Error sources include overrange, under-range. *Cleared* by a write operation to start a conversion.
SR5	0	This bit is automatically *cleared*.
SR4	0	This bit is automatically *cleared*.
SR3	1	This bit is automatically *set*.
SR2	0	This bit is automatically *cleared* if the device is an AD7790. It can be used to distinguish between the AD7790 and AD7791, in which the bit is *set*.
SR1–SR0	CH1–CH0	These bits indicate which channel is being converted by the ADC.

MODE REGISTER (RS1, RS0 = 0, 1; POWER-ON/RESET = 0x02)

The mode register is an 8-bit register from which data can be read or to which data can be written. This register is used to configure the ADC for range, enable or disable the buffer, or place the device into power-down mode. Table 9 outlines the bit designations for the mode register. MR0 through MR7 indicate the bit locations, MR denoting the bits are in the mode register. MR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. Any write to the setup register resets the modulator and filter and sets the $\overline{\text{RDY}}$ bit.

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
MD1(0)	MD0(0)	G1(0)	G0(0)	BO(0)	0(0)	BUF(1)	0(0)

Table 9. Mode Register Bit Designations

Bit Location	Bit Name	Description
MR7–MR6	MD1–MD0	Mode Select Bits. These bits select between continuous conversion mode, single conversion mode, and standby mode. In continuous conversion mode, the ADC continuously performs conversions and places the result in the data register. $\overline{\text{RDY}}$ goes low when a conversion is complete. The user can read these conversions by placing the device in continuous read mode whereby the conversions are automatically placed on the DOUT line when SCLK pulses are applied. Alternatively, the user can instruct the ADC to output the conversion by writing to the communications register. After power-on, the first conversion is available after a period 2/ f_{ADC} while subsequent conversions are available at a frequency of f_{ADC}. In single conversion mode, the ADC is placed in power-down mode when conversions are not being performed. When single conversion mode is selected, the ADC powers up and performs a single conversion, which occurs after a period 2/f_{ADC}. The conversion result in placed in the data register, $\overline{\text{RDY}}$ goes low, and the ADC returns to power-down mode. The conversion remains in the data register and $\overline{\text{RDY}}$ remains active (low) until the data is read or another conversion is performed. See Table 10.
MR5–MR4	G1–G0	Range Bits. The AD7790 can be operated with four analog input ranges (see Table 11).
MR3	BO	Burnout Current Enable Bit. When this bit is set to 1 by the user, the 100 nA current sources in the signal path are enabled. When BO = 0, the burnout currents are disabled. The burnout currents can be enabled only when the buffer is active.

Bit Location	Bit Name	Description
MR2	0	This bit must be programmed with a Logic 0 for correct operation.
MR1	BUF	Configures the ADC for buffered or unbuffered mode of operation. If *cleared*, the ADC operates in unbuffered mode, lowering the power consumption of the device. If *set*, the ADC operates in buffered mode, allowing the user to place source impedances on the front end without contributing gain errors to the system.
MR0	0	This bit must be programmed with a Logic 0 for correct operation.

Table 10. Operating Modes

MD1	MD0	Mode
0	0	Continuous Conversion Mode (Default)
0	1	Reserved
1	0	Single Conversion Mode
1	1	Power-Down Mode

Table 11. Analog Input Ranges

G1	G0	Range	AD7790 LSB Size with V_{REF} = +2.5 V (μV)
0	0	$\pm V_{REF}$	76.3
0	1	$\pm V_{REF}/2$	38.14
1	0	$\pm V_{REF}/4$	19.07
1	1	$\pm V_{REF}/8$	9.54

FILTER REGISTER (RS1, RS0 = 1, 0; POWER-ON/RESET = 0x04)

The filter register is an 8-bit register from which data can be read or to which data can be written. This register is used to set the output word rate. Table 12 outlines the bit designations for the filter register. FR0 through FR7 indicate the bit locations, FR denoting the bits are in the filter register. FR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0
0(0)	0(0)	CDIV1(0)	CDIV0(0)	0(0)	FS2(1)	FS1(0)	FS0(0)

Table 12. Filter Register Bit Designatins

Bit Location	Bit Name	Description
FR7–FR6	0	These bits must be programmed with a Logic 0 for correct operation.
FR5–FR4	CLKDIV1–CDIV0	These bits are used to operate the AD7790 in the lower power modes. The clock is internally divided and the power is reduced. 00 Normal Mode 01 Clock Divided by 2 10 Clock Divided by 4 11 Clock Divided by 8
FR3	0	This bit must be programmed with a Logic 0 for correct operation.
FR2–FR0	FS2–FS0	These bits set the output word rate of the ADC. The update rate influences the 50 Hz/60 Hz rejection and noise. The noise is the same for all gain settings. See Table 13 for the allowable update rates in full power mode. In the low power modes, the update rates will be reduced. (See Reduced Current Modes.)

Table 13. Update Rates

FS2	FS1	FS0	f_{ADC} (Hz)	f3dB (Hz)	RMS Noise (μV)	Rejection
0	0	0	120	28	40	25 dB @ 60 Hz
0	0	1	100	24	25	25 dB @ 50 Hz
0	1	0	33.3	8	3.36	
0	1	1	20	4.7	1.6	80 dB @ 60 Hz
1	**0**	**0**	**16.6**	**4**	**1.5**	**65 dB @ 50 Hz/60 Hz (Default Setting)**
1	0	1	16.7	4	1.5	80 dB @ 50 Hz
1	1	0	13.3	3.2	1.2	
1	1	1	9.5	2.3	1.1	62 dB @ 50/60 Hz

DATA REGISTER (RS1, RS0 = 1, 1; POWER-ON/RESET = 0x0000)

The conversion result from the ADC is stored in this data register. This is a read-only register. On completion of a read operation from this register, the $\overline{RDY}$ bit/pin is set.

ADC CIRCUIT INFORMATION

OVERVIEW

The AD7790 is a low power ADC that incorporates a Σ-Δ modulator, a buffer, a PGA, and on-chip digital filtering intend-ed for the measurement of wide dynamic range, low frequency signals such as those in pressure transducers, weigh scales, and temperature measurement applications.

The part has one differential input that can be buffered or unbuffered. Buffering the input channel means that the part can accommodate significant source impedances on the analog input and that R, C filtering (for noise rejection or RFI reduction) can be placed on the analog input, if required. The device requires an external reference of 2.5 nominal. Figure 7 shows the basic connections required to operate the part.

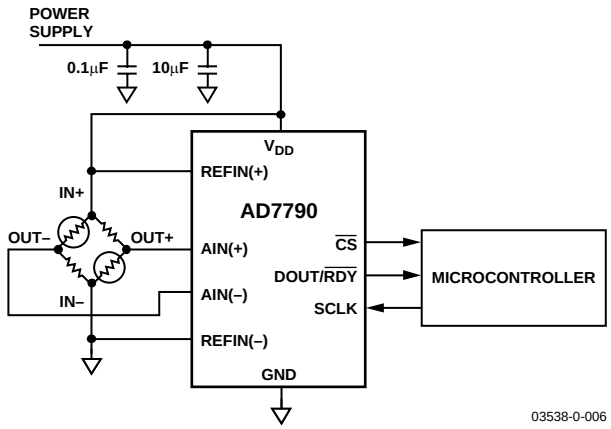


Figure 7. Basic Connection Diagram

The output rate of the AD7790 (f_{ADC}) is user programmable with the settling time equal to $2 \times t_{ADC}$. Normal mode rejection is the major function of the digital filter. Table 13 lists the available output rates from the AD7790. Simultaneous 50 Hz and 60 Hz rejection is optimized when the update rate equals 16.6 Hz as notches are placed at both 50 Hz and 60 Hz with this update rate (see Figure 6).

NOISE PERFORMANCE

Table 14 shows the output rms noise, rms resolution, and peak-to-peak resolution (rounded to the nearest 0.5 LSB) for the different update rates and input ranges for the AD7790. The numbers given are with a reference of 2.5 V. The numbers are typical and generated with a differential input voltage of 0 V. The peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. The second is quantization noise, which is added when the analog input is converted into the digital domain. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source.

Table 14. Typical Peak-to-Peak Resolution (Effective Resolution) vs. Update Rate and Input Range

	Input Range			
Update Rate	**±0.3125**	**±0.625**	**±1.25**	**±2.5**
9.5	16 (16)	16 (16)	16 (16)	16 (16)
13.3	16 (16)	16 (16)	16 (16)	16 (16)
16.7	16 (16)	16 (16)	16 (16)	16 (16)
16.6	16 (16)	16 (16)	16 (16)	16 (16)
20	15.5 (16)	16 (16)	16 (16)	16 (16)
33.3	14.5 (16)	15.5 (16)	16 (16)	16 (16)
100	11.5 (14)	12.5 (15)	13.5 (16)	14.5 (16)
120	11 (13.5)	12 (14.5)	13 (15.5)	14 (16)

REDUCED CURRENT MODES

The AD7790 has a current consumption of 160 μA maximum when operated with the buffer enabled and with a 5 V power supply. The power can be reduced further by setting bits CDIV1 and CDIV0 in the filter register appropriately (see Table 15).

By setting these bits, the internal clock is divided by 2, 4, or 8 before being applied to the modulator and filter, resulting in a reduction in the digital current.

When the internal clock is reduced, the update rate will also be reduced. For example, if the filter bits are set to give an update rate of 16.6 Hz when the AD7790 is operated in full clock mode, the update rate will equal 8.3 Hz in divide by 2 mode. In these low power modes, there may be some degradation in the ADC performance.

Table 15. Low Power Mode Selection

CDIV[1:0]	Clock	Typ Current, Buffered (μA)	Typ Current, Unbuffered (μA)	50 Hz/60 Hz Rejection (dB)
00	1	146	75	70
10	1/2	87	45	72
10	1/4	56	30	88
11	1/8	41	25	89

DIGITAL INTERFACE

As previously outlined, the AD7790's programmable functions are controlled using a set of on-chip registers. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface. All communications with the part must start with a write to the communications register. After power-on or reset, the device expects a write to its communications register. The data written to this register determines whether the next operation is a read operation or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part begins with a write operation to the communications register followed by a write to the selected register. A read operation from any other register (except when continuous read mode is selected) starts with a write to the communications register followed by a read operation from the selected register.

The AD7790's serial interface consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line is used to transfer data into the on-chip registers while DOUT/$\overline{RDY}$ is used for accessing from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT/$\overline{RDY}$) occur with respect to the SCLK signal. The DOUT/ $\overline{RDY}$ pin operates as a Data Ready signal also, the line going low when a new data-word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{CS}$ is used to select a device. It can be used to decode the AD7790 in systems where several components are connected to the serial bus.

Figure 3 and Figure 4 show timing diagrams for interfacing to the AD7790 with $\overline{CS}$ being used to decode the part. Figure 3 shows the timing for a read operation from the AD7790's output shift register while Figure 4 shows the timing for a write operation to the input shift register. In all modes except continuous read mode, it is possible to read the same word from the data register several times even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations have been completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7790. The end of the conversion can be monitored using the $\overline{RDY}$ bit in the status register. This scheme is suitable for interfacing to microcontrollers. If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin. For microcontroller interfaces, it is recommended that SCLK idles high between data transfers.

The AD7790 can be operated with $\overline{CS}$ being used as a frame synchronization signal. This scheme is useful for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{CS}$ since $\overline{CS}$ would normally occur after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

The serial interface can be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7790 line for at least 32 serial clock cycles, the serial interface is reset. This ensures that in 3-wire systems, the interface can be reset to a known state if the interface gets lost due to a software error or some glitch in the system. Reset returns the interface to the state in which it is expecting a write to the communications register. This operation resets the contents of all registers to their power-on values.

The AD7790 can be configured to continuously convert or to perform a single conversion. See Figure 8 through Figure 10.

Single Conversion Mode

In single conversion mode, the AD7790 is placed in shutdown mode between conversions. When a single conversion is initiated by setting MD1 to 1 and MD0 to 0 in the mode register, the AD7790 powers up, performs a single conversion, and then returns to shutdown mode. A conversion will require a time period of $2 \times t_{ADC}$. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ will go high. If $\overline{CS}$ is low, DOUT/$\overline{RDY}$ will remain high until another conversion is initiated and completed. The data register can be read several times, if required, even when DOUT/ $\overline{RDY}$ has gone high.

Continuous Conversion Mode

This is the default power-up mode. The AD7790 will continuously convert, the $\overline{RDY}$ pin in the status register going low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line will also go low when a conversion is complete. To read a conversion, the user can write to the communications register, indicating that the next operation is a read of the data register. The digital conversion will be placed on the DOUT/$\overline{RDY}$ pin as soon as SCLK pulses are applied to the ADC. DOUT/$\overline{RDY}$ will return high when the conversion is read. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion or else the new conversion word will be lost.

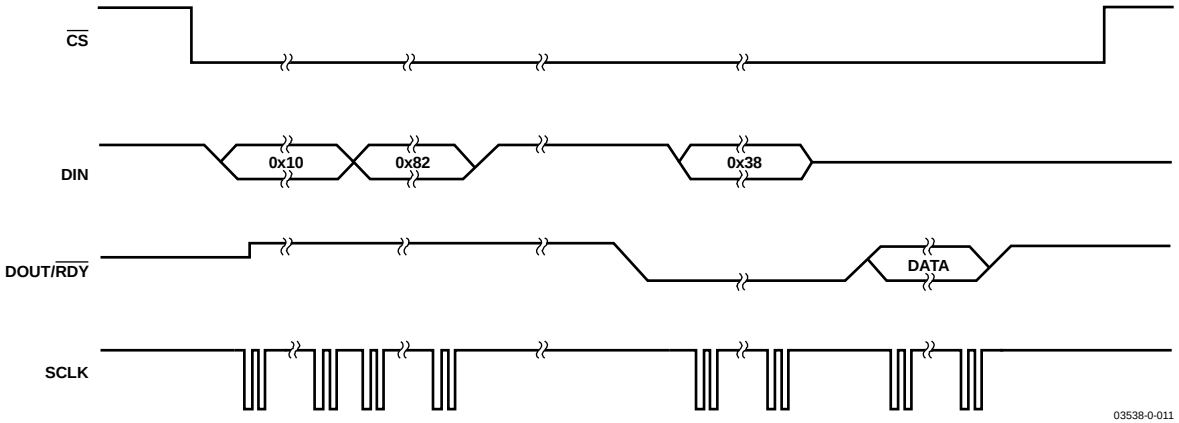


Figure 8. Single Conversion

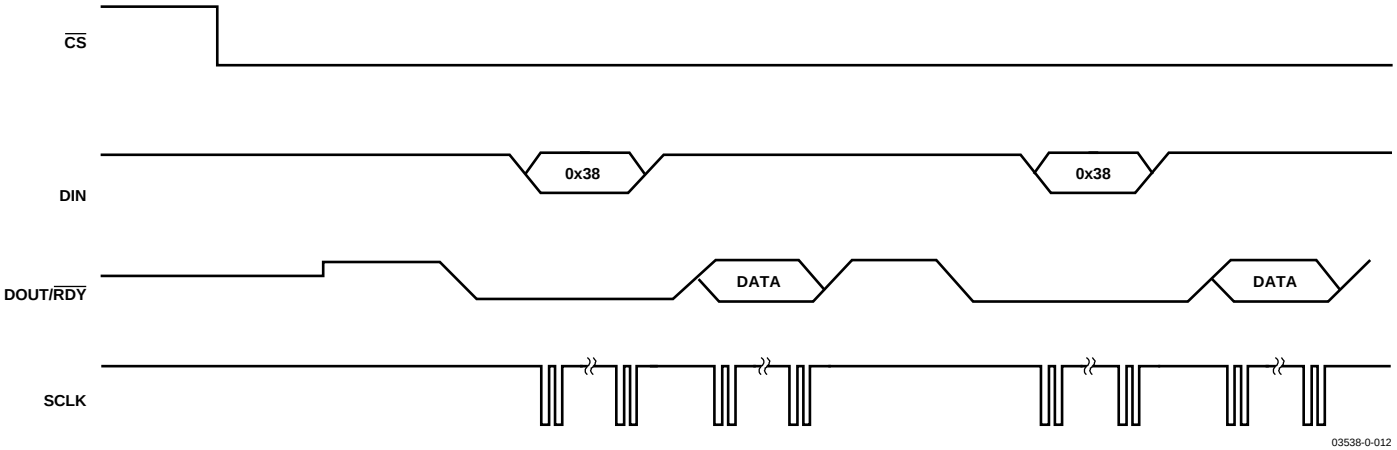


Figure 9. Continuous Conversion

Continuous Read Mode

Rather than write to the communications register each time a conversion is complete to access the data, the AD7790 can be placed in continuous read mode. By writing 001111XX to the communications register, the user only needs to apply the appropriate number of SCLK cycles to the ADC and the 16-bit word will automatically be placed on the DOUT/$\overline{\text{RDY}}$ line when a conversion is complete.

When DOUT/$\overline{\text{RDY}}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC and the data conversion will be placed on the DOUT/$\overline{\text{RDY}}$ line. When the conversion is read, DOUT/$\overline{\text{RDY}}$ will return high until the next conversion is available. In this mode, the data can be read only once. Also, the user must ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion or if insufficient serial clocks are applied to the AD7790 to read the word, the serial output register is reset when the next conversion is complete and the new conversion is placed in the output serial register.

To exit the continuous read mode, the instruction 001110XX must be written to the communications register while the $\overline{\text{RDY}}$ pin is low. While in the continuous read mode, the ADC monitors activity on the DIN line so that it can receive the instruction to exit the continuous read mode. Additionally, a reset will occur if 32 consecutive 1s are seen on DIN. Therefore, DIN should be held low in continuous read mode until an instruction is to be written to the device.

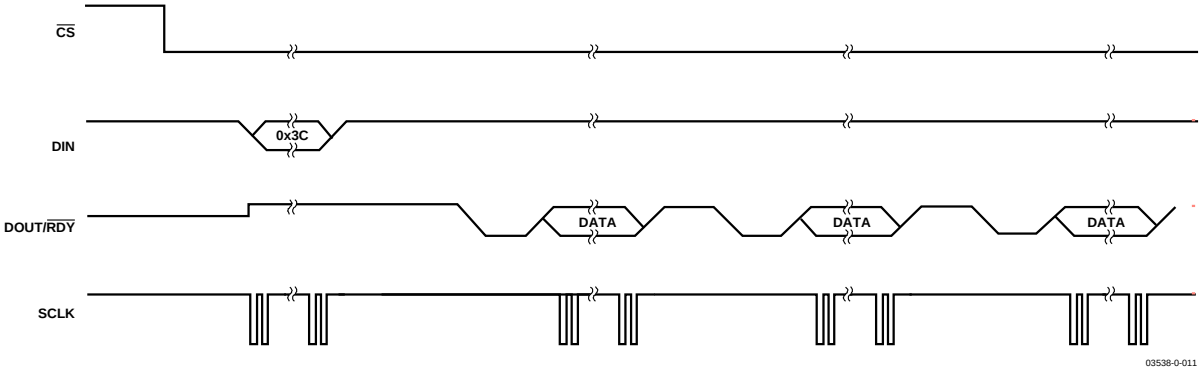


Figure 10. Continuous Read

CIRCUIT DESCRIPTION

ANALOG INPUT CHANNEL

The AD7790 has one differential analog input channel. This is connected to the on-chip buffer amplifier when the device is operated in buffered mode and directly to the modulator when the device is operated in unbuffered mode. In buffered mode (the BUF bit in the mode register is set to 1), the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant source impedances and is tailored for direct connection to external resistive-type sensors such as strain gauges or resistance temperature detectors (RTDs).

When BUF = 0, the part is operated in unbuffered mode. This results in a higher analog input current. Note that this unbuffered input path provides a dynamic load to the driving source. Therefore, resistor/capacitor combinations on the input pins can cause dc gain errors, depending on the output impedance of the source that is driving the ADC input. Table 16 shows the allowable external resistance/capacitance values for unbuffered mode such that no gain error at the 16-bit level is introduced.

Table 16. External R-C Combination for No 16-Bit Gain Error

C (pF)	R (Ω)
50	22.8K
100	13.1K
500	3.3K
1000	1.8K
5000	360

The absolute input voltage range in buffered mode is restricted to a range between GND + 100 mV and V_{DD} – 100 mV. Care must be taken in setting up the common-mode voltage so that these limits are not exceeded. Otherwise, there will be degradation in linearity and noise performance.

The absolute input voltage in unbuffered mode includes the range between GND – 30 mV and V_{DD} + 30 mV as a result of being unbuffered. The negative absolute input voltage limit does allow the possibility of monitoring small true bipolar signals with respect to GND.

PROGRAMMABLE GAIN AMPLIFIER

The output from the buffer on the ADC is applied to the input of the on-chip programmable gain amplifier (PGA). The PGA gain range is programmed via the gain bits G1 and G0 in the mode register. With an external 2.5 V reference applied, the PGA can be programmed to have a bipolar range of ±2.5 V, ±1.25 V, ±625 mV, or ±312.5 mV. These are the ranges that should appear at the input to the on-chip PGA.

BIPOLAR CONFIGURATION

The analog input to the AD7790 accepts a bipolar input voltage range. A bipolar input range does not imply that the part can tolerate negative voltages with respect to system GND. Bipolar signals on the AIN(+) input are referenced to the voltage on the AIN(–) input. For example, if AIN(–) is 2.5 V and the ADC is configured for a gain of 1, the analog input range on the AIN(+) input is 0 V to 5 V.

DATA OUTPUT CODING

The output code is offset binary with a negative full-scale voltage resulting in a code of 000...000, a zero differential input voltage resulting in a code of 100...000, and a positive full-scale input voltage resulting in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN \times GAIN/V_{REF}) + 1]$$

where *AIN* is the analog input voltage, *GAIN* is the PGA gain, and $N = 16$.

REFERENCE INPUT

The AD7790 has a fully differential input capability for the channel. The common-mode range for these differential inputs is from GND to V_{DD}. The reference input is unbuffered and, therefore, excessive R-C source impedances will introduce gain errors. The reference voltage REFIN (REFIN(+) – REFIN(–)) is 2.5 V nominal for specified operation, but the AD7790 is functional with reference voltages from 0.1 V to V_{DD}. In applications where the excitation (voltage or current) for the transducer on the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source will be removed because the application is ratiometric. If the AD7790 is used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7790 include the ADR381 and ADR391 because these are low noise, low power references. If the complete analog section is driven from a 2.5 V power supply, the reference voltage source will require some headroom. In this case, a 2.048 V reference such as the ADR380 is recommended, again low noise, low power references. Also note that the reference inputs provide a high impedance, dynamic load. Because the input impedance of each reference input is dynamic, resistor/capacitor combinations on these inputs can cause dc gain errors, depending on the output impedance of the source that is driving the reference inputs. Reference voltage sources like those recommended above (e.g., ADR391) will typically have low output impedances and are, therefore, tolerant to having decoupling capacitors on

REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor will mean that the reference input sees a significant external source impedance. External decoupling on the REFIN pins would not be recommended in this type of circuit configuration.

V_{DD} MONITOR

Along with converting external voltages, the analog input channel can be used to monitor the voltage on the V_{DD} pin. When the CH1 and CH0 bits in the communications register are set to 1, the voltage on the V_{DD} pin is internally attenuated by 5 and the resultant voltage is applied to the Σ-Δ modulator using an internal 1.17 V reference for analog to digital conversion. This is useful because variations in the power supply voltage can be monitored.

GROUNDING AND LAYOUT

Since the analog inputs and reference inputs of the ADC are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The digital filter will provide rejection of broadband noise on the power supply, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7790 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7790 is so high, and the noise levels from the AD7790 are so low, care must be taken with regard to grounding and layout.

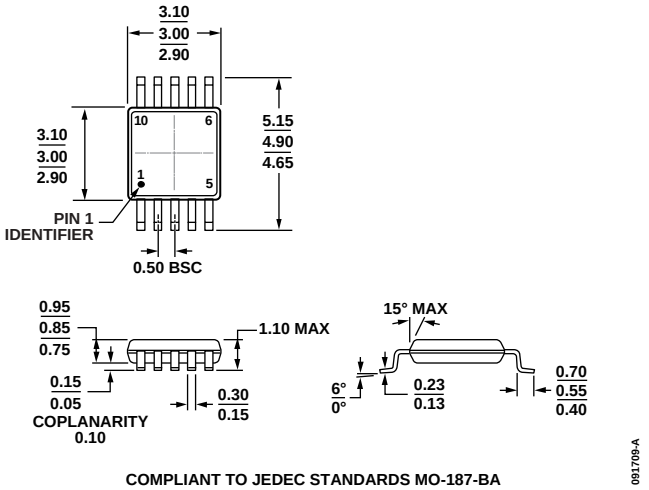
The printed circuit board that houses the AD7790 should be designed such that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it gives the best shielding.

It is recommended that the AD7790's GND pin be tied to the AGND plane of the system. In any layout, it is important that the user keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

The AD7790's ground plane should be allowed to run under the AD7790 to prevent noise coupling. The power supply lines to the AD7790 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. V_{DD} should be decoupled with 10 µF tantalum in parallel with 0.1 µF capacitors to GND. To achieve the best from these decoupling components, they should be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF ceramic capacitors to DGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 11. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD7790BRM	–40°C to +105°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	COS
AD7790BRMZ	–40°C to +105°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	COS#
AD7790BRM-REEL	–40°C to +105°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	COS
AD7790BRMZ-REEL	–40°C to +105°C	10-Lead Mini Small Outline Package (MSOP)	RM-10	COS#

[1] Z = RoHS Compliant Part.

NOTES

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9