MAX14746/MAX14747

USB Detection with Smart Power Selector Li+ Chargers

General Description

The MAX14746/MAX14747 are a series of USB charger detectors with an integrated Smart Power Selector™ linear charger solutions that provide a single-chip solution for charging and charger detection.

The MAX14746/MAX14747 charger detectors are compliant to USB Battery Charger Detection Rev 1.2* and capable of detecting multiple USB battery-charging methods, including Standard Downstream Ports (SDP), Charging Downstream Ports (CDP), and Dedicated Charger Ports (DCP). The devices also detect common proprietary charge adapters, including those from Apple.

The MAX14746/MAX14747 battery chargers feature Smart Power Selector operation, allowing operation with dead or no battery present. The devices limit USB V_{BUS} current based on the detect charger source type. If the charger power source is unable to supply the entire system load, the smart-power control circuit supplements the system load with current from the battery.

The devices protect against overvoltage faults up to 28V.

This series of USB charger detectors are available with several options, with slight variations in, for example, power-up states. These variations are noted throughout this data sheet.

There are five options available, with slight variations in, for example, power-up states (see Ordering Information). The devices are available in a 25-ball, 0.4mm pitch wafer-level package (WLP), and are specified over the -40°C to +85°C extended temperature range.

Applications

- Portable Consumer Devices
- Portable Digital Cameras
- Portable Digital Video Cameras
- Portable Industrial Devices

*Except DCD timeout extended from 900ms to 2s for the MAX14746/MAX14747.

Smart Power Selector $^{\text{TM}}$ is a trademark of Maxim Integrated Products, Inc.

Benefits and Features

- Flexible System Design to Operate with Any USB Charger Source
 - Compliant to USB Battery Charger Rev 1.2 Specification*
 - Supports Proprietary USB Charging Sources, Including Apple
 - · D+/D- Bias Voltage Supported
- Easy to Implement Li+ Battery Charging
 - · Smart Power Selector
 - Fully Compliant with Dead Battery/Weak Battery Charging According to USB 2.0 Specification
 - JEITA Charge Protection
 - · Thermal Protection
 - Internal USB D+/D- Switch to Manage Connection
- Integrates High Level of Protection
 - 28V Tolerant Input on VB
 - ±15kV Human Body Model ESD Protection on CDP and CDN

Ordering Information appears at end of data sheet.



Absolute Maximum Ratings

(All voltages referenced to GND.)
BAT, INT, THM, LED, UOK1, CTYP, IDEF, FSUS,
TDN, TDP, CDN, CDP, SYS, SCL, SDA0.3V to +6V
UOK2/EXTV _{SYS} + 0.3V
SFOUT, CAP0.3V to min ((V _{VB} + 0.3V), +6V)
VB0.3V to +30V
NVP0.3V to (V _{VB} + 0.3V)
Continuous Current into VB, BAT, SYS±3A

Continuous Current into any Other Terminal	±100mA
Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
WLP (derate 19.2mW/°C above +70°C)	1536mW
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Reflow Temperature	+260°C

Package Thermal Characteristics (Note 1)

 WLP

Junction-to-Ambient Thermal Resistance (θ_{JA})52°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

 $(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_{A} = +25^{\circ}\text{C}.)$ (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CHARACTERISTICS						
VB Input Voltage Range	V _{VB}		0		28	V
V _{BAT} Input Voltage Range	V _{BAT}		0		5.5	V
VB Detection Threshold	V	V _{VB} rising	3.8	3.9	4.1	V
VB Detection Threshold	V _{VBDET}	V _{VB} falling	3.0	3.1	3.2	V
VB Overvoltage Threshold	V _{VBOV}	V _{VB} rising	7.2	7.5	7.8	V
VB Overvoltage Hysteresis	V _{VBOV_HYS}			200		mV
VB Valid Trip Point	V _{VB_TRIP}		30	145	290	mV
VB Valid Trip Point Hysteresis	V _{VB_TP_HYS}			275		mV
VB Charger-Detection-Active Supply Current	I _{B_CDETON}	V _{BAT} = 0V, I _{SYS} = 0mA charger detection active, analog switch open			2.5	mA
VB Charger-Detection-Idle Supply Current	IB_CDCIDLE	V _{BAT} = 0V, I _{SYS} = 0mA charger detection idle, analog switch closed			2	mA
V _{CCINT} UVLO Threshold	V _{UVLO}	V _{CCINT} rising (Note 3)	1.6	2.2	2.6	V
V _{CCINT} UVLO Hysteresis	V _{UVLO_HYS}	(Note 3)		50		mV
BAT Overvoltage Threshold	V _{BATOV}	V _{BAT} rising, VB not connected	4.8	5.15	5.7	V
BAT Overvoltage Hysteresis	V _{BATOV_HYS}			100		mV
BAT UVLO Threshold	V _{BAT_UVLO}	V _{BAT} rising (Note 4)	1.9	2.05	2.2	V
BAT UVLO Hysteresis	V _{BAT_UVLOH}			50		mV

Electrical Characteristics (continued)

 $(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_{A} = +25^{\circ}\text{C}.)$ (Note 3)

PARAMETER	SYMBOL	CONI	DITIONS	MIN	TYP	MAX	UNITS
BAT Supply Current With VB	I _{BAT_NOCHG}	V _{BAT} = 4.2V, VB co	onnected,		4	8	μА
BAT Supply Current No VB	I _{BAT_NOVB}	V _{BAT} = 4.2V, VB no	ot connected		6	11	μA
CAP Regulator Voltage	V _{CAP}	V _{VB} = 5V		3.9	4.2	4.7	V
050117.0	.,	V _{VB} = 6.0V, I _{SFOU}	_T = 0mA	5.0	5.25	5.5	.,
SFOUT Regulator Voltage	V _{SFOUT}	V _{VB} = 5.0V, I _{SFOU}	_T = 15mA		4.9		V
SFOUT Overvoltage Protection Voltage	V _{SFOUT_OVP}	(Note 5)			17		V
NVP Clamp Voltage	V _{NVP}	Measured between V _{VB} > 10V	VB and NVP,	5	7	10	V
NVP Resistance	R _{NVP}	V _{VB} < 5V		120	200	300	Ω
THERMAL PROTECTION							
Thermal Shutdown Threshold	T _{SHDN_LIM}	(Note 6)			150		°C
Current Reduce Thermal Threshold	T _{CHG_LIM}	(Note 7)			120		°C
VB-TO-SYS PATH							
SYS Regulation Voltage	V _{SYS_REG}	I _{SYS} = 5mA	MAX14746	V _{BAT} _ REG ⁺ 0.14	V _{BAT} REG ⁺ 0.2	V _{BAT} _ REG ⁺ 0.26	V
			MAX14747		4.8		
VB-to-SYS Voltage Drop	V _{VB_SYS}				40		mV
VB-to-SYS On-Resistance	R _{VB_SYS}	V _{VB} = 4.4V, I _{SYS} =	400mA		160	350	mΩ
Soft-Start Input Current Time	tss_vb_sys				1		ms
		FSUS = 1			0		
		IDEF = 0, IBusLim = 11, ILimSet[2:0] =	= 1, IBusDetSw[1:0] = 000		96.5		
		IDEF = 0, IBusLim = 11, ILimSet[2:0] =	= 1, IBusDetSw[1:0] = 001		475	500	
		IDEF = 0, IBusLim = 11, ILimSet[2:0] =	= 1, IBusDetSw[1:0] = 010		633		
USB Input Current Limit	I _{LIMIT}	IDEF = 0, IBusLim = 11, ILimSet[2:0] =	= 1, IBusDetSw[1:0] = 011		737		mA
		IDEF = 0, IBusLim = 11, ILimSet[2:0] =	= 1, IBusDetSw[1:0] = 100		944		
		IDEF = 0, IBusLim = 11, ILimSet[2:0] =	= 1, IBusDetSw[1:0] = 101		1048		
		IDEF = 0, IBusLim = 11, ILimSet[2:0] =	= 1, IBusDetSw[1:0] = 110		1570		
		IDEF = 0, IBusLim = 11, ILimSet[2:0] =	= 1, IBusDetSw[1:0] = 111		1885		-

Electrical Characteristics (continued)

 $(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_{A} = +25^{\circ}\text{C}.)$ (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER PATH						
BAT to SYS On-Resistance	D	V _{BAT} = 5V, I _{BAT} = 400mA		40	80	mΩ
DAT to 313 Off-Nesistance	R _{BAT_SYS}	V _{BAT} = 1.9V, I _{BAT} = 100mA		83		11152
BAT to SYS Switch-On Threshold	V _{BAT_SYS_ON}	V _{SYS} falling	10	22	35	mV
BAT to SYS Switch-Off Threshold	V _{BAT_SYS_OFF}	V _{SYS} rising	-3	-1.5	0	mV
		SysMin[2:0] = 000, V _{BAT} > 3.6V		V _{BAT} + 0.1		
		SysMin[2:0] = 000, V _{BAT} < 3.4V		3.6		
		SysMin[2:0] = 001, V _{BAT} < 3.4V		3.7		
SYS Charger Current-	.,	SysMin[2:0] = 010, V _{BAT} < 3.4V		3.8		
Limiting Threshold Voltage	V _{SYS_LIM}	SysMin[2:0] = 011, V _{BAT} < 3.4V		3.9		
		SysMin[2:0] =100, V _{BAT} < 3.4V	3.86	4	4.14	
		SysMin[2:0] =101, V _{BAT} < 3.4V		4.1		
		SysMin[2:0] =110, V _{BAT} < 3.4V		4.2		
		SysMin[2:0] =111, V _{BAT} < 3.4V		4.3		
Charger Current Soft-Start Time				1		ms
BATTERY CHARGER LEVELS						
		IPChg[1:0] = 00		30		
Precharge Current	I _{PCHG}	IPChg[1:0] = 01		50		mA
3	1 0110	IPChg[1:0] = 10		70		_
		PChg[1:0] = 11		100		
		VPChg = 0, VPChgLow[1:0] = 00, V _{BAT} rising		2.15		_
		VPChg = 0, VPChgLow[1:0] = 01, V _{BAT} rising	2.15	2.25	2.35	
		VPChg = 0, VPChgLow[1:0] = 10, V _{BAT} rising		2.35		
Prequalification Threshold	V _{BAT_PCHG}	VPChg = 0, VPChgLow[1:0] = 11, V _{BAT} rising		2.45		V
1. Toqualiloudion Tilloonolu	*BAI_PCHG	VPChg = 1, VPChgHigh[1:0] = 00, V _{BAT} rising		2.7		
		VPChg = 1, VPChgHigh[1:0] = 01, V _{BAT} rising	2.70	2.80	2.90	1
		VPChg = 1, VPChgHigh[1:0] = 10, V _{BAT} rising		2.9		
		VPChg = 1, VPChgHigh[1:0] = 11, V _{BAT} rising		3		1
Prequalification Threshold Hysteresis	V _{BAT_PCHG_HYS}			100		mV

Electrical Characteristics (continued)

 $(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_{A} = +25^{\circ}\text{C}.)$ (Note 3)

PARAMETER	SYMBOL	CONI	DITIONS	MIN	TYP	MAX	UNITS	
		IFChg[2:0] = 000			700			
		IFChg[2:0] = 001 300				1		
		IFChg[2:0] = 010		180	200	220		
BAT Charge Current Set		IFChg[2:0] = 011			600			
Range	IFCHG	IFChg[2:0] = 100			800		mA	
		IFChg[2:0] = 101			900		1	
		IFChg[2:0] = 110			350			
		IFChg[2:0] = 111			450			
		ChgDone[2:0] = 00	0		10			
		ChgDone[2:0] = 00	1		20			
		ChgDone[2:0] =			40			
		010	TA = 0°C to +60°C	30		50		
Charge Done Qualification	I _{CHG_DONE}	ChgDone[2:0] = 01	1		50		mA	
		ChgDone[2:0] = 100			60			
		ChgDone[2:0] = 101			80			
		ChgDone[2:0] = 11	0		100			
		ChgDone[2:0] = 11	1		120			
		BatRegSel = 0, Ba	tRegLow[1:0] = "00"		4.05			
		BatRegSel = 0, Ba	tRegLow[1:0] = "01"		4.1			
		BatRegSel = 0, Ba	tRegLow[1:0] = "10"		4.15			
		BatRegSel = 0, Bat T _A =+25°C	tRegLow[1:0] = "11",	4.179	4.2	4.221		
		BatRegSel = 0, Bat T _A =-40°C to +85°C	tRegLow[1:0] = "11",	4.158	4.2	4.242		
BAT Regulation Voltage	V _{BAT_REG}	BatRegSel = 1, Ba	tRegHi[2:0] = "000"		4.25		V	
		BatRegSel = 1, Ba	tRegHi[2:0] = "001"	= "001" 4.3			1	
		BatRegSel = 1, Ba	tRegHi[2:0] = "010"		4.35			
		BatRegSel = 1, Ba	tRegHi[2:0] = "011"		4.4			
		BatRegSel = 1, Ba	tRegHi[2:0] = "100"		4.45			
		BatRegSel = 1, Ba	tRegHi[2:0] = "101"		4.5			
		BatRegSel = 1, Ba	tRegHi[2:0] = "110"		4.55		1	
		BatRegSel = 1, Ba	tRegHi[2:0] = "111"		4.6			

 $(V_{VB} = 5.0V, V_{BAT} = 4.2V, T_{A} = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.}$ Typical values are at $V_{BAT} = 3.6V, V_{VB} = 5.0V, V_{SYS} = V_{SYS_REG}, T_{A} = +25^{\circ}\text{C}.)$ (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN TYP	MAX	UNITS
		BatReChg[1:0] = 00	50		
DAT Dashanna Thuashald		BatReChg[1:0] = 01	100		
BAT Recharge Threshold	V _{BAT_RECHG}	BatReChg[1:0] = 10	150		mV
		BatReChg[1:0] = 11	200		
BATTERY CHARGER TIMING					•
		PChgTmr[1:0] = 00	30		
Maximum Prequalification		PChgTmr[1:0] = 01	60		Minutes
Time	t _{PCHG}	PChgTmr[1:0] = 10	120		Minutes
		PChgTmr[1:0] = 11	240		
		FChgTmr[1:0] = 00	75		
Mavimum Fast Charge Time		FChgTmr[1:0] = 01	150		Minutes
Maximum Fast-Charge Time	t _{FCHG}	FChgTmr[1:0] = 10	300		Minutes
		FChgTmr[1:0] = 11	600		
	tтоснg	MtChgTmr[1:0] = 00	30		
Maintain Channa Tina		MtChgTmr[1:0] = 01	15		Minutes
Maintain-Charge Time		MtChgTmr[1:0] = 10	0		Minutes
		MtChgTmr[1:0] = 11	60		
Charge-Timer Accuracy	osc		-10	+10	%
Charge-Timer Extend Threshold	IFC_HALF	Charge current reduced due to overcurrent or overtemperature condition (Note 10)	50		%I _{FCHG}
Charge-Timer Suspend Threshold	I _{FC_FIFTH}	Charge current reduced due to overcurrent or overtemperature condition (Note 10)	20		%I _{FCHG}
BATTERY DETECTION		,			- 1
		BatDetCntl = 0, V _{BAT} > V _{BAT_UVLO}	61		ms
V _{VB} Rising to Battery Detection Valid Delay	t _{BUS_BATDET}	BatDetCntl = 0, V _{BAT} < V _{BAT_UVLO}	1.031		s
tion valid Delay	_	BatDetCntl = 1	46		ms
V _{BAT} Falling to BatDet		BatDetCntl = 0	1.015		s
Update Delay	tBATDET_F	BatDetCntl = 1	15		ms
		BatDetCntl = 0, V _{BAT} > V _{BAT UVLO}	1.03		_
V _{BAT} Rising to BatDet	t _{BATDET_R}	BatDetCntl = 0, V _{BAT} < V _{BAT_UVLO}	1.015		s
Update Delay	_	BatDetCntl = 1	15		ms

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PARAMETER	SYMBOL	CC	ONDITIONS	MIN	TYP	MAX	UNITS
JEITA BATTERY PACK MONIT	OR AND NTC DE	TECTION		·			
THM Hot Threshold		Vfalling	MAX14746		23.8		0/ \/
THIN HOL THIESHOID	T ₄	V _{THM} falling	MAX14747		19		%V _{CAP}
THM Warm Threshold	T ₃	V _{THM} falling	MAX14746		33.7		%V _{CAP}
Triwi wariii Triiesiioid	13	V I HM railing	MAX14747		30		70 V CAP
THM Cool Threshold	T ₂	V _{THM} rising	MAX14746		63.3		%V _{CAP}
Triwi Cool Triiconola	12	V I HIM Homig	MAX14747		66.75		70 V CAP
THM Cold Threshold	T ₁	V _{THM} rising	MAX14746		72.3		%V _{CAP}
	- 1	- 1111019	MAX14747		77.2		
THM Disable Threshold	T _{HMDIS}	V _{THM} rising			96.6		%V _{CAP}
THM Threshold Hysteresis	T _{HMHYS}				60		mV
THM Input Leakage Current	I _{LTHM}			-1		+1	μA
THM Detection Time	t _{THM}				15		ms
CHARGER STATUS OUTPUT	(LED)						
Output Logic-Low Voltage	V _{OLED}	I _{SINK} = 10mA			35	100	mV
Temperature Suspend Mode Blink Period	t _{TSUS}	Blinking with 50 ⁴	% duty cycle		1.5		s
Timeout Mode Blink Period	tтімоит	Blinking with 50°	% duty cycle		0.15		s
Pulse Time for Fresh Battery Insertion					1		s
IMPEDANCE-MODE BATTERY	DETECTION			·			
Discharge Current	I _{DIS}	V _{BAT} = 3.6V		6	10	14	mA
Replace Current	I _{RPL}	V _{BAT} = 3.6V, V _S	YS > 4.0V	6	10	14	mA
Test Current Mismatch	I _{DR_MIS}			-15		+15	%
Discharge Replace Time	t _{DIS_RPL}	V _{BAT} = 3.6V			15		ms

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER DETECTION						
V _{DP_SRC} Voltage	V _{DP_SRC}	I _{LOAD} = 0 to 200μA	0.5	0.6	0.7	V
V _{DAT_REF} Voltage	V _{DAT_REF}		0.25	0.3	0.35	V
V _{LGC} Voltage	V _{LGC}		1.15	1.24	1.5	V
I _{DM_SINK} Current	I _{DM_SINK}	V _{OUT} = 0.15V to 3.6V	50	80	110	μA
I _{DP_SRC} Current	I _{DP_SRC}	V _{OUT} = 0V to 2.5V	5.5	8.4	10	μA
R _{DM_DWN}	R_{DM_DWN}		14.25	20	24.8	kΩ
I _{WEAK} Current	I _{WEAK}		0.01	0.1	0.3	μA
25% Resistor-Divider Ratio	R ₂₅		22.5	25	27.5	%
47% Resistor-Divider Ratio	R ₄₇		43.3	47	51.7	%
71% Resistor-Divider Ratio	R ₇₁		69.5	71.6	73.5	%
USB Charger Detect Time	t _{DPSRC_ON}		40		60	ms
V _{BUS} Debounce Time	t _{MDEB}		20	30	40	ms
DCD Debounce	tDCD_DEB		36	40	44	ms
DCD Timeout	t _{DCD_TO}			2000		ms
USB ANALOG SWITCH PERFO	RMANCE (TDN/	TDP)				
Analog-Signal Range	V _{TDN} V _{TDP}		0		V _{CCINT}	V
On-Resistance	R _{ONUSB}	V _{BAT} = 3.0V, I _{CDN} , I _{CDP} = 10mA, V _{CDN} , V _{CDP} = 0 to 3.0V		3	6	Ω
On-Resistance Match Between Channels	DR _{ONUSB}	V _{BAT} = 3.0V, I _{CDN} , I _{CDP} = 10mA, V _{CDN} , V _{CDP} = 400mV			0.5	Ω
On-Resistance Flatness	R _{FLATUSB}	V _{BAT} = 3.0V, I _{CDN} , I _{CDP} = 10mA, V _{CDN} , V _{CDP} = 0 to 3V		0.3	1	Ω
Off-Leakage Current	I _{LUSB_OFF}	Switch open, $V_{TDN}/V_{TDP} = 0.3V/2.5V$, $V_{CDP}/V_{CDN} = 2.5V/0.3V$	-360		+360	nA
On-Leakage Current	I _{LUSB_ON}	Switch closed, $V_{TDN}/V_{TDP}/V_{CDN}/V_{CDP} = 0.3V/2.5V$	-360		+360	nA
Analog Switch Turn-On Time	t _{ON}	I^2 C stop to switch on, R_L = 50Ω		0.5	1	ms
Analog Switch Turn-Off Time	t _{OFF}	I^2 C stop to switch on, R_L = 50Ω		0.1	1	ms
On-Capacitance	C _{ON}	V _{IN} = 0.5V _{P-P} DC = 0V, f = 240MHz		6		pF
Off-Capacitance	C _{OFF}	V _{IN} = 0.5V _{P-P} DC = 0V, f = 240MHz		3.5		pF

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Off-Isolation	V _{ISO}	$R_S = R_L = 50\Omega$, $f = 20kHz$, $V_{IN} = 0.5V_{P-P}$		-60		dB
DIGITAL INPUTS/OUTPUTS (ID	EF, CTYP, INT, U	JOK_, FSUS)				
Input Logic High-Voltage	V _{IH}		1.4			V
Input Logic Low-Voltage	V _{IL}				0.4	V
Leakage Current	I _{LEAK}	CTYP, INT, UOK_ only	-250		+250	nA
Open-Drain Output Logic-Low	V _{ODOL}				0.4	V
STARTUP TIMINGS						
VB to SYS Rise		IBusLim = 0, FSUSMsK = 0, IDEF = 0		205		ms
VB to SFOUT Rise		SFoutAsrt = 0		205		ms
VB to CTYP Falling Edge				205		ms
CTYP to UOK1 Falling Edge	tsys_uok1_f			5.5		ms
UOK1 to UOK2 Falling Edge Delay	tuok1_uok2	If UOK2 option enabled		400		ms
I ² C TIMING SPECIFICATIONS	(FIGURE 1)					
I ² C Maximum Clock Frequency	f _{SCL}			400		kHz
Bus Free Time Between STOP and START Conditions	t _{BUF}		1.3			μs
START Condition Setup Time	t _{SU:STA}		0.6			μs
Repeated Start Condition Setup Time	t _{SU:STA}		0.6			μs
START Condition Hold Time	thd:sta		0.6			μs
STOP Condition Setup Time	t _{SU:STO}		0.6			μs
Clock Low Period	t _{LOW}		1.3			μs
Clock High Period	t _{HIGH}		0.6			μs
Data Valid to SCL Rise Time	t _{SU:DAT}	Write-setup time	100			ns
Data Hold Time to SCL Fall	t _{HD:DAT}	Write-hold time	0			ns
SCL, SDA Spike Suppression	t _{SP}	Duration of spike on SCL and SDA that is not detected as a valid edge		50		ns
PROTECTION SPECIFICATION	IS					
		Human Body Model		±15		
ESD Protection, CDP/CDN		IEC61000-4-2 Air Gap		±4		kV
		IEC61000-4-2 Contact		±5		
ESD Protection, All Other Pins		Human Body Model		±2		kV

- Note 2: All units are production tested at +25°C. Specifications over temperature are guaranteed by design.
- $V_{CCINT} = V_{CAP}$ (if CAP is present) or V_{BAT} (if CAP is not present). Note 3:
- Note 4: Threshold is valid when V_{VBDET} < V_{VB} < V_{VBOV}. When V_{SYS} < V_{BAT UVLO}, the BAT-SYS switch opens and BAT is connected to SYS through a diode.
- When $V_{VB} > V_{SFOUT_OVP}$, SFOUT LDO turns off. Note 5:
- Note 6: When the die temperature exceeds T_{SFOUT_TLIM}, SFOUT regulator and SYS limiter turns off. V_{SYS} is supplied by V_{BAT}.
- Note 7: When the die temperature exceeds T_{CHG} LIM, charger current starts to reduce.

 Note 8: V_{SYS}_LIM is the SYS voltage below which the charger starts to limit the charging current.
- Note 9: When V_{SYS} drops below V_{SYS} HLD, the battery charger does not move to the maintain charge state.
- Note 10: The charge timer extend threshold is the charge current level below which the charge timer clock runs at half speed. The charge timer suspend threshold is the charge current level below which the charge timer clock is paused.

Timing Diagram

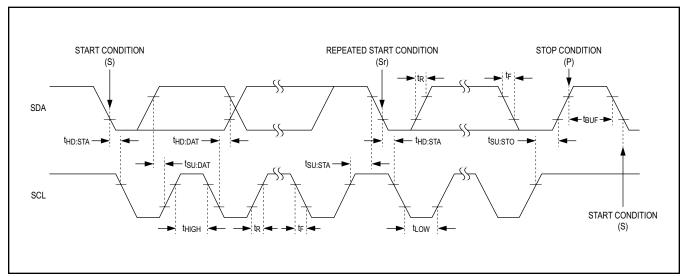
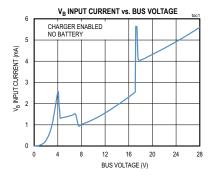


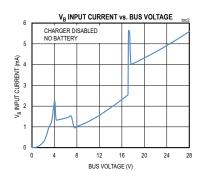
Figure 1. I²C Timing Diagram

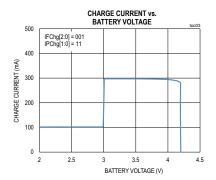
Maxim Integrated | 10 www.maximintegrated.com

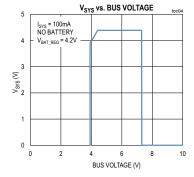
Typical Operating Characteristics

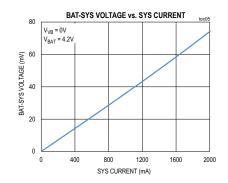
 $(V_{BAT} = 3.6V, V_{VB} = 5V, T_{A} = +25^{\circ}C, \text{ unless otherwise noted.})$

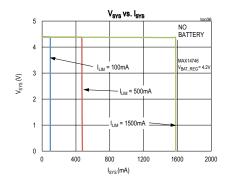


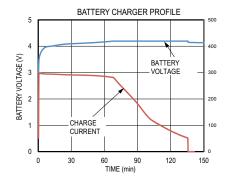


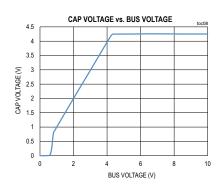






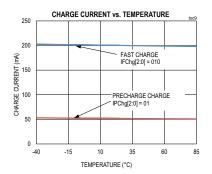


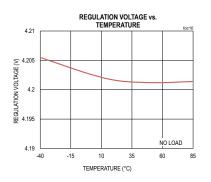


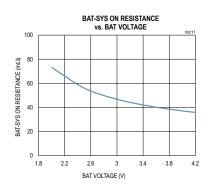


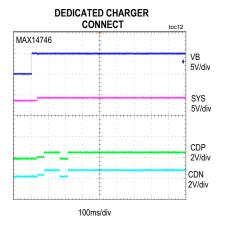
Typical Operating Characteristics (continued)

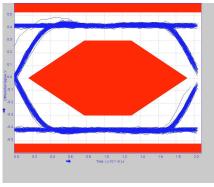
 $(V_{BAT} = 3.6V, V_{VB} = 5V, T_{A} = +25^{\circ}C, \text{ unless otherwise noted.})$

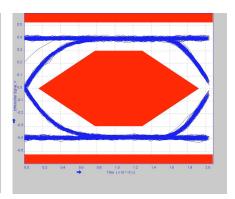


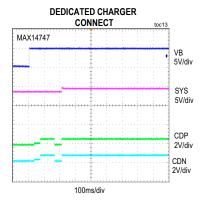


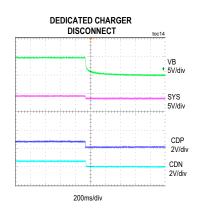






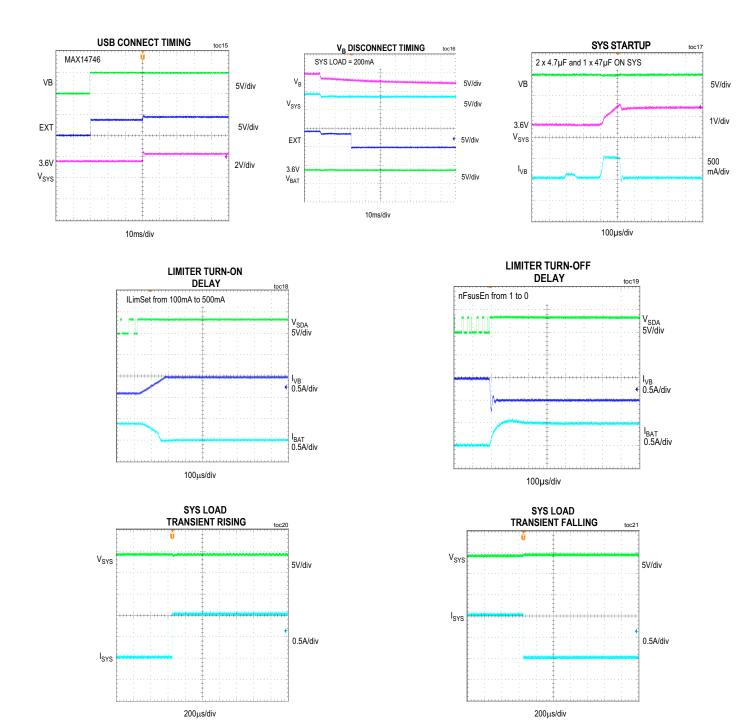




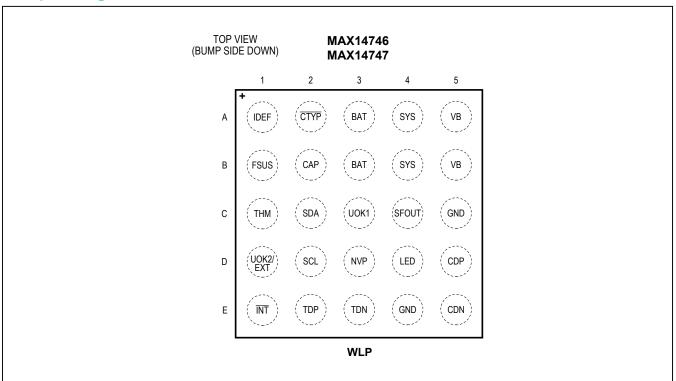


Typical Operating Characteristics (continued)

 $(V_{BAT} = 3.6V, V_{VB} = 5V, T_A = +25^{\circ}C, \text{ unless otherwise noted.})$



Bump Configuration



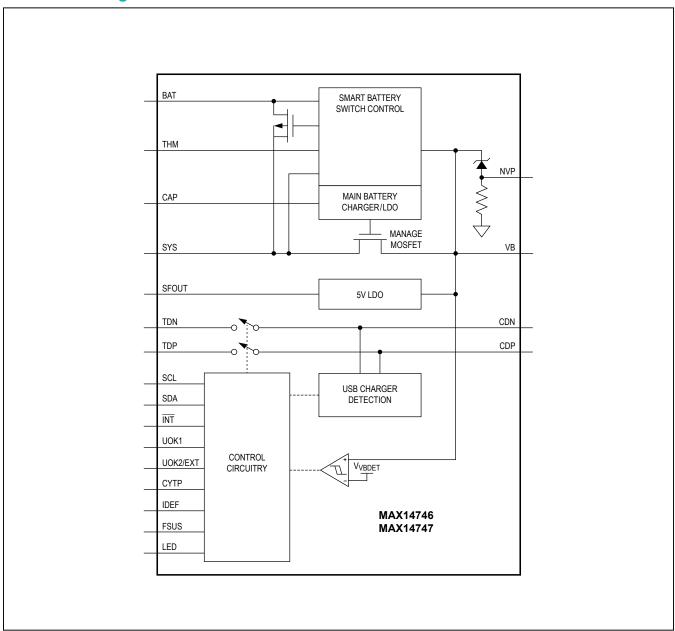
Bump Descriptions

BUMP	NAME	FUNCTION
A1	IDEF	Current-Limit Setting Input. IDEF has an internal $470k\Omega$ pulldown resistor to GND. IDEF is only active if FSUSMsk bit is set to 0 and FSUS is LOW 0 = Input current limit determined by I ² C settings (IBusLim, ILimSet, IBusDetSw bits) 1 = Input current limit set to 100mA
A2	CTYP	Charger Type Output. CTYP is an open-drain output that asserts when DCP, CDP, or Apple 2A adapter is detected.
A3, B3	BAT	Battery Connection. Connect a single-cell Li+ battery from BAT to GND. Connect a capacitor from BAT to GND with a minimum value of 10µF and a maximum value of 30µF.
A4, B4	SYS	System Load Connection. Connect SYS to the system load. Bypass SYS with a $10\mu F$ low-ESR ceramic capacitor to GND as close as possible to the device. Connect $50\mu F$ additional capacitance to GND away from the device.
A5, B5	VB	USB V_{BUS} Input. VB is the input for the overvoltage protector. VB is monitored to detect the presence of a USB input power supply. Bypass VB with a 1µF ceramic capacitor to GND as close as possible to the device.
B1	FSUS	Force-Suspend Enable Input. FSUS is only active if the FSUSMsk bit is set to 0. FSUS has a 470kΩ pulldown resistor to GND. 0 = Current limit determined by IDEF/I ² C configuration 1 = Input current limit is forced to 0

Bump Description (continued)

ВИМР	NAME	FUNCTION
B2	CAP	Internal LDO Bypass Connection. Connect a 1µF ceramic capacitor from CAP to GND as close as possible to the device. Connect the pullup resistor for the battery thermistor output (THM) to CAP. Ensure that the total load current out of CAP is less than 2mA.
C1	THM	Battery Temperature Thermistor Measurement Input
C2	SDA	I ² C Serial Data Input/Output. Connect an external pullup resistor on SDA to the logic supply voltage.
C3	UOK1	SYS Voltage Valid and Battery Detect Output. UOK1 is an open-drain output.
C4	SFOUT	Protected LDO Output. SFOUT is powered from VB. Bypass SFOUT with a 1µF ceramic capacitor to GND as close as possible to the device. SFOUT can power the on-board USB 2.0 Hi-Speed host.
C5, E4	GND	Ground
D1	UOK2/EXT	UOK2: Delayed SYS Voltage Valid and Battery-Detect Output. UOK2 is an open-drain output. EXT: Push-Pull Output Control for External SYS-BAT pMOS Switch. Output pulled high to BAT when the charger is not present.
D2	SCL	I ² C Serial Clock Input. Connect an external pullup resistor on SCL to the logic supply voltage.
D3	NVP	Gate Bias and Protection for External PFET. NVP protects VB from negative voltages. Leave unconnected if not used.
D4	LED	Charging Fault Indicator. LED is an open-drain output that indicates a battery charging fault. When a JEITA temperature fault is detected, LED is pulsed at 50% duty cycle with a period of 1.5s. When a charge timer fault is detected, or the BAT overvoltage threshold (V _{BATOV}) is exceeded, LED is pulsed at 50% duty cycle with a period of 0.15s. Connect LED to GND if unused.
D5	CDP	USB Connector D+ Input
E1	INT	Interrupt Output. INT is an open-drain output that asserts whenever an unmasked interrupt occurs. Connect an external pullup resistor on INT to the logic supply voltage.
E2	TDP	USB Transceiver D+ Connection. Connect TDP to device microprocessor USB transceiver D+ line.
E3	TDN	USB Transceiver D- Connection. Connect TDN to device microprocessor USB transceiver D- line.
E5	CDN	USB Connector D- Input

Functional Diagram



MAX14746/MAX14747

USB Detection with Smart Power Selector Li+ Chargers

Detailed Description

The MAX14746/MAX14747 charger detector solutions integrate a smart-power selector with a linear charger that allows charging a Li+ battery and a powering system to load off the same USB power source. When the USB power source is not present or cannot provide enough power, the Li+ battery helps power the system. The devices protect against voltage faults and transients on VB up to 28V without interrupting operation.

The MAX14746/MAX14747 are compliant to USB Battery Charger Detection Rev 1.2* as well, as special chargers that bias the D+/D- lines. The devices limit VB input current based on the type of charging device that is detected and two digital inputs (IDEF and FSUS).

The devices monitor overcurrent and overtemperature faults and automatically manages the charger. Configurable interrupts and status information allow the system microcontroller to intervene.

Negative Voltage Protection

The MAX14746/MAX14747 feature a gate protection circuit for an external PFET that protects against negative voltages on V_{BUS}. The NVP output has a resistor to GND and a voltage clamp for the gate of the PFET. The voltage clamp limits the gate-to-source voltage to 7.0V (typ) when the V_{BUS} voltage is positive. If a negative voltage is present on V_{BUS}, e.g., by a backwards connector, then the PFET turns off and provides negative voltage protection. This negative voltage protection requires that a device downstream from the MAX14746/MAX14747 provide reverse-current blocking on V_{BUS}. This is required to allow the PFET to turn off. When the drain of the PFET is negative, current flows out of VB. If this reverse current is limited to a small value, V_{VB} drops and the PFET gate-to-source voltage will drop below the threshold voltage.

Supply Voltage Selector

The MAX14746/MAX14747 select their power source themselves by monitoring the voltages at VB and BAT. The devices select V_{VB} when it is present; otherwise, V_{BAT} .

Smart Power Selector

The MAX14746/MAX14747 feature circuitry that seamlessly distributes power between the USB power supply input on VB, the battery on BAT, and system load on SYS when both an external charger adaptor and a battery are connected.

*Except DCD timeout extended from 900ms to 2s for the MAX14746/MAX14747.

When the system load requirements are less than the input current limit, residual power from the input charges the battery. When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load. When the battery is connected and there is no external power input, the battery powers the system. When an external power input is connected and the battery is discharged or not present, VB powers the system.

USB Charger Detection

The MAX14746/MAX14747 charger detection circuitry support full USB Battery Charger Rev 1.2* detection. The devices detect all charger types, including standard USB ports, charging downstream ports (CDPs), and dedicated chargers. The devices also support Apple power adaptors with resistor dividers on the D+/D- pins at 500mA, 1000mA, and 2000mA current levels. See Charger Detection Timing Diagram.

System Load Switch

The MAX14746/MAX14747 feature an internal MOSFET that connect SYS to BAT for the battery to provide power to the system load. If the USB supply is at the current limit, the devices enable the switch to prevent the system voltage from falling below the battery voltage by supplying extra current from the battery. The battery is not charged if the system load continuously exceeds the input current limit, so this feature is useful for handling loads that are nominally below the input current limit but have high-current peaks exceeding the input current limit. The system uses battery energy during these peaks, but VB charges the battery at all other times.

External System Load Switch

The UOK2/EXT pin can be configured to function as a control signal for an external system load switch.

When the EXT functionality is enabled, the UOK2/EXT pin can drive the gate of an external PMOS connected between SYS and BAT.

When a valid VB voltage is present, EXT is pulled up to V_{SYS} . When VB is disconnected and V_{SYS} is equal to V_{BAT} , the EXT pin is driven to GND. This feature provides an extremely low-impedance SYS-BAT connection.

Input-Current Limiter

The input-current limiter distributes power from the external USB supply to the system load and battery charger. The input current limiter consists of a MOSFET bulk management to optimize the use of available power.

Invalid VB Voltage Protection

The MAX14746/MAX14747 enter overvoltage lockout (OVL) if V_{VB} is above the overvoltage threshold. OVL protects the device and downstream circuitry from high-voltage stress up to 28V. The internal circuit remains powered, the charger turns off, the system load switch closes, and an interrupt triggers during OVL. V_{VB} is also invalid if it is less than V_{BAT} or less than the USB undervoltage threshold. The device takes the same actions as OVL while V_{VB} is invalid.

VB Input Current Limit

The device limits VB input current to prevent input overload. Three methods can set the input current limit:

- a) Set the current limit automatically based on the capabilities of the source as indicated by the ChgTyp [3.0] value read from I²C (register 0x02).
- b) Set the current limit manually over I2C.
- c) Set the current limit manually using the IDEF and/ or FSUS inputs.

Thermal Limiting

If the local temperature exceeds 120°C (typ), the MAX14746/MAX14747 attempt to limit temperature increase by reducing the input current from VB. The system load has priority over charger current, so the device lowers the charge current to reduce overall input current. If the temperature continues to rise and reaches 150°C (typ), the device disconnects VB and the battery powers the entire system load.

Adaptive Battery Charging

The battery charger draws power from SYS while VB powers the system. The device reduces charge current to prevent V_{SYS} from falling if the total load exceeds the input current limit.

JEITA Compliant Battery Protection/ Charging

The MAX14746/MAX14747 monitor the temperature of the battery for safe charging of Li+ batteries according to JEITA standards. The devices measure the battery pack temperature by using a resistor divider formed by a pullup resistor connected to CAP and the battery pack thermistor. The external pullup allows matching to different thermistor nominal values. The JEITA circuitry supports thermistors with different β values, but the value must be fixed to choose the CAP pullup resistor. Typical $\boldsymbol{\beta}$ values are 4250 (MAX14747) and 3380 (MAX14746). The THM input measures the voltage across the resistor divider. There are five temperature zones of operation and the charger termination voltage is controlled based on the pack temperature. The charger is automatically controlled and the active current temperture zone can be read from the JEITAStat[3:0] bits over I2C (register 0x03).

Register Map and Descriptions

F		BIT5	1 1	BIT4	BIT3	BIT2	BIT1	BIT0
0x00 R					Chip_Id[7:0]			
0x01 R)	Chip_Rev[7:0]			
0x02 R ChgTyp[3:0]	ChgTyp[3:0	0:6]]		BatDet		ChgStat[2:0]	:0]
0x03 R VLim Lim U		n	UsbOVP	SysBatV	UsbOk		JeitaStat[2:0]	::0]
0x04 R RFU RFU	RFU		RFU	RFU	ThrmSd	ChgTReg	DCDTmr	ChgTmo
0x05 CoR ChgTypInt UsbOVPInt S		S	SysBatVInt	RFU	BatDetInt	ChgStatInt	ChgTRegInt	ChgTmoInt
0x06 CoR VLimInt DCDTmrInt	DCDTmrlnt		lLimInt	ThrmSdInt	UsbOkInt	JeitaStatInt	JeitaHighTInt	JeitaTSdInt
0x07 R/W ChgTypIntM UsbOVPIntM Sy	UsbOVPIntM		SysBatVIntM	RFU	BatDetIntM	ChgStatIntM	ChgTRegIntM	ChgTmoIntM
0x08 R/W VLimIntM DCDTmrIntM	DCDTmrlntM		LimIntM	ThrmSdIntM	UsbOkIntM	JeitaStatIntM	JeitaHighTIntM	JeitaTSdIntM
0x09 R/W RFU RFU			nFsusEn	FSUSMsk	RFU	RFU	DCDEn	RFU
0x0A R/W IBusLim RFU	RFU		RFU		ILimSet[2:0]		sngl	IBusDetSw[2:0]
0x0B R/W RFU RFU	RFU		RFU		IFChg[2:0]		RFU	RFU
0x0C R/W JeitaEn BatUOKMsk Ba		Bé	BatDetCntl	ChgEn	RFU		ChgDone[2:0]	2:0]
0x0D R/W RFU RFU	RFU		MtChg	MtChgTmr[1:0]	FChgTmr[1:0]	nr[1:0]	PC	PChgTmr[1:0]
0x0E R/W BatReChg[1:0]	Chg[1:0]		BatRegl	BatRegLow[1:0]	BatRegSel		BatRegHi[2:0]	2:0]
0x0F R/W RFU RFU	RFU		RFU	RFU	RFU	RFU	RFU	RFU
0x10 R/W VPChg IPChg[1:0]	IPChg[1:	=	0]	VPChg	VPChgLow[1:0]	VPChg	VPChgHigh[1:0]	BatDetChgM
0x11 R/W SFOutOrd SFOutAsrt	SFOutAsrt		AnSwC	AnSwCntl[1:0]	ChgTypMan	ChgAutoStart	BatDetChgEn	UsbCompl
0x12 R/W ChgAutoStp SFOutData			RFU	RFU		SysMin[2:0]		RFU
0x13 R					ILimMon[7:0]			

RFU = Reserved for future use. Do not change from default value.

^{**} Register resets to default value on VB rising edge.

Chip ID Register

ADDRESS:	0x00										
MODE:	Read Only										
BIT	7	6	5	4	3	2	1	0			
NAME				Chip_	Id[7:0]			•			
RESET		SEE TABLE 4									
Chip_ld[7:0]	The Chip_ld[[7:0] bits show	information ab	out the versior	of the MAX14	1746/MAX1474	7.				

Chip Revision Register

ADDRESS:	0x01									
MODE:	Read Only									
BIT	7	6	5	4	3	2	1	0		
NAME		Chip_Rev[7:0]								
RESET				SEE T	ABLE 4					
Chip_Rev[7:0]	The Chip_Re	ev[7:0] bits sh	ow information	about the revi	sion of the MA	X14746/MAX1	4747 silicon.			

Status A Register

ADDRESS:		0x02						
MODE:		Read Only						
BIT	7	6	5	4	3	2	1	0
NAME		ChgTy	/p[3:0]		BatDet		ChgStat[2:0]]
RESET				SEE T	ABLE 4			
ChgTyp[3:0]	0000 = Nothi 0001 = SDP. 0010 = CDP. 0011 = DCP. 0100 = Apple 0101 = Apple 0110 = Apple 0111 = Non-s current limit i	ing attached. In automatic n In automatic n In automatic n e 500mA charge 1A charger. In 2A charger. In standard charg s set to 0mA. r charger (D+/I	node, the curr node, the curr node, the curr er. In automati n automatic m a automatic m er (D+/D- > 0.	rent limit is set to rent limit is set to rent limit is set to rent limit is set to rent limit is set to tic mode, the curren ode, the curren ode, the curren ode, the curren ode, the curren ode, the curren ode, the curren	o 500mA (Or 10 o 1.5A. o 1.5A. o 1.5A. urrent limit is set to stimit is se	00mA if UsbCott to 500mA 500mA. 1.5A. a PS2 adapto	er). In automat	
BatDet	BatDet indica 0 = No batter 1 = Battery d	ry detected.	of the battery	detection wher	NB is present			
ChgStat[2:0]	000 = Charg 001 = Charg 010 = Precha 011 = Fast cl 100 = Fast c 101 = Mainta 110 = Mainta	er off. ing suspended arge in progres harge in progre	due to overte s. ess using cons ess using cons ogress. r done.	of the battery of emperature. stant-current mo stant-voltage m	ode.			

^{*}POR value depends on external conditions.

Status B Register

ADDRESS:		0x03						
MODE:		Read Only			-1			
BIT	7	6	5	4	3	2	1	0
NAME	VLim	lLim	UsbOVP	SysBatV	UsbOk		JeitaStat[2:0]	
RESET				SEE T	ABLE 4			
RFU	Reserved for	future use.						
VLim	0 = VB input	es when the in voltage under voltage limited	limit	drop-out.				
lLim	0 = VB input	s when the VB current under current limited	limit.	reaches the lim	it.			
UsbOVP	VB Overvolta 0 = VB OVP 1 = VB OVP		Status					
SysBatV	charge the be charge curre valid condition a) V _{SYS} - V _B b) V _{SYS} = V _S 0 = Charge co	attery. If the tot	al load exceed SYS from colla following two: yp)	ds the input cur apsing. The reg	rent limit, an ac	daptive char	draws power from ger control loop re nt is done looking	educes
UsbOk		resent or outsid		oresent and val ge.	id.			
JeitaStat[2:0]	000 = T < 0°C 001 = 0°C < 010 = 10°C < 011 = 45°C < 100 = No the 101 = NTC ir	C or T > 60°C. T < 10°C. T < 45°C. T < 45°C. T < 60°C. T < 60°C. T < 60°C. Thistor detected to the control of t	ed (THM high o y JeitaEn.	due to external	ery monitor is co	urrently dete	ecting.	

Status C Register

ADDRESS:		0x04							
MODE:		Read Only							
BIT	7	6	5	4	3	2	1	0	
NAME	RFU	RFU	RFU	RFU	ThrmSd	ChgTReg	DCDTmr	ChgTmo	
RESET				SEE TA	ABLE 4				
RFU	Reserved for	future use.							
ThrmSd	0 = Device n	cates when the ot in thermal should the the othermal shutd	nutdown.	ermal shutdow	n.				
ChgTReg	0 = Device n	ChgTReg indicates when the device is reducing charger current to prevent overheating. 0 = Device not reducing charger current or charger disabled. 1 = Device reducing charger current.							
DCDTmr	0 = DCD time	icates when a der not expired der has been rur	or not running.		exceeds t _{DCD}	_TO.			
ChgTmo	0 = Charger	cates when the has not reache has reached a	d a timeout cor	ndition or is dis	sabled.		dicate this faul	It condition.	

Interrupt A Register

ADDRESS:	0x05								
MODE:	Clear on Rea	d							
BIT	7	6	5	4	3	2	1	0	
NAME	ChgTypInt	UsbOVPInt	SysBatVInt	RFU	BatDetInt	ChgStatInt	ChgTRegInt	ChgTmoInt	
RESET				SEE T	ABLE 4				
ChgTypInt	ChgTypInt is s	et when there	is a change i	in ChgTyp[3:0]	in register 0x0)2.			
UsbOVPInt	UsbOVPInt is	set when ther	e is a change	in UsbOVP in	register 0x03.				
SysBatVint	SysBatVint is	SysBatVint is set when there is a change in SysBatV in register 0x03.							
BatDetInt	BatDetInt is se change in bat		•	n BatDet or the	e first battery de	etection comp	letes after a PC	R or a	
ChgStatInt	ChgStatInt is after a POR.	set when there	is a change	in ChgStat[2:0] in register 0x	02 or the first	charger status i	is entered	
ChgTRegInt	ChgTRegInt is	set when the	re is a chang	e in ChgTReg	in register 0x0-	4.			
ChgTmoInt	ChgTmoInt is	set when there	e is a change	in ChgTmo in	register 0x04.				

Interrupt B Register

ADDRESS:		0x06							
MODE:		Clear on Rea	ad						
BIT	7	6	5	4	3	2	1	0	
NAME	VLimInt	DCDTmrInt	lLimInt	ThrmSdInt	UsbOkInt	JeitaStatInt	JeitaHighTInt	JeitaTSdInt	
RESET				SEE	TABLE 4				
VLimInt	VLimInt is se	t when the VB	voltage reac	hes the input v	oltage limit.				
DCDTmrInt	DCDTmrInt is	s set when a D	CD timeout of	occurs.					
lLimInt	ILimInt is set	ILimInt is set when the VB current reaches the input current limit.							
ThrmSdInt	ThrmSdInt is	ThrmSdInt is set when there is a change in ThrmSd in register 0x04.							
UsbOkInt	UsbOkInt is s	et when there	is a change	in UsbOk in reo	gister 0x03.				
JeitaStatInt	JeitaStatInt is	set when ther	e is a chang	e in JeitaStat[2	:0] in register (0x03.			
JeitaHighTInt	JeitaHighTIn	is set when th	e JEITA mor	itor enters the	high battery te	emperature ran	ge (45°C < T < 6	0°С).	
JEITATSDINT	JeitaTSdInt is (T < 0°C or T		JEITA monit	or enters the ve	ery low or very	high battery te	emperature range	Э	

Interrupt Mask A Register

ADDRESS:		0x07							
MODE:		Read/Write							
ВІТ	7	6	5	4	3	2	1	0	
NAME	ChgTypIntM	UsbOVPIntM	SysBatVIntM	RFU	BatDetIntM	ChgStatIntM	ChgTRegIntM	ChgTmoIntM	
RESET		,		SE	E TABLE 4				
ChgTypIntM	ChgTypIntM n 0 = Masked. 1 = Not maske	nasks the ChgTy	pInt interrupt in	the IntA	A register (0x05	5).			
UsbOVPIntM	UsbOVPIntM 0 = Masked. 1 = Not maske	masks the UsbC	VPInt interrupt	in the Ir	ntA register (0x	05).			
SysBatVIntM	SysBatVintM	masks the SysB	atVint interrupt i	n the in	tA register (0x0	05).			
BatDetIntM	0 = Masked.	BatDetIntM masks the BatDetInt interrupt in the IntA register (0x05). 0 = Masked. 1 = Not masked.							
ChgStatIntM	ChgStatIntM r 0 = Masked. 1 = Not maske	masks the ChgS	tatInt interrupt ir	the Int	A register (0x0	5).			
ChgTRegIntM	0 = Masked.	ChgTRegIntM masks the ChgTRegInt interrupt in the IntA register (0x05).							
ChgTmoIntM	ChgTmoIntM 0 = Masked. 1 = Not maske	masks the ChgT	molnt interrupt i	n the Ir	tA register (0x	05).			

Interrupt Mask B Register

ADDRESS:		0x08						
MODE:		Read/Write						
BIT	7	6	5	4	3	2	1	0
NAME	VLimIntM	DCDTmrIntM	ILimIntM	ThrmSdIntM	UsbOkIntM	JeitaStatIntM	JeitaHighTIntM	JeitaTSdIntM
RESET				SI	EE TABLE 4			
VLimIntM	VLimIntM r	masks the VLim	Int interrup	t in the IntB re	gister (0x06).			
DCDTmrIntM	DCDTmrln 0 = Maske 1 = Not ma		CDTmrInt	interrupt in the	IntB register	(0x06).		
lLimIntM	ILimIntM m 0 = Maske 1 = Not ma		t interrupt	in the IntB regi	ster (0x06).			
ThrmSdIntM	0 = Maske	ThrmSdIntM masks the ThrmSdInt interrupt in the IntB register (0x06). 0 = Masked. 1 = Not masked.						
UsbOkIntM	UsbOkIntN 0 = Maske 1 = Not ma		OkInt inte	rrupt in the Int	3 register (0x0	06).		
JeitaStatIntM	JeitaStatIn 0 = Maske 1 = Not ma		eitaStatInt	interrupt in the	IntB register	(0x06).		
JeitaHighTIntM	JeitaHighT 0 = Maske 1 = Not ma		JeitaHigh1	FInt interrupt in	the IntB regis	ster (0x06).		
JeitaSdIntM	JeitaSdIntl 0 = Maske 1 = Not ma		itaSdInt int	errupt in the In	tB register (0x	x06).		

Charger Detection Control A Register

ADDRESS:		0x09						
MODE:		Read/Write*						
BIT	7	6	5	4	3	2	1	0
NAME	RFU	RFU	nFsusEn	FSUSMsk	RFU	RFU	DCDEn	RFU
RESET				SEE TA	ABLE 4			
RFU	Reserved for	future use.						
nFsusEn	rent limit. If F	SUSMsk = 1, to be is forced into	hen nFsusEn	trol. If FSUSMs controls the for e and the curre	ce suspend cu	rrent limit.	ls the force sus	pend cur-
FSUSMsk	0 = FSUS inp	asks the function of the controls for bit controls for	ce-suspend mo	ode.				
DCDTEn	DCDTEn ena 0 = Not enab 1 = Enabled.	ables data cont led.	act detection.					

^{*}Register resets to default value on VB rising edge.

Input-Current Limit Control Register

ADDRESS:		0x0A						
MODE:		Read/Write*						
BIT	7	6	5	4	3	2	1	0
NAME	IBusLim	RFU	RFU		ILimSet[2:0]		IBusDe	tSw[1:0]
RESET				SEE T	ABLE 4			
IBusLim	0 = Automation bits in registe	er 0x02).	ırrent limit is d	etermined usir	g adaptor dete	ection status (C		
RFU	Reserved for	future use.						
ILimSet[2:0]	ILimSet[2:0]: 000 = 100mA 001 = 500mA 010 = 600mA 011 = 700mA 100 = 900mA 101 = 1000m 110 = 1500m 111 = 2000m	A A A A	rrent limit in m	anual mode wh	nen IBusDetSw	v[1:0] = 11.		
IBusDetSw [1:0]	IBusDetSw[1 00 = 0mA 01 = 100mA 10 = 500mA 11 = set by IL	:0] sets the cui	rent limit on V	B in manual m	ode.			

^{*}Register resets to default value on VB rising edge.

Charge Control Register A

ADDRESS:		0x0B	0x0B						
MODE:		Read/Write*							
BIT	7	6	5	4	3	2	1	0	
NAME	RFU	RFU	RFU		IFChg[2:0]		RFU	RFU	
RESET		SEE TABLE 4							
RFU	Reserved for	Reserved for future use.							
IFChg[2:0]	IFChg[2:0]: 000 = 700m 001 = 300m 010 = 200m 011 = 600m 100 = 800m 101 = 900m 110 = 350m 111 = 450m	nA nA nA nA nA nA	er current in fas	st-charge mod	e.				

^{*}POR value depends on external conditions.

Charger Control B Register

ADDRESS:		0x0C								
MODE:		Read/Write*								
BIT	7	6	5	4	3	2	1	0		
NAME	JeitaEn	BatUOKMsk	BatUOKMsk BatDetCntl ChgEn RFU ChgDone[2:0]							
RESET				SEE TAI	BLE 4					
JeitaEn	0 = JEITA m always read: 1 = JEITA m	bles JEITA batte onitoring of them s 101. onitoring of them status of the the	mistor disabled.	JeitaStat[2:0]						
BatUOKMsk	0 = Battery o	masks the UOr detection signals detection signals	are generated							
BatDetCntl	0 = BatDet s	selects which me status bit will indi status bit will indi	cate battery pre	esence based	on the impeda	nce method.		M.		
ChgEn	ChgEn enab 0 = Charger 1 = Charger		charger. ChgEn	does not affec	ct the SYS nod	e.				
RFU	Reserved fo	r future use.								
ChgDone[2:0]	ChgDone[2:: 000 = 10mA 001 = 20mA 010 = 40mA 011 = 50mA 100 = 60mA 101 = 80mA 110 = 100mA	A	hold current wh	en constant-v	oltage fast cha	rging is done.				

^{*}Register resets to default value on VB rising edge.

Charger Timer Register

ADDRESS:		0x0D							
MODE:		Read/Write*	Read/Write*						
BIT	7	6	5	4	3	2	1	0	
NAME	RFU	RFU	MtChg1	Γmr[1:0]	FChg ⁻	Tmr[1:0]	PChgT	mr[1:0]	
RESET				SEE	TABLE 4				
RFU	Reserved f	or future use.							
MtChgTmr[1:0]	00 = 30min 01 = 15min 10 = 0min	MtChgTmr[1:0] sets the maintain charge timer when ChgAutoStp is register 0x12 is 1. 00 = 30min 01 = 15min 10 = 0min 11 = 60min							
FChgTmr[1:0]	FChgTmr[1:0] sets the fast charge timer. 00 = 75min 01 = 150min 10 = 300min 11 = 600min								
PChgTmr[1:0]	PChgTmr[7 00 = 30min 01 = 60min 10 = 120m 11 = 240mi	in	e charge timer.						

^{*}Register resets to default value on VB rising edge.

Charger Detection Control A Register

ADDRESS:	0x0E							
MODE:	Read/Write	e*						
BIT	7	7 6 5 4 3 2 1 0						
NAME	BatRe0	Chg[1:0]	BatRe	gLow[1:0]	BatRegSel		BatRegHi[2:0]
RESET				SE	E TABLE 4			
BatReChg[1:0]	age less th 00 = 50mV 01 = 100m 10 = 150m	BatReChg[1:0] sets the recharge threshold in relation to V_{BAT} . Once V_{BAT} falls to below the regulation voltage less this amount, the MAX14746/MAX14747 will recharge it. 00 = 50mV 01 = 100mV 10 = 150mV 11 = 200mV						
BatRegLow[1:0]	BatRegLov 00 = 4.05V 01 = 4.10V 10 = 4.15V 11 = 4.20V		e battery regu	llation voltage	when BatRegSel	= 0.		
BatRegSel		G + 200mV. Note: 1 properly. It RegLow			ry regulation voltagen such that VSYS			
BatRegHi[2:0]	BatRegHi s 000 = 4.25' 001 = 4.30' 010 = 4.35' 011 = 4.40' 100 = 4.45' 101 = 4.50' 111 = 4.60'	V V V V V	ery regulation	voltage when	BatRegSel = 1			

^{*}Register resets to default value on VB rising edge.

Precharge Control Register

ADDRESS:	0x10									
MODE:	Read/Write*									
BIT	7	7 6 5 4 3 2 1 0								
NAME	VPChg	IPC	ng[1:0]	VPCh	JLow[1:0]	VPChg	High[1:0]	BatDetChgM		
RESET				SEE TA	ABLE 4					
VPChg	battery voltage 0 = Use VPChg	VPChg selects which voltage threshold setting to use for pre-charging. The charger uses precharging until the battery voltage rises above the threshold or the timer expires. 0 = Use VPChgLow[1:0]. 1 = Use VPChgHigh[1:0].								
IPChg[1:0]	IPChg[1:0] sets 00 = 30mA 01 = 50mA 10 = 70mA 11 = 100mA	s the prechar	ge current.							
VPChgLow [1:0]	VPChgLow[1:0 00 = 2.15V 01 = 2.25V 10 = 2.35V 11 = 2.45V] sets the pre	echarge voltage	threshold wh	nen VPChg = 0).				
VPChgHigh [1:0]	VPChgHigh[1:0 00 = 2.70V 01 = 2.80V 10 = 2.90V 11 = 3.00V	0] sets the pr	echarge voltage	threshold w	hen VPChg = 1	1.				
BatDetChgM	BatDetChgM m 0 = BatDet stat 1 = BatDet stat (i.e., it is possib	te affects cha te does not a	rger behavior p	er state diagi havior.	am.					

^{*}Register resets to default value on VB rising edge.

Charger Detection Control B Register

ADDRESS:	0x11	<u> </u>		·				·		
MODE:	Read/Write*									
BIT	7 6 5 4 3 2 1									
NAME	SFOutOrd	SFOutAsrt	AnSw	Cntl[1:0]	ChgTypMan*	ChgAutoStart	BatDetChgEn	UsbCompl		
RESET					SEE TABLE 4			•		
SFOutOrd	0 = Force SF	SFOutOrd enables the SFOUT output. 0 = Force SFOUT to off. The internal LDO is disabled and V _{SFOUT} is 0V. 1 = SFOUT is automatically controlled by the VB voltage presence and the SFOutAsrt bit.								
SFOutAsrt	0 = SFOUT to complete.	ontrols the per turns on after a turns on immed	a complete	charger dete	ection cycle. VB o	does not pass cu	rrent until charger	detection is		
AnSwCntl[1:0]	00 = Automa tected. 01 = Switche 10 = Switche	0] controls the tic mode. The es forced open es forced open es forced close	switches a			tion and closed i	f an SDP or CDP	are de-		
ChgTypMan*	Set to 1 to fo 0 = Disable	e Manual Dete rce charger de charger detect	etection. Af	ter the detec	tion completes th	ne bit resets to 0.				
ChgAutoStart	0 = Charger	Charger Auto-Restart Control 0 = Charger remains in maintain charge done even when V _{BAT} is less than charge restart threshold. 1 = Charger automatically restarts when V _{BAT} drops below charge restart threshold.								
BatDetChgEn	0 = The char	BatDetChgEn enables running the charger during battery detection. 0 = The charger is not allowed to turn on during battery detection if ChgEn = 0 in register 0x0C. 1 = The charger is allowed to turn on during battery detection even when ChgEn = 0 in register 0x0C.								
UsbCompl	0 = If an SDF	is detected ir	n auto curr	ent limit setti	•	an SDP port. ut current limit is ut current limit is				

^{*}Register resets to default value on VB rising edge.

Charger Control C Register

ADDRESS:		0x12						
MODE:		Read/Write*						
BIT	7	6	5	4	3	2	1	0
NAME	ChgAutoStp	SFOutData	RFU	RFU		SysMin[2:0]		RFU
RESET				SEE TA	BLE 4			
ChgAutoStp	ChgAutoStp c 0 = Auto stop 1 = Auto stop	disabled.	sition from mai	ntain charge r	node to main	tain charge don	e.	
SFOutData	by the SFOut0 0 = SFOUT is	Ord and SFOutA turned on for a	Asrt settings in I valid charger	register 0x11. types (see Ch	ngTyp[3:0] in	register 0x02). gTyp[3:0] = 010		is overridden
SysMin[2:0]		es the charge c				ches V _{SYS_LIN} V _{SYS} < V _{SYS_}		
RFU	Reserved for future use. Must be set to 1.							

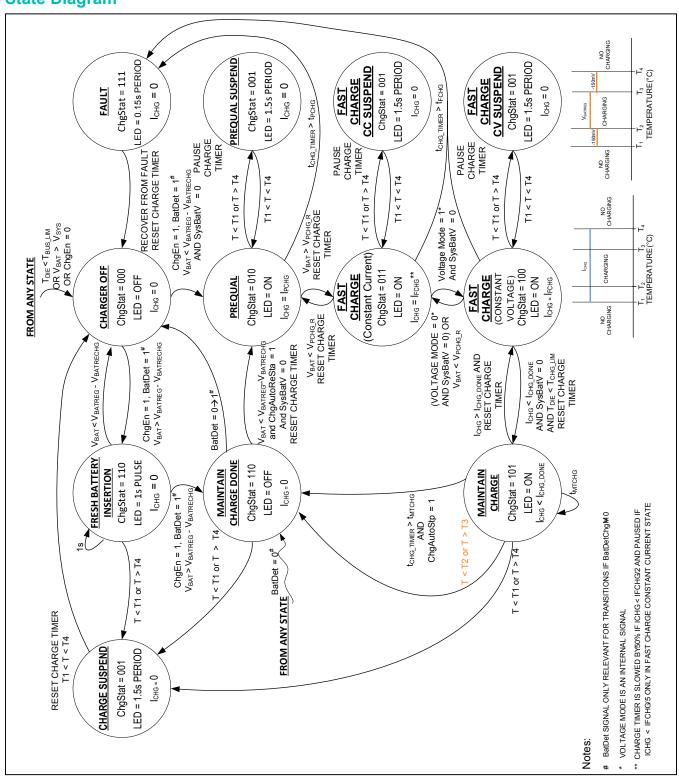
^{*}Register resets to default value on VB rising edge.

Current-Limit Monitor Register

ADDRESS:	0x13									
MODE:	Read Only*	Read Only*								
BIT	7	6	5	4	3	2	1	0		
NAME				ILimMoi	n[7:0]					
RESET				SEE TAI	BLE 4					
ILimMon[7:0]	SEE TABLE 4 ILimMon[7:0] reads out the VB input current limit setting that is currently used. 0000 0000 = 0mA 0000 0001 = 100mA 0000 0010 = 500mA 0000 1000 = 700mA 0000 1000 = 700mA 0001 0000 = 900mA 0010 0000 = 1500mA 1000 0000 = 2000mA									

^{*}Register resets to default value on VB rising edge.

State Diagram



Applications Information

I²C Interface

The MAX14646/MAX14647 contain an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

Start, Stop, And Repeated Start Conditions

When writing to the MAX14646/MAX14647 using I²C, the master sends a START condition (S) followed by the MAX14646/MAX14647 I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 2.

Slave Address

Set the Read/Write bit high to configure the MAX14646/MAX14647 to read mode (Table 1). Set the Read/Write bit low to configure the MAX14646/MAX14647 to write mode. The address is the first byte of information sent to the MAX14646/MAX14647 after the START condition.

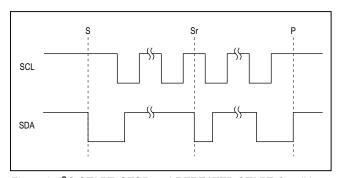


Figure 2. I²C START, STOP and REPEATED START Conditions

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the <u>Start, Stop, And Repeated Start Conditions</u> section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (<u>Figure 3</u>). The following procedure describes the single byte write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends 8 data bits
- 7) The slave asserts an ACK on the data line
- 8) The master generates a STOP condition

Table 1, I2C Slave Addresses

ADDRESS FORMAT	HEX	BINARY
7-bit slave ID (MAX14746)	0x12	0001 010
Write Address (MAX14746)	0x14	0001 0100
Read Address (MAX14746)	0x15	0001 0101
7-bit slave ID (MAX14747)	0x02	0000 010
Write Address (MAX14747)	0x04	0000 0100
Read Address (MAX14747)	0x05	0000 0101

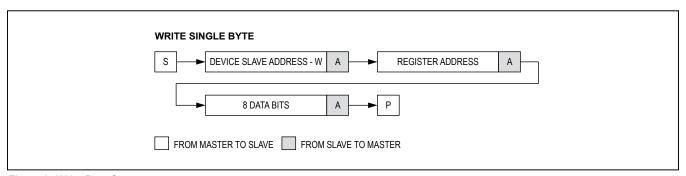


Figure 3. Write Byte Sequence

MAX14746/MAX14747

USB Detection with Smart Power Selector Li+ Chargers

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (<u>Figure 4</u>). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends eight data bits
- 7) The slave asserts an ACK on the data line
- 8) Repeat 6 and 7 N-1 times
- 9) The master generates a STOP condition

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (<u>Figure 5</u>). The following procedure describes the single byte read operation:

- 1)The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3)The addressed slave asserts an ACK on the data line
- 4)The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends a REPEATED START condition
- 7)The master sends the 7-bit slave address plus a read bit (high)
- 8)The addressed slave asserts an ACK on the data line
- 9)The slave sends eight data bits
- 10) The master asserts a NACK on the data line
- 11) The master generates a STOP condition

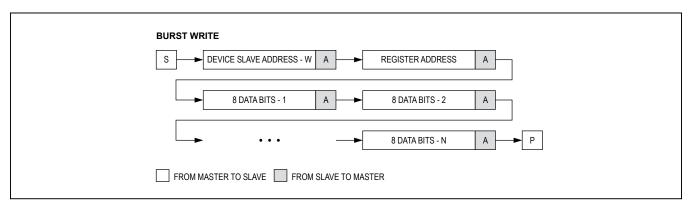


Figure 4. Burst Write Sequence

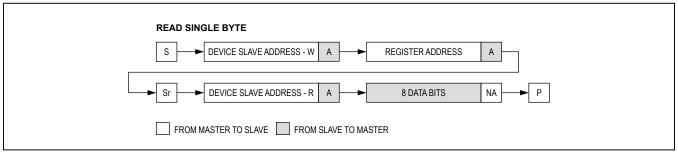


Figure 5. Read Byte Sequence

MAX14746/MAX14747

USB Detection with Smart Power Selector Li+ Chargers

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (<u>Figure 6</u>). The following procedure describes the burst byte read operation:

- 1)The master sends a START condition
- 2)The master sends the 7-bit slave address plus a write bit (low)
- 3)The addressed slave asserts an ACK on the data line
- 4)The master sends the 8-bit register address
- 5)The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6)The master sends a REPEATED START condition
- 7)The master sends the 7-bit slave address plus a read bit (high)
- 8)The slave asserts an ACK on the data line

- 9)The slave sends eight data bits
- 10) The master asserts an ACK on the data line
- 11) Repeat 9 and 10 N-2 times
- 12) The slave sends the last eight data bits
- 13) The master asserts a NACK on the data line
- 14) The master generates a STOP condition

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX14746 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 7). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

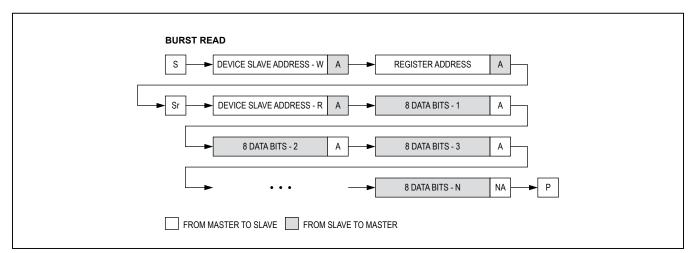


Figure 6. Burst Read Sequence

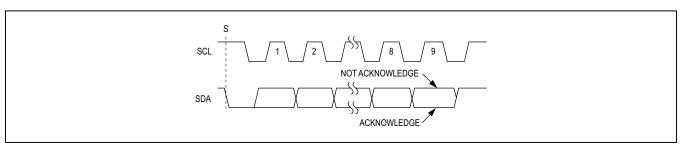


Figure 7. Acknowledge

High-ESD Protection

Electrostatic Discharge (ESD)-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV Human Body Model (HBM) encountered during handling and assembly. CDP and CDN are further protected against ESD up to ±15kV (HBM) without damage. The ESD structures withstand high ESD in both normal operation and when the device is powered down. After an ESD event, the MAX14746/MAX14747 continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 8 shows the Human Body Model. Figure 9 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor

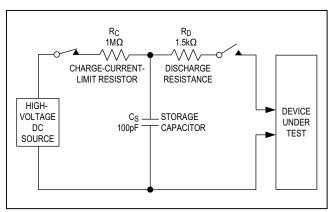


Figure 8. Human Body ESD Test Model

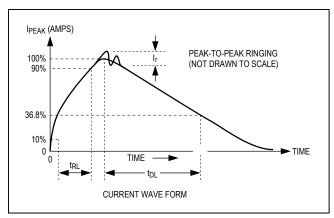


Figure 9. Human Body Current Waveform

charged to the ESD voltage of interest that is then discharged into the device through a $1.5k\Omega$ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX14746/MAX14747 are specified for ±4kV Air-Gap and ±5kV Contact Discharge IEC 61000-4-2 on the CDP and CDN pins.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 10), the ESDwithstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 11 shows the current waveform for the ±6kV IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Contact Discharge method connects the probe to the device before the probe is energized.

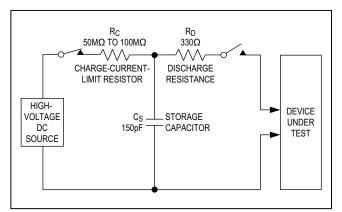


Figure 10. IEC61000-4-2 ESD Test Model

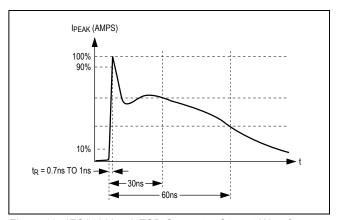


Figure 11. IEC61000-4-2 ESD Generator Current Waveform

Table 2. Part Selection

PART NUMBER	EXT/UOK2 FUNCTION	BATTERY OVP	
MAX14746B	EXT	Disabled	
MAX14747	EXT	Enabled	

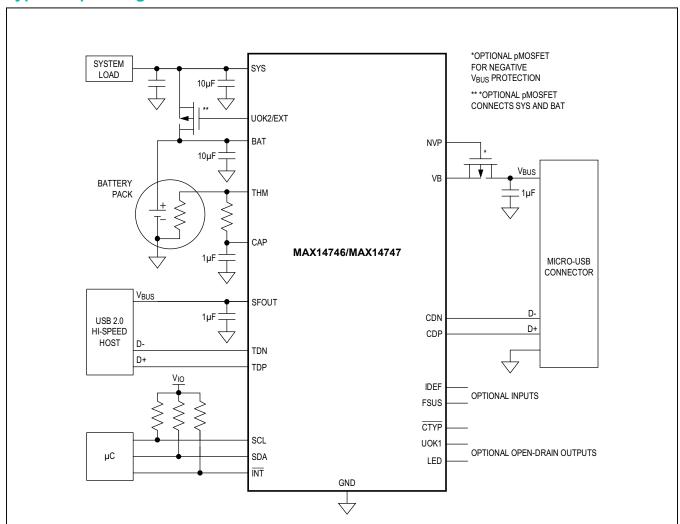
Table 3. Register Bit Default Values

REGISTER BITS	MAX14746B	MAX14747
IBusLim	Manual	Automatic
ILimSet[2:0]	500mA	500mA
IFChg[2:0]	600mA	200mA
ChgEn	Enabled	Disabled
BatReChg[1:0]	100mV	100mV
BatRegLow[1:0]	4.20V	4.20V
BatDetIntM	Masked	Masked
ChgStatIntM	Masked	Masked
VPChg	VPChgHigh	VPChgLow
IPChg[1:0]	100mA	50mA
VPChgLow[1:0]	2.45V	2.25V
VPChgHigh[1:0]	3.00V	2.80V
SFoutAsrt	Immediately	Delayed
FSUSMsk	FSUS	FSUS
BatDetChgM	Not Masked	Not Masked
JeitaEn	Enabled	Enabled
BatDetCntl	Thermistor	Thermistor
ChgDone[2:0]	50mA	60mA
ChgAutoStart	Enabled	Enabled
BatDetChgEn	Enabled	Enabled
UsbCmpl	500mA	500mA
BatRegSel	BatRegLow	BatRegLow
BatRegHi[2:0]	4.35V	4.35V
SFoutData	All Chargers	All Chargers
SysMin[2:0]	4.3V	4.3V
MAX_VSYS_REG	VBAT_REG + 0.2V	4.8V

Table 4. Register Default Values

REGISTER	REGISTER	DEFAULT	VALUES
ADDRESS	NAME	MAX14746B	MAX14747
0x00	Chip_ld	0x2E	0x30
0x01	Chip_Rev	0x01	0x11
0x02	StatusA	0x00	0x00
0x03	StatusB	0x46	0x46
0x04	StatusC	0x00	0x00
0x05	IntA	0xA0	0xA0
0x06	IntB	0xA4	0xA4
0x07	IntMaskA	0x00	0x00
0x08	IntMaskB	0x00	0x00
0x09	CDetCntlA	0x22	0x22
0x0A	ILimCntl	0x87	0x07
0x0B	ChgCntlA	0x0C	0x08
0x0C	ChgCntlB	0xF3	0xE4
0x0D	ChgTmr	0x2E	0x2E
0x0E	ChgVSet	0x72	0x72
0x0F	JeitaCntl	0x00	0x00
0x10	ChgPCntl	0xFE	0x2A
0x11	CDetCntlB	0xC6	0x86
0x12	ChgCntlC	0x8F	0x81
0x13	ILimMon	0x00	0x00

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	BUMP-PACKAGE
MAX14746BEWA+	-40°C to +85°C	25 WLP
MAX14747EWA+	-40°C to +85°C	25 WLP

⁺Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BICMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE	LAND
TYPE	CODE	NO.	PATTERN NO.
25 WLP	W252J2+1	21-0453	Refer to Application Note 1891

MAX14746/MAX14747

USB Detection with Smart Power Selector Li+ Chargers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/15	Initial release	_
1	1/17	Updated for Pass 2 material	3, 11, 13, 19–33, 39
2	11/17	Removed future product asterisks	40

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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