NCP1340

High-Voltage, Quasi-Resonant, Controller Featuring Valley Lock-Out Switching

The NCP1340 is a highly integrated quasi−resonant flyback controller suitable for designing high−performance off−line power converters. With an integrated active X2 capacitor discharge feature, the NCP1340 can enable no−load power consumption below 30 mW.

The NCP1340 features a proprietary valley−lockout circuitry, ensuring stable valley switching. This system works down to the 6th valley and transitions to frequency foldback mode to reduce switching losses. As the load decreases further, the NCP1340 enters quiet−skip mode to manage the power delivery while minimizing acoustic noise.

To help ensure converter ruggedness, the NCP1340 implements several key protective features such as internal brownout detection, a non−dissipative Over Power Protection (OPP) for constant maximum output power regardless of input voltage, a latched overvoltage and NTC−ready overtemperature protection through a dedicated pin, and line removal detection to safely discharge the X2 capacitors when the ac line is removed.

If transient load capability is desired, the NCP1341 offers the same performance and features with the addition of power excursion mode (PEM).

Features

- Integrated High−Voltage Startup Circuit with Brownout Detection
- Integrated X2 Capacitor Discharge Capability
- Wide V_{CC} Range from 9 V to 28 V
- 28 V V_{CC} Overvoltage Protection
- Abnormal Overcurrent Fault Protection for Winding Short Circuit or Saturation Detection
- Internal Temperature Shutdown
- Valley Switching Operation with Valley−Lockout for Noise−Free Operation
- Frequency Foldback with 25 kHz Minimum Frequency Clamp for Increased Efficiency at Light Loads
- Skip Mode with Quiet−Skip Technology for Highest Performance During Light Loads
- Minimized Current Consumption for No Load Power Below 30 mW
- Frequency Jittering for Reduced EMI Signature
- Latching or Auto−Recovery Timer−Based Overload Protection
- Adjustable Overpower Protection (OPP)
- Fixed or Adjustable Maximum Frequency Clamp
- Fault Pin for Severe Fault Conditions, NTC Compatible for OTP
- 4 ms Soft−Start Timer

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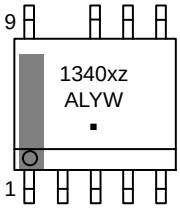
SOIC−8 NB
D SUFFIX
CASE 751

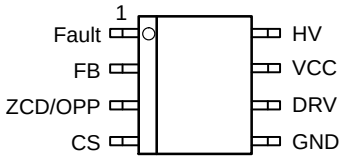
SOIC−9 NB
D SUFFIX
CASE 751BP

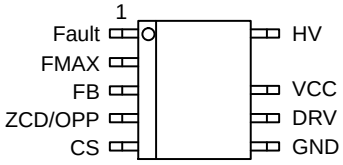
MARKING DIAGRAM



1340xz	= Specific Device Code
x	= A or B
z	= 1, 2, 3, 4, 5, 6, or 7
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS





(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information n on page 3 of this data sheet.

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TYPICAL APPLICATION SCHEMATIC

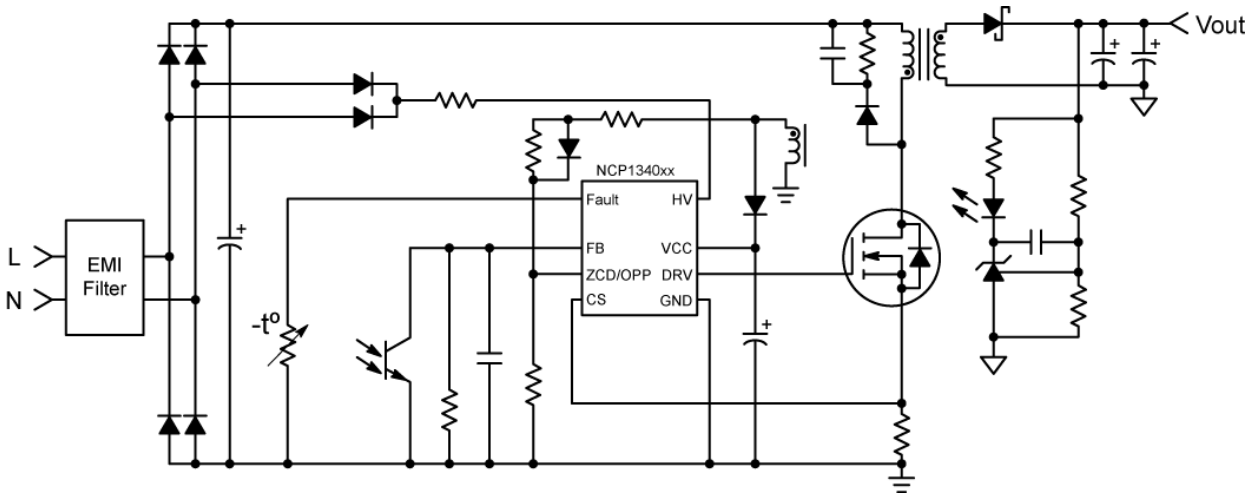

Figure 1. NCP1340 8−Pin Typical Application Circuit

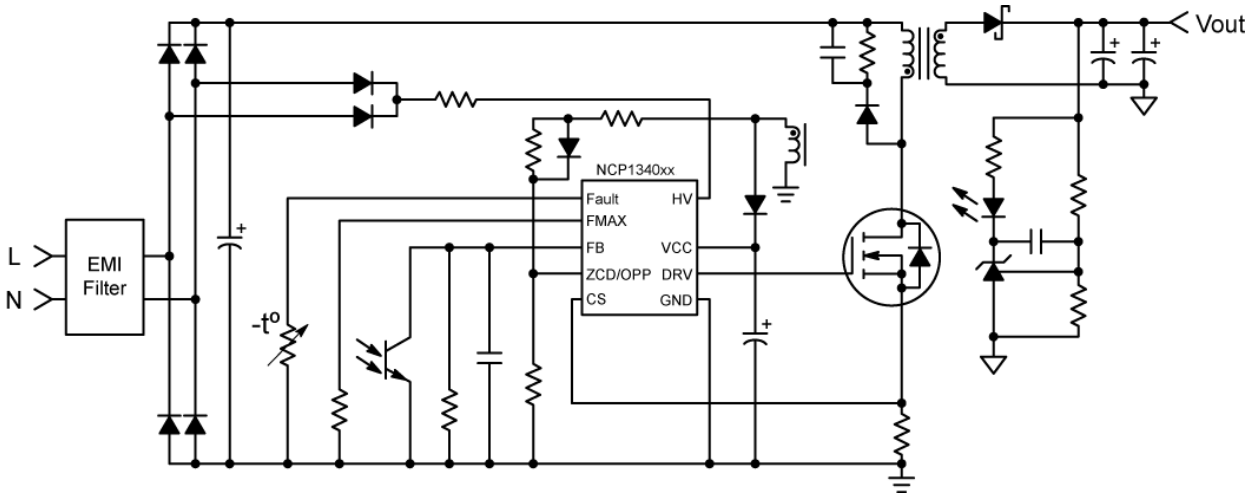

Figure 2. NCP1340 9−Pin Typical Application Circuit

Table 1. ORDERING INFORMATION TABLE

Orderable Part Number	Device Marking	Package	Shipping†
NCP1340A3D1R2G	1340A3	SOIC−9	2500 / Tape & Reel
NCP1340B1DR2G	1340B1	SOIC−8	2500 / Tape & Reel
NCP1340B3D1R2G	1340B3	SOIC−9	2500 / Tape & Reel
NCP1340B4D1R2G	1340B4	SOIC−9	2500 / Tape & Reel
NCP1340B5D1R2G	1340B5	SOIC−9	2500 / Tape & Reel
NCP1340A6DR2G	1340A6	SOIC−8	2500 / Tape & Reel
NCP1340B6DR2G	1340B6	SOIC−8	2500 / Tape & Reel
NCP1340B7D1R2G	1340B7	SOIC−9	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 2. DEVICE DIFFERENTIATION TABLE

Ordering Code	Pins	Fault Pin	FMAX Pin	X2	OTP/Overload Protection	Frequency Clamp	R_{FB} Pullup	V_{CC} OVP	I_{FB} Pullup	Jitter
NCP1340A3D1R2G	9	Yes	Yes	Yes	Latched	Adjustable	400 kΩ	Yes	100 μA	1.3kHz
NCP1340B1DR2G	8	Yes	No	Yes	Auto−Restart	None	400 kΩ	Yes	100 μA	1.3kHz
NCP1340B3D1R2G	9	Yes	Yes	Yes	Auto−Restart	Adjustable	400 kΩ	Yes	100 μA	1.3kHz
NCP1340B4D1R2G	9	Yes	Yes	Yes	Auto−Restart	Adjustable	20 kΩ	No	None	1.3kHz
NCP1340B5D1R2G	9	Yes	Yes	Yes	Auto−Restart	Adjustable	20 kΩ	Yes	None	None
NCP1340A6DR2G	8	Yes	No	Yes	Latched	None	20 kΩ	Yes	None	None
NCP1340B6DR2G	8	Yes	No	Yes	Auto−Restart	None	20 kΩ	Yes	None	None
NCP1340B7D1R2G	9	Yes	Yes	No	Auto−Restart	Adjustable	20 kΩ	Yes	None	None

FUNCTIONAL BLOCK DIAGRAM

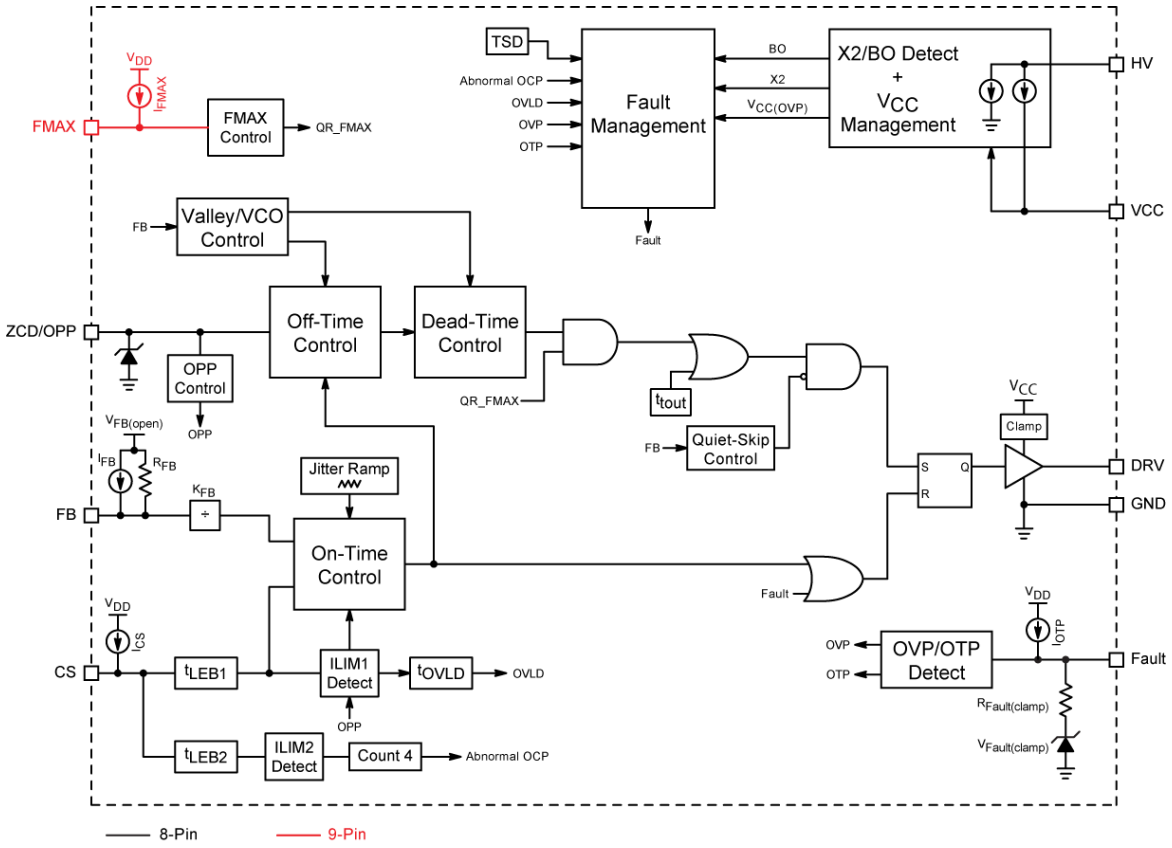

Figure 3. NCP1340 Block Diagram

Table 3. PIN FUNCTIONAL DESCRIPTION

8−Pin	9−Pin	Pin Name	Function
1	1	Fault	The controller enters fault mode if the voltage on this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor.
−	2	FMAX	A resistor to ground sets the value for the maximum switching frequency clamp. If this pin is pulled above 4 V, the maximum frequency clamp is disabled.
2	3	FB	Feedback input for the QR Flyback controller. Allows direct connection to an optocoupler.
3	4	ZCD/OPP	A resistor divider from the auxiliary winding to this pin provides input to the demagnetization detection comparator and sets the OPP compensation level.
4	5	CS	Input to the cycle−by−cycle current limit comparator.
5	6	GND	Ground reference.
6	7	DRV	This is the drive pin of the circuit. The DRV high−current capability (−0.5 /+0.8 A) makes it suitable to effectively drive high gate charge power MOSFETs.
7	8	VCC	This pin is the positive supply of the IC. The circuit starts to operate when V_{CC} exceeds 17 V and turns off when V_{CC} goes below 9 V (typical values). After start−up, the operating range is 9 V up to 28 V.
−	9	N/C	Removed for creepage distance.
8	10	HV	This pin is the input for the high voltage startup and brownout detection circuits. It also contains the line removal detection circuit to safely discharge the X2 capacitors when the line is removed.

Table 4. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High Voltage Startup Circuit Input Voltage	$V_{HV(MAX)}$	−0.3 to 700	V
High Voltage Startup Circuit Input Current	$I_{HV(MAX)}$	20	mA
Supply Input Voltage	$V_{CC(MAX)}$	−0.3 to 30	V
Supply Input Current (Note 1)	$I_{CC(MAX)}$	30	mA
Supply Input Voltage Slew Rate	dV_{CC}/dt	1	V/μs
Fault Input Voltage	$V_{Fault(MAX)}$	−0.3 to V_{CC} + 0.7 V	V
Fault Input Current	$I_{Fault(MAX)}$	10	mA
Zero Current Detection and OPP Input Voltage	$V_{ZCD(MAX)}$	−0.3 to V_{CC} + 0.7 V	V
Zero Current Detection and OPP Input Current	$I_{ZCD(MAX)}$	−2/+5	mA
Maximum Input Voltage (Other Pins)	V_{MAX}	−0.3 to 5.5	V
Maximum Input Current (Other Pins)	I_{MAX}	10	mA
Driver Maximum Voltage (Note 2)	V_{DRV}	−0.3 to $V_{DRV(high)}$	V
Driver Maximum Current	$I_{DRV(SRC)}$ $I_{DRV(SNK)}$	500 800	mA
Operating Junction Temperature	T_J	−40 to 125	°C
Storage Temperature Range	T_{STG}	–60 to 150	°C
Power Dissipation (T_A = 25°C, 1 oz. Cu, 42 mm^2 Copper Clad Printed Circuit) DR2G Suffix, SOIC−8 D1R2G Suffix, SOIC−9	$P_{D(MAX)}$	 450 330	mW
Thermal Resistance (T_A = 25°C, 1 oz. Cu, 42 mm^2 Copper Clad Printed Circuit) DR2G Suffix, SOIC−8 D1R2G Suffix, SOIC−9	$R_{\theta JA}$	 225 300	°C/W
ESD Capability Human Body Model per JEDEC Standard JESD22−A114F (All pins except HV) Human Body Model per JEDEC Standard JESD22−A114F (HV Pin) Charge Device Model per JEDEC Standard JESD22−C101F Latch−Up Protection per JEDEC Standard JESD78E		 2000 800 1000 ±100	 V V V mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The V_{CC} pin is rated to handle the full transient current of the DRV pin.
2. Maximum driver voltage is limited by the driver clamp voltage, $V_{DRV(high)}$, when V_{CC} exceeds the driver clamp voltage. Otherwise, the maximum driver voltage is V_{CC}.

Table 5. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 2.4 V, V_{CS} = 0 V, V_{ZCD} = 0 V, V_{FMAX} = 0 V, C_{VCC} = 100 nF , C_{DRV} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
START−UP AND SUPPLY CIRCUITS						
Supply Voltage	dV/dt = 0.1 V/ms					V
Startup Threshold	V_{CC} increasing	$V_{CC(on)}$	16.0	17.0	18.0	
Discharge Voltage During Line Removal	V_{CC} decreasing	$V_{CC(X2_reg)}$	17.0	18.0	19.0	
Minimum Operating Voltage	V_{CC} decreasing	$V_{CC(off)}$	8.5	9.0	9.5	
Operating Hysteresis	$V_{CC(on)} - V_{CC(off)}$	$V_{CC(HYS)}$	7.5	–	–	
Internal Latch / Logic Reset Level	V_{CC} decreasing	$V_{CC(reset)}$	4.5	6.5	7.5	
Transition from I_{start1} to I_{start2}	V_{CC} increasing, I_{HV} = 650 μA	$V_{CC(inhibit)}$	0.40	0.70	1.05	
$V_{CC(off)}$ Delay	V_{CC} decreasing	$t_{delay(VCC_off)}$	25	32	40	μs
Startup Delay	Delay from $V_{CC(on)}$ to DRV Enable	$t_{delay(start)}$	–	–	500	μs
Minimum Voltage for Start−Up Current Source		$V_{HV(MIN)}$	–	–	40	V
Inhibit Current Sourced from V_{CC} Pin	V_{cc} = 0 V	I_{start1}	0.2	0.5	0.65	mA
Start−Up Current Sourced from V_{CC} Pin	$V_{cc} = V_{cc(on)} – 0.5$ V	I_{start2}	2.4	3.75	5.0	mA
Start−Up Circuit Off−State Leakage Current	V_{HV} = 162.5 V V_{HV} = 325 V V_{HV} = 700 V	$I_{HV(off1)}$ $I_{HV(off2)}$ $I_{HV(off3)}$	– – –	– – –	15 20 50	μA
Supply Current						mA
Fault or Latch	$V_{CC} = V_{CC(on)} – 0.5$ V	I_{CC1}	–	0.115	0.150	
Skip Mode (excluding FB current)	V_{FB} = 0 V	I_{CC2}	–	0.230	0.315	
Operating Current	f_{sw} = 50 kHz, C_{DRV} = open	I_{CC3}	–	1.0	1.5	
V_{CC} Overvoltage Protection Threshold		$V_{CC(OVP)}$	27	28	29	V
V_{CC} Overvoltage Protection Delay		$t_{delay(VCC_OVP)}$	25	32	40	μs
X2 CAPACITOR DISCHARGE (ALL VERSIONS EXCEPT B7)						
Line Voltage Removal Detection Timer		$t_{line(removal)}$	65	100	135	ms
Discharge Timer Duration		$t_{line(discharge)}$	21	32	43	ms
Line Detection Timer Duration		$t_{line(detect)}$	21	32	43	ms
V_{CC} Discharge Current	V_{CC} = 20 V	$I_{CC(discharge)}$	13	18	23	mA
HV Discharge Level		$V_{HV(discharge)}$	–	–	30	V
BROWNOUT DETECTION						
System Start−Up Threshold	V_{HV} increasing	$V_{BO(start)}$	107	112	116	V
Brownout Threshold	V_{HV} decreasing	$V_{BO(stop)}$	93	98	102	V
Hysteresis	V_{HV} increasing	$V_{BO(HYS)}$	9.0	14	–	V
Brownout Detection Blanking Time	V_{HV} decreasing	$t_{BO(stop)}$	40	70	100	ms
GATE DRIVE						
Rise Time	V_{DRV} from 10% to 90%	$t_{DRV(rise)}$	–	20	40	ns
Fall Time	V_{DRV} from 90% to 10%	$t_{DRV(fall)}$	–	5	30	ns
Current Capability						mA
Source		$I_{DRV(SRC)}$	–	500	–	
Sink		$I_{DRV(SNK)}$	–	800	–	
High State Voltage	$V_{CC} = V_{CC(off)}$ + 0.2 V, R_{DRV} = 10 kΩ V_{CC} = 30 V, R_{DRV} = 10 kΩ	$V_{DRV(high1)}$ $V_{DRV(high2)}$	8.0 10	– 12	– 14	V
Low Stage Voltage	V_{Fault} = 0 V	$V_{DRV(low)}$	–	–	0.25	V

Table 5. ELECTRICAL CHARACTERISTICS: (V_{CC} = 12 V, V_{HV} = 120 V, V_{Fault} = open, V_{FB} = 2.4 V, V_{CS} = 0 V, V_{ZCD} = 0 V, V_{FMAX} = 0 V, C_{VCC} = 100 nF , C_{DRV} = 100 pF, for typical values T_J = 25°C, for min/max values, T_J is – 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
FEEDBACK						
Open Pin Voltage Versions B5/B6/A6		$V_{FB(open)}$	4.9 4.8	5.0 5.0	5.1 5.1	V
V_{FB} to Internal Current Setpoint Division Ratio		K_{FB}	–	4	–	–
Internal Pull−Up Resistor Version B6	V_{FB} = 0.4 V	R_{FB}	350 17	400 20	420 23	kΩ
Internal Pull−Up Current Version B6		I_{FB}	90 –	100 0	108 –	μA
Valley Thresholds						V
Transition from 1st to 2nd valley	V_{FB} decreasing	V_{1to2}	1.316	1.400	1.484	
Transition from 2nd to 3rd valley	V_{FB} decreasing	V_{2to3}	1.128	1.200	1.272	
Transition from 3rd to 4th valley	V_{FB} decreasing	V_{3to4}	1.034	1.100	1.166	
Transition from 4th to 5th valley	V_{FB} decreasing	V_{4to5}	0.940	1.000	1.060	
Transition from 5th to 6th valley	V_{FB} decreasing	V_{5to6}	0.846	0.900	0.954	
Transition from 6th to 5th valley	V_{FB} increasing	V_{6to5}	1.410	1.500	1.590	
Transition from 5th to 4th valley	V_{FB} increasing	V_{5to4}	1.504	1.600	1.696	
Transition from 4th to 3rd valley	V_{FB} increasing	V_{4to3}	1.598	1.700	1.802	
Transition from 3rd to 2nd valley	V_{FB} increasing	V_{3to2}	1.692	1.800	1.908	
Transition from 2nd to 1st valley	V_{FB} increasing	V_{2to1}	1.880	2.000	2.120	
Maximum Frequency Clamp Versions A2/B2 Versions A3/B3 Versions A3/B3 Versions B4	 V_{FMAX} = 0.7 V V_{FMAX} = 3.5 V V_{FMAX} = 3.5 V	 f_{MAX1} f_{MAX2} f_{MAX3} f_{MAX3}	 100 300 60 68	 110 360 75 75	 120 420 85 78	kHz
FMAX Secondary Mode Threshold	9−Pin Versions Only	$V_{FMAX(mode)}$	3.85	4.00	4.15	V
FMAX Pin Source Current		I_{FMAX}	9.0	10	11	μA
Maximum On Time		$t_{on(MAX)}$	28	32	40	μs
DEMAGNETIZATION INPUT						
ZCD threshold voltage	V_{ZCD} decreasing	$V_{ZCD(trig)}$	35	60	90	mV
ZCD hysteresis	V_{ZCD} increasing	$V_{ZCD(HYS)}$	15	25	55	mV
Demagnetization Propagation Delay	V_{ZCD} step from 4.0 V to −0.3 V	t_{demag}	–	80	250	ns
ZCD Clamp Voltage Positive Clamp Negative Clamp	 I_{QZCD} = 5.0 mA I_{QZCD} = −2.0 mA	 $V_{ZCD(MAX)}$ $V_{ZCD(MIN)}$	 12.4 −0.9	 12.7 −0.7	 13 0	V
Blanking Delay After Turn−Off		$t_{ZCD(blank)}$	600	700	800	ns
Timeout After Last Demagnetization Detection	While in soft−start After soft−start complete	$t_{(tout1)}$ $t_{(tout2)}$	80 5.1	100 6.0	120 6.9	μs
CURRENT SENSE						
Current Limit Threshold Voltage	V_{CS} increasing	V_{ILIM1}	0.760	0.800	0.840	V
Leading Edge Blanking Duration	DRV minimum width minus $t_{delay(ILIM1)}$	t_{LEB1}	220	265	330	ns
Current Limit Threshold Propagation Delay	Step V_{CS} 0 V to V_{ILIM1} + 0.5 V, V_{FB} = 4 V	$t_{delay(ILIM1)}$	–	95	175	ns
PWM Comparator Propagation Delay	Step V_{CS} 0 V to 0.7 V, V_{FB} = 2.4	$t_{delay(PWM)}$	–	125	175	ns
Minimum Peak Current Freeze Setpoint		V_{freeze}	170	200	230	mV
Abnormal Overcurrent Fault Threshold	V_{CS} increasing, V_{FB} = 4 V	V_{ILIM2}	1.125	1.200	1.275	V
Abnormal Overcurrent Fault Blanking Duration	DRV minimum width minus $t_{delay(ILIM2)}$	t_{LEB2}	80	110	140	ns

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Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
CURRENT SENSE						
Abnormal Overcurrent Fault Propagation Delay	Step V_{CS} 0 V to V_{ILIM2} + 0.5 V, V_{FB} = 4 V	$t_{delay(ILIM2)}$	–	80	175	ns
Number of Consecutive Abnormal Overcurrent Faults to Enter Latch Mode		n_{ILIM2}	–	4	–	
Overpower Protection Delay	V_{CS} dv/dt = 1 V/μs, measured from $V_{OPP(MAX)}$ to DRV falling edge	$t_{OPP(delay)}$	–	95	175	ns
Overpower Signal Blanking Delay		$t_{OPP(blank)}$	220	280	330	ns
Pull−Up Current Source	V_{CS} = 1.5 V	I_{CS}	0.7	1.0	1.5	μA
JITTERING (All Except Version B6)						
Jitter Frequency		f_{jitter}	1.0	1.3	1.6	kHz
Peak Jitter Voltage Added to PWM Comparator		V_{jitter}	90	100	115	mV
FAULT PROTECTION						
Soft−Start Period	Measured from 1st DRV pulse to V_{CS} = V_{ILIM1}	t_{SSTART}	2.8	4.0	5.0	ms
Flyback Overload Fault Timer	V_{CS} = V_{ILIM1}	t_{OVLD}	120	160	200	ms
Overvoltage Protection (OVP) Threshold	V_{Fault} increasing	$V_{Fault(OVP)}$	2.79	3.00	3.21	V
OVP Detection Delay	V_{Fault} increasing	$t_{delay(OVP)}$	22.5	30	37.5	μs
Overtemperature Protection (OTP) Threshold (Note 3)	V_{Fault} decreasing	$V_{Fault(OTP_in)}$	380	400	420	mV
Overtemperature Protection (OTP) Exiting Threshold (Note 3)	V_{Fault} increasing Versions B Only	$V_{Fault(OTP_out)}$	874	910	966	mV
OTP Detection Delay	V_{Fault} decreasing	$t_{delay(OTP)}$	22.5	30	37.5	μs
OTP Pull−Up Current Source	V_{Fault} = $V_{Fault(OTP_in)}$ + 0.2 V	I_{OTP}	42.5	45.0	48.5	μA
Fault Input Clamp Voltage		$V_{Fault(clamp)}$	1.15	1.7	2.25	V
Fault Input Clamp Series Resistor		$R_{Fault(clamp)}$	1.32	1.55	1.78	kΩ
Autorecovery Timer		$t_{restart}$	1.8	2.0	2.2	s
LIGHT/NO LOAD MANAGEMENT						
Minimum Frequency Clamp		f_{MIN}	21.5	25	27.0	kHz
Dead−Time Added During Frequency Foldback	V_{FB} = 400 mV	$t_{DT(MAX)}$	34	–	–	μs
Quiet−Skip Timer		t_{quiet}	1.25	–	–	ms
Skip Threshold	V_{FB} decreasing	V_{skip}	350	400	450	mV
Skip Hysteresis	V_{FB} increasing	$V_{skip(HYS)}$	20	50	70	mV
THERMAL PROTECTION						
Thermal Shutdown	Temperature increasing	T_{SHDN}	–	140	–	°C
Thermal Shutdown Hysteresis	Temperature decreasing	$T_{SHDN(HYS)}$	–	40	–	°C

3. NTC with R110 = 8.8 kΩ

INTRODUCTION

The NCP1340 implements a quasi−resonant flyback converter utilizing current−mode architecture where the switch−off event is dictated by the peak current. This IC is an ideal candidate where low parts count and cost effectiveness are the key parameters, particularly in ac−dc adapters, open−frame power supplies, etc. The NCP1340 incorporates all the necessary components normally needed in modern power supply designs, bringing several enhancements such as non−dissipative overpower protection (OPP), brownout protection, and frequency reduction management for optimized efficiency over the entire power range. Accounting for the needs of extremely low standby power requirements, the controller features minimized current consumption and includes an automatic X2 capacitor discharge circuit that eliminates the need to install power−consuming resistors across the X2 input capacitors.

- **High−Voltage Start−Up Circuit:** Low standby power consumption cannot be obtained with the classic resistive start−up circuit. The NCP1340 incorporates a high−voltage current source to provide the necessary current during start−up and then turns off during normal operation.
- **Internal Brownout Protection:** The ac input voltage is sensed via the high−voltage pin. When this voltage is too low, the NCP1340 stops switching. No restart attempt is made until the ac input voltage is back within its normal range.
- **X2−Capacitor Discharge Circuitry:** Per the IEC60950 standard, the time constant of the X2 input capacitors and their associated discharge resistors must be less than 1 s in order to avoid electrical shock when the user unplugs the power supply and inadvertently touches the ac input cord terminals. By providing an automatic means to discharge the X2 capacitors, the NCP1340 eliminates the need to install X2 discharge resistors, thus reducing power consumption.
- **Quasi−Resonant, Current−Mode Operation:** Quasi−Resonant (QR) mode is a highly efficient mode of operation where the MOSFET turn−on is synchronized with the point where its drain−source voltage is at the minimum (valley). A drawback of this mode of operation is that the operating frequency is inversely proportional to the system load. The NCP1340 incorporates a valley lockout (VLO) and frequency foldback technique to eliminate this drawback, thus maximizing the efficiency over the entire power range.
- **Valley Lockout:** In order to limit the maximum frequency while remaining in QR mode, one would traditionally use a frequency clamp. Unfortunately, this can cause the controller to jump back and forth between two different valleys, which is often undesirable. The NCP1340 patented VLO circuitry solves this issue by determining the operating valley based on the system load, and locking out other valleys unless a significant change in load occurs.
- **Frequency Foldback:** As the load continues to decrease, it becomes beneficial to reduce the switching frequency. When the load is light enough, the NCP1340 enters frequency foldback mode. During this mode, the peak current is frozen and dead−time is added to the switching cycle, thus reducing the frequency and switching operation to discontinuous conduction mode (DCM). Dead−time continues to be added until skip mode is reached, or the switching frequency reaches its minimum level of 25 kHz.
- **Skip Mode:** To further improve light or no−load power consumption while avoiding audible noise, the NCP1340 enters skip mode when the operating frequency reaches its minimum value. foldback isavoid acoustic noise, the circuit prevents the switching frequency from decaying below 25 kHz. This allows regulation via burst of pulses at 25 kHz or greater instead of operating in the audible range.
- **Quiet−Skip:** To further reduce acoustic noise, the NCP1340 incorporates a novel circuit to prevent the skip mode burst period from entering the audible range as well.
- **Internal OPP:** In order to limit power delivery at high line, a scaled version of the negative voltage present on the auxiliary winding during the on−time is routed to the ZCD/OPP pin. This provides the designer with a simple and non−dissipative means to reduce the maximum power capability as the bulk voltage increases.
- **Frequency Jittering:** In order to reduce the EMI signature, a low frequency triangular voltage waveform is added to the iniput of the PWM comparator. This helps by spreading out the energy peaks during noise analysis.
- **Internal Soft−Start:** The NCP1340 includes a 4 ms soft−start to prevent the main power switch from being overly stressed during start−up. Soft−start is activated each time a new startup sequence occurs or during auto−recovery mode.
- **Dedicated Fault Input:** The NCP1340 includes a dedicated fault input. It can be used to sense an overvoltage condition and latch off the controller by pulling the pin above the overvoltage protection (OVP) threshold. The controller is also disabled if the Fault pin is pulled below the overtemperature protection (OTP) threshold. The OTP threshold is configured for use with a NTC thermistor.

- **Overload/Short−Circuit Protection:** The NCP1340 implements overload protection by limiting the maximum time duration for operation during overload conditions. The overload timer operates whenever the maximum peak current is reached. In addition to this, special circuitry is included to prevent operation in CCM during extreme overloads, such as an output short−circuit.
- **Maximum Frequency Clamp:** The NCP1340 includes a maximum frequency clamp. In all versions, the clamp is available disabled or fixed at 110 kHz. In the 9−pin versions, the clamp can be adjusted via an external resistor from the FMAX Pin to ground. It can also be disabled by pulling the FMAX pin above 4 V.

HIGH VOLTAGE START−UP

The NCP1340 contains a multi−functional high voltage (HV) pin. While the primary purpose of this pin is to reduce standby power while maintaining a fast start−up time, it also incorporates brownout detection and line removal detection.

The HV pin must be connected directly to the ac line in order for the X2 discharge circuit to function correctly. Line and neutral should be diode “ORed” before connecting to the HV pin as shown in Figure 4. The diodes prevent the pin voltage from going below ground. A resistor in series with the pin should be used to protect the pin during EMC or surge testing. A low value resistor should be used (<5 kΩ) to reduce the voltage offset during start−up.

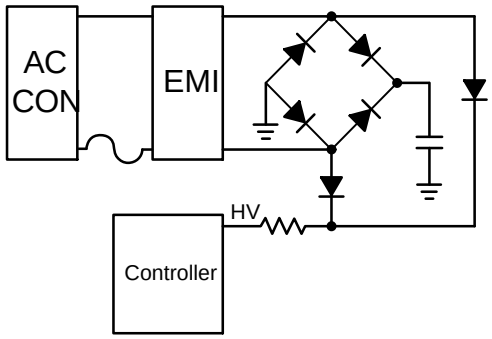


Figure 4. High−Voltage Input Connection

Start−up and V_{CC} Management

During start−up, the current source turns on and charges the V_{CC} capacitor with I_{start2} (typically 6 mA). When V_{cc} reaches $V_{CC(on)}$ (typically 16.0 V), the current source turns off. If the input voltage is not high enough to ensure a proper start−up (i.e. V_{HV} has not reached $V_{BO(start)}$), the controller will not start. V_{CC} then begins to fall because the controller bias current is at I_{CC2} (typically 1 mA) and the auxiliary supply voltage is not present. When V_{CC} falls to $V_{CC(off)}$ (typically 10.5 V), the current source turns back on and charges V_{CC}. This cycle repeats indefinitely until V_{HV} reaches $V_{BO(start)}$. Once this occurs, the current source immediately turns on and charges V_{CC} to $V_{CC(on)}$, at which point the controller starts (see Figure 6).

When V_{CC} is brought below $V_{CC(inhibit)}$, the start−up current is reduced to I_{start1} (typically 0.5 mA). This limits power dissipation on the device in the event that the V_{CC} pin is shorted to ground. Once V_{CC} rises back above $V_{CC(inhibit)}$, the start−up current returns to I_{start2}.

Once V_{CC} reaches $V_{CC(on)}$, the controller is enabled and the controller bias current increases to I_{CC3} (typically 2.0 mA). However, the total bias current is greater than this due to the gate charge of the external switching MOSFET. The increase in I_{CC} due to the MOSFET is calculated using Equation 1.

$$\Delta I_{CC} = f_{sw} \cdot Q_G \cdot 10^{-3} \quad \text{(eq. 1)}$$

where ΔI_{CC} is the increase in milliamps, f_{sw} is the switching frequency in kilohertz and Q_G is the gate charge of the external MOSFET in nanocoulombs.

C_{VCC} must be sized such that a V_{CC} voltage greater than $V_{CC(off)}$ is maintained while the auxiliary supply voltage increases during start−up. If C_{VCC} is too small, V_{CC} will fall below $V_{CC(off)}$ and the controller will turn off before the auxiliary winding supplies the IC. The total I_{CC} current after the controller is enabled (I_{CC3} plus ΔI_{CC}) must be considered to correctly size C_{VCC}.

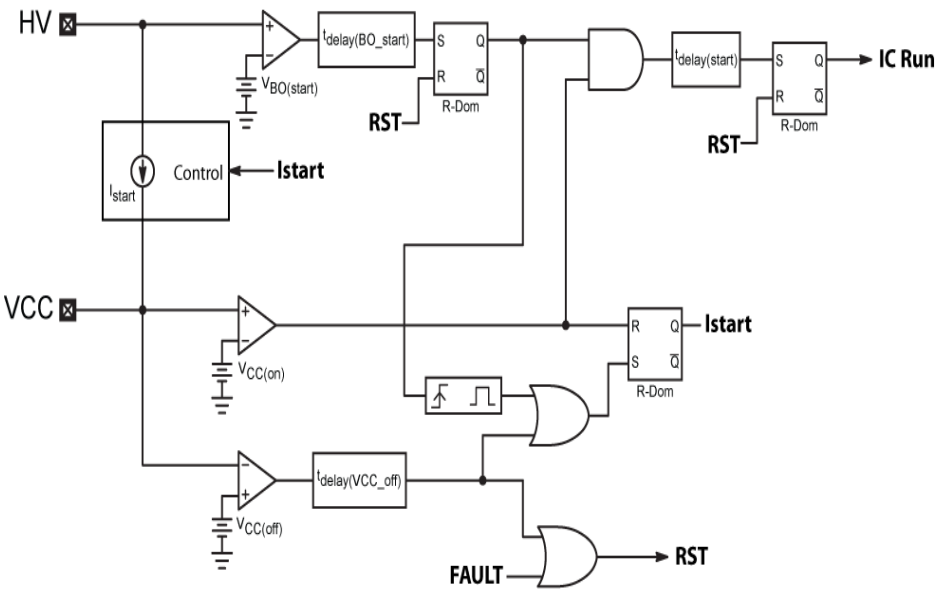


Figure 5. Start−up Circuitry Block Diagram

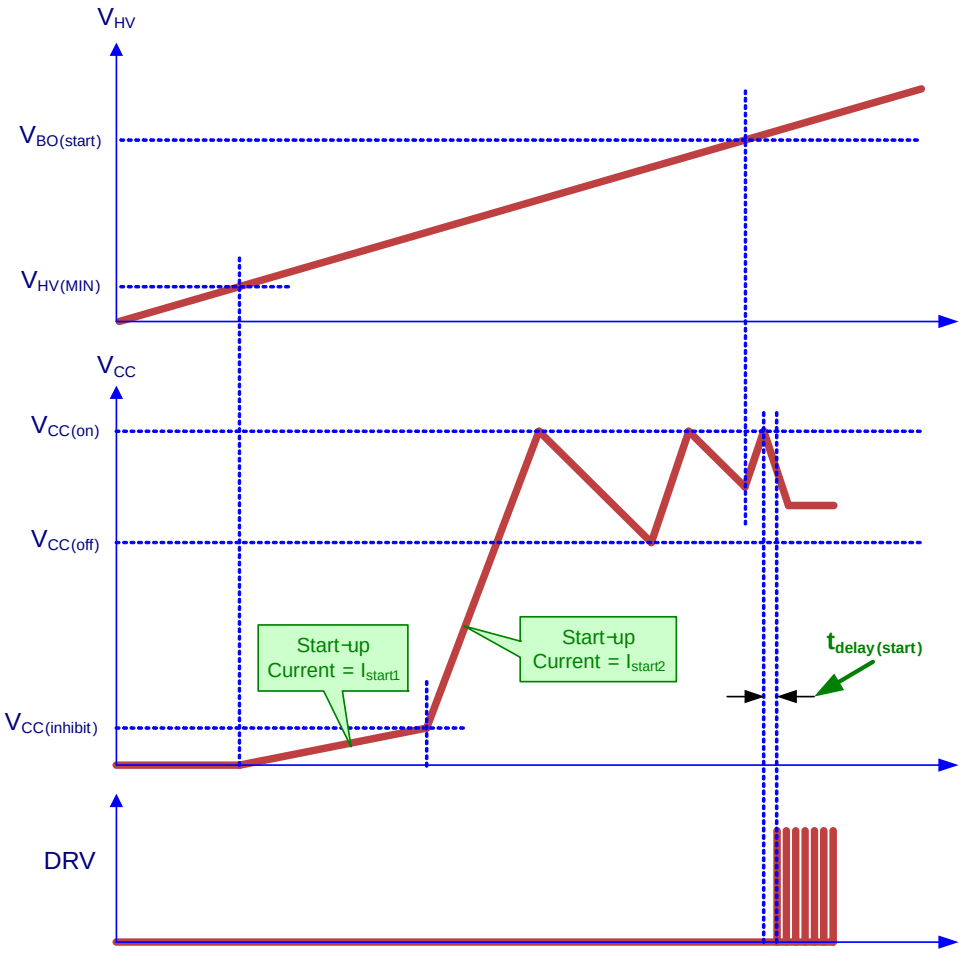


Figure 6. Start−up Timing

DRIVER

The NCP1340 maximum supply voltage, $V_{CC(MAX)}$, is 28 V. Typical high−voltage MOSFETs have a maximum gate voltage rating of 20 V. The DRV pin incorporates an active voltage clamp to limit the gate voltage on the external MOSFETs. The DRV voltage clamp, $V_{DRV(high)}$ is typically 12 V with a maximum limit of 14 V.

REGULATION CONTROL

Peak Current Control

The NCP1340 is a peak current−mode controller, thus the FB voltage sets the peak current flowing in the transformer and the MOSFET. This is achieved by sensing the MOSFET current across a resistor and applying the resulting voltage ramp to the non−inverting input of the PWM comparator through the CS pin. The current limit threshold is set by applying the FB voltage divided by K_{FB} (typically 4) to the inverting input of the PWM comparator. When the current sense voltage ramp exceeds this threshold, the output driver is turned off, however, the peak current is affected by several functions (see Figure 7):

The peak current level is clamped during the soft−start phase. The setpoint is actually limited by a clamp level ramping from 0 to 0.8 V within 4 ms.

In addition to the PWM comparator, a dedicated comparator monitors the current sense voltage, and if it reaches the maximum value, V_{ILIM} (typically 800 mV), the gate driver is turned off and the overload timer is enabled. This occurs even if the limit imposed by the feedback voltage is higher than V_{ILIM1}. Due to the parasitic capacitances of the MOSFET, a large voltage spike often appears on the CS Pin at turn−on. To prevent this spike from falsely triggering the current sense circuit, the current sense signal is blanked for a short period of time, t_{LEB1} (typically 275 ns), by a leading edge blanking (LEB) circuit. Figure 7 shows the schematic of the current sense circuit.

The peak current is also limitied to a minimum level, V_{freeze} (0.2 V, typically). This results in higher efficiency at light loads by increasing the minimum energy delivered per switching cycle, while reducing the overall number of switching cycles during light load.

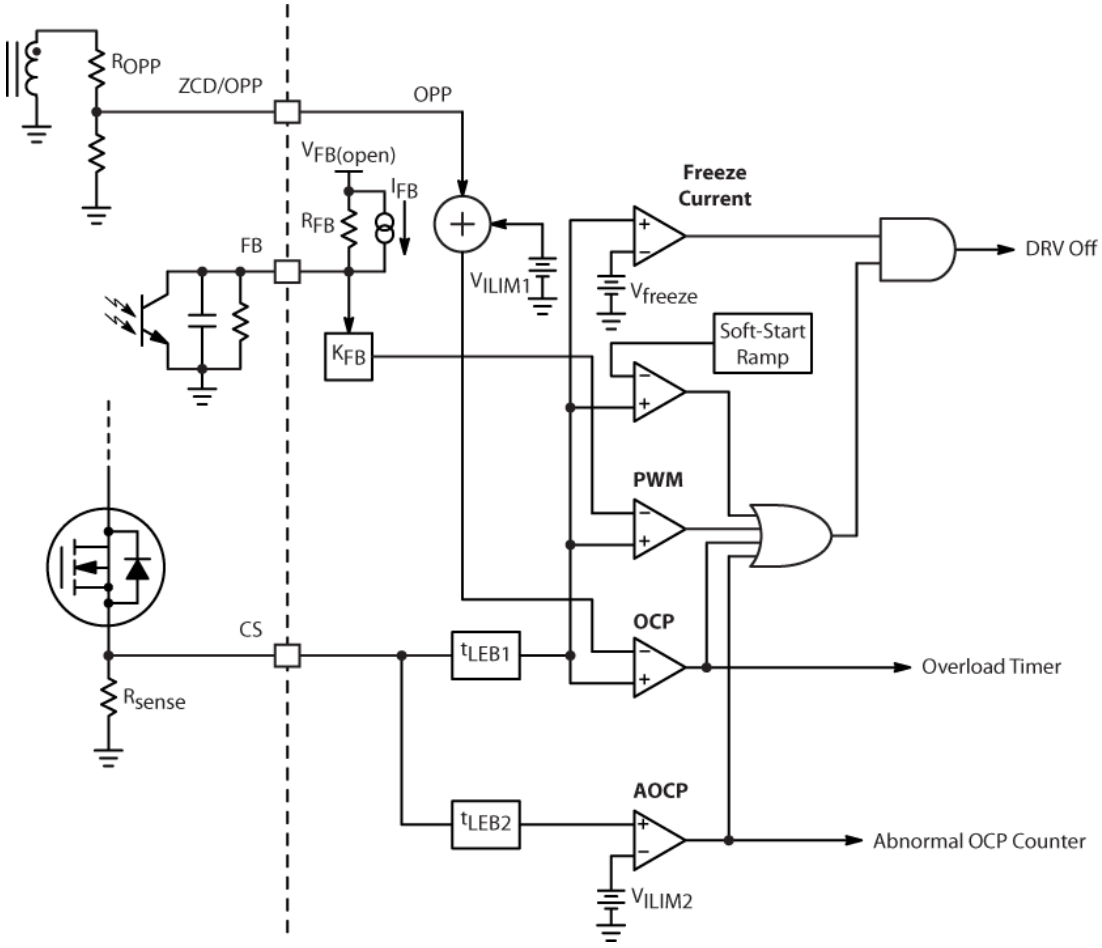


Figure 7. Current Sense Logic

Zero Current Detection

The NCP1340 is a quasi−resonant (QR) flyback controller. While the power switch turn−off is determined by the peak current set by the feedback loop, the switch turn−on is determined by the transformer demagnetization. The demagnetization is detected by monitoring the transformer auxiliary winding voltage.

Turning on the power switch once the transformer is demagnetized has the benefit of reduced switching losses. Once the transformer is demagnetized, the drain voltage starts ringing at a frequency determined by the transformer magnetizing inductance and the drain lump capacitance, eventually settling at the input voltage. A QR flyback controller takes advantage of the drain voltage ringing and turns on the power switch at the drain voltage minimum or “valley” to reduce switching losses and electromagnetic interference (EMI).

As shown by Figure 13, a valley is detected once the ZCD pin voltage falls below the demagnetization threshold, $V_{ZCD(trig)}$, typically 55 mV. The controller will either switch once the valley is detected or increment the valley counter, depending on the FB voltage.

Overpower Protection

The average bulk capacitor voltage of the QR flyback varies with the RMS line voltage. Thus, the maximum power capability at high line can be much higher than desired. An integrated overpower protection (OPP) circuit provides a relatively constant output power limit across the input voltage on the bulk capacitor, V_{bulk}. Since it is a high−voltage rail, directly measuring V_{bulk} will contribute losses in the sensing network that will greatly impact the standby power consumption. The NCP1340 OPP circuit achieves this without the need for a high−voltage sensing network, and is essentially lossless.

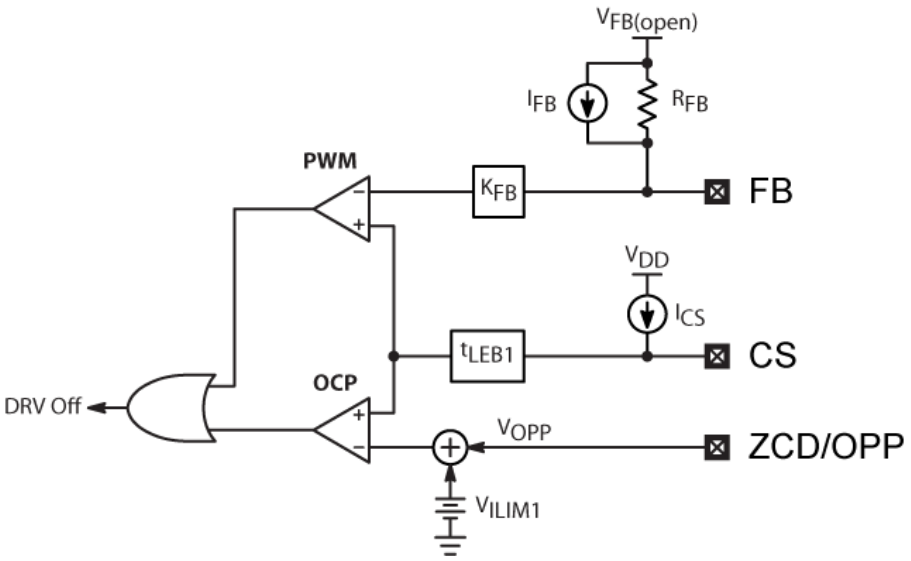


Figure 8. OPP Circuit Schematic

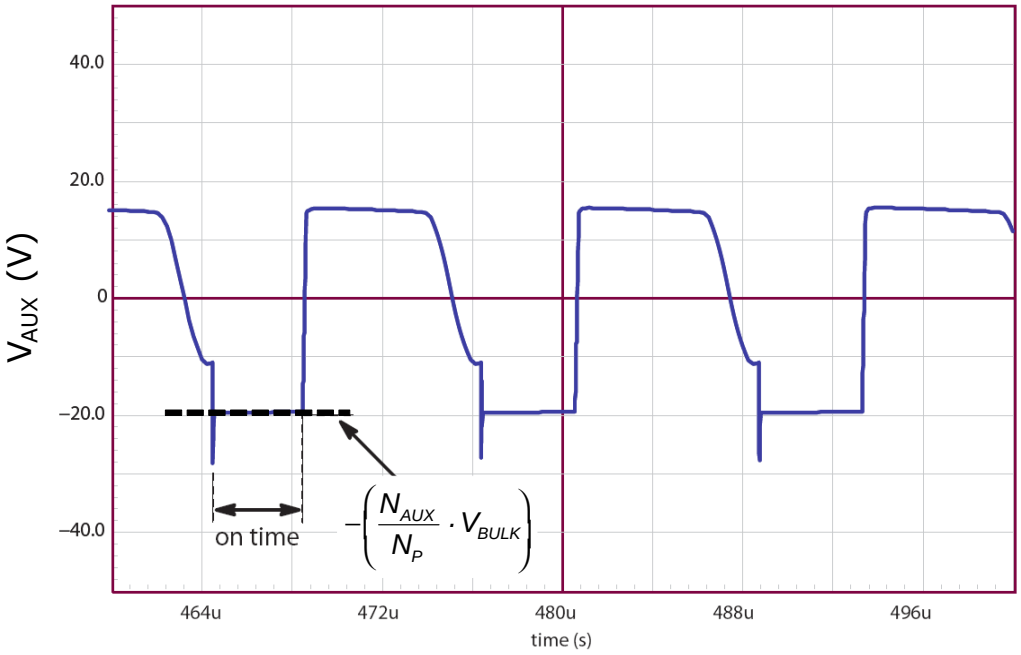


Figure 9. Auxiliary Winding Voltage

Since the auxiliary winding voltage during the power switch on time is a reflection of the input voltage scaled by the primary to auxiliary winding turns ratio, $N_{P:AUX}$ (see Figure 9), OPP is achieved by scaling down reflected voltage during the on−time and applying it to the ZCD pin as a negative voltage, V_{OPP}. The voltage is scaled down by a resistor divider comprised of R_{OPPU} and R_{OPPL}. The maximum internal current setpoint ($V_{CS(OPP)}$) is simply the sum of V_{OPP} and the peak current sense threshold, V_{ILIM1}. Figure 8 shows the schematic for the OPP circuit.

The adjusted peak current limit is calculated using Equation 2. For example, a V_{OPP} of −150 mV results in a peak current limit of 650 mV in NCP1340.

$$V_{CS(OPP)} = V_{OPP} + V_{ILIM1} \qquad \text{(eq. 2)}$$

To ensure optimal zero−crossing detection, a diode is needed to bypass R_{OPPU} during the off−time. Equation 3 is used to calculate R_{OPPU} and R_{OPPL}.

$$\frac{R_{ZCD} + R_{OPPU}}{R_{OPPL}} = -\frac{N_{P:AUX} \cdot V_{bulk} - V_{OPP}}{V_{OPP}} \qquad \text{(eq. 3)}$$

R_{OPPU} is selected once a value is chosen for R_{OPPL}. R_{OPPL} is selected large enough such that enough voltage is available for the zero−crossing detection during the off−time. It is recommended to have at least 8 V applied on the ZCD pin for good detection. The maximum voltage is internally clamped to V_{CC}. The off−time voltage on the ZCD Pin is given by Equation 4.

$$V_{ZCD} = \frac{R_{OPPL}}{R_{ZCD} + R_{OPPL}} \cdot (V_{AUX} - V_F) \qquad \text{(eq. 4)}$$

Where V_{AUX} is the voltage across the auxiliary winding and V_F is the D_{OPP} forward voltage drop.

The ratio between R_{ZCD} and R_{OPPL} is given by Equation 5. It is obtained by combining Equations 3 and 4.

$$\frac{R_{ZCD}}{R_{OPPL}} = \frac{V_{AUX} - V_F - V_{ZCD}}{V_{ZCD}} \qquad \text{(eq. 5)}$$

A design example is shown below:

System Parameters:

V_{AUX} = 18 V

V_F = 0.6 V

$N_{P:AUX}$ = 0.18

The ratio between R_{ZCD} and R_{OPPL} is calculated using Equation 5 for a minimum V_{ZCD} of 8 V.

$$\frac{R_{ZCD}}{R_{OPPL}} = \frac{18\ V - 0.6\ V - 8\ V}{8\ V} = 1.2\ k\Omega$$

R_{ZCD} is arbitrarily set to 1 kΩ. R_{OPPL} is also set to 1 kΩ because the ratio between the resistors is close to 1.

The NCP1340 maximum overpower compensation or peak current setpoint reduction is 31.25% for a V_{OPP} of −250 mV. We will use this value for the following example:

Substituting values in Equation 3 and solving for R_{OPPU} we obtain:

$$\frac{R_{ZCD} + R_{OPPU}}{R_{OPPL}} = \frac{0.18 \cdot 370\ V - (-0.25\ V)}{-0.25\ V} = 271$$

$$R_{OPPU} = 271 \cdot R_{OPPL} - R_{ZCD}$$

$$R_{OPPU} = 271 \cdot 1\ k\Omega - 1\ k\Omega = 270\ k\Omega$$

For optimum performance over temperature, it is recommended to keep R_{OPPL} below 3 kΩ.

Soft−Start

Soft−start is achieved by ramping up an internal reference, V_{SSTART}, and comparing it to the current sense signal. V_{SSTART} ramps up from 0 V once the controller initially powers up. The peak current setpoint is then limited by the V_{SSTART} ramp resulting in a gradual increase of the switch current during start−up. The soft−start duration, t_{SSTART}, is typically 4 ms.

During startup, demagnetization phases are long and difficult to detect since the auxiliary winding voltage is very small. In this condition, the 6 μs steady−state timeout is generally shorter than the inductor demagnetization period. If it is used to restart a switching cycle, it can cause operation in CCM for several cycles until the voltage on the ZCD pin is high enough to prevent the timer from running. Therefore, a longer timeout period, t_{tout1} (typically 100 μs), is used during soft−start to prevent CCM operation.

Frequency Jittering

In order to help meet stringent EMI requirements, the NCP1340 features frequency jittering to average the energy peaks over the EMI frequency range. As shown in Figure 10, the function consists of summing a 0 to 100 mV, 1.3 kHz triangular wave (V_{jitter}) with the CS signal immediately before the PWM comparator. This current acts to modulate the on−time and hence the operation frequency.

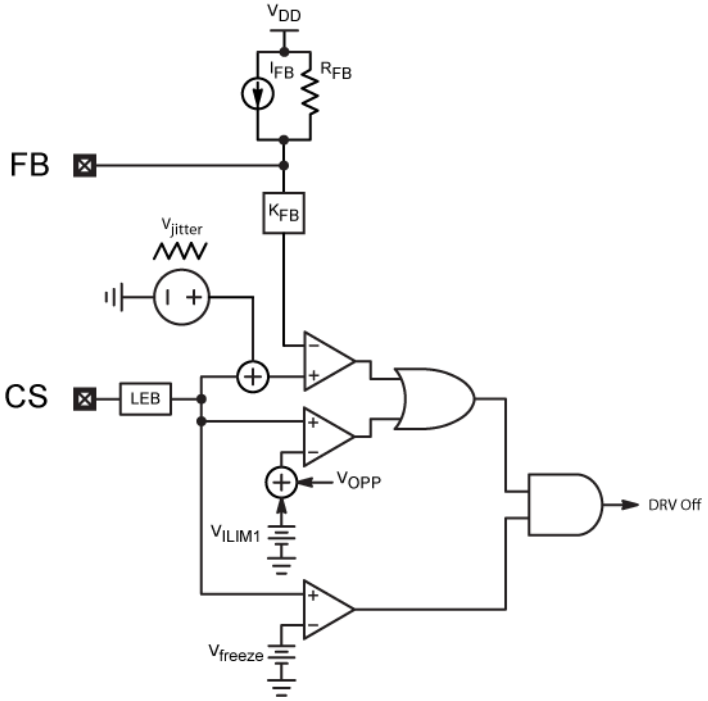


Figure 10. Jitter Implementation

Since the jittering function modulates the peak current level, the FB signal will attempt to compensate for this effect in order to limit the output voltage ripple. Therefore, the bandwidth of the feedback loop must be well below the jitter frequency, or the jitter function will be filtered by the loop.

Due to the frozen peak current, the effect of the jittering circuit will not be seen during frequency foldback mode.

Maximum Frequency Clamp

The NCP1340 includes a maximum frequency clamp. In all versions, the clamp is available disabled or fixed at 110 kHz. In the 9−pin versions, the clamp can be adjusted via an external resistor from the FMAX Pin to ground. It can also be disabled by pulling the FMAX pin above 4 V. The maximum frequency can be programmed using Equation 6, and is shown in Figure 11.

$$F_{SW(MAX)} = \frac{261\ kHz * 1\ V}{R_{FMAX} * 10\ \mu A} \qquad \text{(eq. 6)}$$

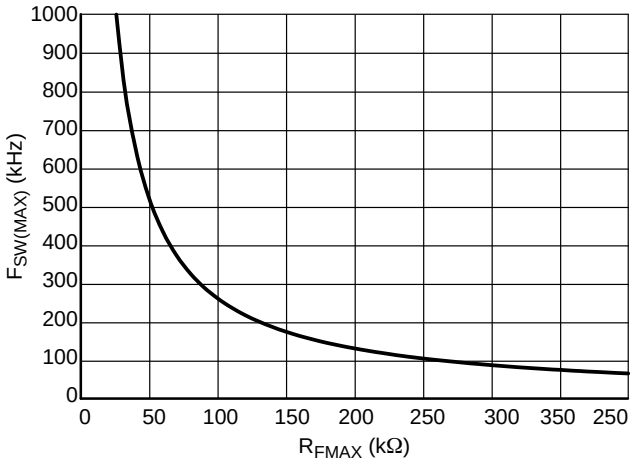


Figure 11. $F_{SW(MAX)}$ vs. R_{FMAX}

LIGHT LOAD MANAGEMENT

Valley Lockout Operation

The operating frequency of a traditional QR flyback controller is inversely proportional to the system load. In other words, a load reduction increases the operating frequency. A maximum frequency clamp can be useful to limit the operating frequency range. However, when used by itself, such an approach often causes instabilities since when this clamp is active, the controller tends to jump (or hesitate) between two valleys, thus generating audible noise.

Instead, the NCP1340 also incorporates a patented valley lockout (VLO) circuitry to eliminate valley jumping. Once a valley is selected, the controller stays locked in this valley until the output power changes significantly. This technique extends the QR mode operation over a wider output power range while maintaining good efficiency and limiting the maximum operating frequency.

The operating valley (1st, 2nd, 3rd, 4th, 5th or 6th) is determined by the FB voltage. An internal counter increments each time a valley is detected by the ZCD/OPP Pin. Figure 12 shows a typical frequency characteristic obtainable at low line in a 65 W application.

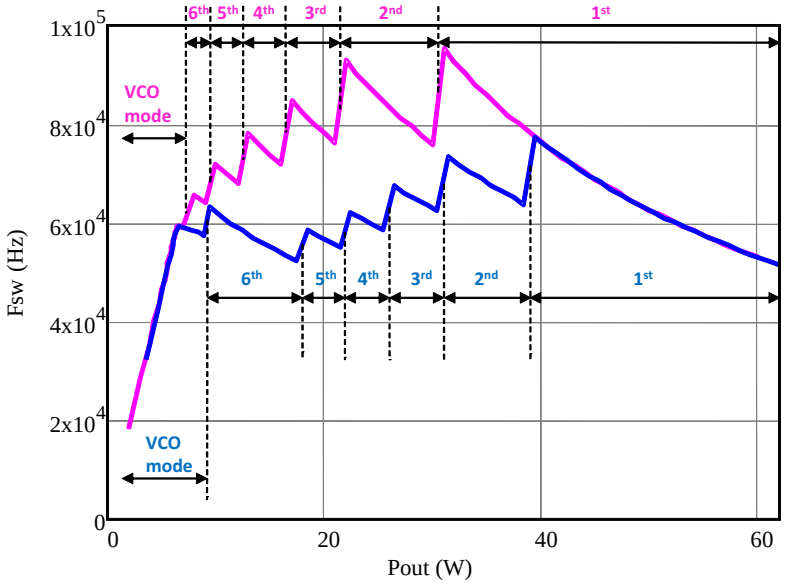


Figure 12. Valley Lockout Frequency vs. Output Power

When an “n” valley is asserted by the valley selection circuitry, the controller is locked in this valley until the FB voltage decreases to the lower threshold (“n+1” valley activates) or increases to the “n valley threshold” + 600 mV (“n−1” valley activates). The regulation loop adjusts the peak current to deliver the necessary output power. Each valley selection comparator features a 600 mV hysteresis that helps stabilize operation despite the FB voltage swing produced by the regulation loop.

Table 6. VALLEY FB THRESHOLDS (typical values)

FB Falling		FB Rising	
1st to 2nd valley	1.400 V	2nd to 1st valley	2.000 V
2nd to 3rd valley	1.200 V	3rd to 2nd valley	1.800 V
3rd to 4th valley	1.100 V	4th to 3rd valley	1.700 V
4th to 5th valley	1.000 V	5th to 4th valley	1.600 V
5th to 6th valley	0.900 V	6th to 5th valley	1.500 V

Valley Timeout

In case of extremely damped oscillations, the ZCD comparator may not be able to detect the valleys. In this condition, drive pulses will stop while the controller waits for the next valley or ZCD event. The NCP1340 ensures continued operation by incorporating a maximum timeout period after the last demagnetization detection. The timeout signal acts as a substitute for the ZCD signal to the valley counter. Figure 13 shows the valley timeout circuit schematic. The steady state timeout period, t_{tout2}, is set at 6 μs (typical) to limit the frequency step.

During startup, the voltage offset added by the OPP diode, D_{OPP}, prevents the ZCD Comparator from accurately detecting the valleys. In this condition, the steady state timeout period will be shorter than the inductor demagnetization period causing CCM operation. CCM operation lasts for a few cycles until the voltage on the ZCD pin is high enough to detect the valleys. A longer timeout period, t_{tout1}, (typically 100 μs) is set during soft−start to limit CCM operation.

In VLO operation, the number of timeout periods are counted instead of valleys when the drain−source voltage oscillations are too damped to be detected. For example, if the FB voltage sets VLO mode to turn on at the fifth valley, and the ZCD ringing is damped such that the ZCD circuit is only able to detect:

- Valleys 1 to 4: the circuit generates a DRV pulse 6 μs (steady−state timeout delay) after the 4th valley detection.
- Valleys 1 to 3: the timeout delay must run twice, and the circuit generates a DRV pulse 12 μs after the 3rd valley detection.

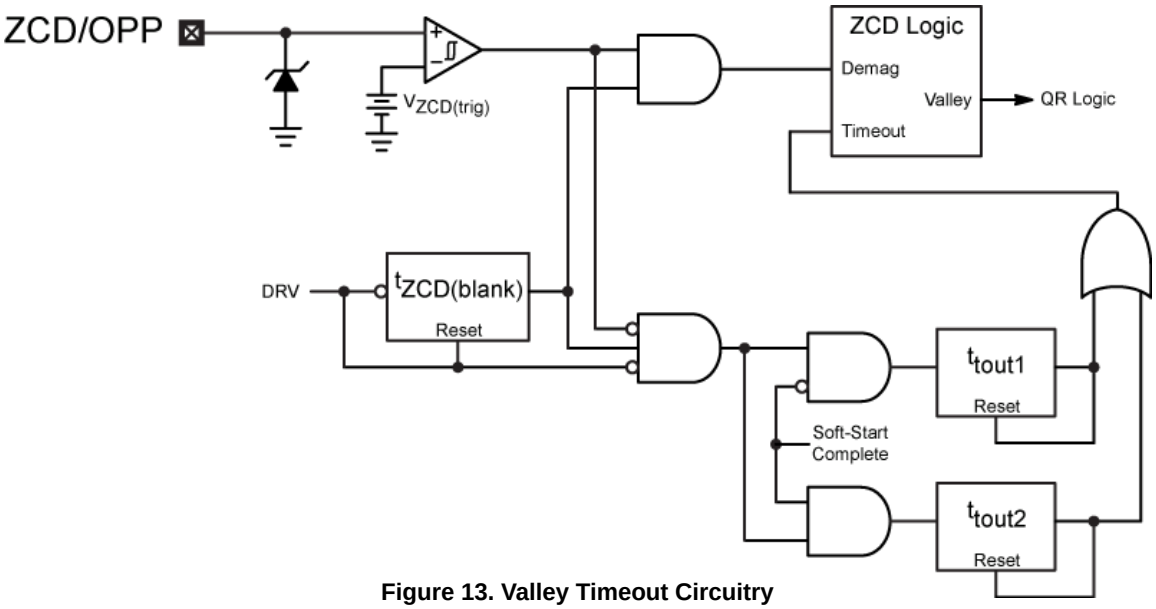


Figure 13. Valley Timeout Circuitry

Frequency Foldback

As the output load decreases (FB voltage decreases), the valleys are incremented from 1 to 6. When the sixth valley is reached, if the FB voltage further decreases to 0.8 V, the peak current setpoint becomes internally frozen to V_{freeze} (0.2 V typically), and the controller enters frequency foldback mode (FF). During this mode, the controller regulates the power delivery by modulating the switching frequency.

In frequency foldback mode, the controller reduces the switching frequency by adding dead−time after the 6th valley is detected. This dead−time increases as the FB voltage decreases. There is no discontinuity when the system transitions from VLO to FF and the frequency smoothly reduces as FB decreases.

The dead−time circuit is designed to add 0 μs dead−time when V_{FB} = 0.8 V and linearly increases the total dead−time to $t_{DT(MAX)}$ (32 μs minimum) as V_{FB} falls down to 0.4 V. The minimum frequency clamp prevents the switching frequency from dropping below 25 kHz to eliminate the risk of audible noise.

Figure 14 summarizes the VLO to FF operation with respect to the FB voltage.

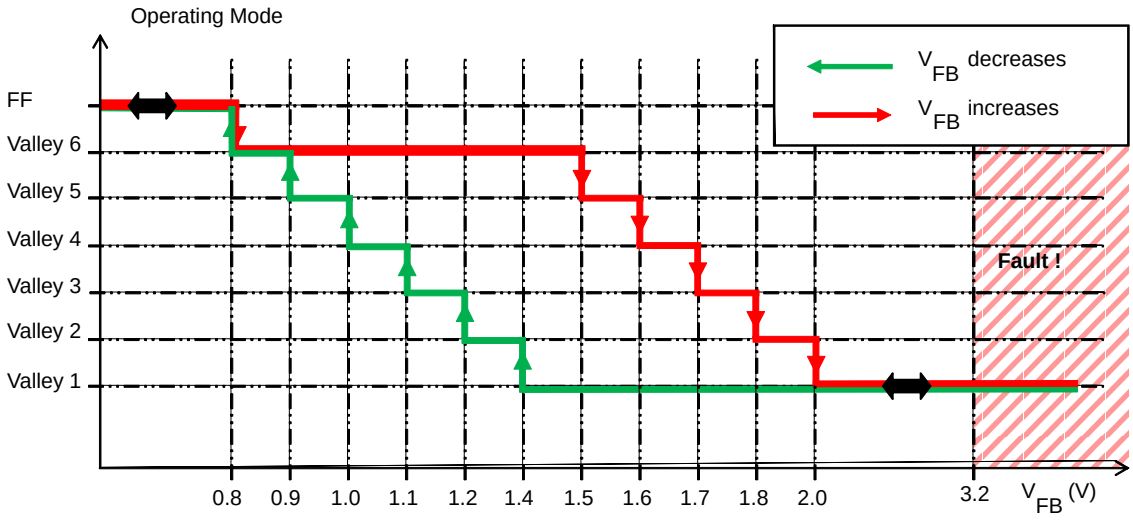


Figure 14. Valley Lockout Thresholds

Minimum Frequency Clamp and Skip Mode

As mentioned previously, the circuit prevents the switching frequency from dropping below f_{MIN} (25 kHz typical). When the switching cycle would be longer than 40 μs, the circuit forces a new switching cycle. However, the f_{MIN} clamp cannot generate a DRV pulse until the demagnetization is completed. In other words, it will not cause operation in CCM.

Since the NCP1340 forces a minimum peak current and a minimum frequency, the power delivery cannot be continuously controlled down to zero. Instead, the circuit starts skipping pulses when the FB voltage drops below the skip level, V_{skip}, and recovers operation when V_{FB} exceeds V_{skip} + $V_{skip(HYS)}$. This skip−mode method provides an efficient method of control during light loads.

Quiet−Skip

To further avoid acoustic noise, the circuit prevents the burst frequency during skip mode from entering the audible range by limiting it to a maximum of 800 Hz. This is achieved via a timer (t_{quiet}) that is activated during Quiet−Skip. The start of the next burst cycle is prevented until this timer has expired.

As the output power decreases, the switching frequency decreases. Once it hits 25 kHz, the skip−in threshold is reached and burst mode is entered − switching stops as soon as the currnet drive pulses ends – it does not stop immediately.

Once switching stops, FB will rise. As soon as FB crosses the skip−exit threshold, drive pulses will resume, but the controller remains in burst mode. At this point, a 1250 μs (min) timer, t_{quiet}, is started together with a count−to−3 counter. The next time the FB voltage drops below the skip−in threshold, drive pulses stop at the end of the current pulse as long as 3 drive pulses have been counted (if not, they do not stop until the end of the 3rd pulse). They are not allowed to start again until the timer expires, even if the skip−exit threshold is reached first. It is important to note that the timer will not force the next cycle to begin – i.e. if the natural skip frequency is such that skip−exit is reached after the timer expires, the drive pulses will wait for the skip−exit threshold.

This means that during no−load, there will be a minimum of 3 drive pulses, and the burst−cycle period will likely be much longer than 1250 μs. This operation helps to improve efficiency at no−load conditions.

In order to exit burst mode, the FB voltage must rise higher than 1 V. If this occurs before t_{quiet} expires, the drive pulses will resume immediately – i.e. the controller won't wait for the timer to expire. Figure 15 provides an example of how Quiet−Skip works.

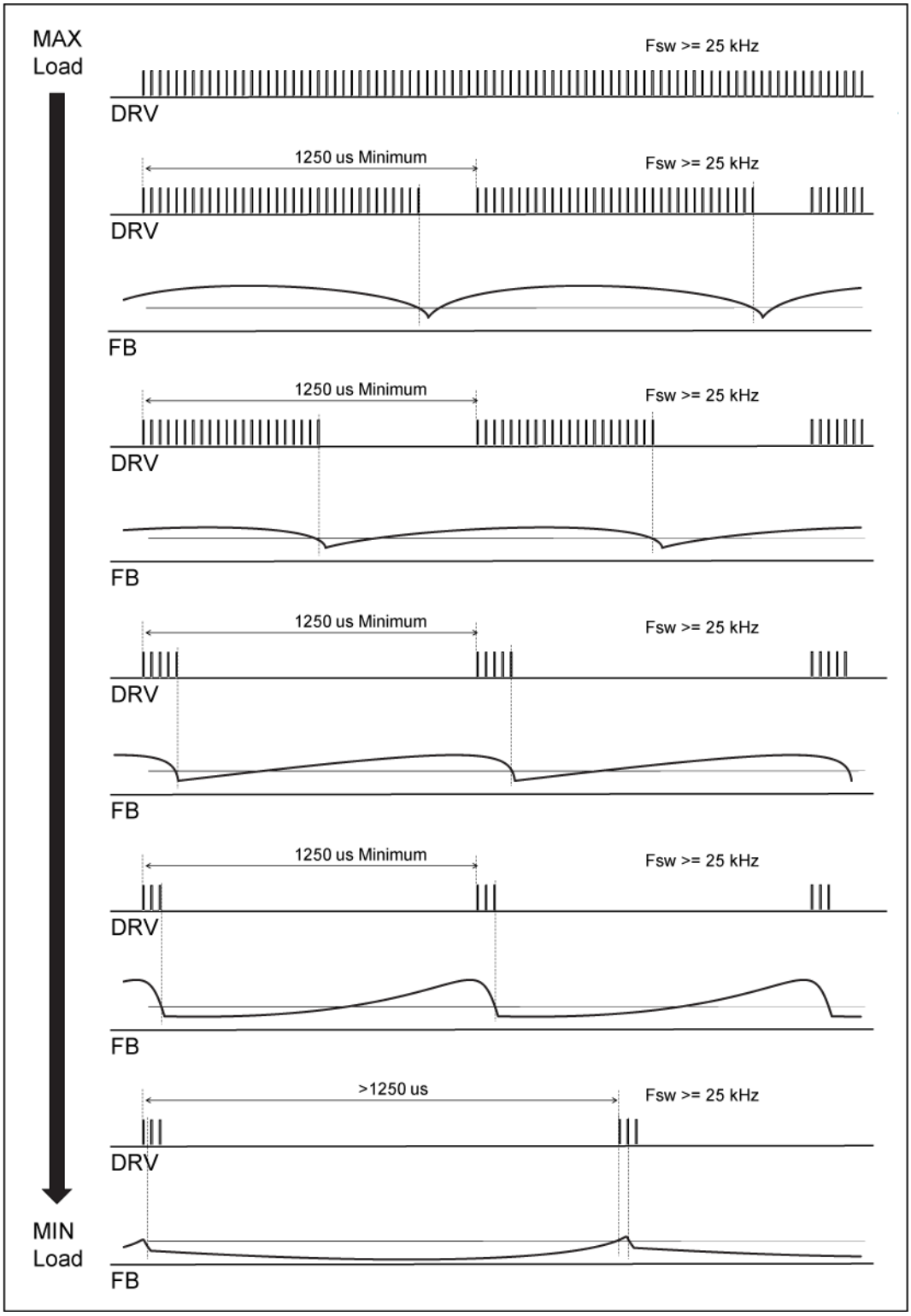


Figure 15. Quiet−Skip Timing Diagram

FAULT MANAGEMENT

The NCP1340 contains three separate fault modes. Depending on the type of fault, the device will either latch off, restart when the fault is removed, or resume operation after the auto−recovery timer expires.

Latching Faults

Some faults will cause the NCP1340 to latch off. These include the abnormal OCP (AOCP), V_{CC} OVP, and the external latch input. When the NCP1340 detects a latching fault, the driver is immediately disabled. The operation during a latching fault is identical to that of a non−latching fault except the controller will not attempt to restart at the next $V_{CC(on)}$, even if the fault is removed. In order to clear the latch and resume normal operation, V_{CC} must first be allowed to drop below $V_{CC(reset)}$ or a line removal event must be detected. This operation is shown in Figure 16.

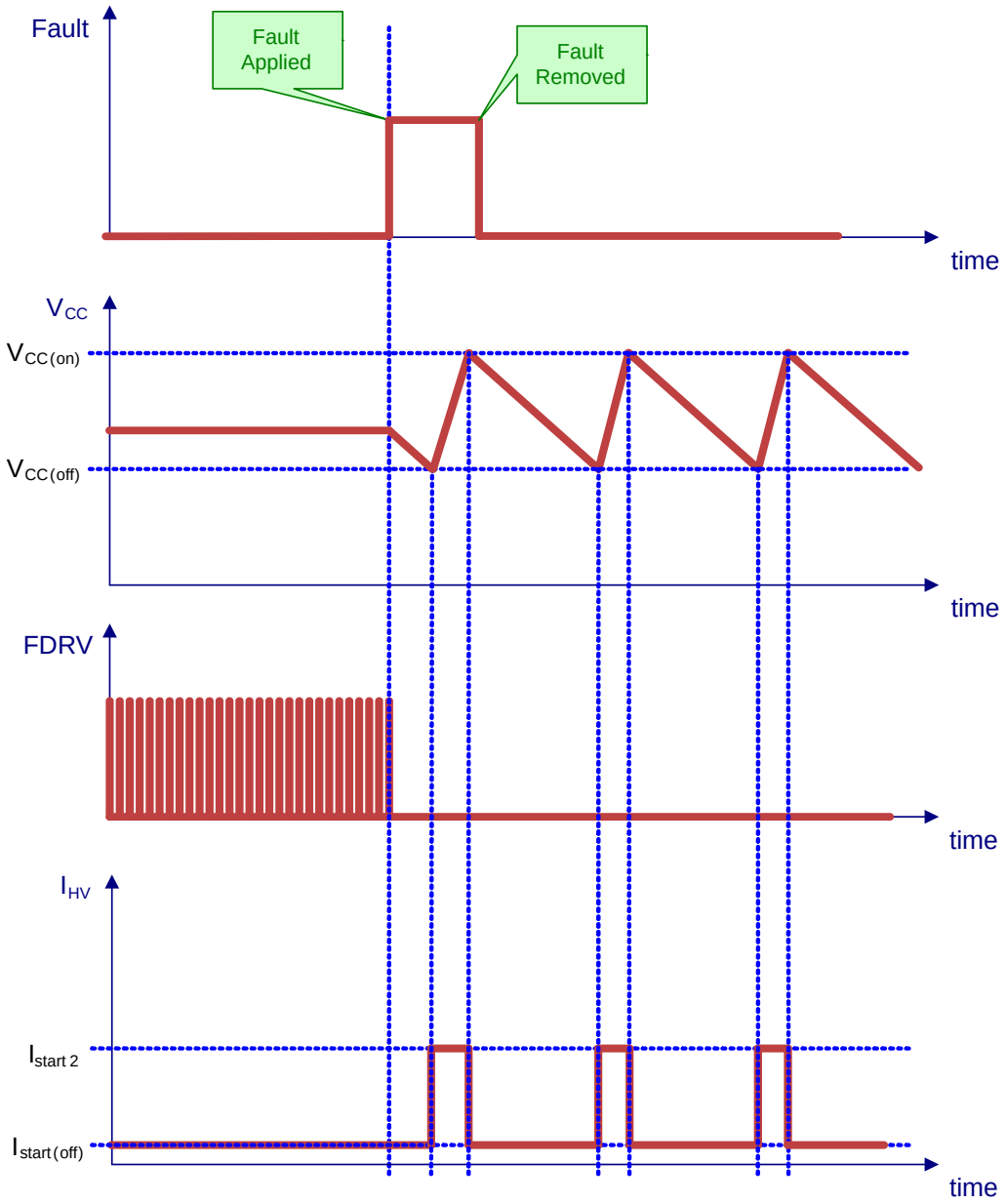


Figure 16. Operation During Latching Fault

Non−Latching Faults

When the NCP1340 detects a non−latching fault (brownout or thermal shutdown), the drivers are disabled, and V_{CC} falls towards $V_{CC(off)}$ due to the IC internal current consumption. Once V_{CC} reaches $V_{CC(off)}$, the HV current source turns on and C_{VCC} begins to charge towards $V_{CC(on)}$. When V_{CC}, reaches $V_{CC(on)}$, the cycle repeats until the fault is removed. Once the fault is removed, the NCP1340 is re−enabled when V_{CC} reaches $V_{CC(on)}$ according to the initial power−on sequence, provided V_{HV} is above $V_{BO(start)}$. This operation is shown in Figure 17. When V_{HV} is reaches $V_{BO(start)}$, V_{CC} immediately charges to $V_{CC(on)}$. If V_{CC} is already above $V_{CC(on)}$ when the fault is removed, the controller will start immediately as long as V_{HV} is above $V_{BO(start)}$.

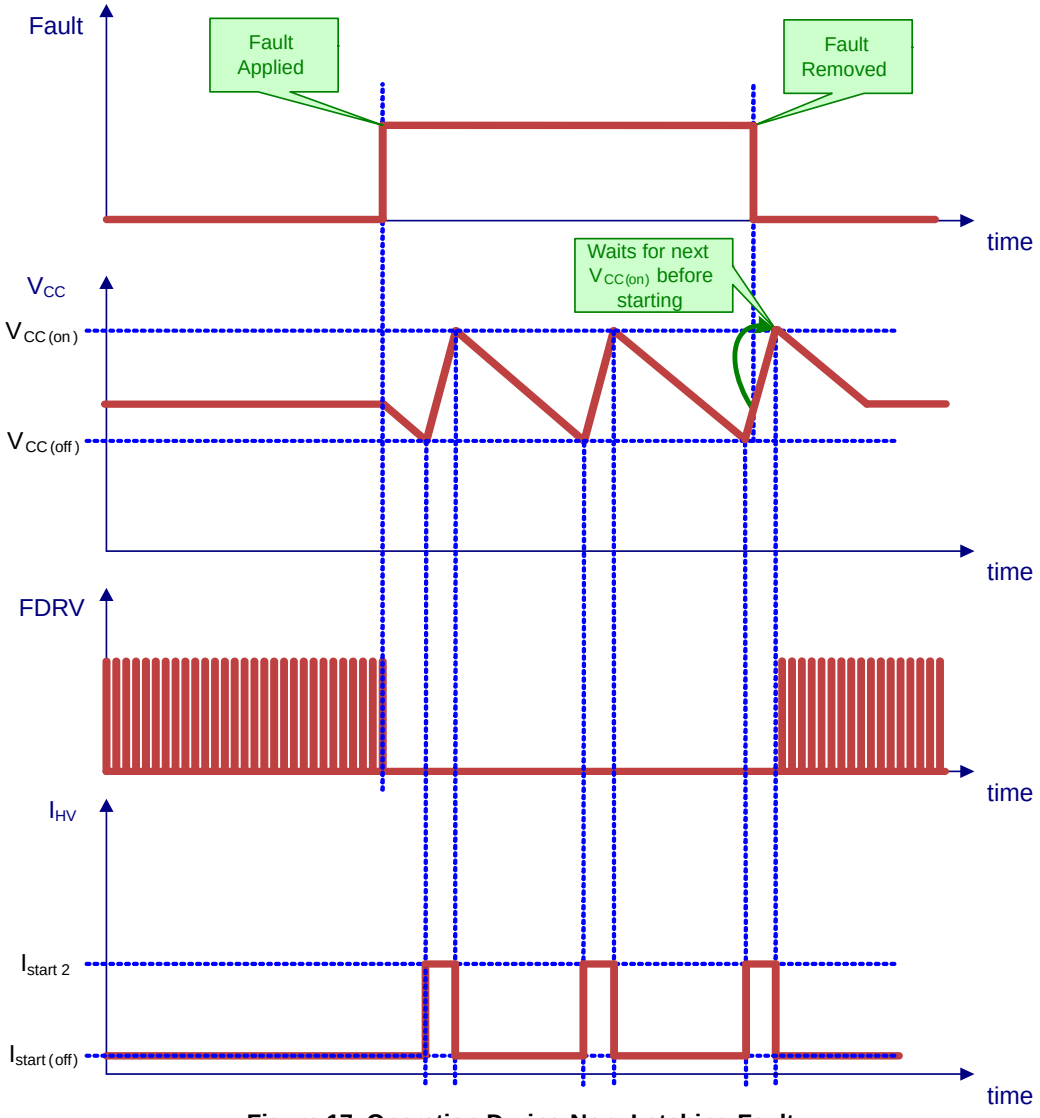


Figure 17. Operation During Non−Latching Fault

Auto−recovery Timer Faults

Some faults faults cause the NCP1340 auto−recovery timer to run. If an auto−recovery fault is detected, the gate drive is disabled and the auto−recovery timer, $t_{autorec}$ (typically 1.2 s), starts. While the auto−recovery timer is running, the HV current source turns on and off to maintain V_{cc} between $V_{cc(off)}$ and $V_{cc(on)}$. Once the auto−recovery timer expires, the controller will attempt to start normally at the next $V_{CC(on)}$ provided V_{HV} is above $V_{BO(start)}$. This operation is shown in Figure 18.

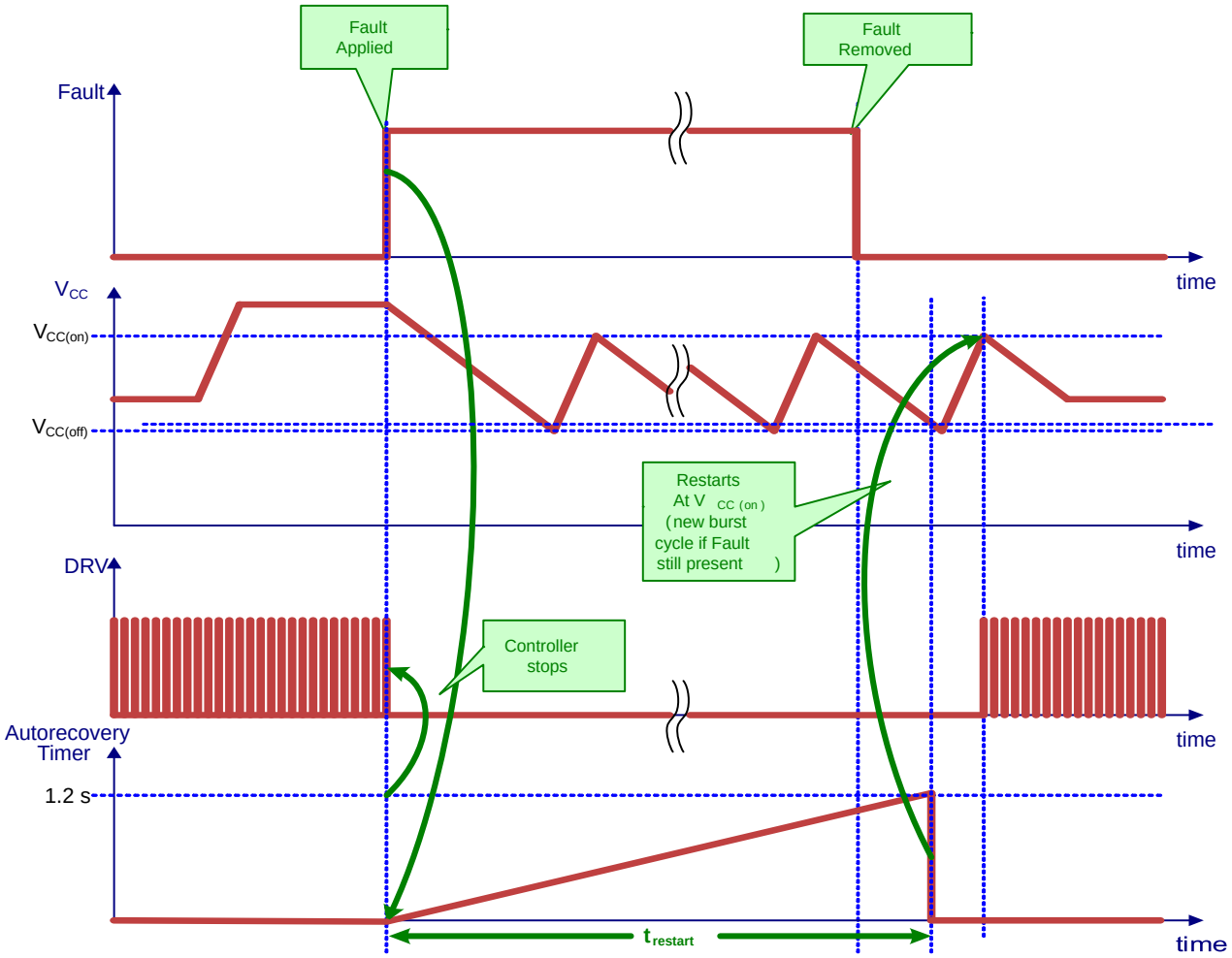


Figure 18. Operation During Auto−Recovery Fault

PROTECTION FEATURES

Brownout Protection

A timer is enabled once V_{HV} drops below its disable threshold, $V_{BO(stop)}$ (typically 99 V). The controller is disabled if V_{HV} doesn't exceed $V_{BO(stop)}$ before the brownout timer, t_{BO} (typically 54 ms), expires. The timer is set long enough to ignore a two cycle dropout. The timer starts counting once V_{HV} drops below $V_{BO(stop)}$.

Figure 19 shows the brownout detector waveforms during a brownout.

When a brownout is detected, the controller stops switching and enters non−latching fault mode (see Figure 17). The HV current source alternatively turns on and off to maintain V_{CC} between $V_{CC(on)}$ and $V_{CC(off)}$ until the input voltage is back above $V_{BO(start)}$.

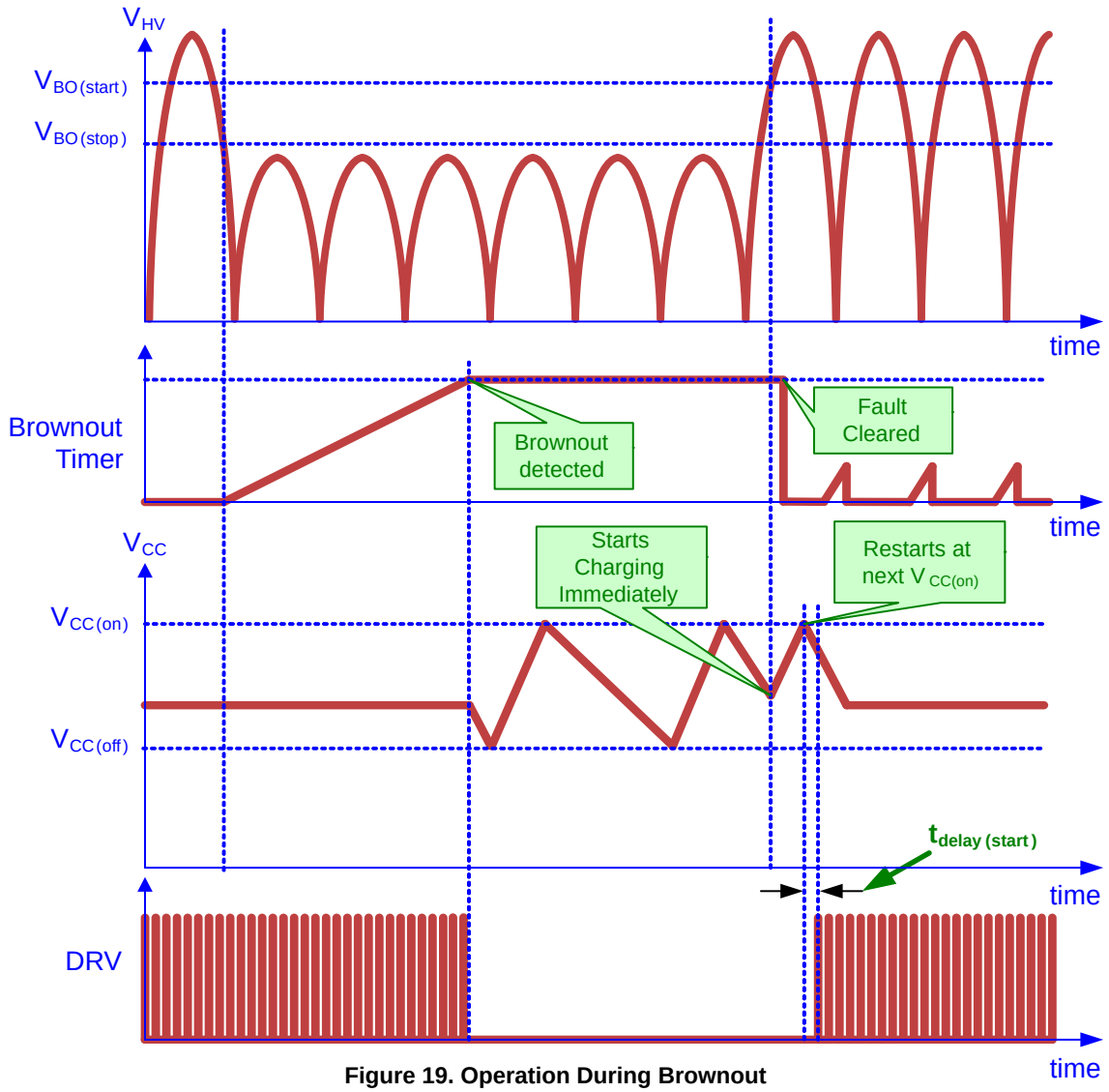


Figure 19. Operation During Brownout

Line Removal Detection and X2 Capacitor Discharge

Safety agency standards require the input filter capacitors to be discharged once the ac line voltage is removed. A resistor network is the most common method to meet this requirement. Unfortunately, the resistor network consumes power across all operating modes and it is a major contributor of input power losses during light−load and no−load conditions.

The NCP1340 eliminates the need for external discharge resistors by integrating active input filter capacitor discharge circuitry. A novel approach is used to reconfigure the high voltage startup circuit to discharge the input filter capacitors upon removal of the ac line voltage. The line removal detection circuitry is always active to ensure safety compliance.

The line removal is detected by digitally sampling the voltage present at the HV pin, and monitoring the slope.

A timer, $t_{line(removal)}$ (typically 100 ms), is used to detect when the slope of the input signal is negative or below the resolution level. The timer is reset any time a positive slope

is detected. Once the timer expires, a line removal condition is acknowledged initiating an X2 capacitor discharge cycle, and the controller is disabled.

If V_{CC} is above $V_{CC(on)}$, it is first discharged to $V_{CC(on)}$. A second timer, $t_{line(discharge)}$ (typically 32 ms), is used for the time limiting of the discharge phase to protect the device against overheating. Once the discharge phase is complete, $t_{line(discharge)}$ is reused while the device checks to see if the line voltage is reapplied. During the discharge phase, if V_{CC} drops to $V_{CC(on)}$, it is quickly recharged to $V_{CC(X2_reg)}$. The discharging process is cyclic and continues until the ac line is detected again or the voltage across the X2 capacitor is lower than $V_{HV(discharge)}$ (30 V maximum). This feature allows the device to discharge large X2 capacitors in the input line filter to a safe level.

It is important to note that the HV pin cannot be connected to any dc voltage due to this feature, i.e. directly to the bulk capacitor.

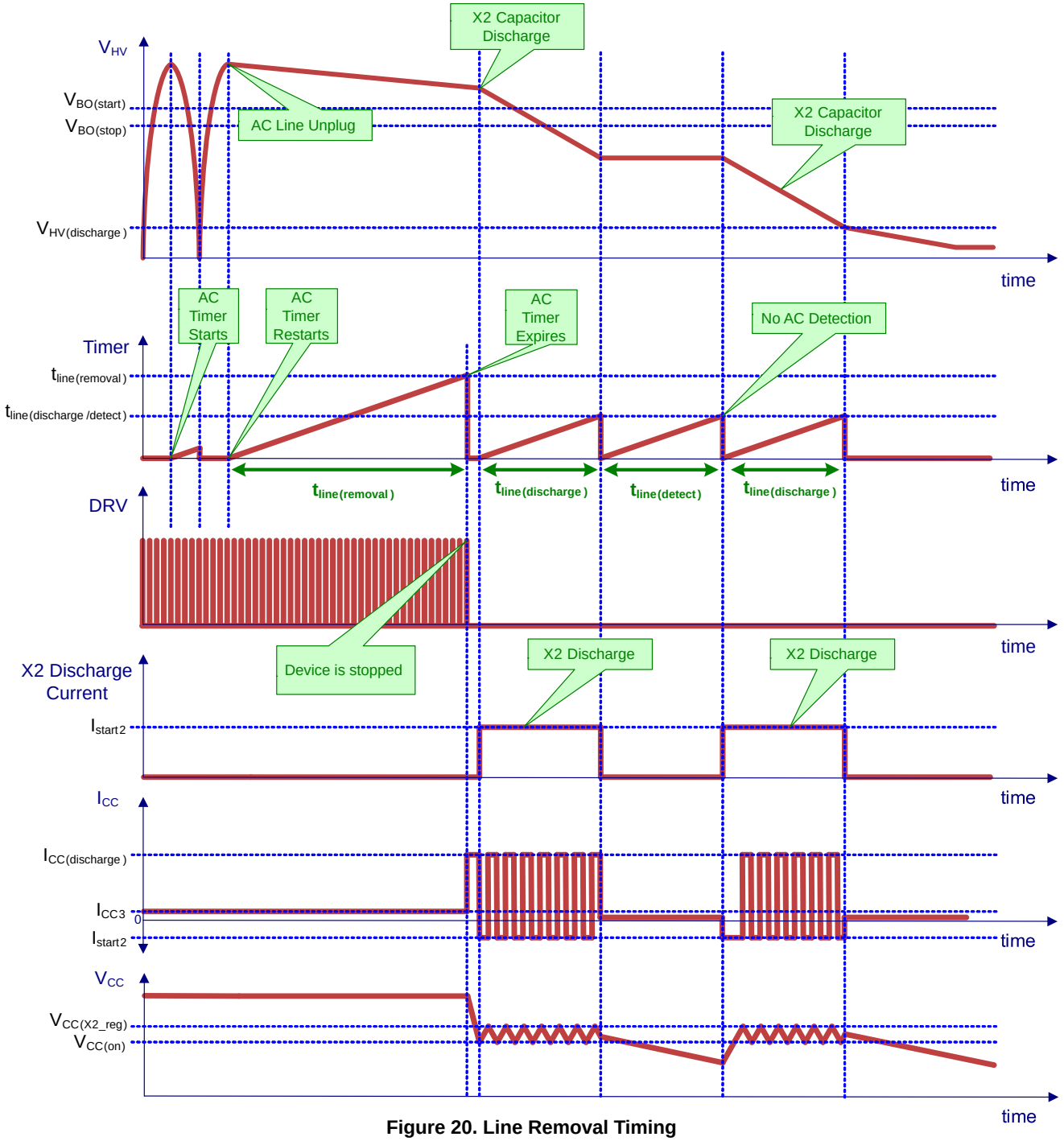


Figure 20. Line Removal Timing

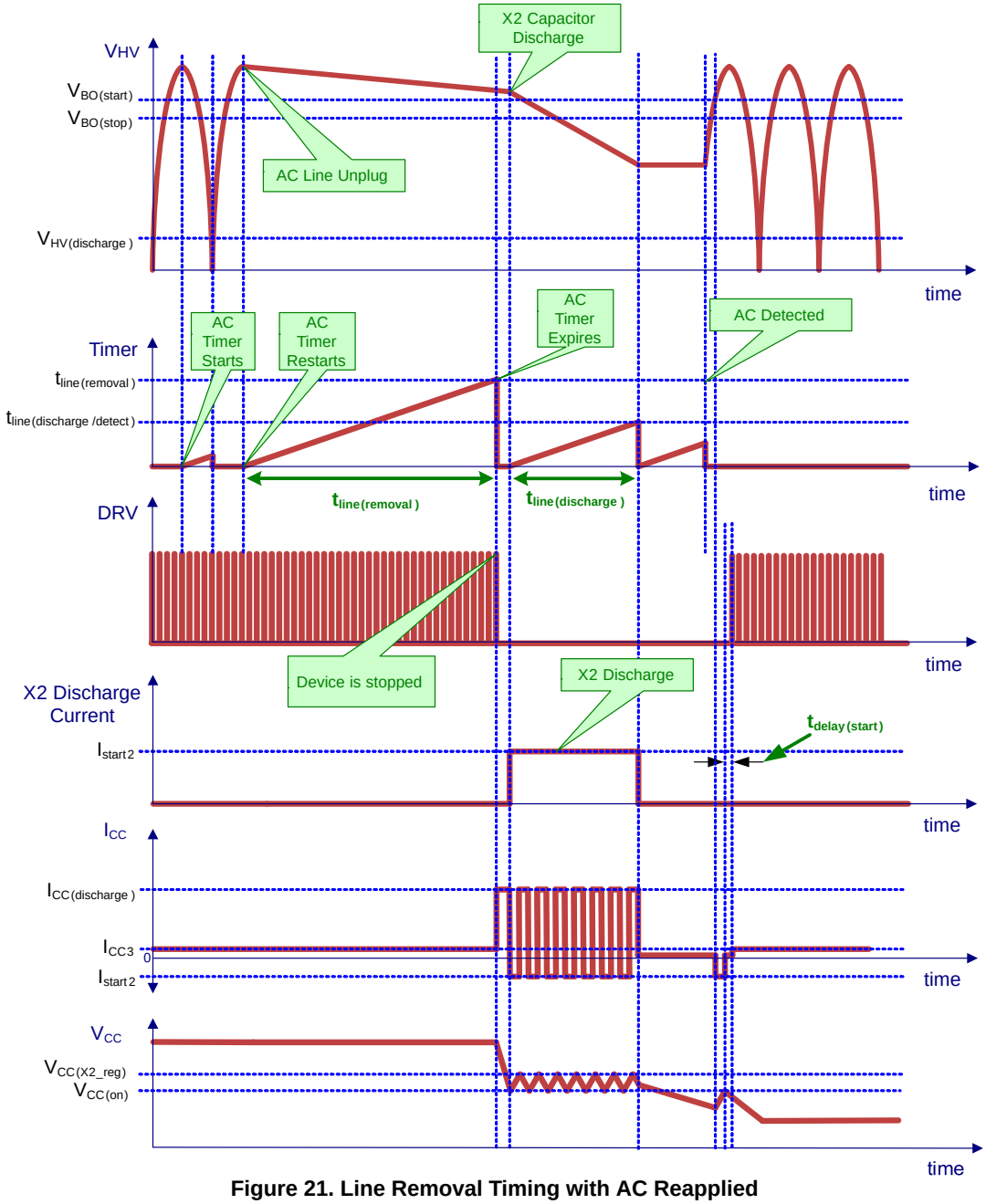


Figure 21. Line Removal Timing with AC Reapplied

An over temperature protection block monitors the junction temperature during the discharge process to avoid thermal runaway, in particular during open/short pins safety tests. Please note that the X2 discharge capability is also active at all times, including off−mode and before the controller actually starts to pulse (e.g. if the user unplugs the converter during the start−up sequence).

Dedicated Fault Input

The NCP1340 includes a dedicated fault input accessible via the Fault pin (8−pin and 9−pin versions only). The controller can be latched by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$ (typically 3.0 V). The controller is disabled if the Fault pin voltage is pulled below the lower fault threshold, $V_{Fault(OTP_in)}$ (typically 0.4 V). The lower threshold is normally used for detecting an overtemperature fault. The controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Figure 22 shows the architecture of the Fault input.

The Fault input signal is filtered to prevent noise from triggering the fault detectors. Upper and lower fault detector blanking delays, $t_{delay(OVP)}$ and $t_{delay(OTP)}$,are both typically 30 μs. A fault is detected if the fault condition is asserted for a period longer than the blanking delay.

OVP

An active clamp prevents the Fault pin voltage from reaching the upper latch threshold if the pin is open. To reach the upper threshold, the external pull−up current has to be higher than the pull−down capability of the clamp (set by $R_{Fault(clamp)}$ at $V_{Fault(clamp)}$), i.e., approximately 1 mA.

The upper fault threshold is intended to be used for an overvoltage fault using a zener diode and a resistor in series from the auxiliary winding voltage. The controller is latched once V_{Fault} exceeds $V_{Fault(OVP)}$.

Once the controller is latched, it follows the behavior of a latching fault according to Figure 16 and is only reset if V_{CC} is reduced to $V_{CC(reset)}$, or X2 discharge is activated. In the typical application these conditions occur only if the ac voltage is removed from the system.

OTP

The lower fault threshold is intended to be used to detect an overtemperature fault using an NTC thermistor. A pull up current source, $I_{Fault(OTP)}$ (typically 45.5 μA), generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{Fault(OTP_in)}$.

The controller bias current is reduced during power up by disabling most of the circuit blocks including $I_{Fault(OTP)}$. This current source is enabled once V_{CC} reaches $V_{CC(on)}$. A filter capacitor is typically connected between the Fault and GND pins. This will result in a delay before V_{Fault} reaches its steady state value once $I_{Fault(OTP)}$ is enabled. Therefore, the lower fault comparator (i.e. overtemperature detection) is ignored during soft−start.

Version A latches off the controller after an overtemperature fault is detected according to Figure 16. In Version B, the controller is re−enabled once the fault is removed such that V_{Fault} increases above $V_{Fault(OTP_out)}$, the auto−recovery timer expires, and V_{CC} reaches $V_{CC(on)}$ as shown in Figure 18.

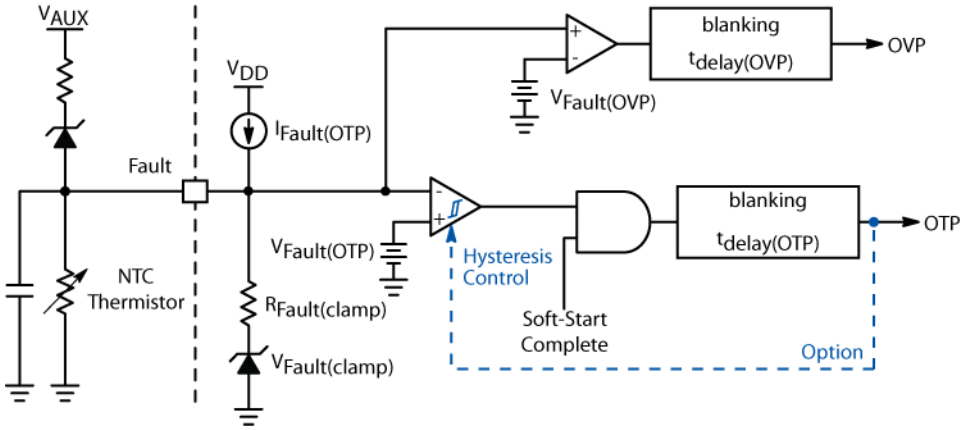


Figure 22. Fault Pin Internal Schematic

Overload Protection

The overload timer integrates the duration of the overload fault. That is, the timer count increases while the fault is present and reduces its count once it is removed. The overload timer duration, t_{OVLD}, is typically 160 ms. When the overload timer expires, the controller detects an overload condition does one of the following:

- The controller latches off (version A) or
- Enters a safe, low duty−ratio auto−recovery mode (version B).

Figure 23 shows the overload circuit schematic, while Figure 24 and Figure 25 show operating waveforms for latched and auto−recovery overload conditions.

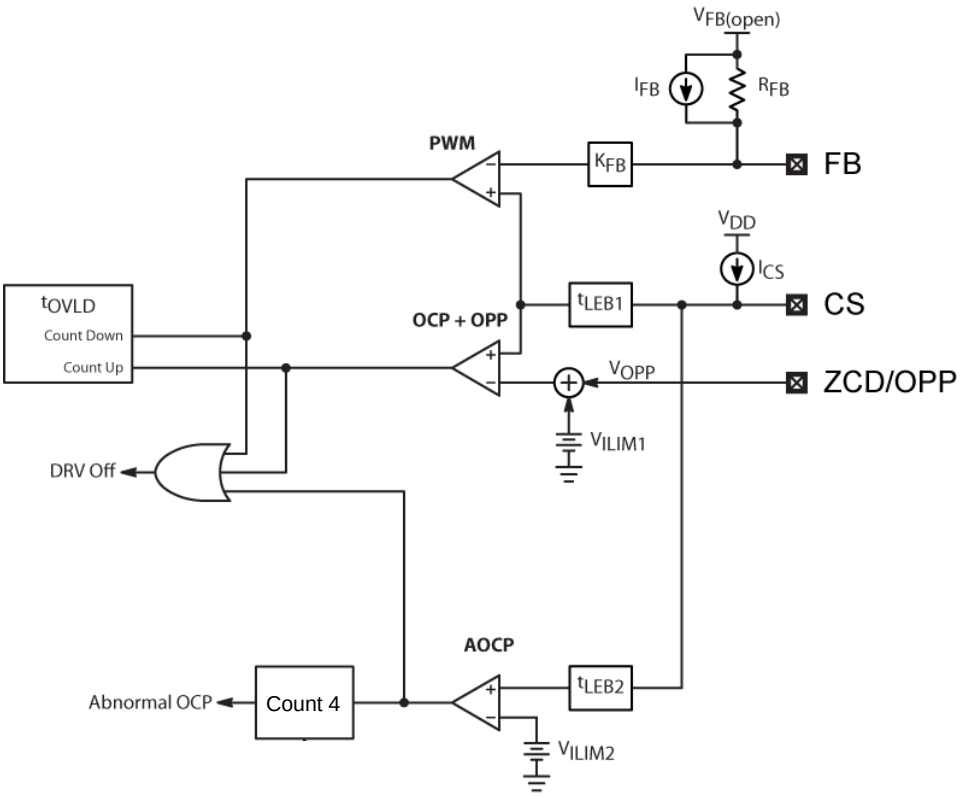


Figure 23. Overload Circuitry

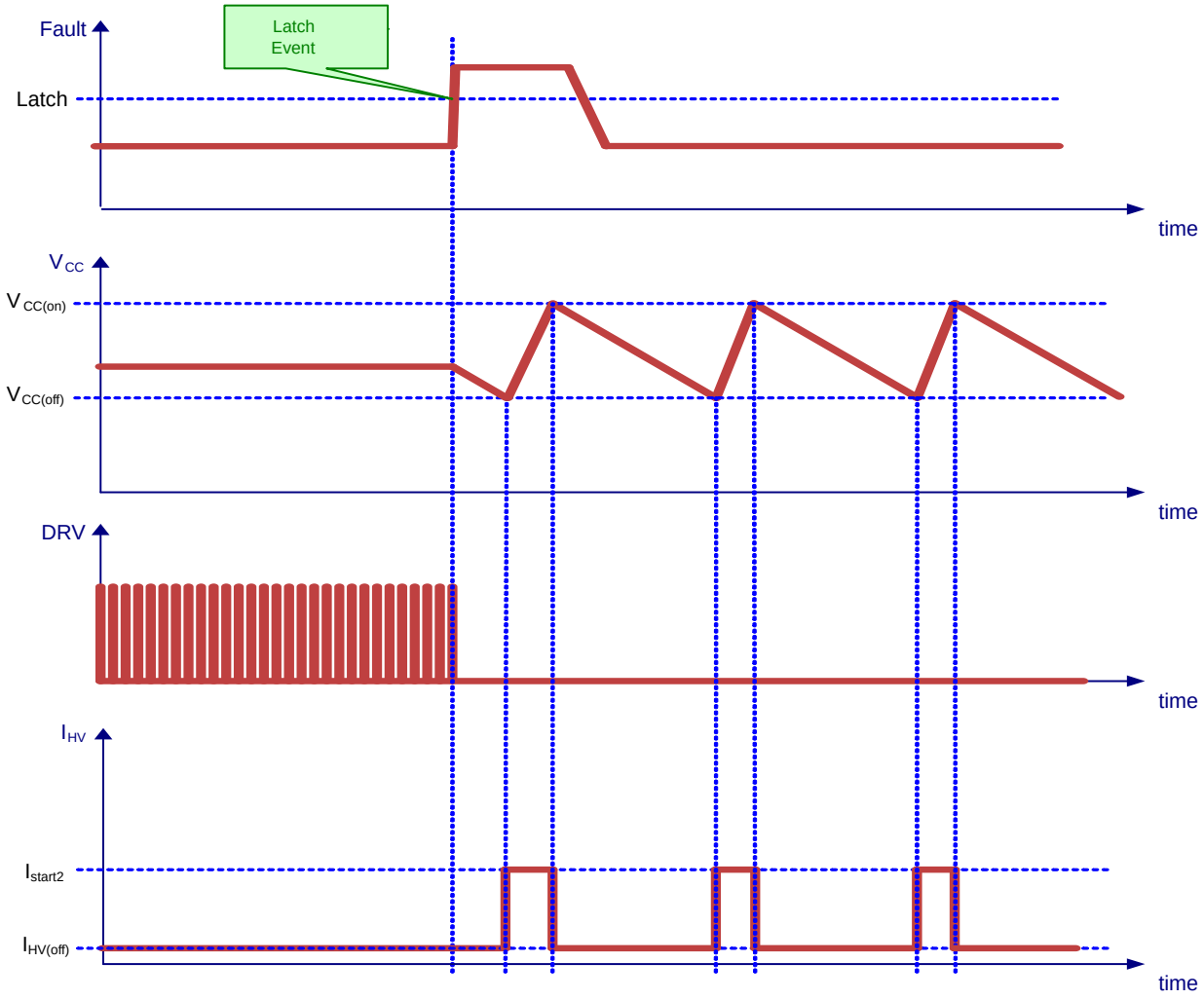


Figure 24. Latched Overload Operation

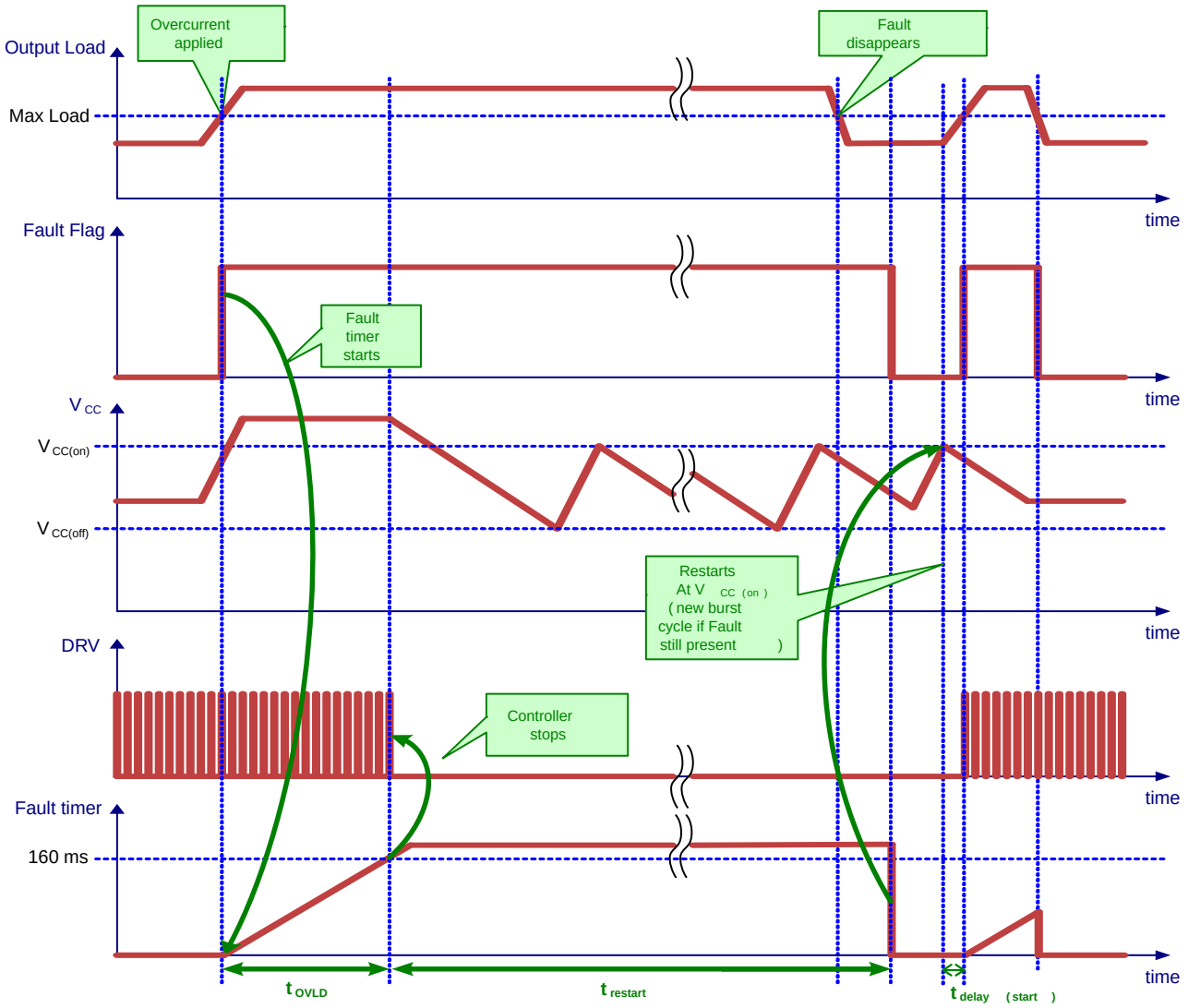


Figure 25. Auto−Recovery Overload Operation

Abnormal Overcurrent Protection (AOCP)

Under some severe fault conditions, like a winding short−circuit, the switch current can increase very rapidly during the on−time. The current sense signal significantly exceeds V_{ILIM1}, but because the current sense signal is blanked by the LEB circuit during the switch turn−on, the power switch current can become huge and cause severe system damage.

The NCP1340 protects against this fault by adding an additional comparator for Abnormal Overcurrent Fault detection. The current sense signal is blanked with a shorter LEB duration, t_{LEB2}, typically 125 ns, before applying it to the Abnormal Overcurrent Fault Comparator. The voltage threshold of the comparator, V_{ILIM2}, typically 1.2 V, is set 50% higher than V_{ILIM1}, to avoid interference with normal operation. Four consecutive Abnormal Overcurrent faults cause the controller to enter latch mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a DRV pulse occurs without activating the Fault Overcurrent Comparator.

Current Sense Pin Failure Protection

A 1 μA (typically) pull−up current source, I_{CS}, pulls up the CS pin to disable the controller if the pin is left open.

Additionally, the maximum on−time, $t_{on(MAX)}$ (32 μs typically), prevents the MOSFET from staying on permanently if the CS Pin is shorted to GND.

Output Short Circuit Protection

During an output short−circuit, there is not enough voltage across the secondary winding to demagnetize the core. Due to the valley timeout feature of the controller, the flux level will quickly walk up until the core saturates. This can cause excessive stress on the primary MOSFET and secondary diode. This is not a problem for the NCP1340, however, because the valley timeout timer is disabled while the ZCD Pin voltage is above the arming threshold. Since the leakage energy is high enough to arm the ZCD trigger, the timeout timer is disabled and the next drive pulse is delayed until demagnetization occurs.

V_{CC} Overvoltage Protection

An additional comparator on the V_{CC} pin monitors the V_{CC} voltage. If VCC exceeds VCC(OVP), the gate drive is disabled and the NCP1340 follows the operation of a latching fault (see Figure 16).

Thermal Shutdown

An internal thermal shutdown circuit monitors the junction temperature of the controller. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN} (typically 140°C). When a thermal shutdown fault is detected, the controller enters a non−latching fault mode as depicted in Figure 17. The controller restarts at the next $V_{CC(on)}$ once the junction temperature drops below below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 40°C.

The thermal shutdown is also cleared if V_{CC} drops below $V_{CC(reset)}$, or a line removal fault is detected. A new power up sequence commences at the next $V_{CC(on)}$ once all the faults are removed.

TYPICAL CHARACTERISTICS

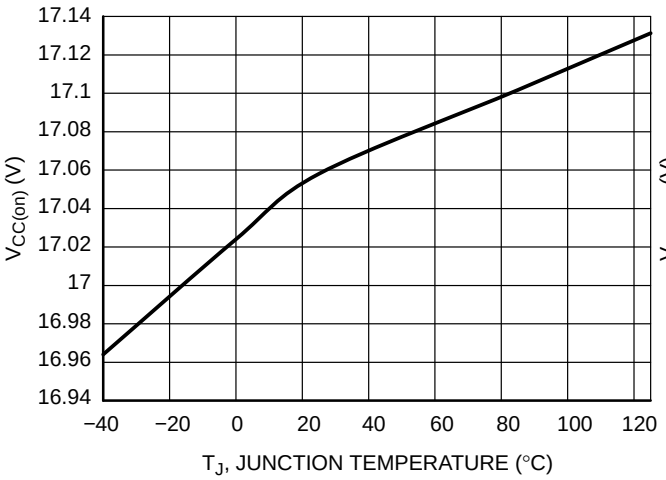


Figure 26. $V_{CC(on)}$ vs. Temperature

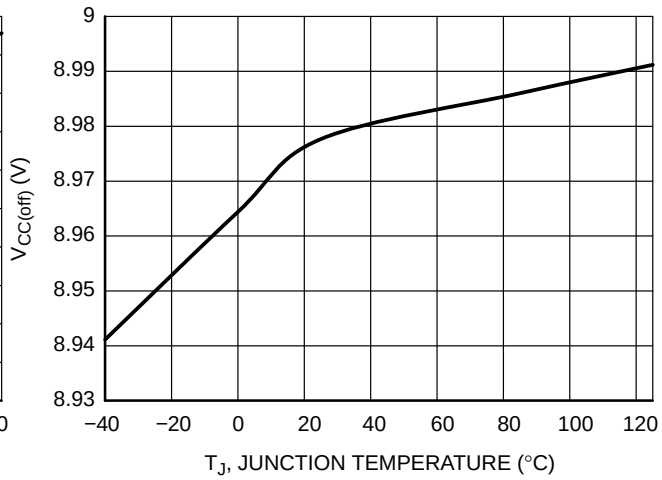


Figure 27. $V_{CC(off)}$ vs. Temperature

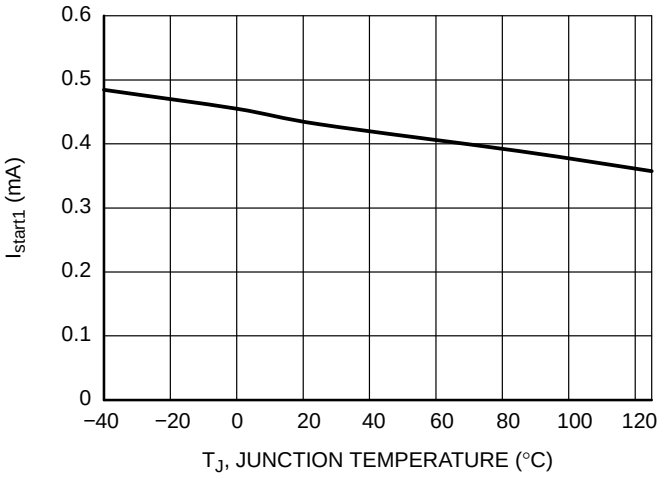


Figure 28. I_{start1} vs. Temperature

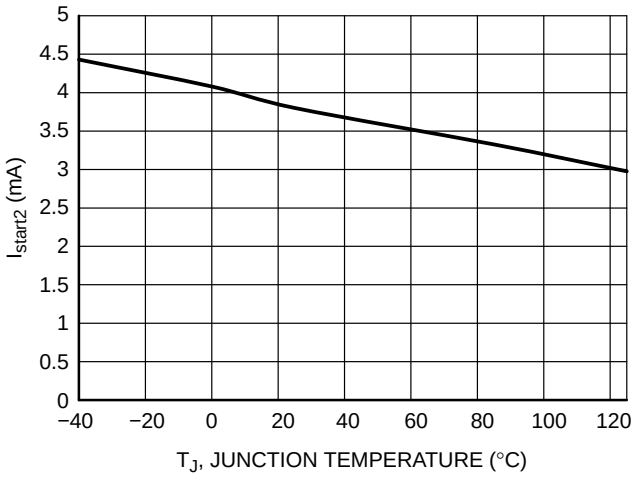


Figure 29. I_{start2} vs. Temperature

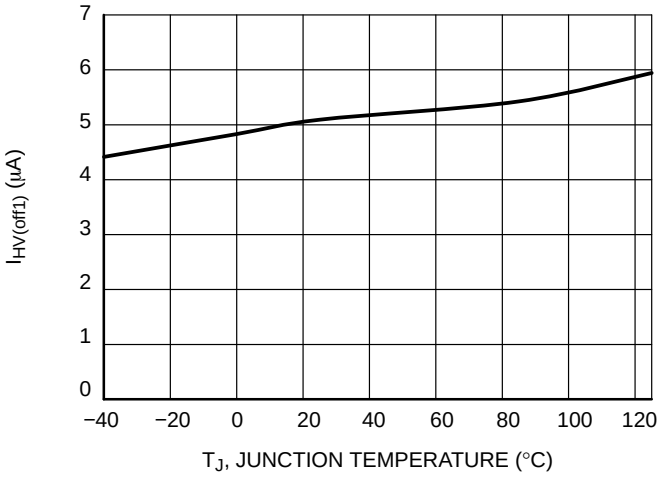


Figure 30. $I_{HV(off1)}$ vs. Temperature

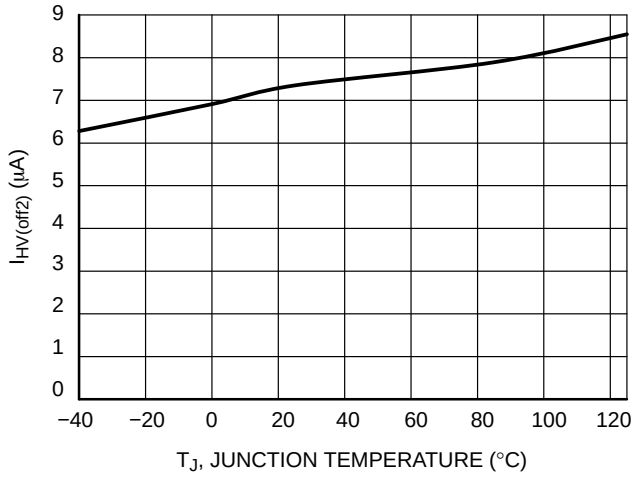


Figure 31. $I_{HV(off2)}$ vs. Temperature

TYPICAL CHARACTERISTICS

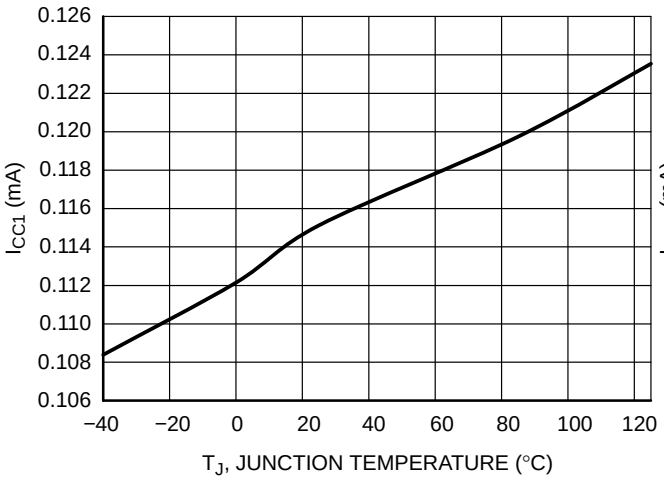


Figure 32. I_{CC1} vs. Temperature

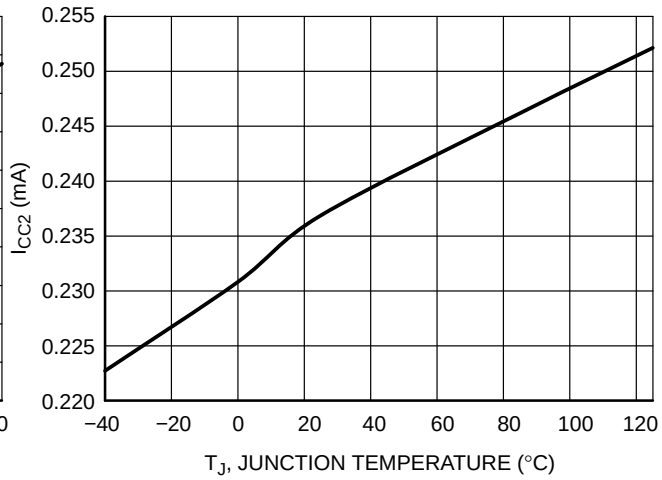


Figure 33. I_{CC2} vs. Temperature

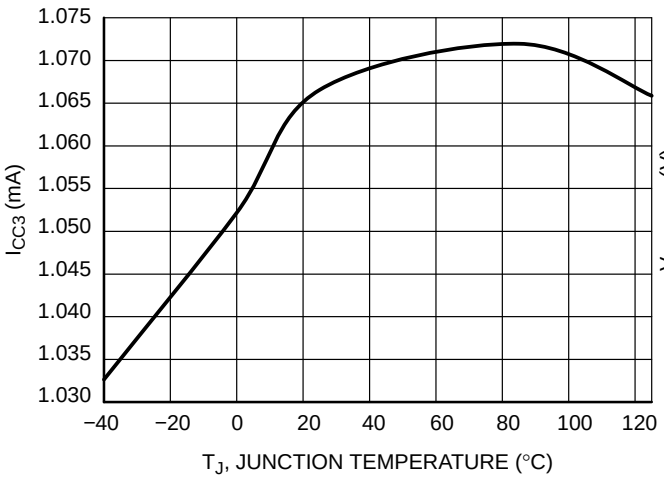


Figure 34. I_{CC3} vs. Temperature

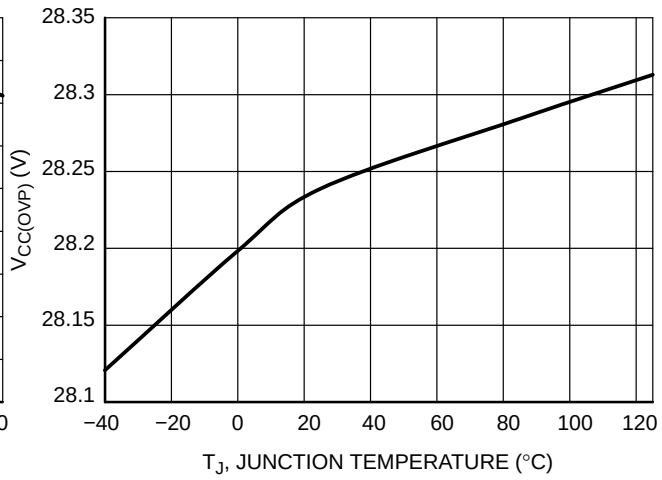


Figure 35. $V_{CC(OVP)}$ vs. Temperature

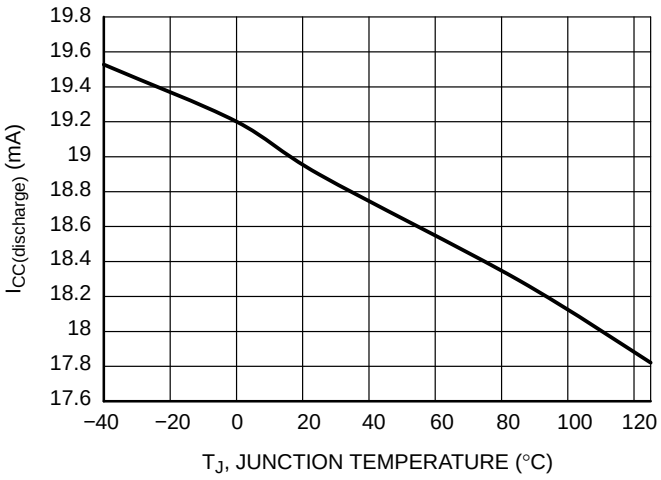


Figure 36. $I_{CC(discharge)}$ vs. Temperature

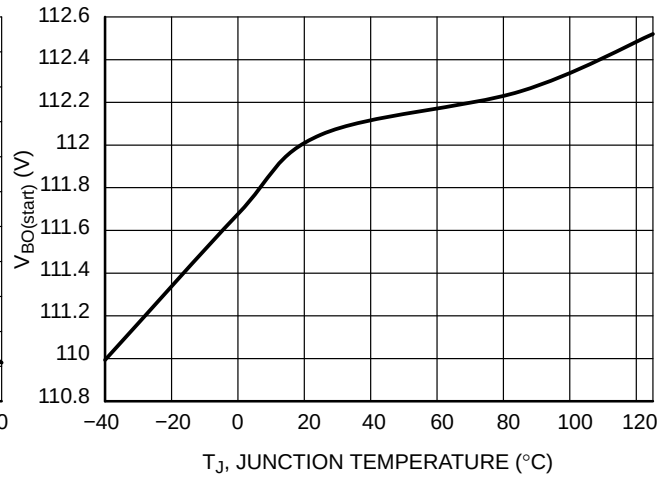


Figure 37. $V_{BO(start)}$ vs. Temperature

TYPICAL CHARACTERISTICS

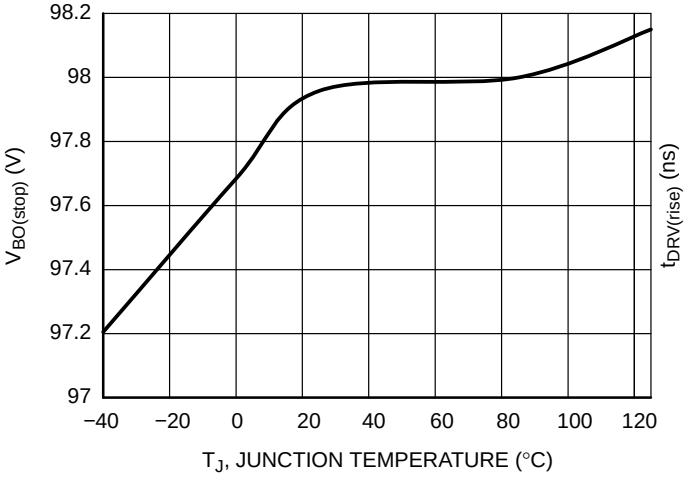


Figure 38. $V_{BO(stop)}$ vs. Temperature

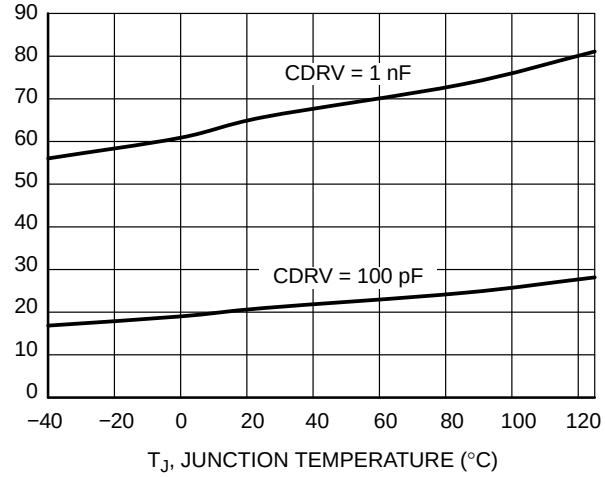


Figure 39. $t_{DRV(rise)}$ vs. Temperature

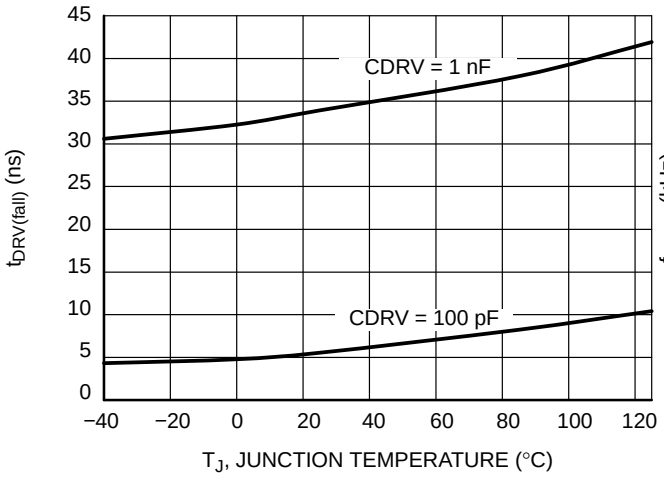


Figure 40. $t_{DRV(fall)}$ vs. Temperature

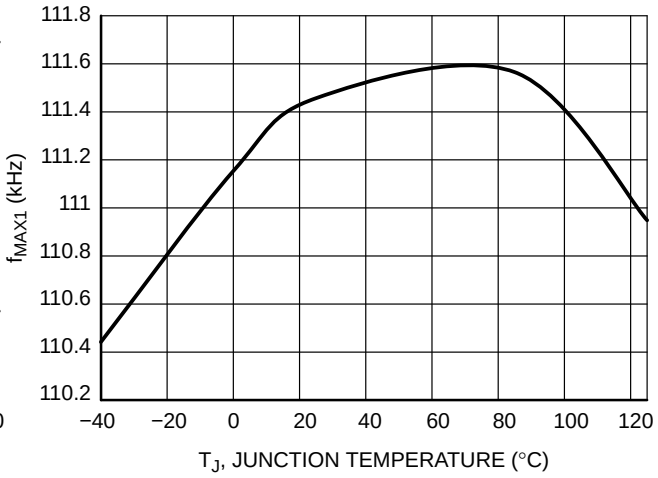


Figure 41. f_{MAX1} vs. Temperature

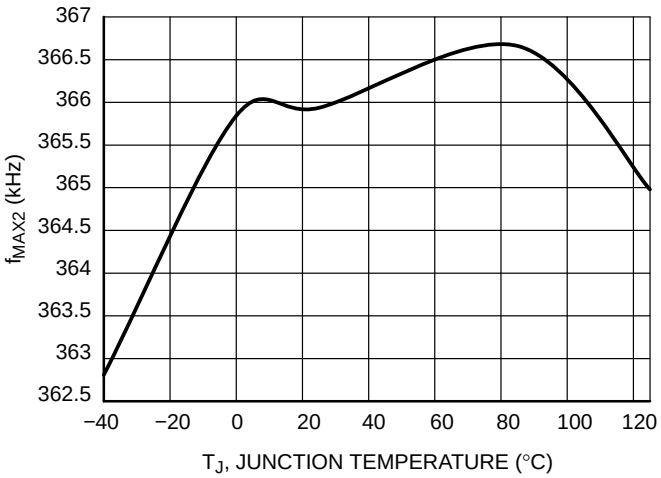


Figure 42. f_{MAX2} vs. Temperature

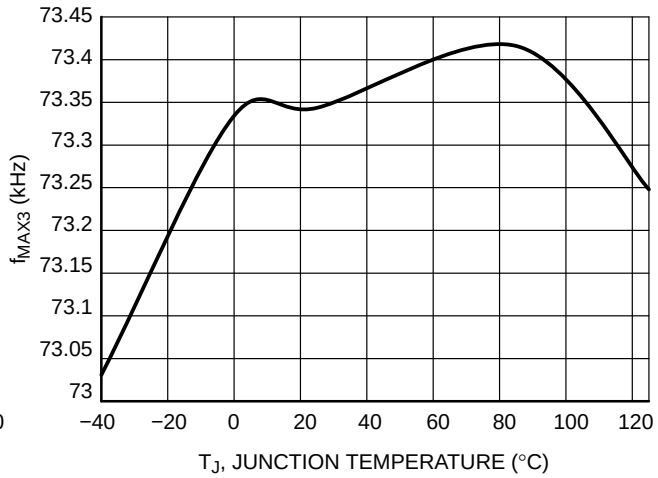


Figure 43. f_{MAX3} vs. Temperature

TYPICAL CHARACTERISTICS

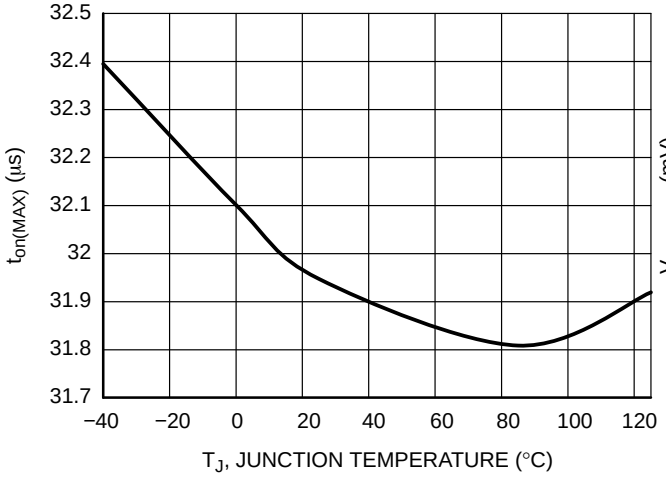


Figure 44. $t_{on(MAX)}$ vs. Temperature

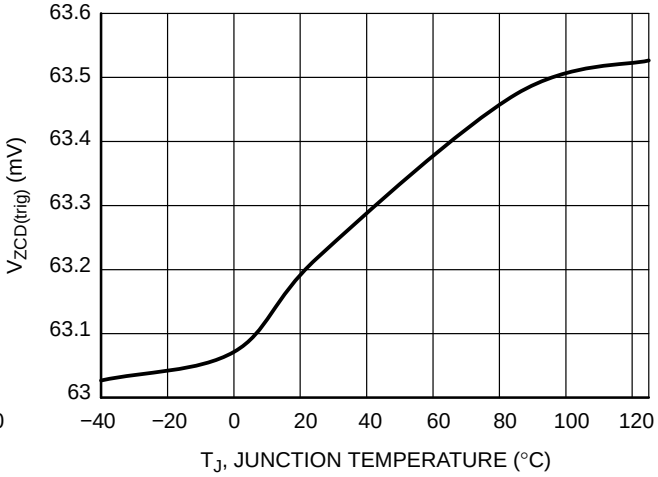


Figure 45. $V_{ZCD(trig)}$ vs. Temperature

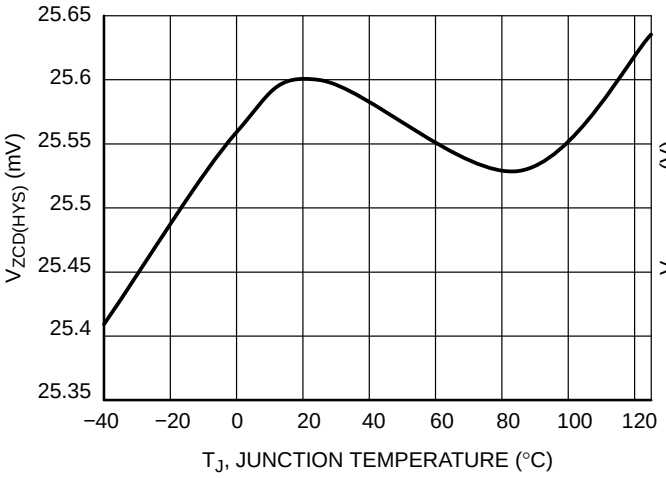


Figure 46. $V_{ZCD(HYS)}$ vs. Temperature

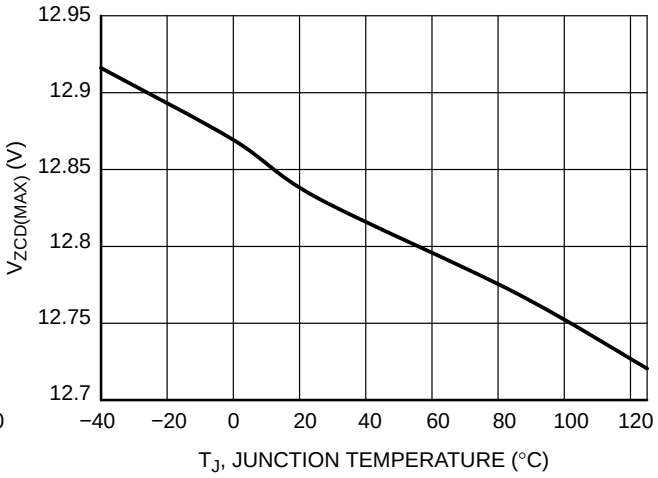


Figure 47. $V_{ZCD(MAX)}$ vs. Temperature

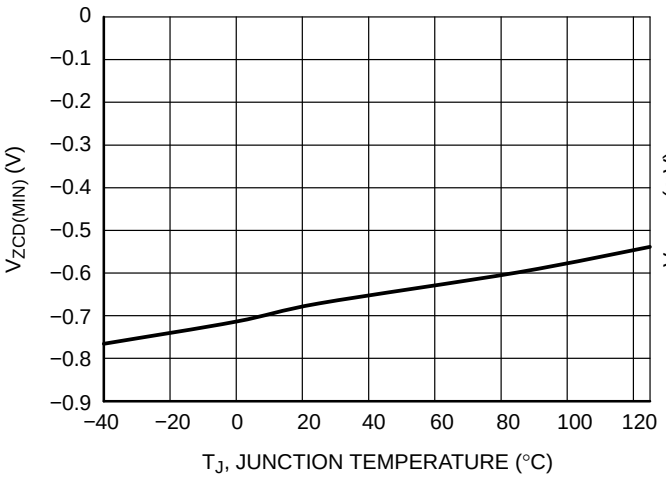


Figure 48. $V_{ZCD(MIN)}$ vs. Temperature

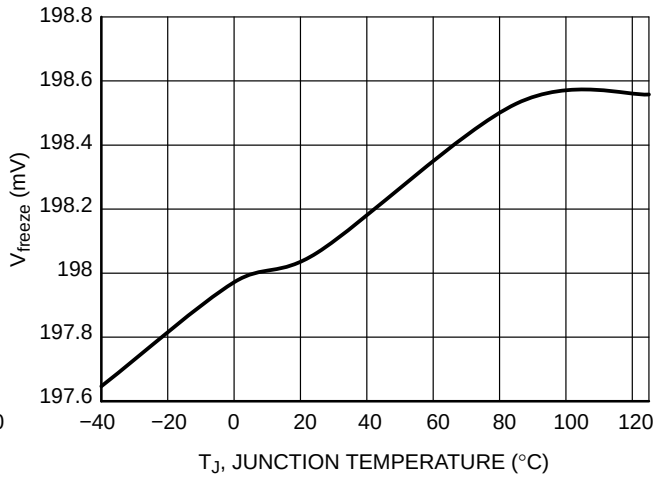


Figure 49. V_{freeze} vs. Temperature

TYPICAL CHARACTERISTICS

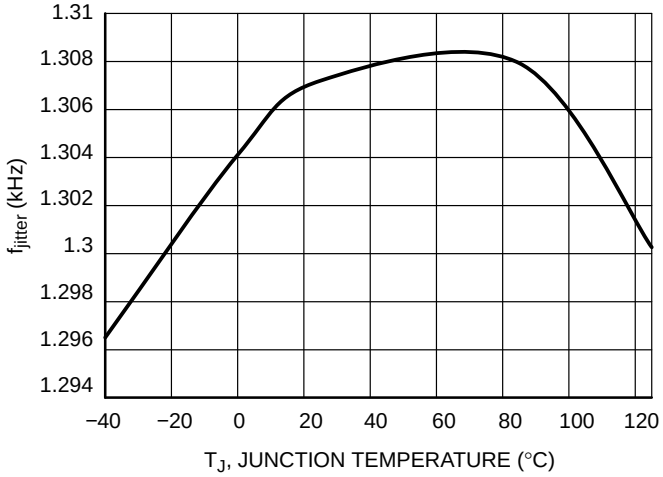


Figure 50. f_{jitter} vs. Temperature

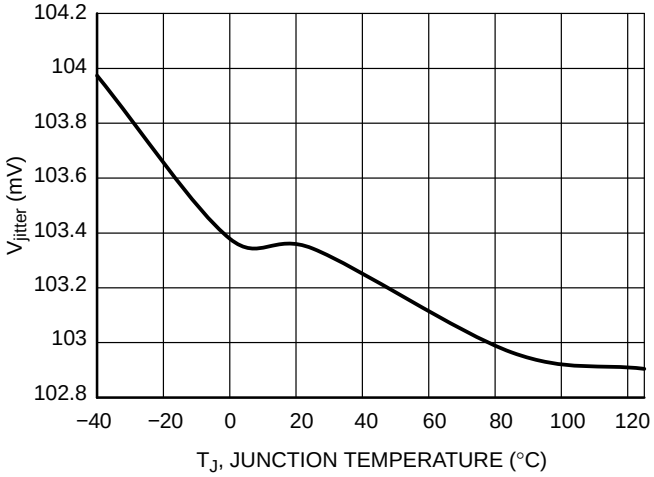


Figure 51. V_{jitter} vs. Temperature

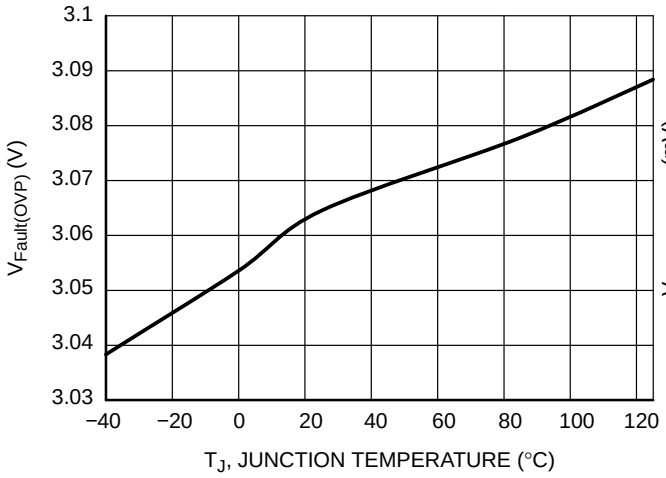


Figure 52. $V_{Fault(OVP)}$ vs. Temperature

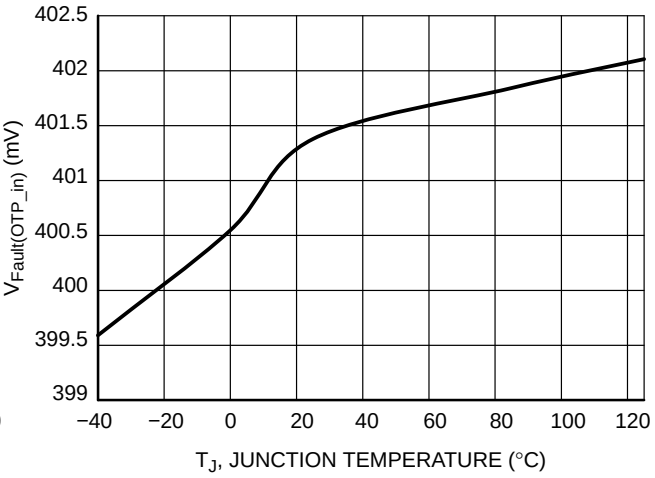


Figure 53. $V_{Fault(OTP_in)}$ vs. Temperature

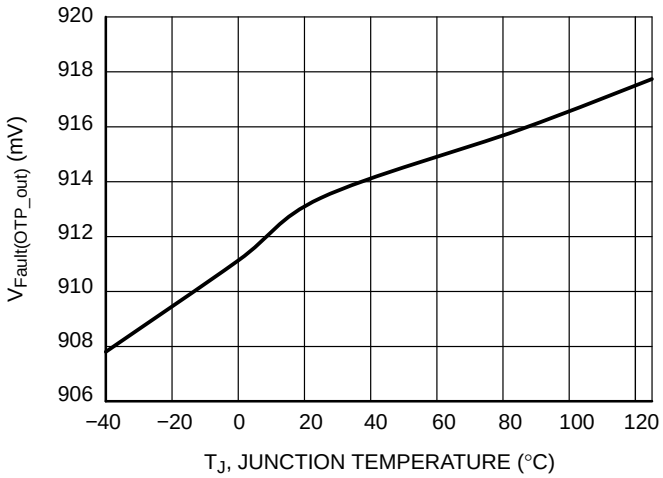


Figure 54. $V_{Fault(OTP_out)}$ vs. Temperature

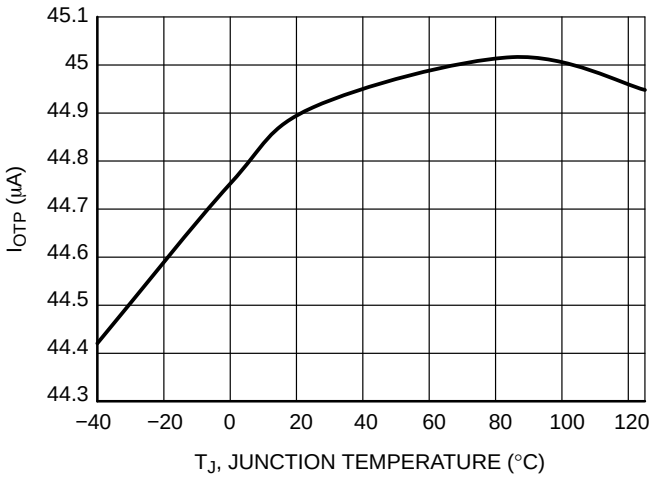


Figure 55. I_{OTP} vs. Temperature

TYPICAL CHARACTERISTICS

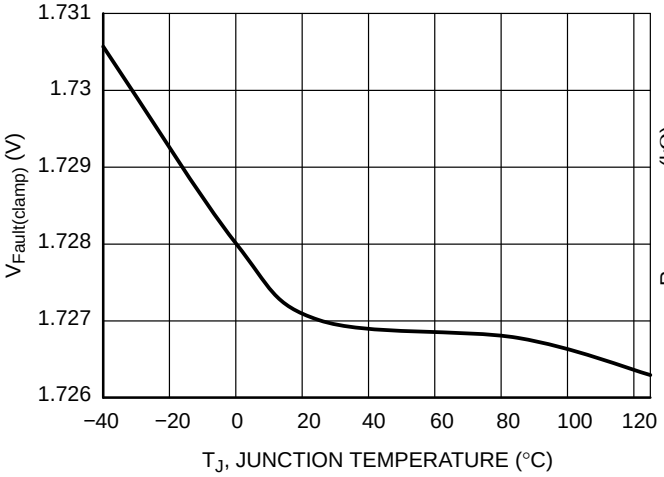


Figure 56. $V_{Fault(clamp)}$ vs. Temperature

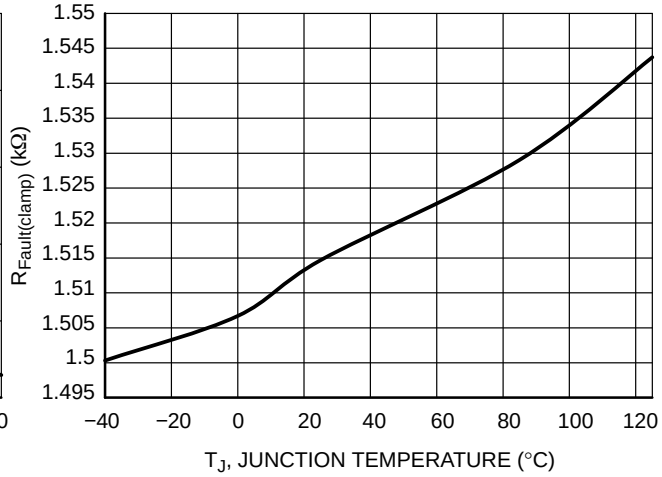


Figure 57. $R_{Fault(clamp)}$ vs. Temperature

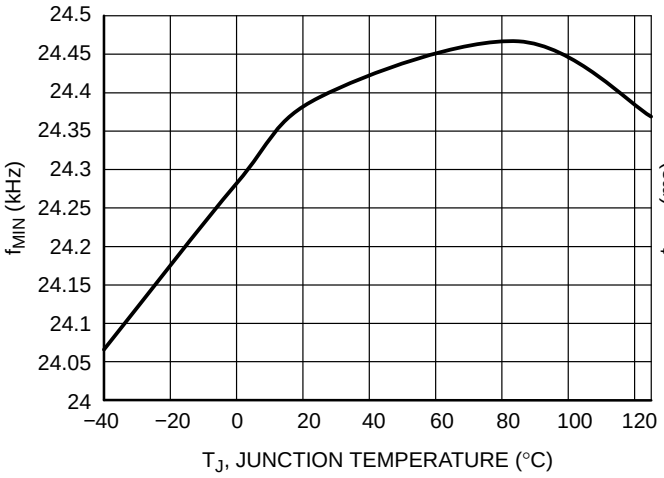


Figure 58. f_{MIN} vs. Temperature

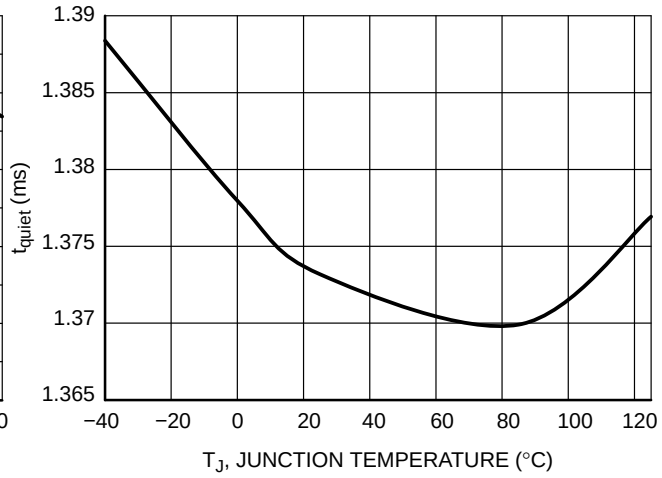


Figure 59. t_{quiet} vs. Temperature

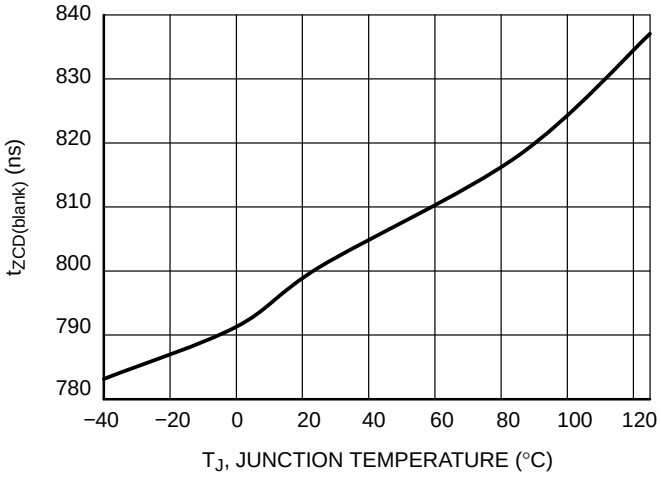


Figure 60. $t_{ZCD(blank)}$ vs. Temperature

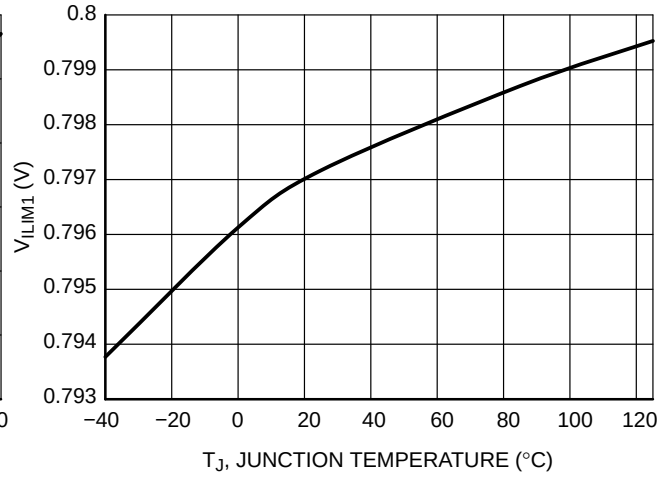


Figure 61. V_{ILIM1} vs. Temperature

TYPICAL CHARACTERISTICS

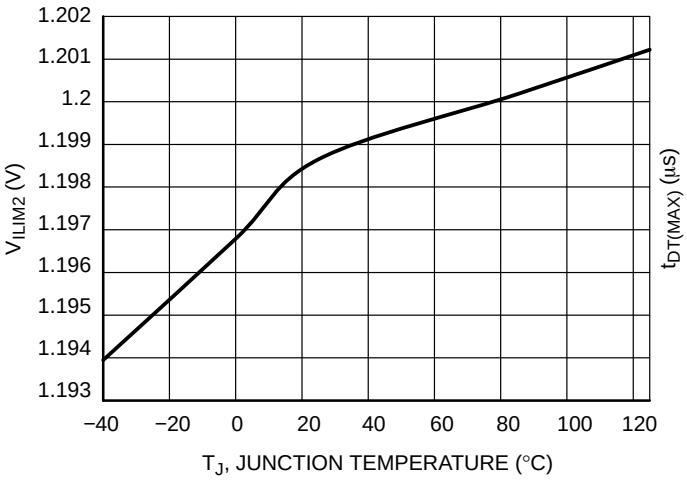


Figure 62. V_{ILIM2} vs. Temperature

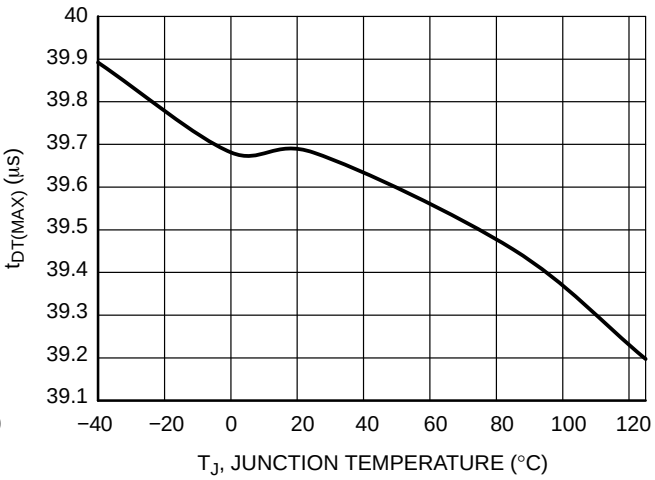


Figure 63. $t_{DT(MAX)}$ vs. Temperature

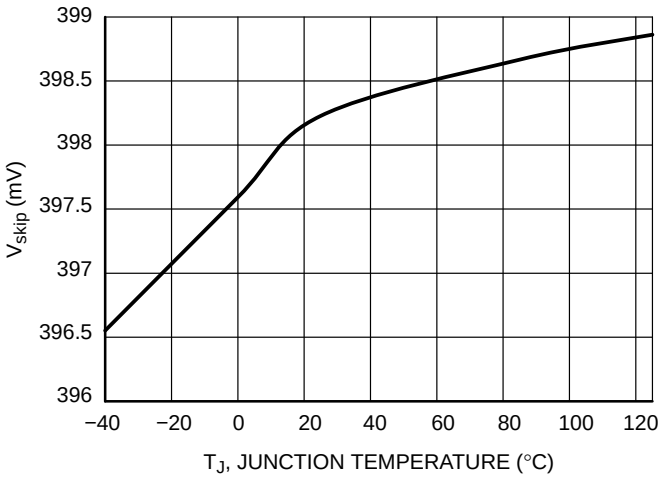
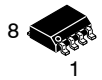


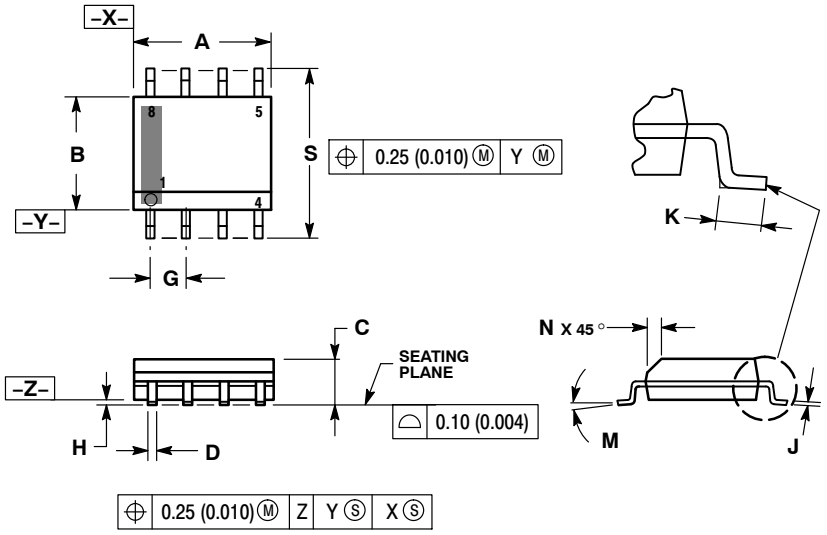
Figure 64. V_{skip} vs. Temperature

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011



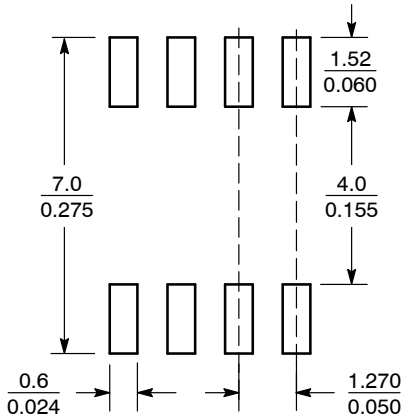
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

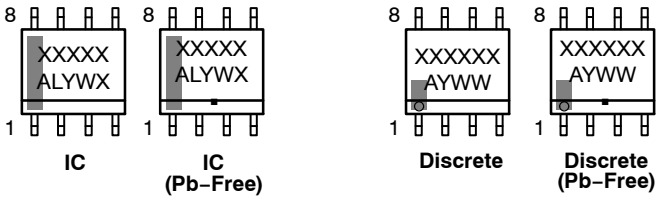
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

STYLES ON PAGE 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

ISSUE	REVISION	DATE
AB	ADDED STYLE 25. REQ. BY S. CHANG.	15 MAR 2004
AC	ADDED CORRECTED MARKING DIAGRAMS. REQ. BY S. FARRETTA.	13 AUG 2004
AD	CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY S. FARRETTA.	18 NOV 2004
AE	UPDATED SCALE ON FOOTPRINT. REQ. BY S. WEST.	31 JAN 2005
AF	UPDATED MARKING DIAGRAMS. REQ. BY S. WEST. ADDED STYLE 26. REQ. BY S. CHANG.	14 APR 2005
AG	ADDED STYLE 27. REQ. BY S. CHANG.	30 JUN 2005
AH	ADDED STYLE 28. REQ. BY S. CHANG.	09 MAR 2006
AJ	ADDED STYLE 29. REQ. BY D. HELZER.	19 SEP 2007
AK	ADDED STYLE 30. REQ. BY I. CAMBALIZA.	16 FEB 2011

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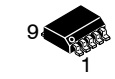
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

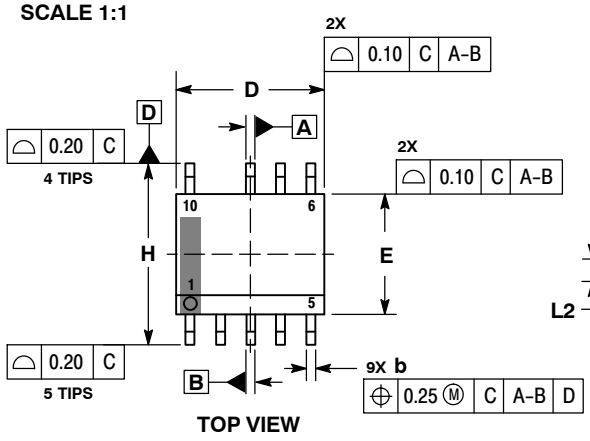
ON Semiconductor®

SOIC−9 NB
CASE 751BP
ISSUE A

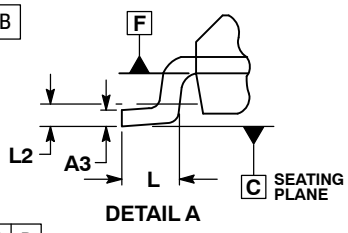
DATE 21 NOV 2011



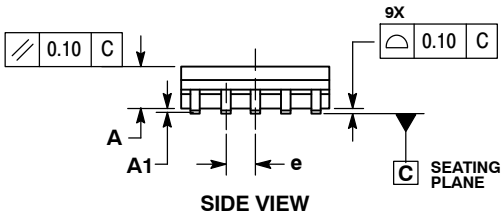
SCALE 1:1



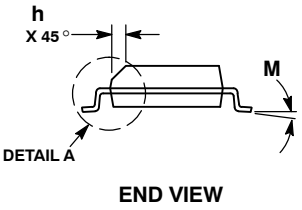
TOP VIEW



DETAIL A



SIDE VIEW

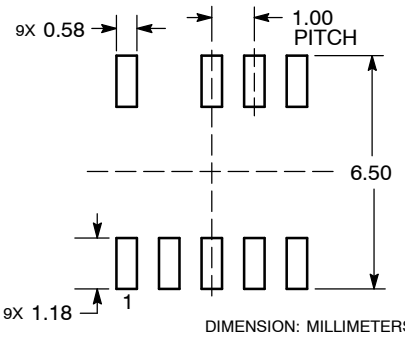


END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF 'b' AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	1.25	1.75
A1	0.10	0.25
A3	0.17	0.25
b	0.31	0.51
D	4.80	5.00
E	3.80	4.00
e	1.00 BSC	
H	5.80	6.20
h	0.37 REF	
L	0.40	1.27
L2	0.25 BSC	
M	0°	8°

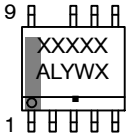
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD		
NEW STANDARD:			
DESCRIPTION:	SOIC−9 NB		PAGE 1 OF 2

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION. REQ. BY M. RAMOS.	06 JUL 2010
A	CHANGED DIMENSION A MINIMUM FROM 1.35 TO 1.25. REQ. BY I. CAMBALIZA.	21 NOV 2011

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Данный компонент на территории Российской Федерации

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Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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