

### Typical Applications

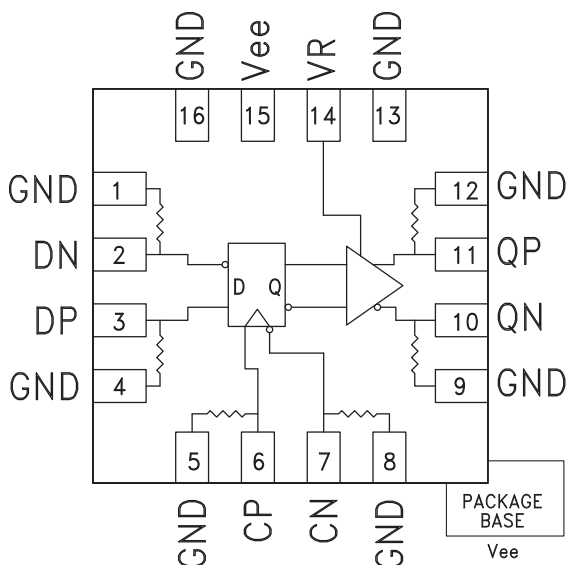
The HMC723LP3E is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 13 Gbps
- Digital Logic Systems up to 13 GHz

### Features

- Supports High Data Rates: up to 13 Gbps
- Differential & Single-Ended Operation
- Fast Rise and Fall Times: 19 / 17 ps
- Low Power Consumption: 260 mW typ.
- Programmable Differential Output Voltage Swing: 700 - 1300 mV
- Propagation Delay: 105 ps
- Single Supply: -3.3V
- 16 Lead 3x3mm SMT Package: 9mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC723LP3E is a D-type Flip Flop designed to support data transmission rates of up to 13 Gbps, and clock frequencies as high as 13 GHz. During normal operation, data is transferred to the outputs on the positive edge of the clock. Reversing the clock inputs allows for negative-edge triggered applications. The HMC723LP3E also features an output level control pin, VR, which allows for loss compensation or for signal level optimization.

All input signals to the HMC723LP3E are terminated with 50 Ohms to ground on-chip, and maybe either AC or DC coupled. The differential outputs of the HMC723LP3E may be either AC or DC coupled. Outputs can be connected directly to a 50 Ohm to ground terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to a non-ground DC voltage. The HMC723LP3E operates from a single -3.3V DC supply and is available in a RoHS compliant 3x3 mm SMT package.

### Electrical Specifications, $T_A = +25^{\circ}\text{C}$ , $V_{ee} = -3.3\text{V}$

| Parameter            | Conditions                 | Min. | Typ. | Max  | Units |
|----------------------|----------------------------|------|------|------|-------|
| Power Supply Voltage |                            | -3.6 | -3.3 | -3.0 | V     |
| Power Supply Current |                            |      | 80   |      | mA    |
| Maximum Data Rate    |                            |      | 13   |      | Gbps  |
| Maximum Clock Rate   |                            |      | 13   |      | GHz   |
| Input High Voltage   |                            | -0.5 |      | 0.5  | V     |
| Input Low Voltage    |                            | -1.0 |      | 0.0  | V     |
| Input Return Loss    | Frequency <13 GHz          |      | 10   |      | dB    |
| Output Amplitude     | Single-Ended, peak-to-peak |      | 550  |      | mVp-p |
|                      | Differential, peak-to-peak |      | 1100 |      | mVp-p |
| Output High Voltage  |                            |      | -10  |      | mV    |

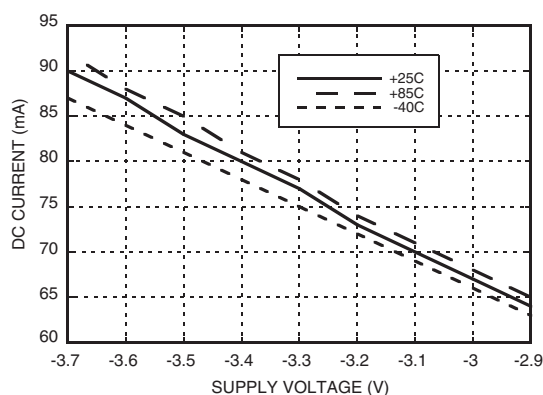
## 13 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP w/ PROGRAMMABLE OUTPUT VOLTAGE

### Electrical Specifications, (continued)

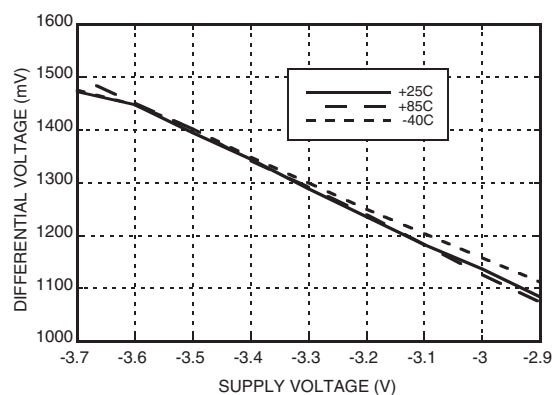
| Parameter                           | Conditions                                      | Min. | Typ.    | Max | Units  |
|-------------------------------------|-------------------------------------------------|------|---------|-----|--------|
| Output Low Voltage                  |                                                 |      | -570    |     | mV     |
| Output Rise / Fall Time             | Differential, 20% - 80%                         |      | 19 / 17 |     | ps     |
| Output Return Loss                  | Frequency <13 GHz                               |      | 10      |     | dB     |
| Random Jitter Jr                    | rms                                             |      |         | 0.2 | ps rms |
| Deterministic Jitter, Jd            | peak-to-peak, 2 <sup>15</sup> -1 PRBS input [1] |      | 2       |     | ps, pp |
| Propagation Delay Clock to Data, td |                                                 |      | 105     |     | ps     |
| Clock Phase Margin                  | 13 GHz                                          |      | 320     |     | deg    |
| Set Up & Hold Time, t <sub>SH</sub> |                                                 |      | 6       |     | ps     |

[1] Deterministic jitter calculated by simultaneously measuring the jitter of a 300 mV, 13 GHz, 2<sup>15</sup>-1 PRBS input, and a single-ended output

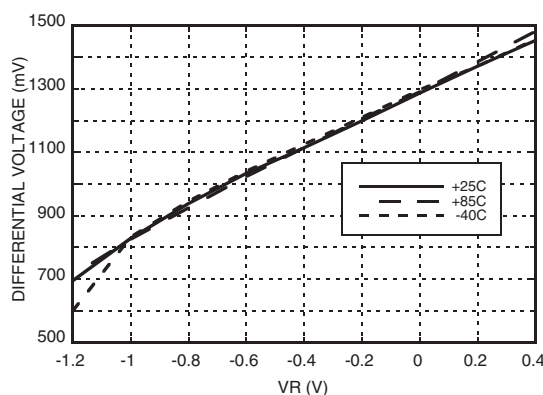
### DC Current vs. Supply Voltage [1] [2]



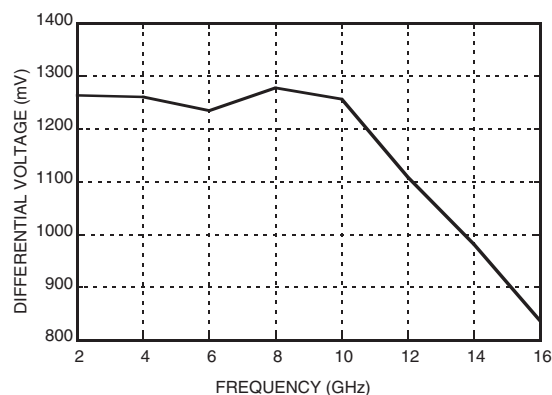
### Output Differential vs. Supply Voltage [1] [3]



### Output Differential vs. VR [3]



### Output Differential vs. Frequency [1]



[1] VR = 0.0V

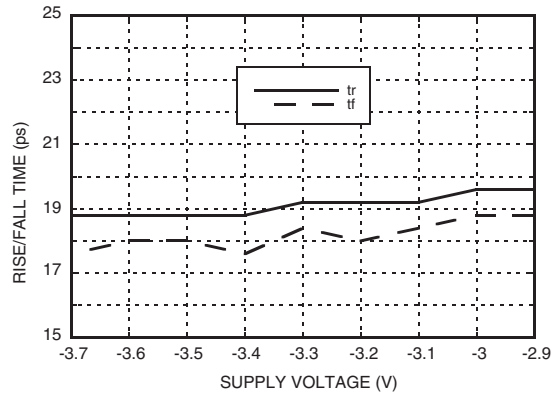
[2] Frequency = 13 GHz

[3] Frequency = 10 GHz

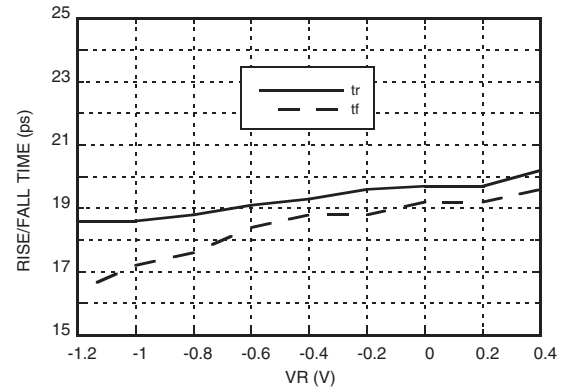


**13 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP  
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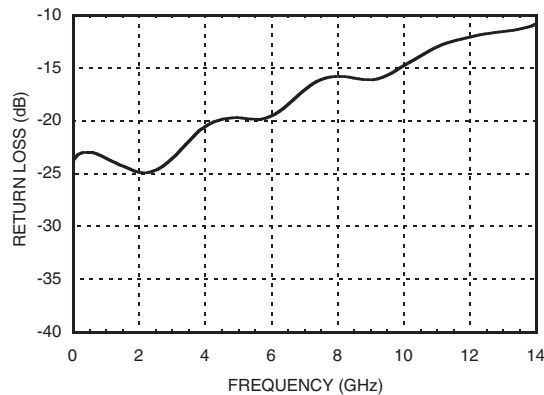
**Rise / Fall Time vs. Supply Voltage [2]**



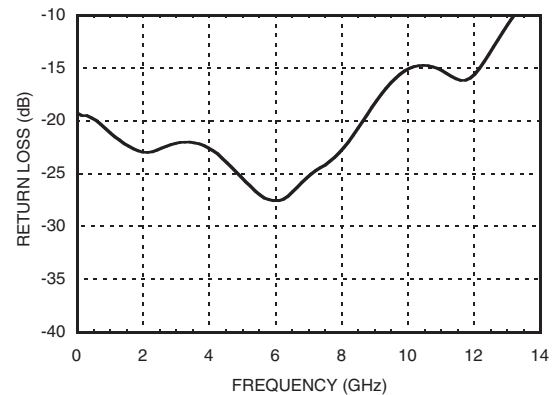
**Rise / Fall Time vs. VR [2]**



**Input Return Loss vs. Frequency**



**Output Return Loss vs. Frequency**



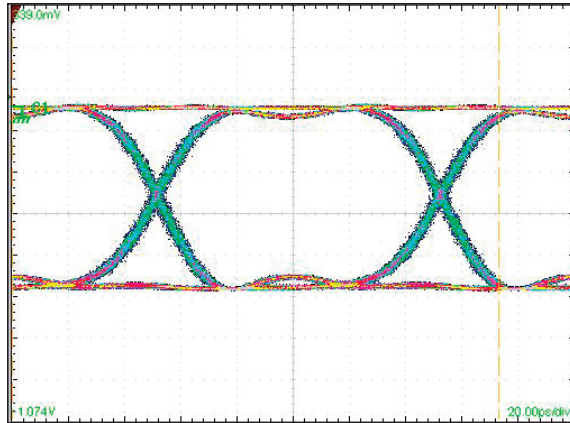
[1] VR = 0.0V

[2] Frequency = 13 GHz

[3] Frequency = 10 GHz

**13 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP  
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**Eye Diagram**



[1] Test Conditions:

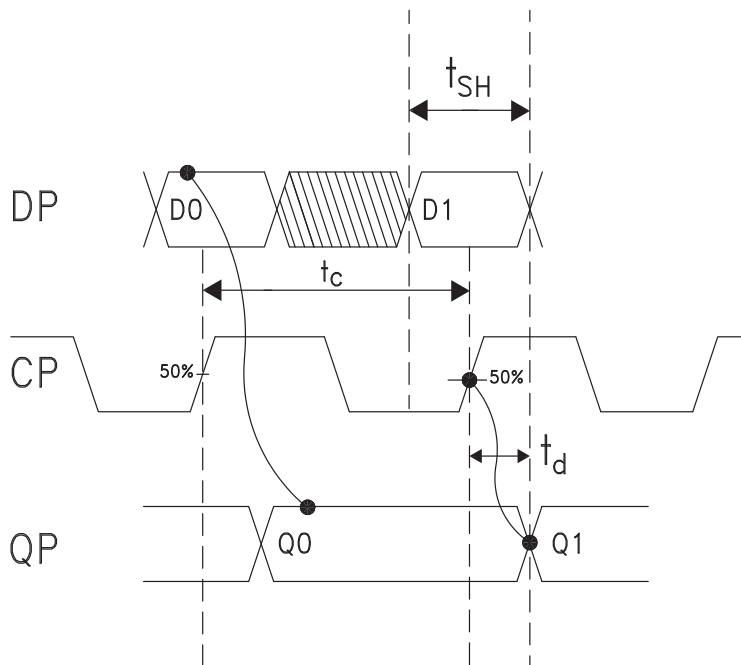
Pattern generated with an Agilent N4903A Serial BERT.

Eye Diagram presented on a Tektronix CSA 8000.

Device input = 13 Gbps PN code,  $V_{in} = 300\text{mVp-p}$  differential.

Both output channels shown.

**Timing Diagram**



$$t_c = \frac{1}{f_{\text{clock}}}$$

$t_{SH}$  = Setup and Hold Time

$$\text{CPM} = \text{Clock Phase Margin} = 360^\circ \frac{t_c - t_{SH}}{t_c}$$

**Truth Table**

| Input                                               |        | Outputs                                                  |
|-----------------------------------------------------|--------|----------------------------------------------------------|
| D                                                   | C      | Q                                                        |
| L                                                   | L -> H | L                                                        |
| H                                                   | L -> H | H                                                        |
| Notes:<br>D = DP - DN<br>C = CP - CN<br>Q = QP - QN |        | H - Positive voltage level<br>L - Negative voltage level |



**13 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP  
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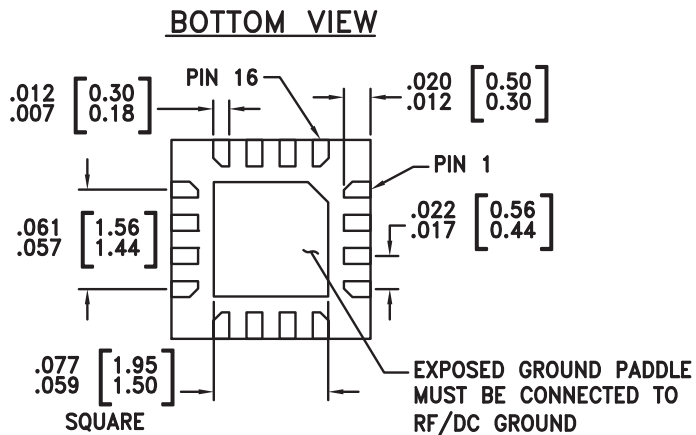
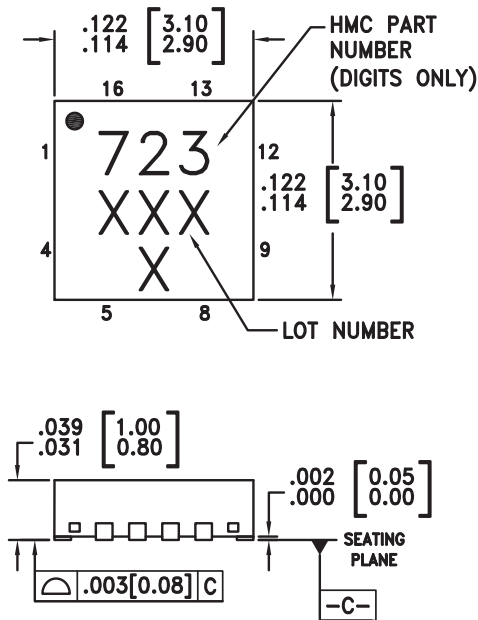
**Absolute Maximum Ratings**

|                            |                 |
|----------------------------|-----------------|
| Power Supply Voltage (Vee) | -3.75V to +0.5V |
| Input Signals              | -2V to +0.5V    |
| Output Signals             | -1.5V to +1V    |
| Storage Temperature        | -65°C to +150°C |
| Operating Temperature      | -40°C to +85°C  |



**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**

**Outline Drawing**



**NOTES:**

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.  
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE  
SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED  
LAND PATTERN.

**Package Information**

| Part Number | Package Body Material                              | Lead Finish   | MSL Rating          | Package Marking <sup>[3]</sup> |
|-------------|----------------------------------------------------|---------------|---------------------|--------------------------------|
| HMC723LP3E  | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 <sup>[2]</sup> | 723<br>XXXX                    |

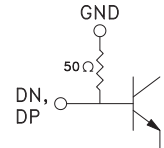
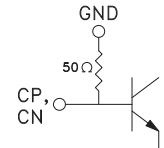
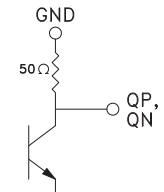
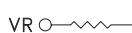
[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

# 13 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP w/ PROGRAMMABLE OUTPUT VOLTAGE

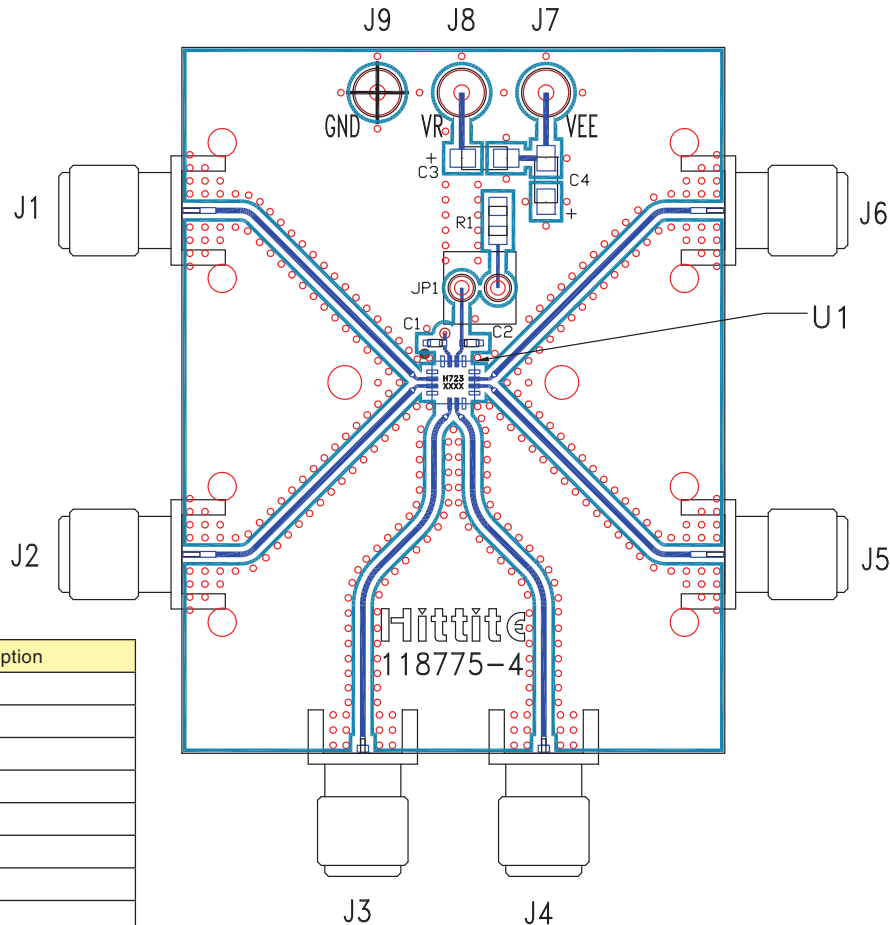
## Pin Descriptions

| Pin Number        | Function | Description                                                                                                                                                                                                                                 | Interface Schematic                                                                   |
|-------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| 1, 4, 5, 8, 9, 12 | GND      | Signal Grounds                                                                                                                                                                                                                              |    |
| 2, 3              | DN, DP   | Data Inputs                                                                                                                                                                                                                                 |    |
| 6, 7              | CP, CN   | Clock Inputs                                                                                                                                                                                                                                |    |
| 10, 11            | QN, QP   | Data Outputs                                                                                                                                                                                                                                |   |
| 13, 16            | GND      | Supply Ground                                                                                                                                                                                                                               |  |
| 14                | VR       | Output level control. Output level may be adjusted by either applying a voltage to VR per "Output Differential vs. VR" plot, or by tying VR to GND with a resistor per the following equation: $V_o(R) = 1.2 / (2.1 + R)$ , R in k $\Omega$ |  |
| 15, Package Base  | Vee      | Negative Supply                                                                                                                                                                                                                             |                                                                                       |



**13 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP  
w/ PROGRAMMABLE OUTPUT VOLTAGE**

**Evaluation PCB**



| Item | Description |
|------|-------------|
| J1   | DN          |
| J2   | DP          |
| J3   | CP          |
| J4   | CN          |
| J5   | QN          |
| J6   | QP          |
| J7   | Vee         |
| J8   | VR          |
| J9   | GND         |

**List of Materials for Evaluation PCB 118777 [1]**

| Item    | Description                                      |
|---------|--------------------------------------------------|
| J1 - J6 | PCB Mount SMA RF Connectors                      |
| J7 - J9 | DC Pin                                           |
| C1, C2  | 100 pF Capacitor, 0402 Pkg.                      |
| C3, C4  | 4.7 $\mu$ F Capacitor, Tantalum                  |
| R1      | 10 Ohm Resistor, 0603 Pkg.                       |
| U1      | HMC723LP3E<br>High Speed Logic, D-Type Flip-Flop |
| PCB [2] | 118775 Evaluation Board                          |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.



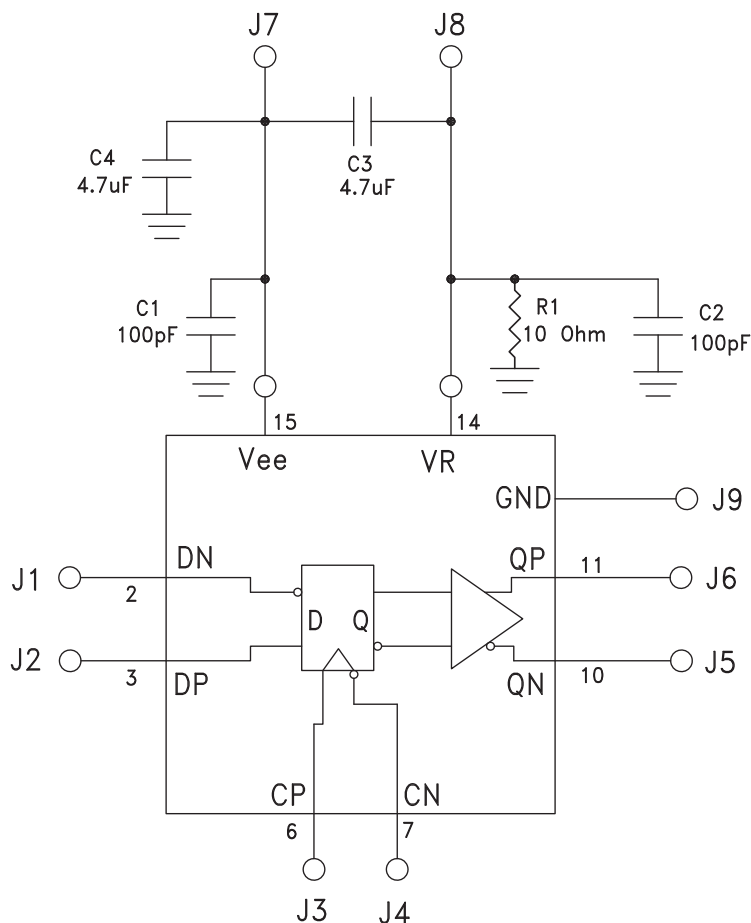
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# HMC723LP3E



## 13 Gbps, FAST RISE TIME D-TYPE FLIP-FLOP w/ PROGRAMMABLE OUTPUT VOLTAGE

## Application Circuit



3

# HIGH SPEED LOGIC - SMT



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