BGS8L2

SiGe:C Low-noise amplifier MMIC with bypass switch for LTE

Rev. 6 — 29 June 2018 Product data sheet

1 General description

The BGS8L2, also known as the LTE3001L, is a Low-Noise Amplifier (LNA) with bypass switch for LTE receiver applications, available in a small plastic 6-pin extremely thin leadless package. The BGS8L2 requires one external matching inductor.

The BGS8L2 delivers system-optimized gain for both primary and diversity applications where sensitivity improvement is required. The high linearity of these low noise devices ensures the required receive sensitivity independent of cellular transmit power level in FDD (Frequency Division Duplex) systems. When receive signal strength is sufficient, the BGS8L2 can be switched off to operate in bypass mode at a 1 µA current, to lower power consumption.

The BGS8L2 can also be used in Digital TV receivers in the frequency range 460 MHz - 740 MHz.

The BGS8L2 is optimized for 460 MHz to 960 MHz.

2 Features and benefits

- Operating frequency from 460 MHz to 960 MHz
- Noise figure = 0.85 dB
- Gain 13 dB
- High input 1 dB compression point of -1 dBm
- Bypass switch insertion loss of 1.9 dB
- $IP3_i$ of 1.5 dBm
- Supply voltage 1.5 V to 3.1 V
- Self-shielding package concept
- Integrated supply decoupling capacitor
- Optimized performance at a supply current of 5.2 mA @ 2.8 V
- Power-down mode current consumption < 1 µA
- Integrated temperature stabilized bias for easy design
- Requires only one input matching inductor
- Input and output DC decoupled
- ESD protection on all pins (HBM > 2 kV)
- Integrated matching for the output
- Available in 6-pins leadless package 1.1 mm × 0.7 mm × 0.37 mm; 0.4 mm pitch: SOT1232
- 180 GHz transit frequency - SiGe:C technology
- Moisture sensitivity level 1

3 Applications

- LNA for LTE reception in smart phones
- Feature phones
- Tablet PCs
- RF front-end modules
- Digital TV receivers

4 Quick reference data

Table 1. Quick reference data

f = 882 MHz; V_{CC} = 2.8 V; $V_{I(CTRL)}$ ≥ 0.8 V; T_{amb} = 25 °C; input matched to 50 Ω using a 8.2 nH inductor; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
I_{CC}	supply current	in gain mode	-	5.2	-	mA
		in bypass mode	-	-	1	µA
G_p	power gain	in gain mode [1]	-	13.0	-	dB
		in bypass mode [1]	-	-1.9	-	dB
NF	noise figure	[1][2]	-	0.85	-	dB
$P_{i(1dB)}$	input power at 1 dB gain compression	[1]	-	-1.0	-	dBm
$IP3_i$	input third-order intercept point	[1]	-	1.5	-	dBm

[1] E-UTRA operating band 5 (869 MHz to 894 MHz).
[2] PCB losses are subtracted.

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BGS8L2	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1.1 × 0.7 × 0.37 mm	SOT1232
OM17005	EVB	BGS8L2 evaluation board	-

6 Marking

Table 3. Marking codes

Type number	Marking code
BGS8L2	M

7 Block diagram

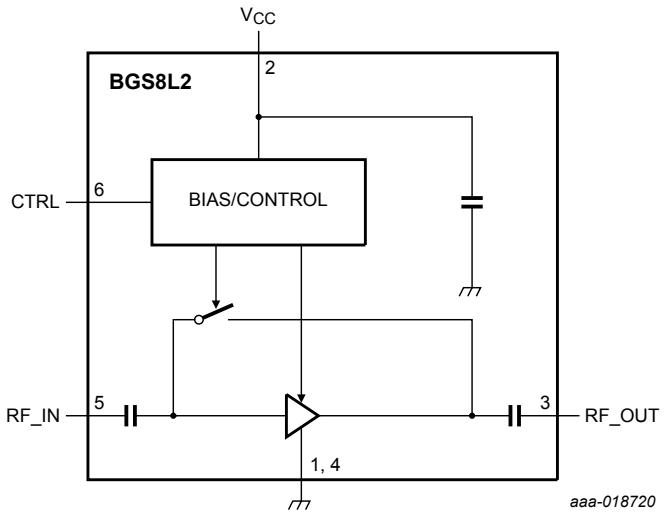


Figure 1. Block diagram

8 Pinning information

8.1 Pinning

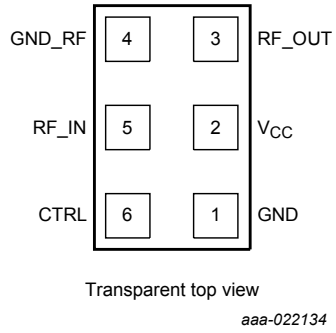


Figure 2. Pin configuration

8.2 Pin description

Table 4. Pinning

Symbol	Pin	Description
GND	1	ground
V_{CC}	2	supply voltage
RF_OUT	3	RF out
GND_RF	4	ground RF
RF_IN	5	RF in
CTRL	6	gain control, switch between gain and bypass mode

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). See section 18.3 "Disclaimers", paragraph "Limiting values".

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	RF input AC coupled [1]	-0.5	+5.0	V
$V_{I(CTRL)}$	input voltage on pin CTRL	$V_{I(CTRL)} < V_{CC} + 0.6$ V [1] [2]	-0.5	+5.0	V
$V_{I(RF\_IN)}$	input voltage on pin RF_IN	DC, $V_{I(RF\_IN)} < V_{CC} + 0.6$ V [1] [2]	-0.5	+5.0	V
$V_{I(RF\_OUT)}$	input voltage on pin RF_OUT	DC, $V_{I(RF\_OUT)} < V_{CC} + 0.6$ V [1] [2] [3]	-0.5	+5.0	V
P_i	input power	[1]	-	26	dBm
P_{tot}	total power dissipation	$T_{sp} \leq 130$ °C	-	55	mW
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	150	°C
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) According to ANSI/ESDA/JEDEC standard JS-001	-	±2	kV
		Charged Device Model (CDM) According to JEDEC standard JESD22-C101C	-	±1	kV

[1] Stresses with pulses of 1 s in duration. V_{CC} connected to a power supply of 2.8 V with 500 mA current limit.
[2] Warning: Due to internal ESD diode protection, to avoid excess current, the applied DC voltage must not exceed V_{CC} + 0.6 V or 5.0 V.
[3] The RF input and RF output are AC coupled through internal DC blocking capacitors.

10 Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.5	-	3.1	V
T_{amb}	ambient temperature		-40	+25	+85	°C
$V_{I(CTRL)}$	input voltage on pin CTRL	OFF state	-	-	0.3	V
		ON state	0.8	-	V_{CC}	V

11 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$		thermal resistance from junction to solder point	225	K/W

12 Characteristics

Table 8. Characteristics at V_{CC} = 1.8 V

460 MHz ≤ f ≤ 960 MHz, V_{CC} = 1.8 V, $V_{I(CTRL)}$ ≥ 0.8 V and T_{amb} = 25 °C. Input matched to 50 Ω using application diagram figure 3 and component values as in table 10. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current		3.0	5.0	7.0	mA
G_p	power gain	f = 470 MHz, L1 = 18 nH [1]	11.5	13.5	15.5	dB
		f = 650 MHz, L1 = 18 nH [1]	12.5	14.5	16.5	dB
		f = 740 MHz, L1 = 18 nH [1]	12.0	14.0	16.0	dB
		f = 740 MHz, L1 = 8.2 nH [1] [2]	11.5	13.5	15.5	dB
		f = 882 MHz, L1 = 8.2 nH [3]	11.0	13.0	15.0	dB
		f = 943 MHz, L1 = 8.2 nH [1] [4]	10.5	12.5	14.5	dB
RL_{in}	input return loss	f = 470 MHz, L1 = 18 nH [5]	-	4.5	-	dB
		f = 650 MHz, L1 = 18 nH	-	12	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	10.5	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]		7.5		dB
		f = 882 MHz, L1 = 8.2 nH [3]	-	12.0	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	13.0	-	dB
RL_{out}	output return loss	f = 470 MHz, L1 = 18 nH	-	10	-	dB
		f = 650 MHz, L1 = 18 nH	-	20.5	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	21.0	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]		21.0		dB
		f = 882 MHz, L1 = 8.2 nH [3]	-	11.0	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	10.0	-	dB
ISL	isolation	f = 470 MHz, L1 = 18 nH	-	28.0	-	dB
		f = 650 MHz, L1 = 18 nH	-	24.0	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	23.0	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]		23.0		dB
		f = 882 MHz, L1 = 8.2 nH [3]	-	22.0	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	21.5	-	dB
NF	noise figure	f = 470 MHz, L1 = 18 nH [1] [6]	-	0.85	1.30	dB
		f = 650 MHz, L1 = 18 nH [1] [6]	-	0.90	1.35	dB
		f = 740 MHz, L1 = 18 nH [1] [2] [6]	-	0.95	1.40	dB
		f = 740 MHz, L1 = 8.2 nH [1] [2] [6]		0.85	1.3	dB
		f = 882 MHz, L1 = 8.2 nH [1] [3] [6]	-	0.85	1.3	dB
		f = 943 MHz, L1 = 8.2 nH [1] [4] [6]	-	0.90	1.35	dB

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 470 MHz, L1 = 18 nH [1]	-13.0	-9.0	-	dBm
		f = 650 MHz, L1 = 18 nH [1]	-12.5	-8.5	-	dBm
		f = 740 MHz, L1 = 18 nH [1] [2]	-11.0	-7.0	-	dBm
		f = 740 MHz, L1 = 8.2 nH [1] [2]	-10.5	-7.5		dBm
		f = 882 MHz, L1 = 8.2 nH [1] [3]	-10	-6.0	-	dBm
		f = 943 MHz, L1 = 8.2 nH [1] [4]	-9.5	-5.5	-	dBm
$IP3_i$	input third-order intercept point	f = 470 MHz, L1 = 18 nH [1]	-10.5	-5.5	-	dBm
		f = 650 MHz, L1 = 18 nH [1]	-6	-1.0	-	dBm
		f = 740 MHz, L1 = 18 nH [1] [2]	-5.5	-0.5	-	dBm
		f = 740 MHz, L1 = 8.2 nH [1] [2]	-4.0	+1.0		dBm
		f = 882 MHz, L1 = 8.2 nH [1] [3]	-4.0	+1.0	-	dBm
		f = 943 MHz, L1 = 8.2 nH [1] [4]	-4.0	+1.0	-	dBm
K	Rollett stability factor		1	-	-	
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON to 90 % of the gain	-	-	2.7	µs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF to 10 % of the gain	-	-	0.6	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bypass mode						
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.3 V	-	-	1	µA
G_p	power gain	f = 470 MHz, L1 = 18 nH [1]	-3.0	-1.5	0.0	dB
		f = 650 MHz, L1 = 18 nH [1]	-4.0	-2.5	-1.0	dB
		f = 740 MHz, L1 = 18 nH [1] [2]	-4.5	-3.0	-1.5	dB
		f = 740 MHz, L1 = 8.2 nH [1] [2]	-3.1	-1.6	-0.1	dB
		f = 882 MHz, L1 = 8.2 nH [3]	-3.5	-2.0	-0.5	dB
		f = 943 MHz, L1 = 8.2 nH [1] [4]	-3.5	-2.0	-0.5	dB
RL_{in}	input return loss	f = 470 MHz, L1 = 18 nH	-	13.0	-	dB
		f = 650 MHz, L1 = 18 nH	-	7.5	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	6.0	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]	-	14.5	-	dB
		f = 882 MHz, L1 = 8.2 nH [3]	-	11.5	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	10.5	-	dB
RL_{out}	output return loss	f = 470 MHz, L1 = 18 nH	-	12.0	-	dB
		f = 650 MHz, L1 = 18 nH	-	8.0	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	6.5	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]	-	12.5	-	dB
		f = 882 MHz, L1 = 8.2 nH [3]	-	11.0	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	10.5	-	dB
Δφ	phase variation	between gain mode and bypass mode				
		f = 470 MHz, L1 = 18 nH	-	-	-	deg
		f = 650 MHz, L1 = 18 nH	-	-	-	deg
		f = 740 MHz, L1 = 18 nH	-	-	-	deg
		f = 740 MHz, L1 = 8.2 nH				deg
		f = 882 MHz, L1 = 8.2 nH [1]	-5.0	-	+5.0	deg
		f = 943 MHz, L1 = 8.2 nH	-	-	-	deg

[1] Guaranteed by device design; not tested in production.
[2] E-UTRA operating band 17 (734 MHz to 746 MHz).
[3] E-UTRA operating band 5 (869 MHz to 894 MHz).
[4] E-UTRA operating band 8 (925 MHz to 960 MHz).
[5] RL_{in} value can be increased by using a higher value for the series input matching inductor L1.
[6] PCB losses are subtracted.

Table 9. Characteristics at V_{CC} = 2.8 V

460 MHz ≤ f ≤ 960 MHz, V_{CC} = 2.8 V, $V_{I(CTRL)}$ ≥ 0.8 V and T_{amb} = 25 °C. Input matched to 50 Ω using application diagram figure 3 and component values as in table 10.. Unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Gain mode						
I_{CC}	supply current		3.2	5.2	7.2	mA
G_p	power gain	f = 470 MHz, L1 = 18 nH [1]	12.0	14.0	16.0	dB
		f = 650 MHz, L1 = 18 nH [1]	13.0	15.0	17.0	dB
		f = 740 MHz, L1 = 18 nH [1] [2]	12.0	14.0	16.0	dB
		f = 740 MHz, L1 = 8.2 nH [1] [2]	11.5	13.5	15.5	dB
		f = 882 MHz, L1 = 8.2 nH [3]	11	13.0	15	dB
		f = 943 MHz, L1 = 8.2 nH [1] [4]	10.5	12.5	14.5	dB
RL_{in}	input return loss	f = 470 MHz, L1 = 18 nH [5]	-	4.5	-	dB
		f = 650 MHz, L1 = 18 nH	-	12.5	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	11.5	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]	-	8.0	-	dB
		f = 882 MHz, L1 = 8.2 nH [3]	-	12.0	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	14.0	-	dB
RL_{out}	output return loss	f = 470 MHz, L1 = 18 nH	-	9.5	-	dB
		f = 650 MHz, L1 = 18 nH	-	20.5	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	20.0	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]	-	21.0	-	dB
		f = 882 MHz, L1 = 8.2 nH [3]	-	12.5	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	10.5	-	dB
ISL	isolation	f = 470 MHz, L1 = 18 nH	-	28.0	-	dB
		f = 650 MHz, L1 = 18 nH	-	24.0	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	23.0	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]	-	23.0	-	dB
		f = 882 MHz, L1 = 8.2 nH [3]	-	22.0	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	21.5	-	dB
NF	noise figure	f = 470 MHz, L1 = 18 nH [1] [6]	-	0.85	1.30	dB
		f = 650 MHz, L1 = 18 nH [1] [6]	-	0.90	1.35	dB
		f = 740 MHz, L1 = 18 nH [1] [2] [6]	-	0.95	1.40	dB
		f = 740 MHz, L1 = 8.2 nH [1] [2] [6]	-	0.85	1.3	dB
		f = 882 MHz, L1 = 8.2 nH [3] [6]	-	0.85	1.3	dB
		f = 943 MHz, L1 = 8.2 nH [1] [4] [6]	-	0.85	1.3	dB

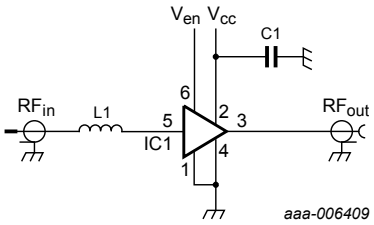
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{i(1dB)}$	input power at 1 dB gain compression	f = 470 MHz, L1 = 18 nH [1]	-8.5	-4.5	-	dBm
		f = 650 MHz, L1 = 18 nH [1]	-7.5	-3.5	-	dBm
		f = 740 MHz, L1 = 18 nH [1] [2]	-6.0	-2.0	-	dBm
		f = 740 MHz, L1 = 8.2 nH [1] [2]	-6.0	-2.0	-	dBm
		f = 882 MHz, L1 = 8.2 nH [1] [3]	-5.0	-1.0	-	dBm
		f = 943 MHz, L1 = 8.2 nH [1] [4]	-4.5	-0.5	-	dBm
$IP3_i$	input third-order intercept point	f = 470 MHz, L1 = 18 nH [1]	-9.5	-4.5	-	dBm
		f = 650 MHz, L1 = 18 nH [1]	-5	0.0	-	dBm
		f = 740 MHz, L1 = 18 nH [1] [2]	-4.5	+0.5	-	dBm
		f = 740 MHz, L1 = 8.2 nH [1] [2]	-3.5	+1.5	-	dBm
		f = 882 MHz, L1 = 8.2 nH [1] [3]	-3.5	+1.5	-	dBm
		f = 943 MHz, L1 = 8.2 nH [1] [4]	-3.5	+1.5	-	dBm
K	Rollett stability factor		1	-	-	
t_{on}	turn-on time	time from $V_{I(CTRL)}$ ON, to 90 % of the gain	-	-	2.1	µs
t_{off}	turn-off time	time from $V_{I(CTRL)}$ OFF, to 10 % of the gain	-	-	0.3	µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bypass mode						
I_{CC}	supply current	$V_{I(CTRL)}$ < 0.3 V	-	-	1	µA
G_p	power gain	f = 470 MHz, L1 = 18 nH [1]	-3.0	-1.5	0.0	dB
		f = 650 MHz, L1 = 18 nH [1]	-4.0	-2.5	-1.0	dB
		f = 740 MHz, L1 = 18 nH [1] [2]	-4.5	-3.0	-1.5	dB
		f = 740 MHz, L1 = 8.2 nH [1] [2]	-3.1	-1.6	-0.1	dB
		f = 882 MHz, L1 = 8.2 nH [3]	-3.4	-1.9	-0.4	dB
		f = 943 MHz, L1 = 8.2 nH [1] [4]	-3.5	-2.0	-0.5	dB
RL_{in}	input return loss	f = 470 MHz, L1 = 18 nH	-	13.0	-	dB
		f = 650 MHz, L1 = 18 nH	-	7.0	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	5.5	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]	-	15.0	-	dB
		f = 882 MHz, L1 = 8.2 nH [3]	-	11.5	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	11.0	-	dB
RL_{out}	output return loss	f = 470 MHz, L1 = 18 nH	-	12.0	-	dB
		f = 650 MHz, L1 = 18 nH	-	8.0	-	dB
		f = 740 MHz, L1 = 18 nH [2]	-	6.5	-	dB
		f = 740 MHz, L1 = 8.2 nH [2]	-	13.0	-	
		f = 882 MHz, L1 = 8.2 nH [3]	-	11.5	-	dB
		f = 943 MHz, L1 = 8.2 nH [4]	-	11.5	-	dB
Δφ	phase variation	between gain mode and bypass mode				
		f = 470 MHz, L1 = 18 nH	-	-	-	deg
		f = 650 MHz, L1 = 18 nH	-	-	-	deg
		f = 740 MHz, L1 = 18 nH	-	-	-	deg
		f = 740 MHz, L1 = 8.2 nH				deg
		f = 882 MHz, L1 = 8.2 nH [1]	-5.0	-	+5.0	deg
		f = 943 MHz, L1 = 8.2 nH	-	-	-	deg

[1] Guaranteed by device design; not tested in production.
[2] E-UTRA operating band 17 (734 MHz to 746 MHz).
[3] E-UTRA operating band 5 (869 MHz to 894 MHz).
[4] E-UTRA operating band 8 (925 MHz to 960 MHz).
[5] RL_{in} value can be increased by using a higher value for the series input matching inductor L1.
[6] PCB losses are subtracted.

13 Application information

13.1 LTE LNA



For a list of component, see Table 10.

Figure 3. Schematics LTE LNA evaluation board

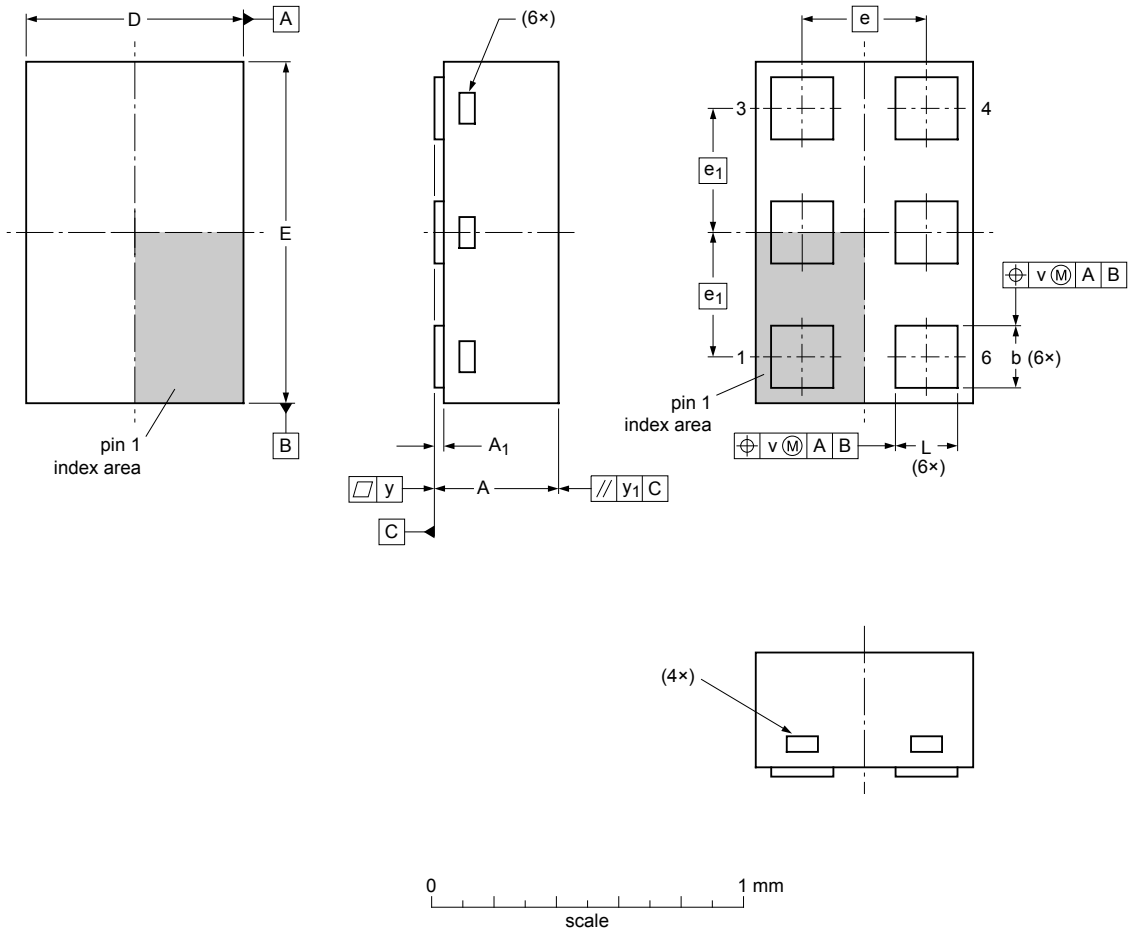
Table 10. List of components

For schematics see, Figure 3.

Component	Description	Value	Remarks
C1	decoupling capacitor	1 µF	to suppress power supply noise
IC1	BGS8L2	-	NXP Semiconductors N.V.
L1	high-quality matching inductor	18 nH	460 < f < 728 MHz Murata LQW15A
		8.2 nH	728 < f < 960 MHz Murata LQW15A

14 Package outline

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1.1 x 0.7 x 0.37 mm **SOT1232**



Dimensions (mm are the original dimensions)

Unit		A	A_1	D	E	e_1	e	b	L	V	Y	Y_1
	min	0.34		0.65	1.05			0.17	0.17			
mm	nom	0.37		0.70	1.10	0.4	0.4	0.20	0.20	0.1	0.05	0.1
	max	0.40	0.04	0.75	1.15			0.25	0.25			

Note
1. Dimension A is including plating thickness.

sot1232_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1232						~~13-04-12~~ 13-11-08

Figure 4. Package outline SOT1232 (XSON6)

15 Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.
Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

16 Abbreviations

Table 11. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
LTE	Long-Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
PCB	Printed-Circuit Board
SiGe:C	Silicon Germanium Carbon

17 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGS8L2 v.6	20180629	product data sheet	-	BGS8L2 v.5
Modifications:	changed $V_{I(CTRL)}$ Max ON state value to V_{cc} at recommended operating conditions			
BGS8L2 v.5	20171116	product data sheet	-	BGS8L2 v.4
Modifications:	• Table 8: added conditions f = 470 MHz, f = 650 MHz, and f = 740 MHz • Table 9: added conditions f = 470 MHz, f = 650 MHz, and f = 740 MHz • Table 10: added value 18 nH			
BGS8L2 v.4	20170117	Product data sheet	-	BGS8L2 v.3
Modifications:	• Section 1: added LTE3001L according to our new naming convention			
BGS8L2 v.3	20160329	Product data sheet	-	BGS8L2 v.2
Modifications:	• Table 8 on page 5: added maximum value in G_p • Table 9 on page 6: added minimum value in $P_{i(1dB)}$ • Table 9 on page 6: added maximum value in $IP3_i$			
BGS8L2 v.2	20160316	Product data sheet	-	BGS8L2 v.1
Modifications:	• added phase variation Table 8 on page 5 and Table 9 on page 6			
BGS8L2 v.1	20151221	Product data sheet	-	-

18 Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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