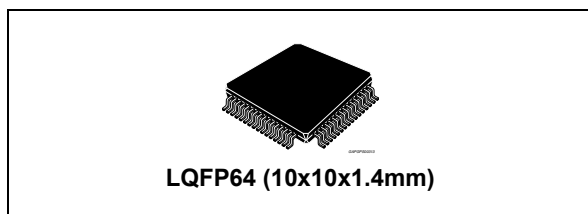


3 band car audio processor

Datasheet - production data



Features

- Input multiplexer
 - QD0 to QD3: quasi-differential stereo input
 - SE0 to SE4: stereo single-ended input
- Loudness
 - 2nd order frequency response
 - Programmable center frequency (400 Hz/800 Hz/2400 Hz)
 - 15 dB with 1 dB steps
 - Selectable high frequency boost
 - Selectable flat-mode (constant attenuation)
- Volume
 - +23 dB to –23 dB with 1 dB step resolution
 - SoftStep control with programmable blend times
- Bass
 - 2nd order frequency response
 - Programmable center frequency (60/70/80/100//110/120/130/150 Hz)
 - Q programmable 1.0/1.25/1.5/2.0
 - DC gain programmable
 - -15 to 15 dB range with 1 dB resolution
 - SoftStep control with programmable blend times
- Middle
 - 2nd order frequency response
 - Programmable center frequency (500 Hz/1 kHz/1.5 kHz/2 kHz)
 - Q programmable 1.0/2.0
 - -15 to 15 dB range with 1 dB resolution
 - SoftStep control with programmable blend times
- Treble
 - 2nd order frequency response
- Center frequency programmable in 4 steps (10/12.5 /15/17.5 kHz)
- -15 to 15 dB range with 1 dB resolution
- SoftStep control with programmable blend times
- High pass filter
 - Two stereo-HPF for output0 and output1
 - 2nd order frequency response
 - Programmable cut off frequency (50/60/80/100/120/150/180/220 Hz)
- Low pass filter
 - One mono-LPF for output2
 - 2nd order low pass filter
 - Programmable cut off frequency (50 Hz/60 Hz/80 Hz/100 Hz/120 Hz)
- Speaker
 - 6 independent SoftStep speaker controls
 - +23 dB to –79 dB with 1 dB steps
 - SoftStep control with programmable blend times
- Output driver
 - Four dedicated outputs for an internal (on-board) power amplifier. (share output driver with line driver)
 - Six line-driver outputs for an external (remote) power amplifier
- Mute functions
 - Direct mute
 - Main/Sub channel: digitally controlled SoftMute with 4 programmable mute-times (0.5 ms/4 ms/8 ms/16 ms)
 - Speaker: digitally controlled SoftMute with 4 programmable mute-times (4 ms/8 ms/32 ms/64 ms)
- AC coupling
 - Three AC-coupling input
 - One AC-coupling output
- Offset detection
 - Offset voltage detection circuit for on-board power amplifier failure diagnosis

Table 1. Device summary

Order code	Package	Packing
TDA7715LV	LQFP64	Tray

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1 Description and block circuit diagram

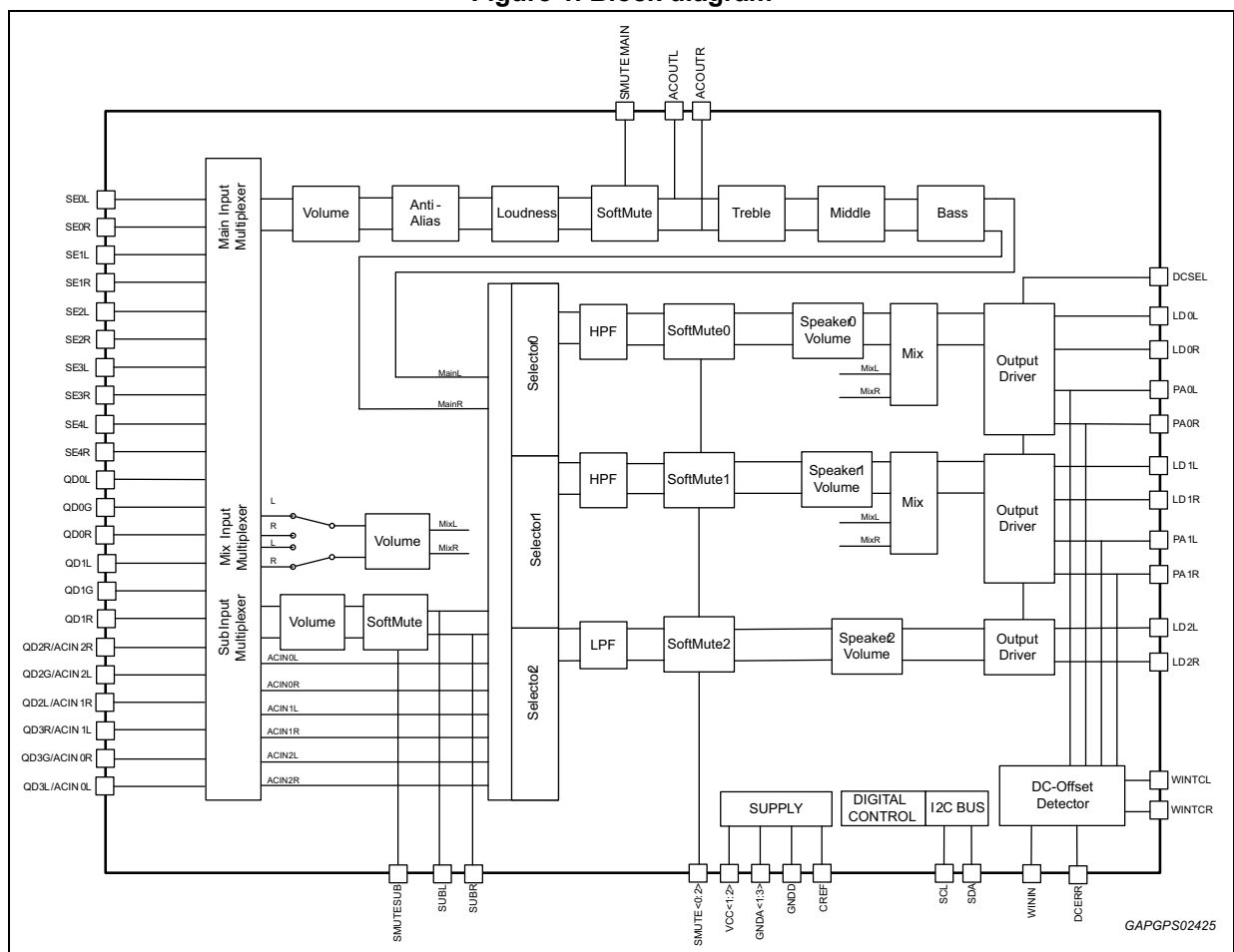
1.1 Description

The TDA7715LV is a high performance signal processor specifically designed for car radio applications.

The device includes a high performance audio processor with fully integrated audio filters and new SoftStep architecture. The digital control allows programming in a wide range of filter characteristics.

1.2 Block circuit diagram

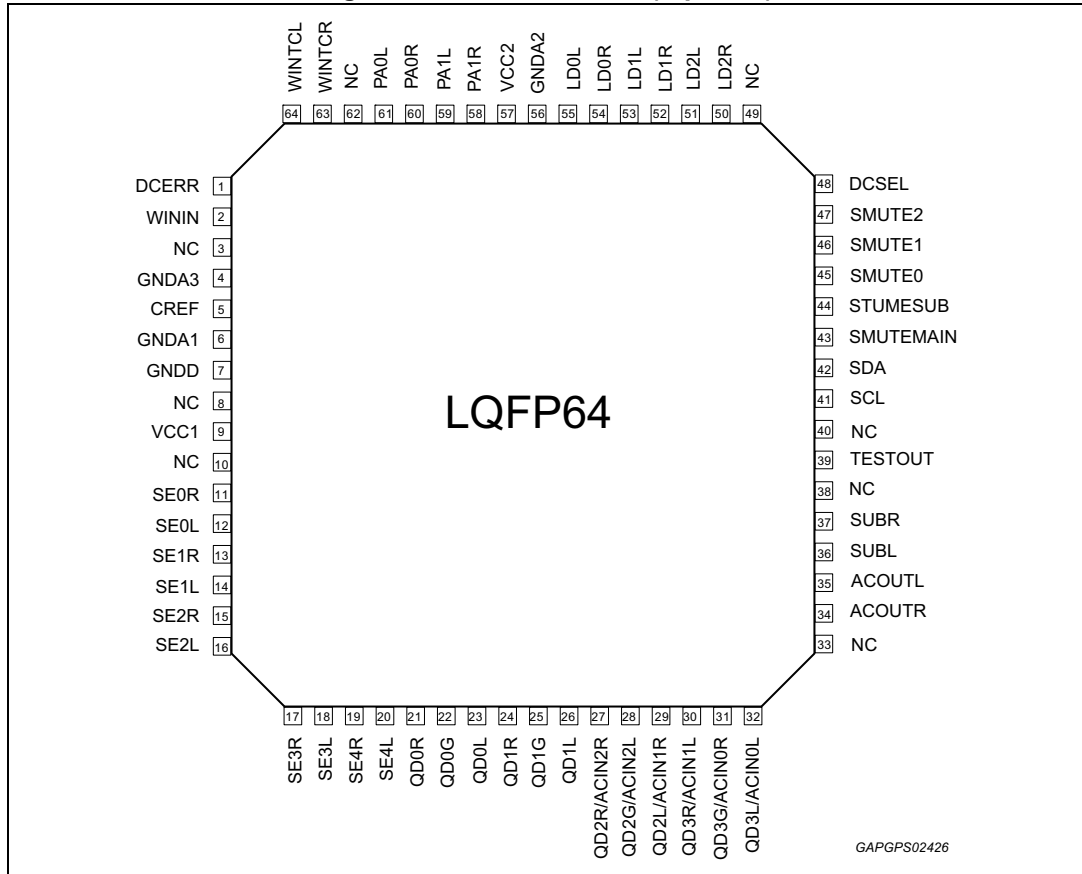
Figure 1. Block diagram



2 Pins connection and description

2.1 Pins connection

Figure 2. Pins connection (top view)



2.2 Pins description

Table 2. Pins description

N#	Pin name	Description	I/O
1	DCERR	DC offset detector output	O
2	WININ	DC offset detector input	I
3	NC	No connected	NC
4	GNDA3	Analog Ground	S
5	CREF	Reference capacitor	O
6	GNDA1	Analog Ground	S
7	GNDD	Digital Ground	S
8	NC	No connected	NC

Table 2. Pins description (continued)

N#	Pin name	Description	I/O
9	VCC1	Supply	S
10	NC	No connected	NC
11	SE0R	Single-end input right	I
12	SE0L	Single-end input left	I
13	SE1R	Single-end input right	I
14	SE1L	Single-end input left	I
15	SE2R	Single-end input right	I
16	SE2L	Single-end input left	I
17	SE3R	Single-end input right	I
18	SE3L	Single-end input left	I
19	SE4R	Single-end input right	I
20	SE4L	Single-end input left	I
21	QD0R	Quasi-differential stereo inputs right	I
22	QD0G	Quasi-differential stereo inputs common	I
23	QD0L	Quasi-differential stereo inputs left	I
24	QD1R	Quasi-differential stereo inputs right	I
25	QD1G	Quasi-differential stereo inputs common	I
26	QD1L	Quasi-differential stereo inputs left	I
27	QD2R/ACIN2R	Quasi-differential stereo inputs right or ac-coupling input	I
28	QD2G/ACIN2L	Quasi-differential stereo inputs common or ac-coupling input	I
29	QD2L/ACIN1R	Quasi-differential stereo inputs left or ac-coupling input	I
30	QD3R/ACIN1L	Quasi-differential stereo inputs right or ac-coupling input	I
31	QD3G/ACIN0R	Quasi-differential stereo inputs common or ac-coupling input	I
32	QD3L/ACIN0L	Quasi-differential stereo inputs left or ac-coupling input	I
33	NC	No connected	NC
34	ACOUTR	AC coupling output, right channel	O
35	ACOUTL	AC coupling output, left channel	O
36	SUBL	Sub channel output left	O
37	SUBR	Sub channel output right	O
38	NC	No connected	NC
39	TESTOUT	Test pin	O
40	NC	No connected	NC
41	SCL	I ² C bus clock	I
42	SDA	I ² C bus data	I/O
43	SMUTEMAIN	External mute pin for main channel	I

Table 2. Pins description (continued)

N#	Pin name	Description	I/O
44	SMUTESUB	External mute pin for sub channel	I
45	SMUTE0	External mute pin for speaker, signal path 0	I
46	SMUTE1	External mute pin for speaker, signal path 1	I
47	SMUTE2	External mute pin for speaker, signal path 2	I
48	DCSEL	Output DC level select	I
49	NC	No connected	NC
50	LD2R	Line driver output right	O
51	LD2L	Line driver output left	O
52	LD1R	Line driver output right	O
53	LD1L	Line driver output left	O
54	LD0R	Line driver output right	O
55	LD0L	Line driver output left	O
56	GND A2	Analog Ground	S
57	VCC2	Supply	S
58	PA1R	Out-section rear output, right channel	O
59	PA1L	Out-section rear output, left channel	O
60	PA0R	Out-section front output, right channel	O
61	PA0L	Out-section front output, left channel	O
62	NC	No connected	NC
63	WINTCR	DC offset detector filter output right channel	O
64	WINTCL	DC offset detector filter output left channel	O

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{th\ j-amb}$	Thermal resistance junction-to-ambient	50	°C/W

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Operating supply voltage	13	V
V_{in_max}	Maximum voltage for signal input pins	7	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C
V_{ESD}	ESD withstand voltage: Human body model Charged device model	$\geq \pm 2000$ $\geq \pm 500$	V

3.3 Electrical characteristics

$V_{CC} = 8.5\text{ V}$; $T_{amb} = 25\text{ °C}$; $R_L = 10\text{ k}\Omega$; all gains = 0 dB; $f = 1\text{ kHz}$; Input = SE1;
Output = PAout; unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
V_{CC}	Supply voltage	-	4.5	8.5	12.5	V
I_S	Supply current	-	36	48	60	mA
Input selector						
R_{IN}	Input resistance	All single ended inputs	70	100	130	k Ω
V_{CL}	Clipping level	All flat, $V_{CC} \geq 5\text{ V}$, THD = 1%	1	1.06	1.1	V_{RMS}
		All flat, $V_{CC} \geq 4.5\text{ V}$, THD = 1%	0.65	0.707	0.75	V_{RMS}
S_{IN}	Input separation	-	80	100	-	dB
Differential stereo inputs						
R_{in}	Input resistance	Differential	70	100	130	k Ω

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
CMRR	Common mode rejection ratio for main source	$V_{CM}=1 V_{RMS}$ @ 1 kHz	46	60	-	dB
		$V_{CM}=1 V_{RMS}$ @ 10 kHz	46	60	-	dB
Loudness control						
A_{MAX}	Max attenuation ⁽¹⁾	-	14	15	16	dB
A_{STEP}	Step resolution ⁽¹⁾	-	0.5	1	1.5	dB
f_{Peak}	Peak frequency ⁽²⁾	f_{P1}	-	400	-	Hz
		f_{P2}	-	800	-	Hz
		f_{P3}	-	2400	-	Hz
Volume control						
G_{MAX}	Max gain ⁽¹⁾	-	21	23	25	dB
A_{MAX}	Max attenuation ⁽¹⁾	-	-26	-23	-20	dB
A_{STEP}	Step resolution ⁽¹⁾	-	0.5	1	1.5	dB
E_A	Attenuation set error	$G = -23$ to $+23$ dB	-1.5	0	1.5	dB
E_T	Tracking error	Gain difference of left/right	-	-	0.8	dB
V_{DC}	DC steps	Adjacent gain step from $+23$ to $+15$ dB	-15	-	+15	mV
		Adjacent gain step from $+15$ to 0 dB	-5	-	+5	mV
		Adjacent attenuation step	-2	-	2	mV
SoftStep						
T_{SS}	Soft step time	T_1	5	7.5	12.5	ms
		T_2	10	15	25	ms
SoftMute						
A_{MUTE}	Mute attenuation	-	80	100	-	dB
T_{D1}	Delay time (main & sub channel)	T_1	0.4	0.5	0.6	ms
		T_2	3	4	5	ms
		T_3	6	8	10	ms
		T_4	14	16	18	ms
T_{D2}	Delay time (speaker)	T_1	3	4	5	ms
		T_2	6	8	10	ms
		T_3	29	32	35	ms
		T_4	60	64	68	ms
V_{TH_Low}	Low threshold for MUTE pin ⁽³⁾	-	-	0.8	-	V
V_{TH_High}	High threshold for MUTE pin ⁽³⁾	-	2.4	-	-	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
RPU	Internal pull-up resistor for MUTE Pin	-	25	45	65	kΩ
VPU	Internal pull-up Voltage for MUTE Pin	-	3.1	3.3	3.5	V
Bass control						
Fc	Center frequency ⁽²⁾	f _{C0}	-	60	-	Hz
		f _{C1}	-	70	-	Hz
		f _{C2}	-	80	-	Hz
		f _{C3}	-	100	-	Hz
		f _{C4}	-	110	-	Hz
		f _{C5}	-	120	-	Hz
		f _{C6}	-	130	-	Hz
		f _{C7}	-	150	-	Hz
Q _{BASS}	Quality factor ⁽²⁾	Q ₁	-	1	-	-
		Q ₂	-	1.25	-	-
		Q ₃	-	1.5	-	-
		Q ₄	-	2	-	-
C _{RANGE}	Control range ⁽¹⁾	-	±14	±15	±16	dB
A _{STEP}	Step resolution ⁽¹⁾	-	0.5	1	1.5	dB
DC _{GAIN}	Bass DC gain ⁽¹⁾	DC = off	-1	0	+1	dB
		DC = on, Gain= 14 dB	3.5	4.4	5.5	dB
Middle control						
C _{RANGE}	Control range ⁽¹⁾	-	±14	±15	±16	dB
A _{STEP}	Step resolution ⁽¹⁾	-	0.5	1	1.5	dB
Fc	Center frequency ⁽²⁾	f _{C1}	-	500	-	Hz
		f _{C2}	-	1	-	kHz
		f _{C3}	-	1.5	-	kHz
		f _{C4}	-	2	-	kHz
Q _{Middle}	Quality factor ⁽²⁾	Q ₁	-	1	-	-
		Q ₂	-	2	-	-
Treble control						
C _{RANGE}	Control Range ⁽¹⁾	-	±14	±15	±16	dB
A _{STEP}	Step Resolution ⁽¹⁾	-	0.5	1	1.5	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F _C	Center frequency ⁽²⁾	f _{C1}	-	10	-	kHz
		f _{C2}	-	12.5	-	kHz
		f _{C3}	-	15	-	kHz
		f _{C4}	-	17.5	-	kHz
AC coupling						
R _{IN}	Input resistance	AC inputs	70	100	130	kΩ
V _{CL}	Clipping level	flat, THD = 1%	1	1.06	1.1	V _{RMS}
R _{OUT}	Output impedance	AC outputs	-	20	50	Ω
Speaker volume						
G _{MAX}	Max gain ⁽¹⁾	-	22	23	24	dB
A _{MAX}	Max attenuation ⁽¹⁾	-	-85	-79	-73	dB
A _{STEP}	Step resolution ⁽¹⁾	-	0.5	1	1.5	dB
A _{MUTE}	Mute attenuation	-	80	90	-	dB
E _E	Attenuation set error	G = -20 to +15 dB	-1	-	1	dB
		G = -20 to -79 dB	-4	-	4	dB
V _{DC}	DC steps	Adjacent gain step from +23 to +15 dB	-20	-	+20	mV
		Adjacent gain step from +15 to 0 dB	-10	-	+10	mV
		Adjacent attenuation step	-2	-	2	mV
Highpass						
F _{HP}	High-pass corner frequency ⁽²⁾	f _{C0}	-	50	-	Hz
		f _{C1}	-	60	-	Hz
		f _{C2}	-	80	-	Hz
		f _{C3}	-	100	-	Hz
		f _{C4}	-	120	-	Hz
		f _{C5}	-	150	-	Hz
		f _{C6}	-	180	-	Hz
		f _{C7}	-	220	-	Hz

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Low pass						
F _{LP}	Low pass corner frequency ⁽²⁾	f _{C0}	-	50	-	Hz
		f _{C1}	-	60	-	Hz
		f _{C2}	-	80	-	Hz
		f _{C3}	-	100	-	Hz
		f _{C4}	-	120	-	Hz
Audio outputs						
V _{CL}	Clipping level	THD = 1%; V _{CC} = 5 V Option1	1.6	1.7	1.8	V _{RMS}
		THD = 1%; V _{CC} = 6 V Option2	1.9	2.0	2.1	V _{RMS}
		THD = 1%; V _{CC} = 8.5 V Option3	2.7	2.8	2.9	V _{RMS}
		THD = 1%; V _{CC} = 4.5 V Option1	1.1	1.27	1.35	V _{RMS}
		THD = 1%; V _{CC} = 4.5 V Option2	0.9	0.95	1.0	V _{RMS}
		THD = 1%; V _{CC} = 4.5 V Option3	0.15	0.21	0.27	V _{RMS}
R _{OUT}	Output impedance	PA Output	-	40	100	Ω
		LD Output	-	20	50	Ω
R _L	Output load resistance	-	2	-	-	kΩ
C _L	Output load capacitor	-	-	-	10	nF
V _{DC}	Output DC level	Option1	2.3	2.5	2.7	V
		Option2	2.8	3	3.2	V
		Option3	3.8	4	4.2	V
G _{OUT}	Output gain	Option1	3.5	3.7	3.9	dB
		Option2	5.8	6.0	6.2	dB
		Option3	8.3	8.5	8.7	dB
G _{mix}	Mixing gain	-	5	6	7	dB
V _{TH_Low}	Low threshold for DCSEL pin ⁽³⁾	-	-	-	0.8	V
V _{TH_High}	High threshold for DCSEL pin ⁽³⁾	-	2.4	-	-	V
R _{PU}	Internal pull-up resistor for DCSEL pin	-	32	50	68	kΩ
V _{PU}	Internal pull-up voltage for DCSEL Pin	-	3.1	3.3	3.5	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	
DC offset detection							
V_{th}	Zero comp. window size	V_1	-	± 30	-	mV	
		V_2	-	± 45	-	mV	
		V_3	-	± 60	-	mV	
		V_4	-	± 90	-	mV	
T_{sp}	Max rejected spike length	-	4	11	25	μs	
		-	8	22	38	μs	
		-	10	33	55	μs	
$I_{CHDCErr}$	DCErr charge current	-	3	5	6	μA	
$I_{DISDCErr}$	DCErr discharge current	-	3.5	5	7.5	mA	
V_{OutH}	DCErr high voltage	-	3.1	3.3	3.6	V	
V_{OutL}	DCErr low voltage	-	-	100	500	mV	
V_{TH_Low}	Low threshold for WinIn pin ⁽³⁾	-	-	-	0.8	V	
V_{TH_High}	High threshold for WinIn pin ⁽³⁾	-	2.4	-	-	V	
R_{PU}	Internal pull-up resistor for WinIn pin	-	32	50	68	k Ω	
V_{PU}	Internal pull-up voltage for WinIn pin	-	3.1	3.3	3.5	V	
General							
e_{NO}	Output noise	BW = 20 Hz to 20 kHz; A-Weighted; all gain = 0dB	Option1	-	14	20	μV
			Option2	-	17	23	μV
			Option3	-	23	28	μV
		BW = 20 Hz to 20 kHz; A-Weighted, Output muted	Option1	-	12	18	μV
			Option2	-	14	21	μV
			Option3	-	18	26	μV
S/N	Signal to noise ratio	A-weighted; all gain = 0dB	Option1	99	101	-	dB
			Option2	99	101	-	dB
			Option3	99	101	-	dB
D	Distortion	$V_{IN}=0.5V_{RMS}$; all gain = 0dB	Option1	-	0.01	0.1	%
			Option2	-	0.01	0.1	%
			Option3	-	0.01	0.1	%
S_C	Channel Separation left/right	-	75	90	-	dB	

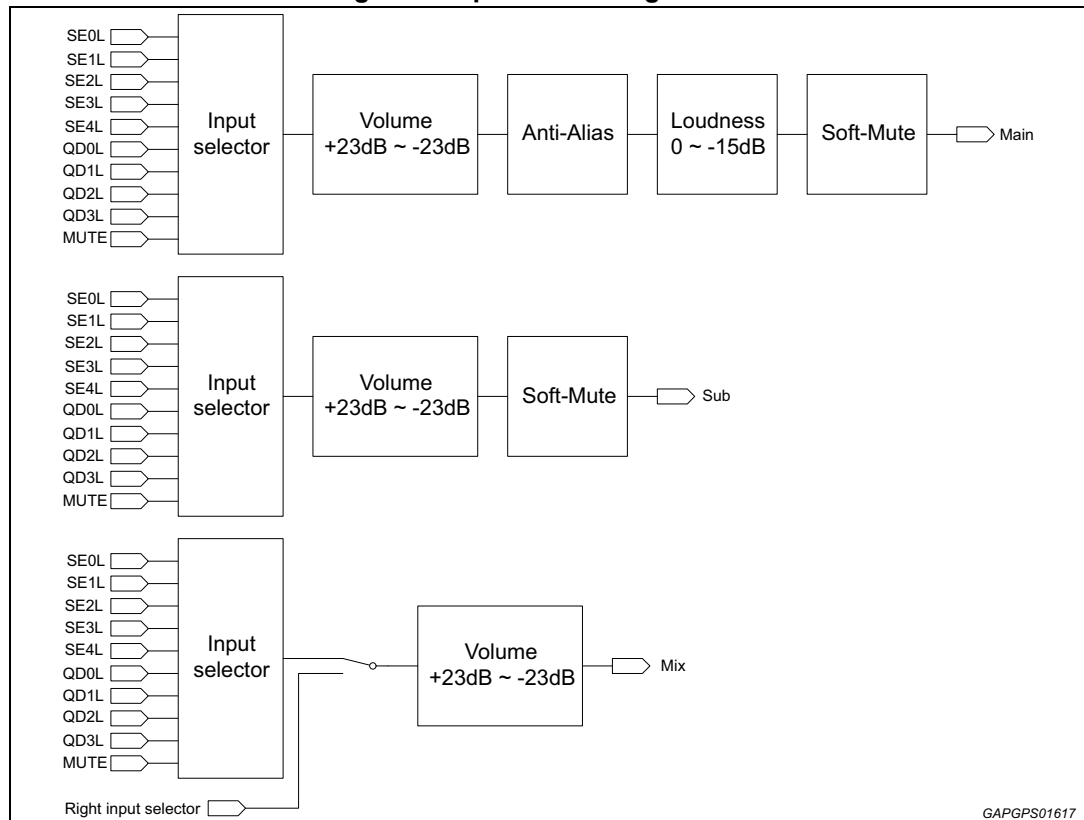
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4 Description of audio processor

4.1 Input stage

Four quasi-differential stereo input and five single-ended inputs are available. The input-section of the TDA7715LV incorporates three independent stereo signal paths, where each of them can be connected to a variety of inputs. For simplicity only the left inputs are shown.

Figure 3. Input section signal flow



4.1.1 Single-ended stereo input (SE0, SE1, SE2, SE3, SE4)

The input-impedance at each input is 100 kΩ.

4.1.2 Quasi-differential stereo Input (QD0, QD1, QD2, QD3)

The QD input is implemented as a buffered quasi-differential stereo stage with 100 kΩ input-impedance at each input.

4.1.3 Fast charge

Each differential input pin features a "fast-charge" switch allowing to quickly charge any external large coupling capacitors upon power-on of the device. When the device is powered-on, the "fast-charge" switches are automatically turned on, for normal operations these switches need to be released by any programming of byte_0.

4.2 Volume

A ± 23 dB input gain is selectable in volume stage. When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks could be either a DC-Offset before the volume-stage or the sudden change of the envelope of the audio signal. With the SoftStep feature both kind of clicks could be reduced to a minimum and are no more audible.

The blend-time from one step to the next is programmable as 7.5 ms or 15 ms. The SoftStep control is described in detail in [Section 4.8](#).

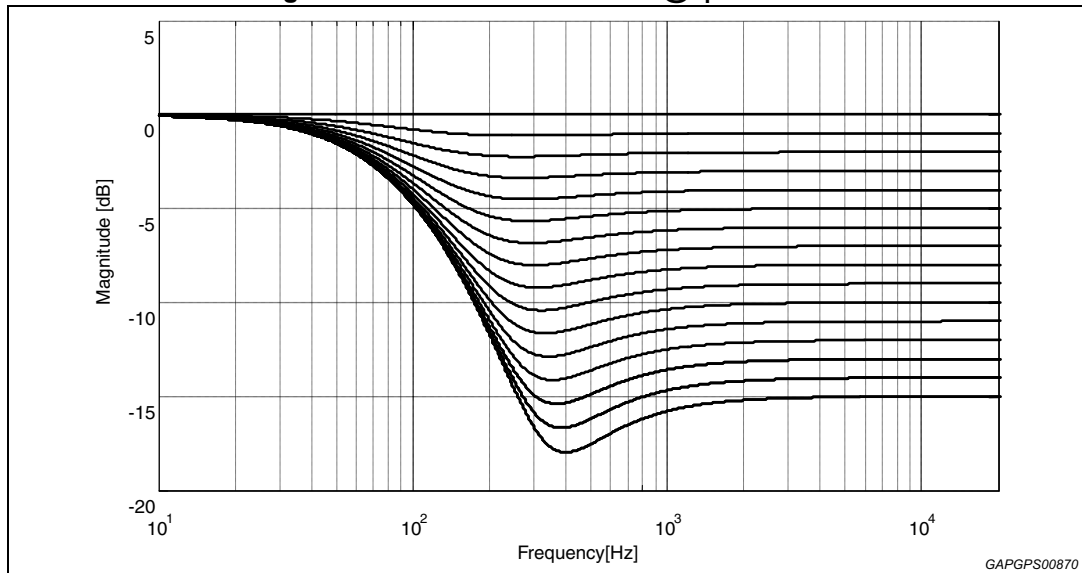
4.3 Loudness

There are four parameters programmable in the loudness stage.

4.3.1 Loudness attenuation

[Figure 4](#) shows the attenuation as a function of frequency at $f_p = 400$ Hz

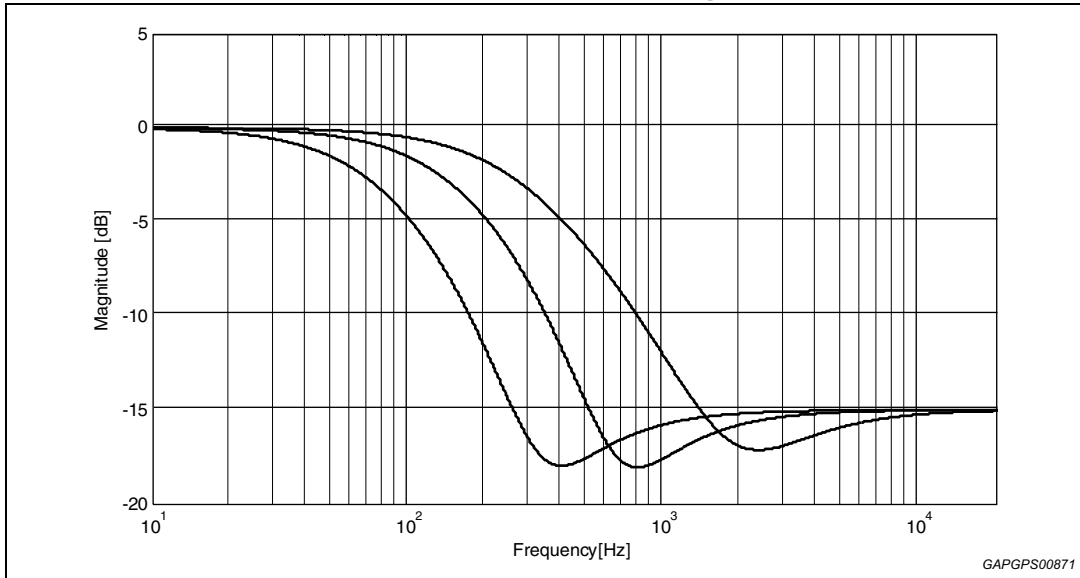
Figure 4. Loudness attenuation @ $f_p = 400$ Hz



4.3.2 Peak frequency

Figure 5 shows the three possible peak-frequencies at 400, 800 and 2400 Hz

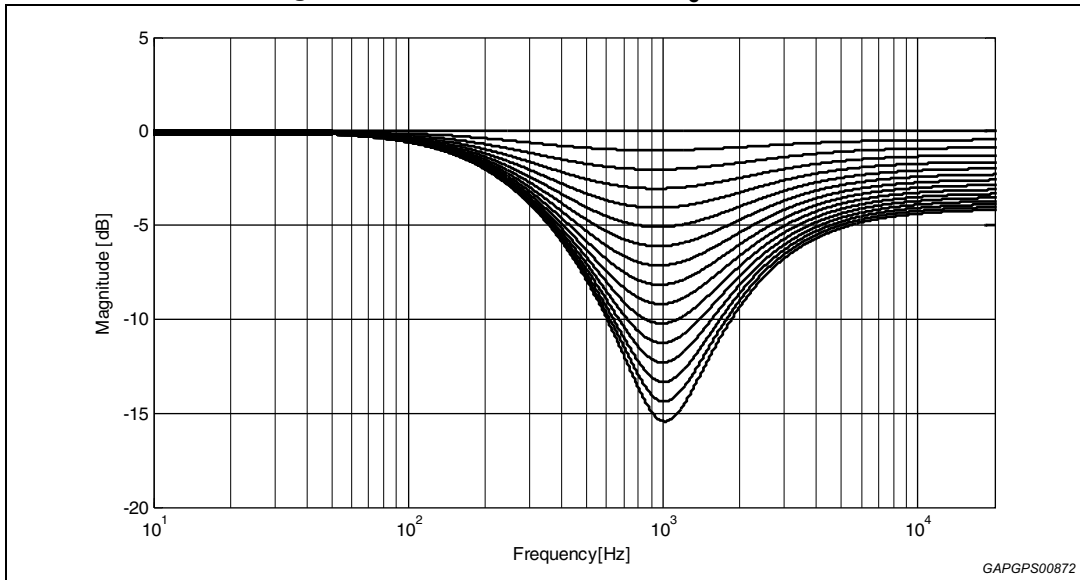
Figure 5. Loudness center frequencies @ attn. = 15 dB



4.3.3 High frequency boost

Figure 6 shows the different loudness shapes in low & high frequency boost.

Figure 6. Loudness attenuation, $f_c = 2.4$ kHz



4.3.4 Flat mode

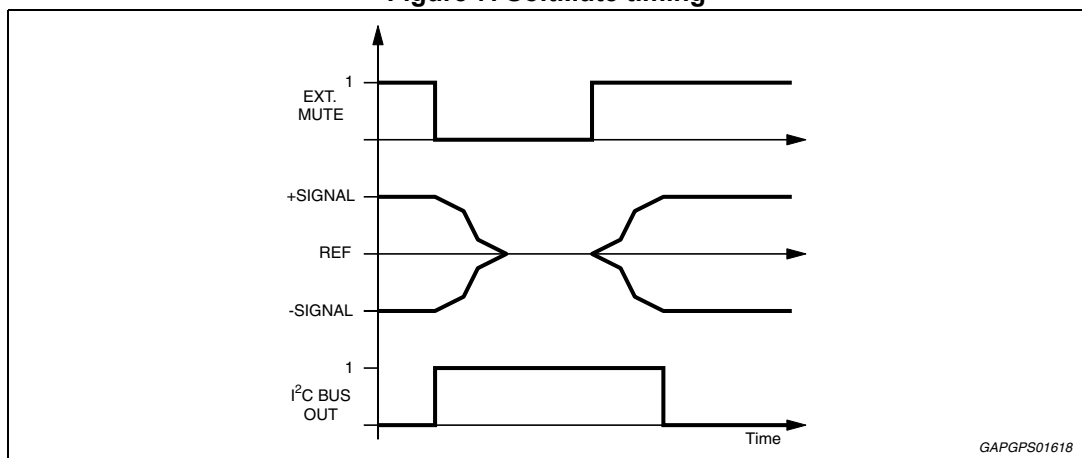
In flat mode the loudness stage works as a 0 dB to -15 dB attenuator.

4.4 SoftMute

The digitally controlled SoftMute stage allows muting/de-muting the signal with an I²C bus programmable slope. The mute process can be activated either by the SoftMute pin or by the I²C-bus. This slope is realized in a special S-shaped curve to mute slowly in the critical regions (see [Figure 7](#)).

For timing purposes the SoftMute bit of the I²C bus output register is set to 1 from the start of muting until the end of de-muting.

Figure 7. SoftMute timing



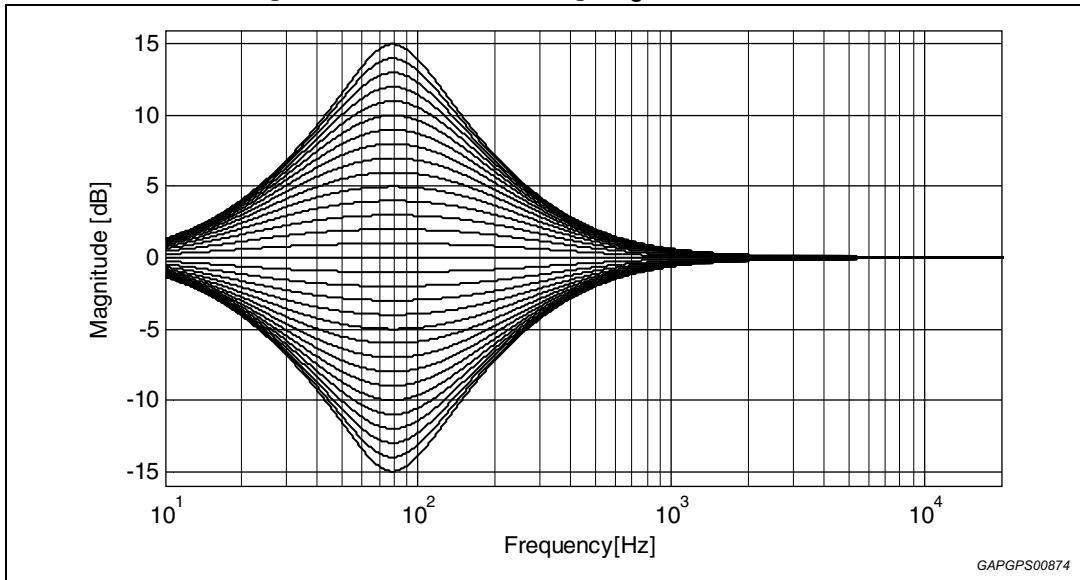
Note: Please note that a started Mute-action is always terminated and could not be interrupted by a change of the mute –signal.

4.5 Bass

4.5.1 Bass attenuation

Figure 8 shows the control range in the frequency domain at 80 Hz center frequency.

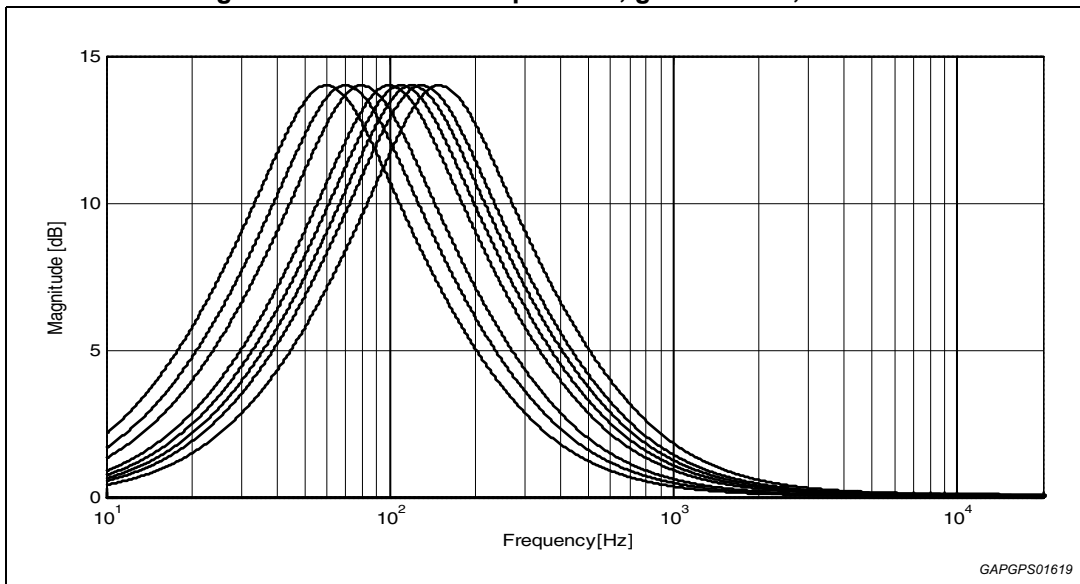
Figure 8. Bass control range; $f_c = 80$ Hz, $Q = 1.0$



4.5.2 Center frequency

Figure 9 shows all the selectable center frequencies at a gain of 14 dB.

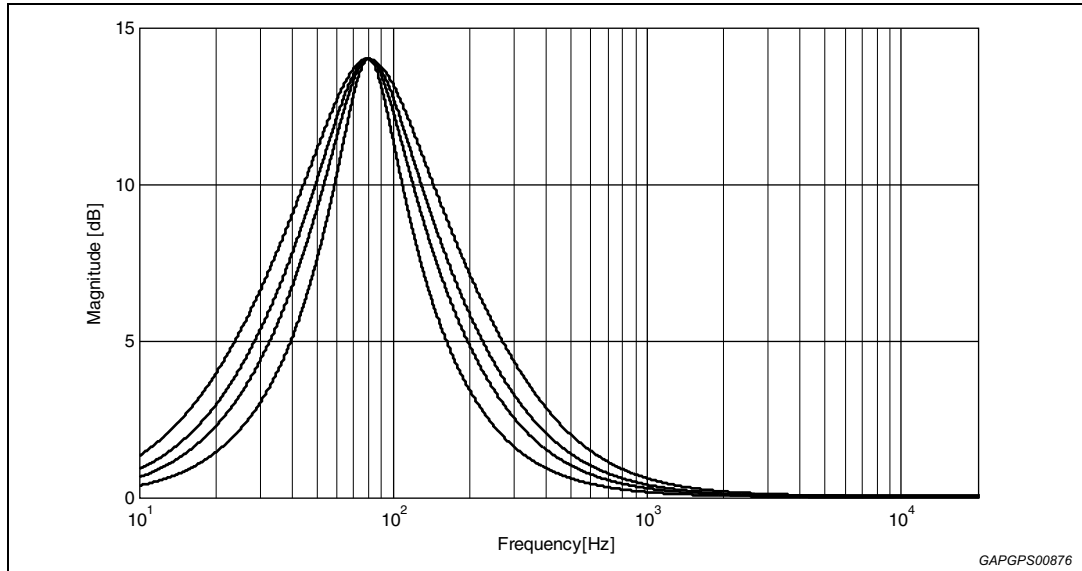
Figure 9. Bass center frequencies; gain = 14 dB, $Q = 1.0$



4.5.3 Quality factors

Figure 10 shows the four selectable filter quality factors at a gain of 14 dB.

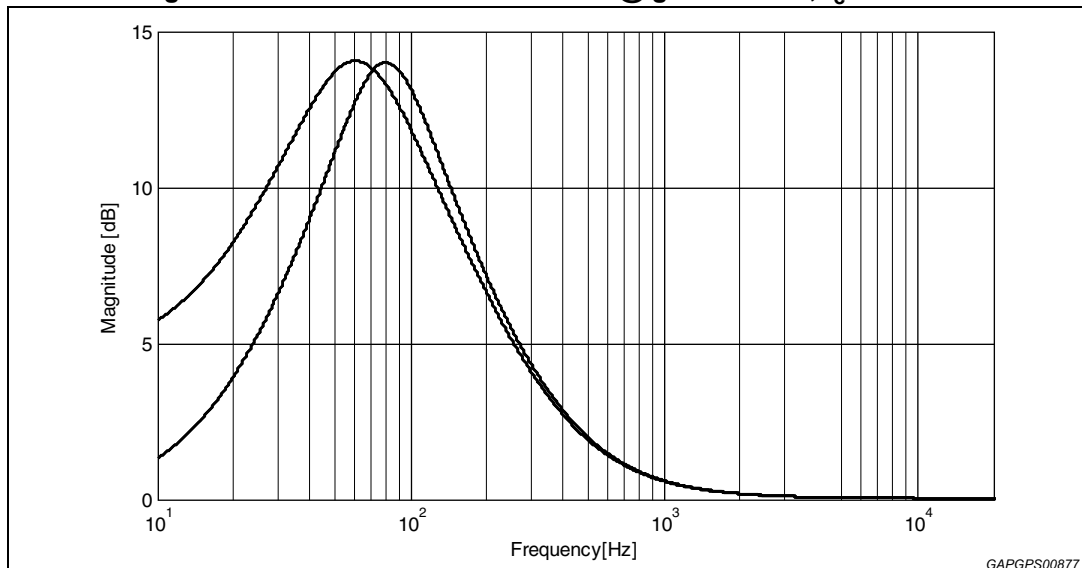
Figure 10. Bass filter quality factors; $f_c = 80$ Hz, gain = 14 dB.



4.5.4 DC Mode

Figure 11 shows the effect of the DC-mode at a filter gain of 14 dB. In this mode the DC-gain is increased by 4.4 dB. In addition the programmed center frequencies and quality factors are decreased by 25%, which realize alternative frequency responses.

Figure 11. Bass normal and DC mode @ gain = 14 dB, $f_c = 80$ Hz



Note: The center frequency, Q and DC-mode can be independently set.

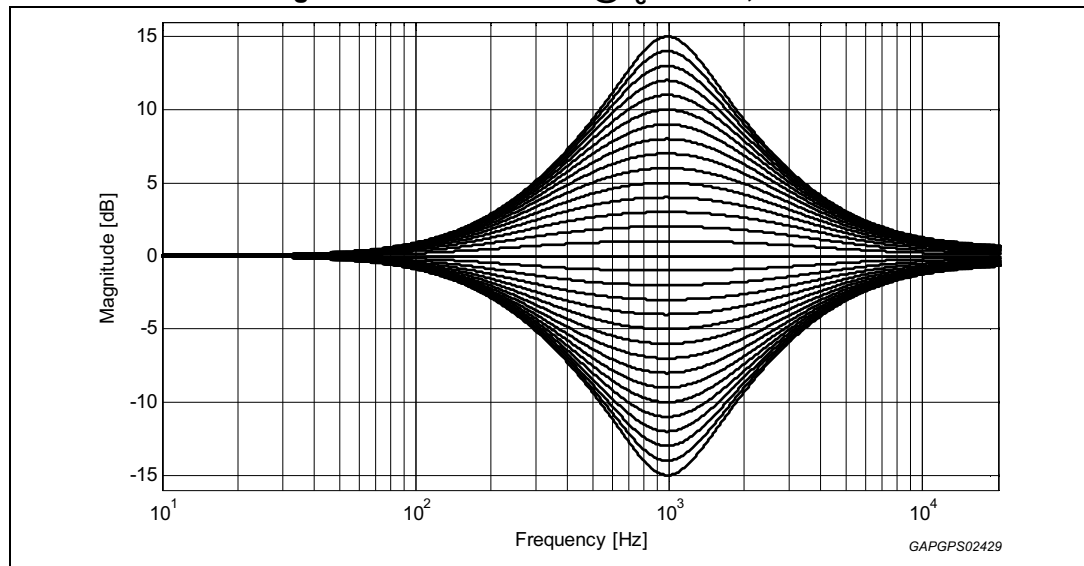
4.6 Middle

There are three parameters programmable in the mid-filter stage.

4.6.1 Middle attenuation

Figure 12 shows the attenuation as a function of frequency at a center frequency of 1 kHz.

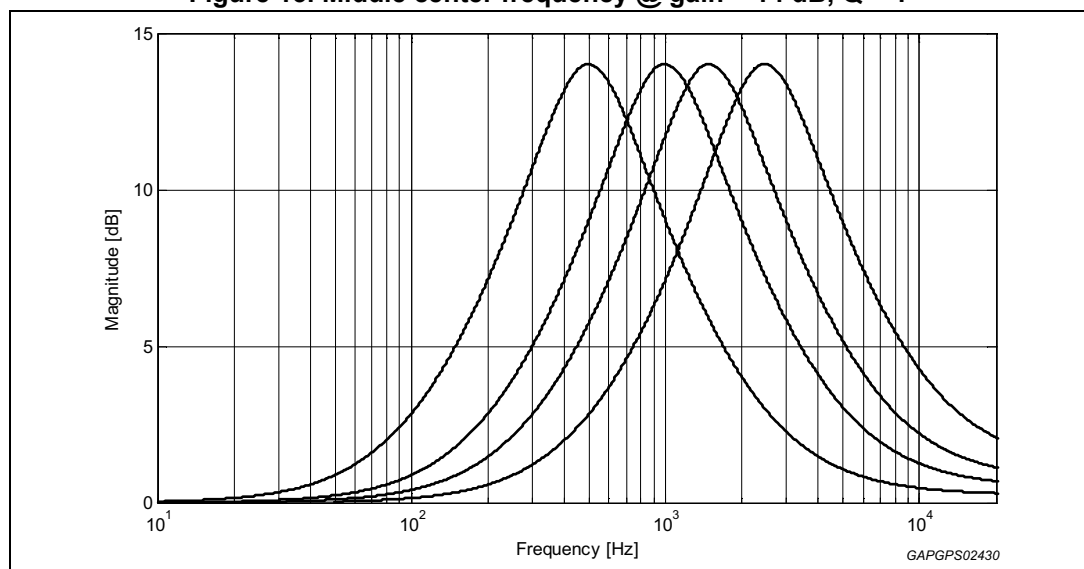
Figure 12. Middle control @ $f_c = 1$ kHz, $Q = 1$



4.6.2 Middle center frequency

Figure 13 shows the four possible center frequencies 500 Hz, 1 kHz, 1.5 kHz and 2.5 kHz.

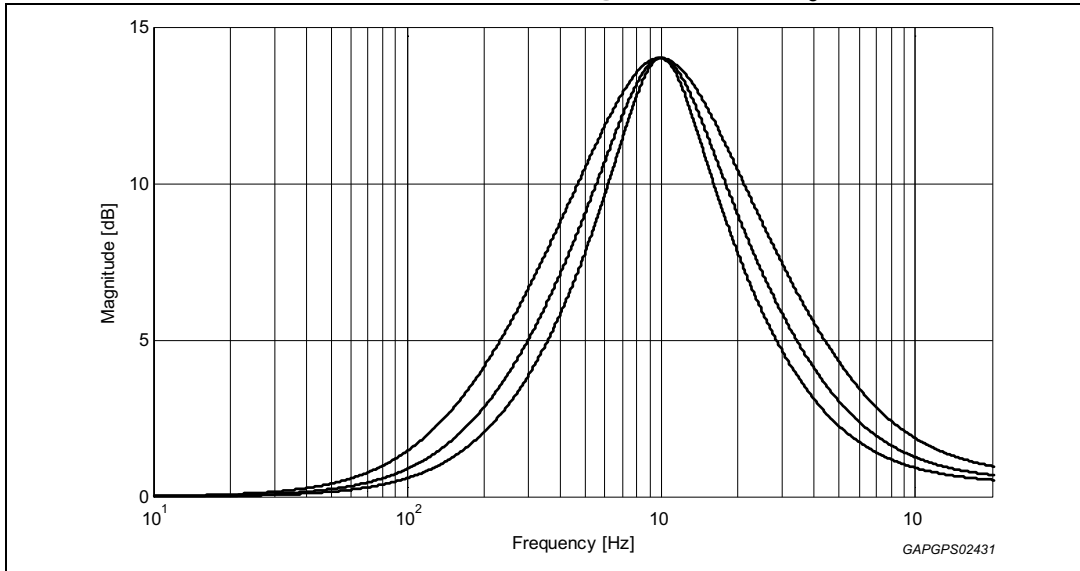
Figure 13. Middle center frequency @ gain = 14 dB, $Q = 1$



4.6.3 Quality factors

Figure 14 shows the two possible quality factors 1 and 2

Figure 14. Middle quality factors @ gain = 14 dB, $f_c = 1$ kHz



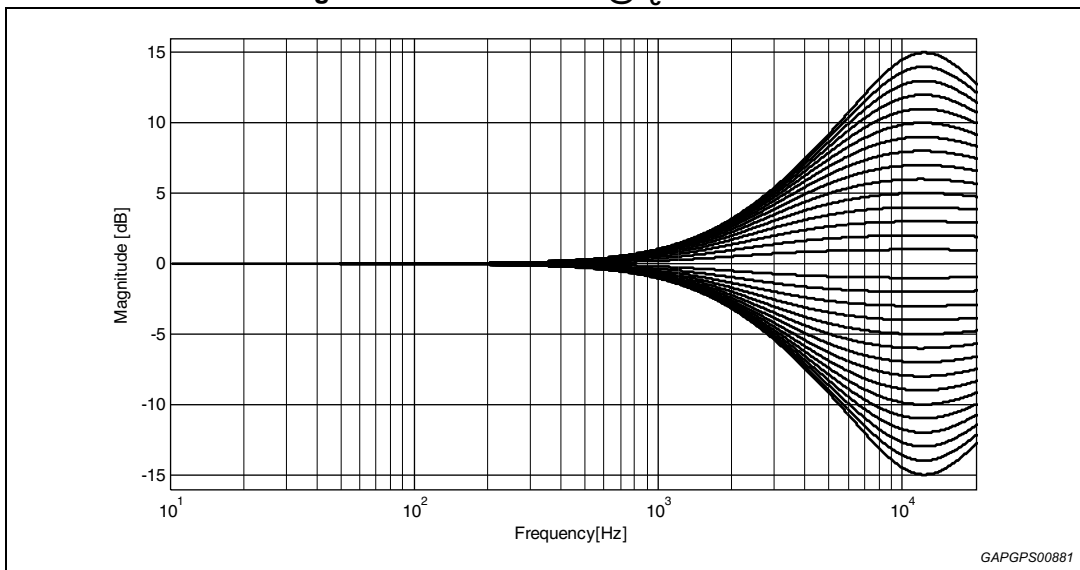
4.7 Treble

There are two parameters programmable in the treble stage.

4.7.1 Treble attenuation

Figure 15 shows the attenuation as a function of frequency at a center frequency of 17.5 kHz.

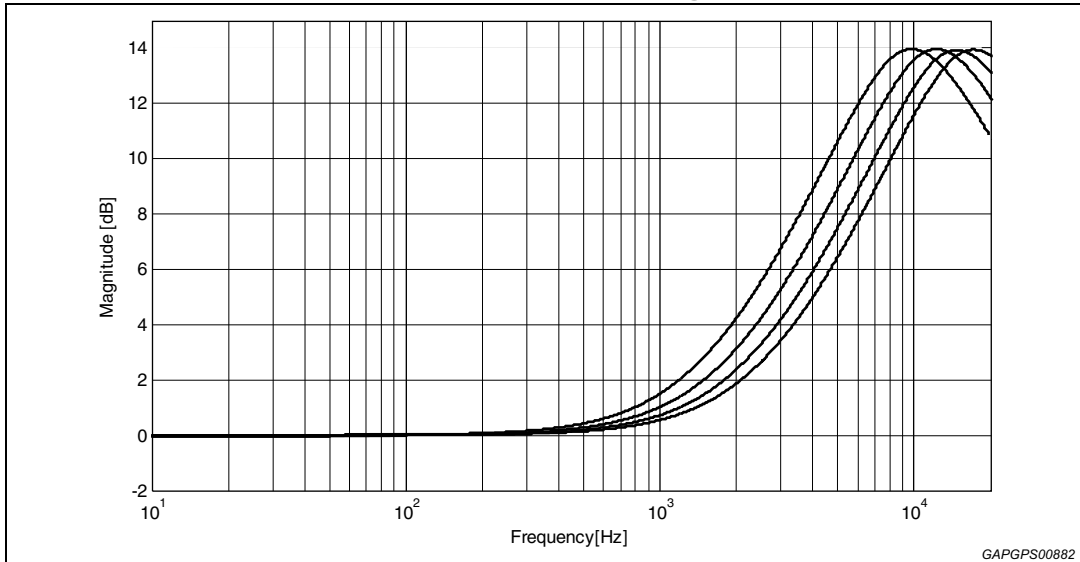
Figure 15. Treble control @ $f_c = 17.5$ kHz



4.7.2 Center frequency

Figure 16 shows the four possible center frequencies 10k, 12.5k, 15k and 17.5 kHz.

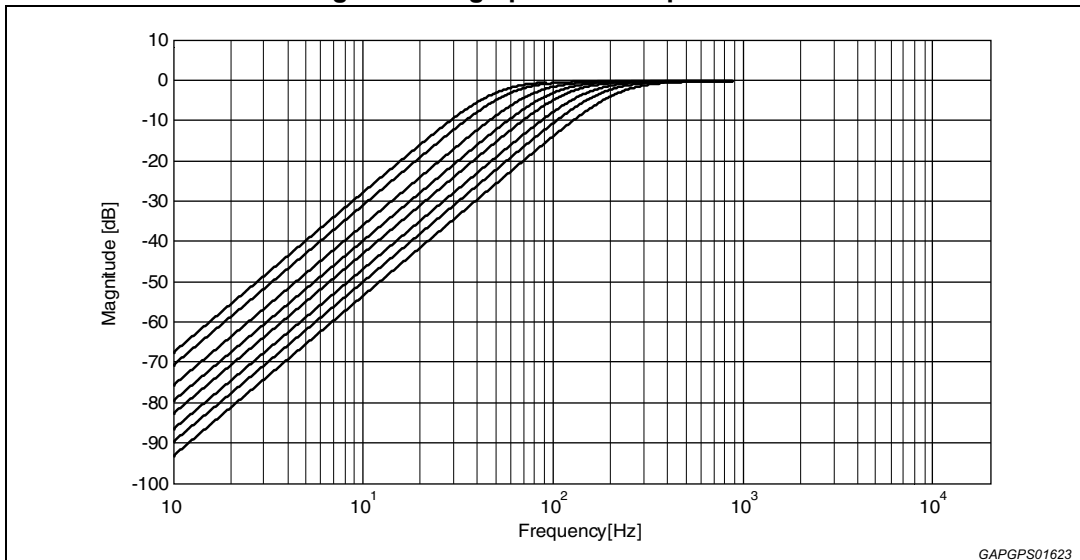
Figure 16. Treble center frequencies @ gain = 14 dB



4.8 High pass filter

The high pass filter has 2 order filter characteristics with programmable cut-off frequency (50/60/80/100/120/150/180/220 Hz)

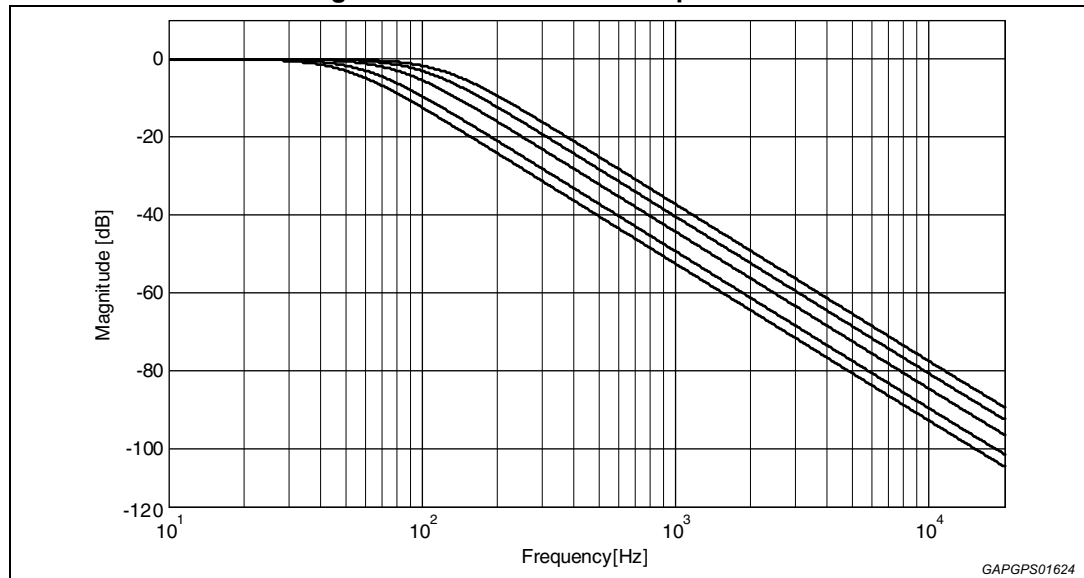
Figure 17. High pass cut frequencies



4.9 Low pass filter

The subwoofer low pass filter has Butterworth characteristics with programmable cut-off frequency (50/60/80/100/120 Hz). The output phase can be selected between 0 deg and 180 deg. The input of subwoofer takes signal from bass filter output or output of input MUX.

Figure 18. Subwoofer cut frequencies

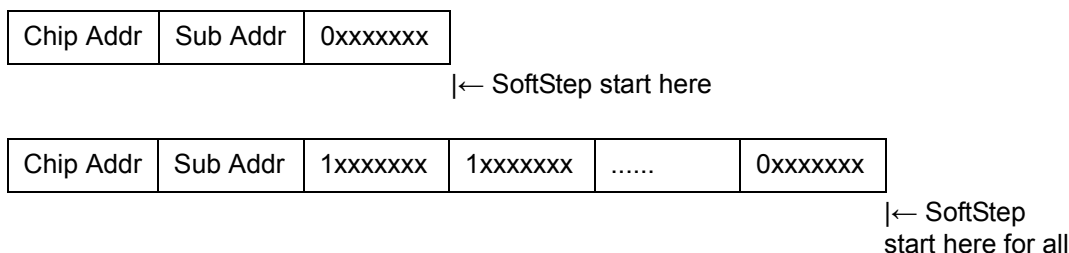


4.10 SoftStep

In this device, the SoftStep function is available for volume, speaker, loudness, treble, middle and bass block. With the SoftStep function, the audible noise of DC offset or the sudden change of signal can be avoided when adjusting the gain setting of the block.

For each block, the SoftStep function is controlled by SoftStep on/off control bit in the control table. The SoftStep transient time selection (7.5 ms or 15 ms) is common for all blocks and it is controlled by SoftStep time control bit. The SoftStep operation of all blocks has a common centralized control. In this case, a new SoftStep operation will not be started before the completion of the previous SoftStep.

There are two different modes to activate the SoftStep operation. The SoftStep operation can be started right after I²C data sending, or the SoftStep can be activated in parallel after data sending of several different blocks. The two modes are controlled by the 'act bit' (it is normally bit7 of the byte.) of each byte. When act bit is '0', which means action, the SoftStep is activated right after the date byte is sent. When the act bit is '1', which means wait, the block goes to wait for SoftStep status. In this case, the block will wait for some other block to activate the operation. The SoftStep operation of all blocks in wait status will be done together with the block which activates the SoftStep. With this mode, all specific blocks can do the SoftStep in parallel. This avoids waiting when the SoftStep is operated one by one. Please note that if a block is set to 'gain1' with act bit = 1, later this block is set to 'gain2' with act bit = 0, in this case the block will do a SoftStep from the currently set gain to 'gain2' but not from the currently set gain to 'gain1' then to 'gain2'.



4.11 DC Offset Detector

Using the DC offset detection circuit (*Figure 19*) an offset voltage difference between the audio power amplifier and the TDA7715LV's Front and Rear outputs can be detected, preventing serious damage to the loudspeakers. The circuit compares whether the signal crosses the zero level inside the audio power at the same time as in the speaker cell. The output of the zero-window-comparator of the power amplifier must be connected with the WinIn-input of the TDA7715LV. The WinIn-input has a 50 kΩ internal pull-up resistor connected to 3.3 V. It is recommended to drive this pin with open-collector outputs or equivalent.

To compensate for errors at low frequencies the WinTCL/R-pin is implemented, with external capacitors introducing the same delay RC-constant = 22.5kΩ * C_{ext} as the AC-coupling introduced between the TDA7715LV and the power amplifier. For the zero window comparators, the time constant for spike rejection as well as the threshold are programmable.

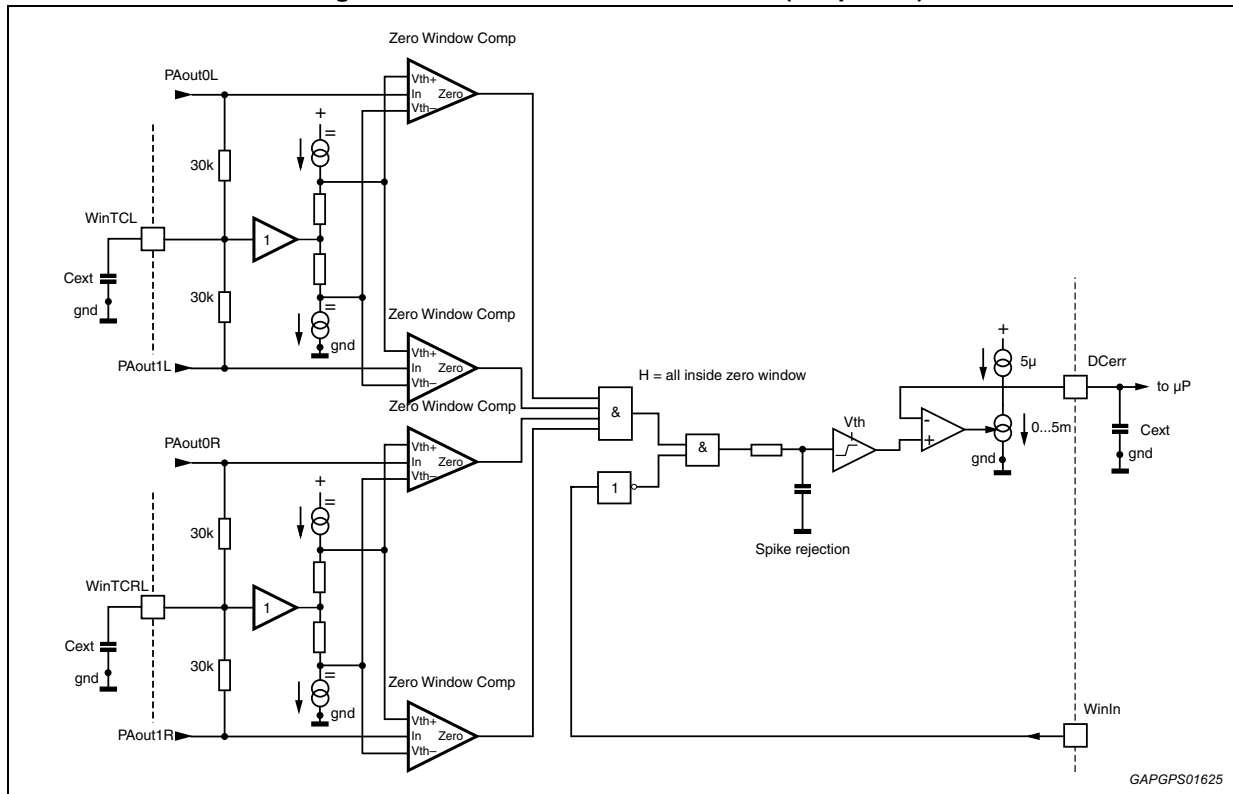
See *Electrical characteristics on page 10*.

A low-active DC-offset error signal appears at the DCErr output if the next conditions are both true:

- a) Front and rear outputs are inside zero crossing windows.
- b) The Input voltage Vwinin is logic low whenever at least one output of the power amplifier is outside the zero crossing windows.

After power-on, the external attached capacitor is rapidly charged (fast-charge) to overcome a false indication. For normal operation these switches need to be released by any programming of byte_0. After that, the "fast-charge" switches can be turned on/off by setting "fast charge = on/off".

Figure 19. DC offset detection circuit (simplified)



4.12 Output stage

The output-section (*Figure 20*) incorporates three independent stereo signal paths, where each can connect to three AC-coupled, single-ended inputs and to some dedicated signals originating from the input-section and/or main-signal-path. The input-impedance at each AC coupled input is 100 kΩ.

Signal path 0 and 1 (front and rear) may optionally enter high-pass filters whereas signal path 2 (other) can be low-pass filtered for subwoofer applications. Anti-radiation filters are integrated for all signal paths. SoftMute stages and a SoftStep volume, that offer fast and click-less muting and/or volume changing follow all three filters.

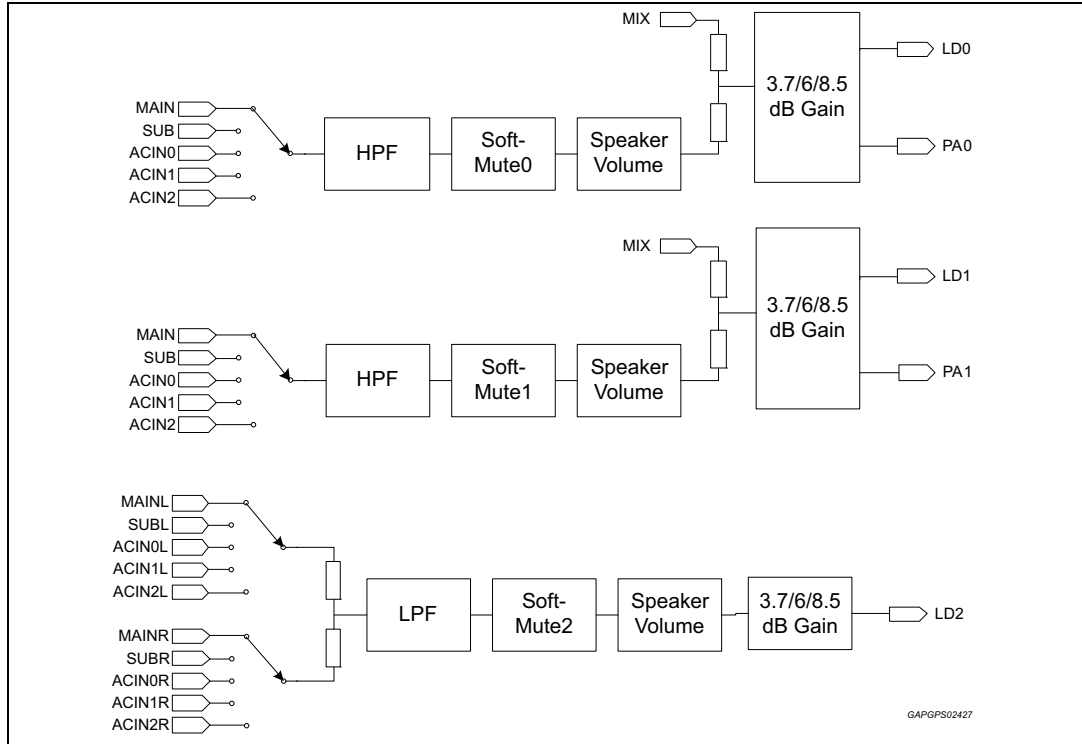
Five stereo pairs of output buffers finally complete the Output-section: Signal-path 2 exclusively feeds a line driver output which is required by external (remote) power amplifiers. The signalpaths 0 & 1 feature both, a line driver output and a dedicated internal (on board) power amplifier output.

The output gain of line-driver is configurable to fit different applications. A specific pin (DCSEL) is used to make it possible to set correct output setting during power-on of the device. In this case it will avoid big DC jump of speaker output when set it later in application control software. The configuration is made by connecting this pin to ground (AC Gain = 6 dB, DC level = 3 V) or leaving it open (AC Gain = 8.5 dB, DC level = 4 V). The output gain is able to be changed after power-on by DCSEL pin (high or low) with pin influence for

output DC level select = PIN, or by I²C bus (Output DC level) with pin influence for output DC level select = I²C. There are 3 options of DC level and AC gain for different applications:

- a) Typical Vcc = 6.0 V: Byte_15 D7D1 = 00, DC level = 3.0 V, AC gain = 6 dB
- b) Typical Vcc = 8.0 V: Byte_15 D7D1 = 01, DC level = 4.0 V, AC gain = 8.5 dB
- c) Typical Vcc = 5.0 V: Byte_15 D7D1 = 1x, DC level = 2.5 V, AC gain = 3.7 dB

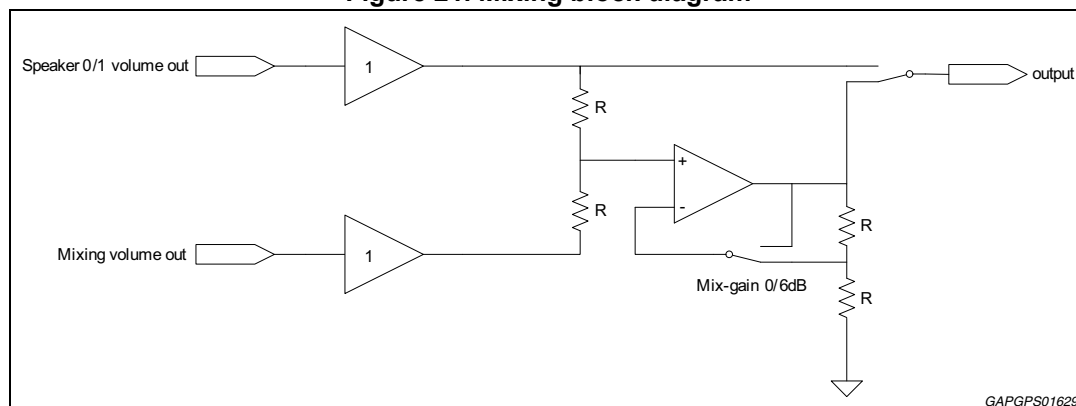
Figure 20. Output-section signal flow



4.13 Mixing

In this device, a very flexible mixing function ([Figure 21](#)) is available to meet all kind of applications. The mixing input is selected by a mixing-multiplexer which is described in [Section 4.1](#). After mixing multiplexer and mixing volume, the mixing signal is mixed with speaker0 or speaker1 volume output. The following 0/6 dB mixing gain offers 2 kind of mixing option, -6 dB/-6 dB mixing or 0 dB/0 dB mixing. The mixing and un-mixing are executed softly.

Figure 21. Mixing block diagram



4.14 Power supply variation

To meet the requirement of automatic stop of car engine at traffic lights, in order to reduce emission of polluting substances TDA7715LV allows a continuous operation when battery falls down. When power supply is 4.5 V it is still fully operational, only the maximum output signal level is reduced accordingly to the available voltage supply.

For electrical characteristics see [Section 3.3 on page 10](#).

4.15 Testing

In the test mode, which can be activated by setting bit D7 of the I²C subaddress byte and bit D0 of the TEST I byte, several internal signals are available at TESTOUT pin.

External clock can be applied to SMUTEMAIN pin by setting bit D2 of the TEST II byte.

To avoid entering test mode, the following setting is recommended to program the device:

- a) Byte_27 = 0xFE
- b) Byte_28 = 0xDE
- c) Byte_29 = 0xFE
- d) Byte_30 = 0xFE
- e) Byte_31 = 0xFE

4.16 Application note

Figure 22. Application schematic

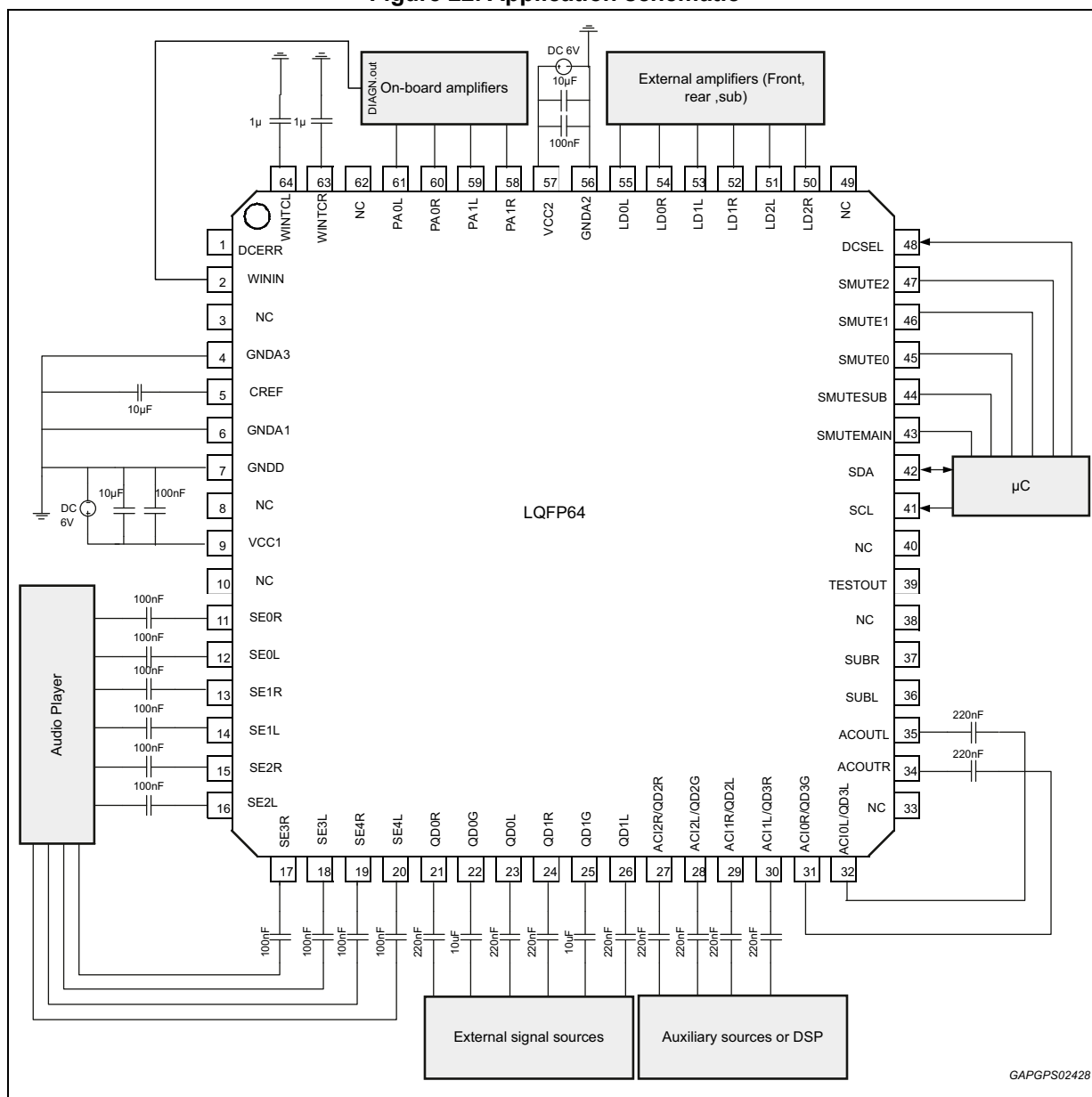


Figure 22 shows a proposal for a typical application. However, the figure only represents one possible interconnection scheme with other devices (the shaded blocks could represent a complex digital sound reproducing/processing system). All capacitor values are suggestions for their size still being dependant on girdling impedance. This is specially true for capacitors located at the WinTC-pins as it can be read in Section 4.11.

In case the DC detector function is not assessed in the application it is recommended to short both the WinTC pins 63 and 64 to device-ground.

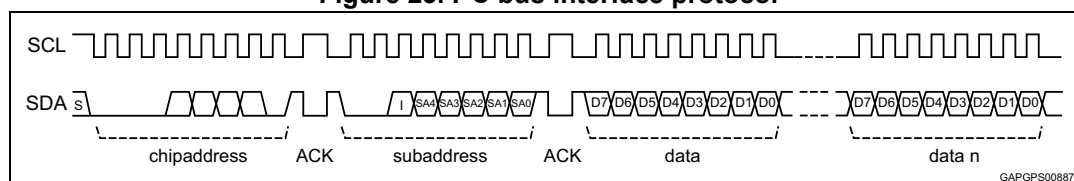
5 I²C bus specification

5.1 Interface protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 400kbits/s
- 3.3 V logic compatible

Figure 23. I²C bus interface protocol



S = Start

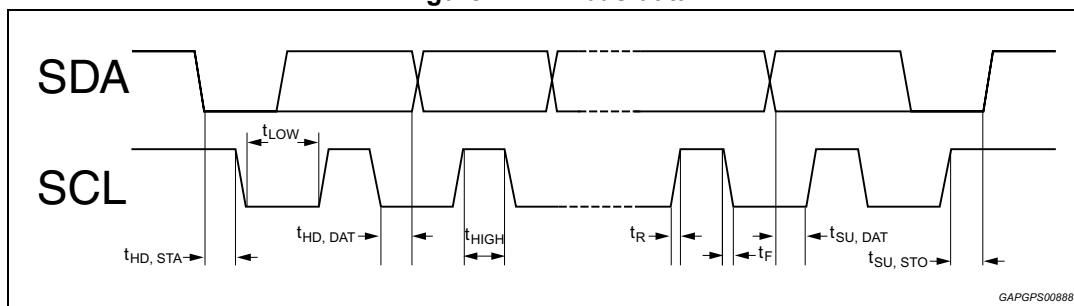
ACK = Acknowledge

5.2 I²C bus electrical characteristics

Table 6. I²C bus electrical characteristics

Symbol	Parameter	Min	Max	Unit
f _{SCL}	SCL clock frequency	-	400	kHz
V _{IH}	High level input voltage	2.4	-	V
V _{IL}	Low level input voltage	-	0.8	V
t _{HD,STA}	Hold time for START	0.6	-	μs
t _{SU,STO}	Setup time for STOP	0.6	-	μs
t _{LOW}	Low period for SCL clock	1.3	-	μs
t _{HIGH}	High period for SCL clock	0.6	-	μs
t _F	Fall time for SCL/SDA	-	300	ns
t _R	Rise time for SCL/SDA	-	300	ns
t _{HD,DAT}	Data hold time	0	-	ns
t _{SU,DAT}	Data setup time	100	-	ns

Figure 24. I²C bus data



5.2.1 Receive mode

S	1	0	0	0	1	0	0	R/W	ACK	TS	X	AI	A4	A3	A2	A1	A0	ACK	DATA	ACK	P
---	---	---	---	---	---	---	---	-----	-----	----	---	----	----	----	----	----	----	-----	------	-----	---

- S = Start
- R/W = "0" -> Receive mode (Chip can be programmed by μ P)
- "1" -> Transmission mode (Data could be received by μ P)
- ACK = Acknowledge
- P = Stop
- TS = Testing mode
- AI = Auto increment

5.2.2 Transmission mode

S	1	0	0	0	1	0	0	R/W	ACK	X	X	BZ	SMM	SMS	SM2	SM1	SM0	ACK	P
---	---	---	---	---	---	---	---	-----	-----	---	---	----	-----	-----	-----	-----	-----	-----	---

- BZ = SoftStep busy ('0' = Busy)
- SMM = SoftMute activated for main channel ('1' = SoftMuted)
- SMS = SoftMute activated for sub channel ('1' = SoftMuted)
- SM2 = SoftMute activated for speaker2 ('1' = SoftMuted)
- SM1 = SoftMute activated for speaker1 ('1' = SoftMuted)
- SM0 = SoftMute activated for speaker0 ('1' = SoftMuted)
- X = Not used

The transmitted data is automatically updated after each ACK. Transmission can be repeated without new chip address.

5.2.3 Reset condition

A power-on-reset is invoked if the supply voltage is below than 3.5 V. After that the registers are initialized to the default data written in the following tables.

Table 7. Subaddress (receive mode)

MSB								LSB	Function
I2	I1	I0	A4	A3	A2	A1	A0		
0	-	-	-	-	-	-	-	Testing mode Off	
1	-	-	-	-	-	-	-	On	
-	x	-	-	-	-	-	-	Not used	
-	-	0	-	-	-	-	-	Auto increment mode Off	
-	-	1	-	-	-	-	-	On	
-	-	-	0	0	0	0	0	Main / Sub selector	
-	-	-	0	0	0	0	1	Mix selector / Anti-alias	
-	-	-	0	0	0	1	0	Volume main	
-	-	-	0	0	0	1	1	Volume sub	
-	-	-	0	0	1	0	0	Volume Mix	
-	-	-	0	0	1	0	1	SoftStep	
-	-	-	0	0	1	1	0	SoftMute I	
-	-	-	0	0	1	1	1	SoftMute II / Middle	
-	-	-	0	1	0	0	0	Loudness	
-	-	-	0	1	0	0	1	Treble filter	
-	-	-	0	1	0	1	0	Middle filter	
-	-	-	0	1	0	1	1	Bass filter	
-	-	-	0	1	1	0	0	Bass / Low pass filter	
-	-	-	0	1	1	0	1	High pass filter	
-	-	-	0	1	1	1	0	Speaker0/1 source selector	
-	-	-	0	1	1	1	1	Output gain / Speaker2 source selector / Middle	
-	-	-	1	0	0	0	0	Speaker0L attenuation	
-	-	-	1	0	0	0	1	Speaker0R attenuation	
-	-	-	1	0	0	1	0	Speaker1L attenuation	
-	-	-	1	0	0	1	1	Speaker1R attenuation	
-	-	-	1	0	1	0	0	Speaker2L attenuation	
-	-	-	1	0	1	0	1	Speaker2R attenuation	
-	-	-	1	0	1	1	0	Not used	
-	-	-	1	0	1	1	1	Not used	
-	-	-	1	1	0	0	0	Mix	
-	-	-	1	1	0	0	1	DC-detector	
-	-	-	1	1	0	1	0	Not used	
-	-	-	1	1	0	1	1	Test I	
-	-	-	1	1	1	0	0	Test II	
-	-	-	1	1	1	0	1	Test III	
-	-	-	1	1	1	1	0	Reserved	
-	-	-	1	1	1	1	1	Reserved	

5.3 Data byte specification

Table 8. Main / sub selector (0)

MSB				LSB				Function				
D7	D6	D5	D4	D3	D2	D1	D0					
-	-	-	-	0	0	0	0	Main Source Selector SE0				
				0	0	0	1	SE1				
				0	0	1	0	SE2				
				0	0	1	1	SE3				
				0	1	0	0	SE4				
				0	1	0	1	QD0				
				0	1	1	0	QD1				
				0	1	1	1	QD2				
				1	0	0	0	QD3				
				1	0	0	1	MUTE				
				1	0	1	0	MUTE				
				1	0	1	1	MUTE				
				1	1	1	x	x	MUTE			
0	0	0	0					Sub Source Selector SE0				
								0	0	0	1	SE1
								0	0	1	0	SE2
								0	0	1	1	SE3
								0	1	0	0	SE4
								0	1	0	1	QD0
								0	1	1	0	QD1
								0	1	1	1	QD2
								1	0	0	0	QD3
								1	0	0	1	MUTE
								1	0	1	0	MUTE
								1	0	1	1	MUTE
								1	1	x	x	MUTE

Table 9. Mix selector / anti-alias / fast charge (1)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	0	0	0	0	Mix Source Selector SE0
				0	0	0	1	SE1
				0	0	1	0	SE2
				0	0	1	1	SE3
				0	1	0	0	SE4
				0	1	0	1	QD0
				0	1	1	0	QD1
				0	1	1	1	QD2
				1	0	0	0	QD3
				1	0	0	1	MUTE
				1	0	1	0	MUTE
				1	0	1	1	MUTE
				1	1	x	x	<u>MUTE</u>
-	-	-	0	-	-	-	-	Mix Left channel <u>Left</u>
			1					<u>Right</u>
-	-	0	-	-	-	-	-	Mix Right channel <u>Left</u>
		1						<u>Right</u>
-	0	-	-	-	-	-	-	Anti-alias filter <u>On</u>
	1							<u>Off</u>
0	-	-	-	-	-	-	-	AC-Coupling / QD selection AC
1								<u>QD</u>

Table 10. Volume main/sub/mix (2-4)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	0	0	0	0	0	0	Gain/Attenuation +0dB
		0	0	0	0	0	0	+1dB
		:	:	:	:	:	:	:
		0	0	1	1	1	1	+15dB
		0	1	0	0	0	0	+16dB
		:	:	:	:	:	:	:
		0	1	0	1	1	1	+23dB
		0	1	1	0	0	0	Not used
		:	:	:	:	:	:	:
		0	1	1	1	1	1	Not used
		1	0	0	0	0	0	-0dB
		:	:	:	:	:	:	:
		1	0	1	1	1	1	-15dB
		:	:	:	:	:	:	:
		1	1	0	1	1	1	<u>-23dB</u>
		:	:	:	:	:	:	:
1	1	1	1	1	1	Not used		
-	0 1	-	-	-	-	-	-	Volume SoftStep On <u>Off</u>
0 1	-	-	-	-	-	-	-	SoftStep action act <u>wait</u>

Table 11. SoftStep (5)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	Loudness SoftStep On <u>Off</u>
-	-	-	-	-	-	0 1	-	Treble SoftStep On <u>Off</u>
-	-	-	-	-	0 1	-	-	Middle SoftStep On <u>Off</u>
-	-	-	-	0 1	-	-	-	Bass SoftStep On <u>Off</u>
-	-	-	0 1	-	-	-	-	Speaker0/Mixing SoftStep ⁽¹⁾ On <u>Off</u>
-	-	0 1	-	-	-	-	-	Speaker1 SoftStep On <u>Off</u>
-	0 1	-	-	-	-	-	-	Speaker2 SoftStep On <u>Off</u>
0 1	-	-	-	-	-	-	-	SoftStep time 7.5ms <u>15ms</u>

1. Mixing SoftStep need to be turned on/off with speaker0 SoftStep.

Table 12. SoftMute I (6)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	x	x	x	x	Not used
-	-	0 0 1 1	0 1 0 1	-	-	-	-	SoftMute time (Main/SUB) 0.5ms 4ms 8ms 16ms
0 0 1 1	0 1 0 1	-	-	-	-	-	-	SoftMute time (Speaker0/1/2) 4ms 8ms 32ms 64ms

Table 13. SoftMute II / middle (7)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	Pin influence for mute <u>Pin and IIC</u> IIC
-	-	-	-	-	-	x	-	Not used
-	-	-	-	-	0 1	-	-	SoftMute main On <u>Off</u>
-	-	-	-	0 1	-	-	-	SoftMute sub On <u>Off</u>
-	-	-	0 1	-	-	-	-	SoftMute Speaker0 On <u>Off</u>
-	-	0 1	-	-	-	-	-	SoftMute Speaker1 On <u>Off</u>
-	0 1	-	-	-	-	-	-	SoftMute Speaker2 On <u>Off</u>
0 1	-	-	-	-	-	-	-	Middle quality factor 1.0 <u>2.0</u>

Table 14. Loudness (8)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	0	0	0	0	Attenuation 0dB
				0	0	0	1	-1dB
				:	:	:	:	:
				1	1	1	0	-14dB
				1	1	1	1	-15dB
-	-	0	0	-	-	-	-	Center frequency Flat
		0	1					400Hz
		1	0					800Hz
		1	1					2400Hz
-	0	-	-	-	-	-	-	High boost On
	1							Off
0	-	-	-	-	-	-	-	SoftStep action act
1								wait

Table 15. Treble filter (9)

MSB				LSB				Function		
D7	D6	D5	D4	D3	D2	D1	D0			
-	-	-	0	1	1	1	1	1	Gain/Attenuation +15dB	
			:	:	:	:	:	:	:	
			0	1	0	1	0	1	0	+10dB
			:	:	:	:	:	:	:	:
			0	0	0	0	0	0	1	+1dB
			0	0	0	0	0	0	0	0dB
			1	0	0	0	0	0	0	<u>0dB</u>
			1	0	0	0	0	0	1	-1dB
			:	:	:	:	:	:	:	:
			1	1	0	1	0	1	0	-10dB
								:		
								-15dB		
-	0	0	-	-	-	-	-	Treble center frequency 10.0kHz		
	0	1						12.5kHz		
	1	0						15.0kHz		
	1	1						17.5kHz		
0	-	-	-	-	-	-	-	SoftStep action act		
1								wait		

Table 16. Middle filter (10)

MSB				LSB				Function	
D7	D6	D5	D4	D3	D2	D1	D0		
-	-	-	0	1	1	1	1	+15dB	
			:	:	:	:	:	:	
			0	1	0	1	0	0	+10dB
			:	:	:	:	:	:	:
			0	0	0	0	0	1	+1dB
			0	0	0	0	0	0	0dB
			1	0	0	0	0	0	<u>0dB</u>
			1	0	0	0	0	1	-1dB
			:	:	:	:	:	:	:
			1	1	0	1	0	0	-10dB
:	:	:	:	:	:	:	:		
1	1	1	1	1	1	1	-15dB		
-	0	0	-	-	-	-	-	Middle center frequency	
	0	1						500Hz	
	1	0						1000Hz	
	1	1						1500Hz	
								2000Hz	
0 1	-	-	-	-	-	-	-	SoftStep action	
								act	
								<u>wait</u>	

Table 17. Bass filter (11)

MSB				LSB				Function		
D7	D6	D5	D4	D3	D2	D1	D0			
-	-	-	0	1	1	1	1	+15dB		
			0	1	1	1	0	0	+14dB	
			:	:	:	:	:	:	:	
			0	0	0	0	0	1	+1dB	
			0	0	0	0	0	0	0dB	
			1	0	0	0	0	0	<u>0dB</u>	
			1	0	0	0	0	1	-1dB	
			:	:	:	:	:	:	:	:
			1	1	1	1	1	0	-14dB	
			1	1	1	1	1	1	1	-15dB
-	0	0	-	-	-	-	-	Bass quality factor		
	0	1						1.0		
	1	0						1.25		
	1	1						1.5		
								<u>2.0</u>		
0 1	-	-	-	-	-	-	-	SoftStep action		
								act		
								<u>wait</u>		

Table 18. Bass / low pass filter (12)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	0	0	0	Bass center frequency 60Hz
					0	0	1	70Hz
					0	1	0	80Hz
					0	1	1	100Hz
					1	0	0	110Hz
					1	0	1	120Hz
					1	1	0	<u>130Hz</u>
					1	1	1	150Hz
-	-	-	-	0	-	-	-	Bass DC mode On
				1				Off
-	0	0	0	-	-	-	-	Low pass filter corner frequency 50Hz
	0	0	1					60Hz
	0	1	0					80Hz
	0	1	1					100Hz
	1	x	x					<u>120Hz</u>
0 1	-	-	-	-	-	-	-	Low pass filter output phase 180 deg
								0 deg

Table 19. High pass filter (13)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	HPF output phase Speaker0 180 deg <u>0 deg</u>
-	-	-	-	0 0 0 0 1 1 1 1	0 0 1 0 0 1 1	0 1 0 1 0 1	-	HPF corner frequency Speaker0 50Hz 60Hz 80Hz 100Hz 120Hz 150Hz 180Hz <u>220Hz</u>
-	-	-	0 1	-	-	-	-	HPF phase Speaker1 180 deg <u>0 deg</u>
0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	-	-	-	-	-	HPF corner frequency Speaker1 50Hz 60Hz 80Hz 100Hz 120Hz 150Hz 180Hz <u>220Hz</u>

Table 20. Speaker0/1 source selector (14)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	0 0 0 0 1	0 0 1 1 x	0 1 0 1 x	Speaker0 source selector acin0 acin1 acin2 sub <u>main</u>
-	-	-	-	0 1	-	-	-	High pass filter bypass Speaker0 Bypass <u>High pass filter</u>
-	0 0 0 0 1	0 0 1 1 x	0 1 0 1 x	-	-	-	-	Speaker1 source selector acin0 acin1 acin2 sub <u>main</u>
0 1	-	-	-	-	-	-	-	High pass filter bypass Speaker1 Bypass <u>High pass filter</u>

Table 21. Output gain / speaker2 source selector (15)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	Pin Influence for output DC level select <u>Pin</u> IIC
0 0 1	-	-	-	-	-	0 1 x	-	Output DC level 3.0 V (AC Gain = 6.0 dB) <u>4.0 V (AC Gain = 8.5 dB)</u> 2.5 V (AC Gain = 3.7 dB)
-	-	-	0 0 0 0 1	0 0 1 1 x	0 0 1 1 x	-	-	Speaker2 source selector acin0 acin1 acin2 sub <u>main</u>
-	0 0 1	0 1 x	-	-	-	-	-	Low pass filter bypass Low pass filter Mono-sum bypass <u>Stereo bypass</u>

Table 22. Speaker attenuation (0L/0R/1L/1R/2L/2R) (16-21)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	0	0	0	0	0	0	0	Gain/Attenuation +0dB
	0	0	0	0	0	0	1	+1dB
	:	:	:	:	:	:	:	:
	0	0	0	1	1	1	1	+15dB
	0	0	1	0	0	0	0	+16dB
	:	:	:	:	:	:	:	:
	0	0	1	0	1	1	1	+23dB
	0	0	1	1	0	0	0	Not used
	:	:	:	:	:	:	:	:
	0	0	1	1	1	1	1	Not used
	0	1	0	0	0	0	0	-0dB
	:	:	:	:	:	:	:	:
	0	1	0	1	1	1	1	-15dB
	:	:	:	:	:	:	:	:
	0	1	1	0	1	1	1	-23dB
	:	:	:	:	:	:	:	:
	1	0	0	0	0	0	0	-32dB
	:	:	:	:	:	:	:	:
	1	1	0	0	0	0	0	-64dB
	:	:	:	:	:	:	:	:
1	1	0	1	1	1	1	-79dB	
1	1	1	1	x	x	x	x	<u>mute</u>
0	-	-	-	-	-	-	-	SoftStep action act
1	-	-	-	-	-	-	-	<u>wait</u>

Note: Not used (22-23).

Table 23. Mix (24)

MSB							LSB		Function
D7	D6	D5	D4	D3	D2	D1	D0		
-	-	-	-	-	-	-	0 1	IIC mix speaker0 <u>Bypass</u> Mix	
-	-	-	-	-	-	0 1	-	Mix gain speaker0 0dB (-6dB/-6dB mix) 6dB (0dB/0dB mix)	
-	-	-	-	-	0 1	-	-	IIC mix speaker1 <u>Bypass</u> Mix	
-	-	-	-	0 1	-	-	-	Mix gain speaker1 0dB (-6dB/-6dB mix) 6dB (0dB/0dB mix)	
-	x	x	x	-	-	-	-	Not used	
0 1	-	-	-	-	-	-	-	SoftStep action act <u>wait</u>	

Table 24. DC-detector (25)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	0 0 1 1	0 1 0 1	Spike rejection time Disable <u>11 μs</u> 22 μs 33 μs
-	-	-	-	0 0 1 1	0 1 0 1	-	-	Zero-comparator Window size ±90mV ±60mV ±45mV <u>±30mV</u>
-	-	-	0 1	-	-	-	-	DC-detector fast charge On <u>Off</u>
x	x	x	-	-	-	-	-	Not used

Note: Not used (26).

Table 25. Test I (27)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	Audio processor testing mode Off On
-	-	-	0 0 0 0 0 0 0 0	0 0 0 1 1 1 1	0 0 1 0 0 1 1	0 1 0 1 0 1 1	-	Test multiplexer ⁽¹⁾ SSCLK SMCLK1 SMCLK2 VDDd_Test (2.52V) LSOUT Clock200k V2V REQ_TEST
-	-	-	1 1 1 1 1 1 1	0 0 0 0 1 1 1	0 0 1 0 0 0 1	0 1 0 1 0 1 1	-	DCO test multiplexer ⁽¹⁾ SSOUT Zero Left Zero Right SDCLK Vthp reference Vthn reference IntZeroErr VDDa_Test (2.52V)
x	x	x	-	-	-	-	-	Not used

1. The control bit needs both I²C test mode on & sub-address test mode on.

Table 26. Test II (28)

MSB				LSB				Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	0 0 1 1	0 1 0 1	Manual set busy signal ⁽¹⁾ Auto Auto <u>Q</u> 1
-	-	-	-	-	-	0 0 1 1	0 1 0 1	Request for clock generator ⁽¹⁾ Allow Allow <u>Stopped</u> Stopped
-	-	-	-	-	0 1	-	-	Clock source ⁽²⁾ External <u>Internal (200kHz)</u>
-	-	-	-	0 1	-	-	-	Oscillator clock ⁽²⁾ 400kHz <u>800kHz</u>
-	-	-	0 1	-	-	-	-	Clock fast mode⁽²⁾ On <u>Off</u>
-	-	0 1	-	-	-	-	-	SoftStep curve ⁽²⁾ <u>S-Curve (soft step time 7.5ms/15ms)</u> Linear Curve (soft step time 5ms/10ms)
x	x	-	-	-	-	-	-	Not used

1. The control bit needs sub-address test mode on.
2. The control bit does not depend on test mode.

Table 27. Test III (29)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
-	-	-	-	-	-	-	0 1	Test architecture ⁽¹⁾ <u>Normal</u> <u>Split</u>
-	-	-	-	-	-	0 1	-	Attenuators gain clock control ⁽²⁾ <u>On</u> <u>Off</u>
-	-	-	-	-	0 1	-	-	Enable clock for speaker volume <u>On</u> <u>Off</u>
-	-	-	-	0 1	-	-	-	Enable clock for volume <u>On</u> <u>Off</u>
-	-	-	0 1	-	-	-	-	Enable clock for treble & bass <u>On</u> <u>Off</u>
-	-	0 1	-	-	-	-	-	Enable clock for loudness & middle <u>On</u> <u>Off</u>
x	x	-	-	-	-	-	-	Not used

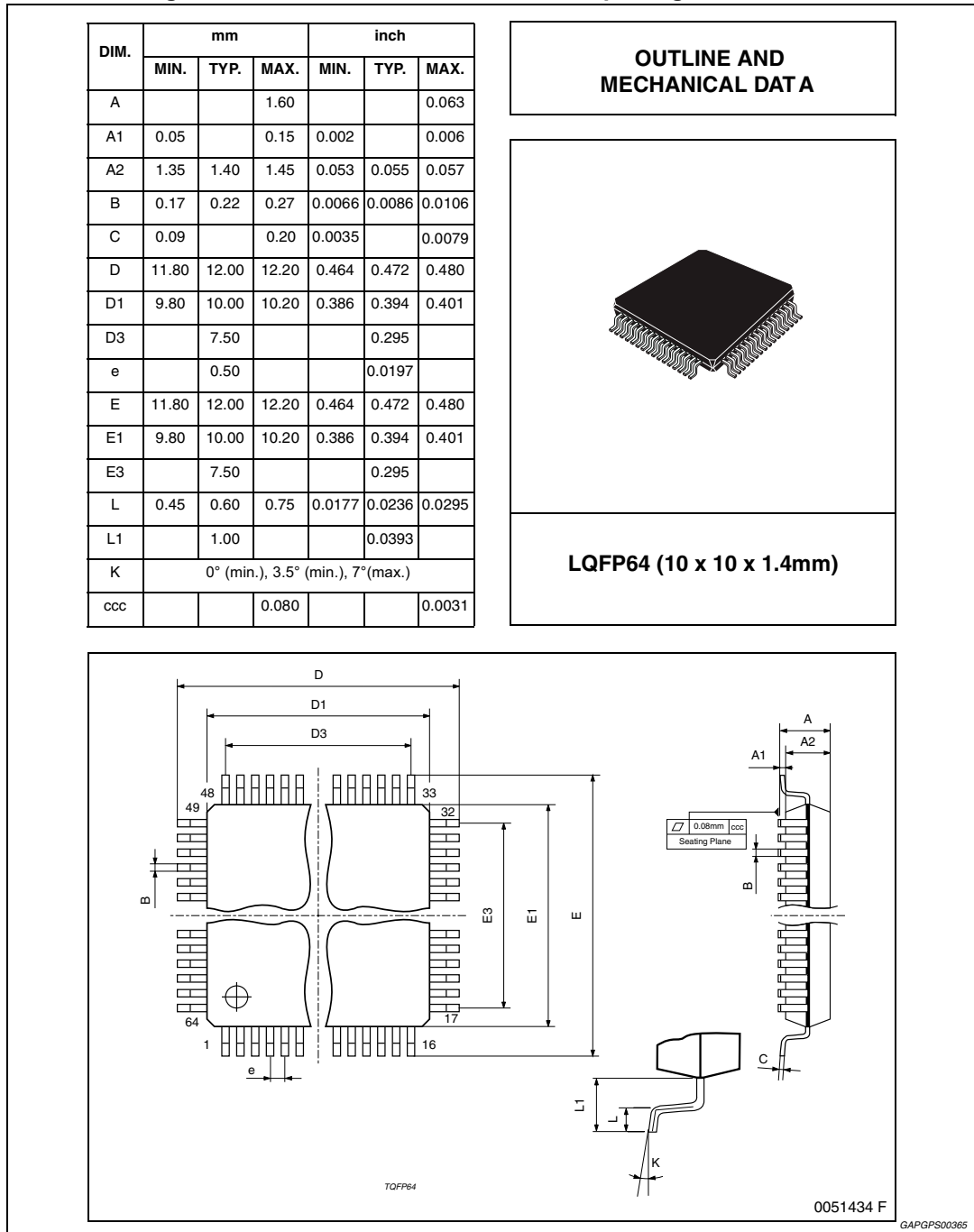
1. The control bit needs sub-address test mode on.
2. The control bit does not depend on test mode.

6 Package information

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Figure 25. LFQP64 mechanical data and package dimensions



7 Revision history

Table 28. Document revision history

Date	Revision	Changes
31-Oct-2013	1	Initial release.

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