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June 2014

FDB9406_F085

N-Channel PowerTrench® MOSFET

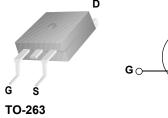
40 V, 110 A, 1.8 mΩ

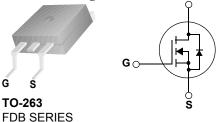
Features

- Typ $R_{DS(on)}$ = 1.31m Ω at V_{GS} = 10V, I_D = 80A
- Typ $Q_{g(tot)}$ = 107nC at V_{GS} = 10V, I_D = 80A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems





For current package drawing, please refer to the Fairchild website at www.fairchildsemi.com/packaging

MOSFET Maximum Ratings T₁ = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units	
V_{DSS}	Drain to Source Voltage		40	V	
V_{GS}	Gate to Source Voltage		±20	V	
	Drain Current - Continuous (V_{GS} =10) (Note 1) T_C = 25°C		110	^	
I _D	Pulsed Drain Current T _C = 25°C		See Figure4	Α	
E _{AS}	Single Pulse Avalanche Energy (Note 2)		174	mJ	
D	Power Dissipation		176	W	
P_D	Derate above 25°C		1.18	W/°C	
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 175	°C	
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.85	°C/W	
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	43	°C/W	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB9406	FDB9406_F085	D2-PAK(TO-263)	330mm	24mm	800 units

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^{\circ}C$, L = 0.045mH, $I_{AS} = 88A$, $V_{DD} = 40V$ during inductor charging and $V_{DD} = 0V$ during time in avalanche. 3: $R_{\theta,JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder
- mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Units

nΑ

Max.

±100

Electrical Characteristics T_J = 25°C unless otherwise noted

Parameter

Gate-to-Source Leakage Current

Off Characteristics							
B _{VDSS}	Drain-to-Source Breakdown Voltage	I _D = 250μA, \	/ _{GS} = 0V	40	-	-	V
1	Drain-to-Source Leakage Current	V _{DS} =40V,	$T_{\rm J} = 25^{\rm o}{\rm C}$	-	-	1	μΑ
Drain-to-Source Leakage Current	$V_{GS} = 0V$	$T_J = 175^{\circ}C(Note 4)$	-	-	1	mA	

 $V_{GS} = \pm 20V$

Test Conditions

Min.

Тур.

On Characteristics

Symbol

 I_{GSS}

V _{GS(th)}	Gate-to-Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		2.0	2.83	4.0	V
R _{DS(on)} Drain-to-Source On Resistance	I _D = 80A,	$T_{\rm J} = 25^{\rm o}{\rm C}$	-	1.31	1.8	$m\Omega$	
R _{DS(on)}	R _{DS(on)} Drain-to-Source On Resistance	V _{GS} = 10V	$T_J = 175^{\circ}C(Note 4)$	-	2.2	2.8	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	V 05V V	V _{DS} = 25V, V _{GS} = 0V, -f = 1MHz		7710	-	pF
C _{oss}	Output Capacitance				2015	-	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1101112			140	-	pF
R_g	Gate Resistance	f = 1MHz	f = 1MHz		2.7	-	Ω
Q _{g(ToT)}	Total Gate Charge at 10V	V _{GS} = 0 to 10V	V _{DD} = 32V	-	107	138	nC
Q _{g(th)}	Threshold Gate Charge	V _{GS} = 0 to 2V	V _{GS} = 0 to 2V I _D = 80A		14	19	nC
Q _{gs}	Gate-to-Source Gate Charge				33	-	nC
Q_{qd}	Gate-to-Drain "Miller" Charge				18	-	nC

Switching Characteristics

t _{on}	Turn-On Time	V_{DD} = 20V, I_{D} = 80A, V_{GS} = 10V, R_{GEN} = 6 Ω	-	-	160	ns
t _{d(on)}	Turn-On Delay		1	32	-	ns
t _r	Rise Time		-	81	-	ns
t _{d(off)}	Turn-Off Delay		-	50	-	ns
t _f	Fall Time		-	23	-	ns
t _{off}	Turn-Off Time		-	-	93	ns

Drain-Source Diode Characteristics

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 80A, V_{GS} = 0V$	-	-	1.25	V
t _{rr}	Reverse-Recovery Time	$I_F = 80A$, $dI_{SD}/dt = 100A/\mu s$,	-	85	110	ns
Q_{rr}	Reverse-Recovery Charge	V _{DD} =32V	-	122	160	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

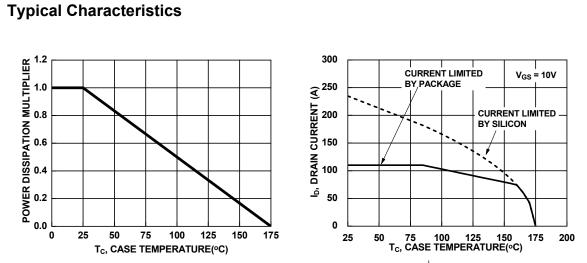
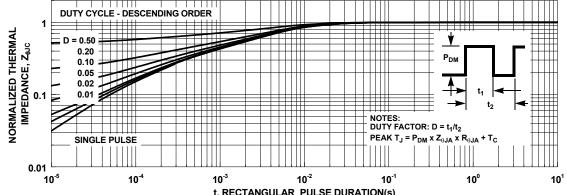


Figure 1. Normalized Power Dissipation vs. Case Temperature

Figure 2. Maximum Continuous Drain Current vs.

Case Temperature



t, RECTANGULAR PULSE DURATION(s)
Figure 3. Normalized Maximum Transient Thermal Impedance

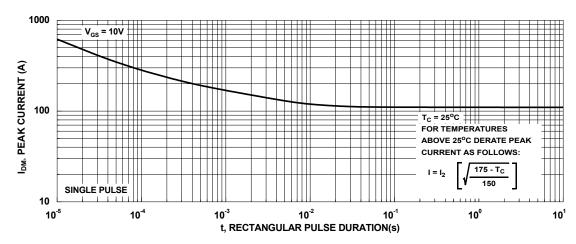


Figure 4. Peak Current Capability

Typical Characteristics

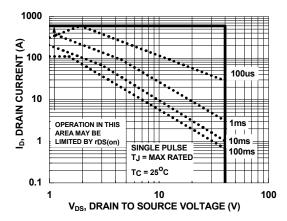
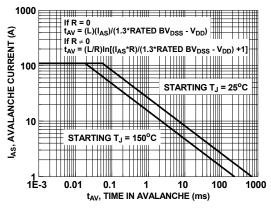


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching

Capability

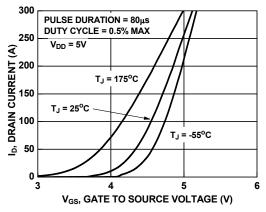


Figure 7. Transfer Characteristics

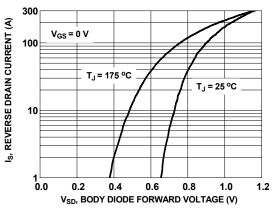


Figure 8. Forward Diode Characteristics

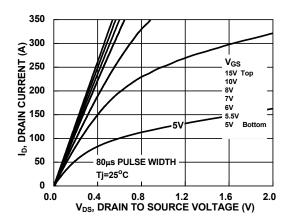


Figure 9. Saturation Characteristics

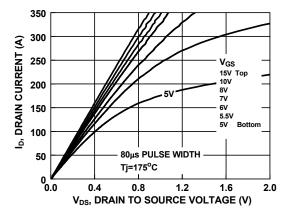


Figure 10. Saturation Characteristics

Typical Characteristics

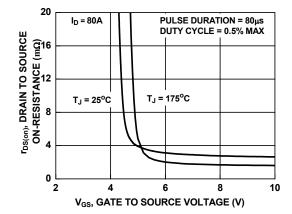


Figure 11. R_{DSON} vs. Gate Voltage

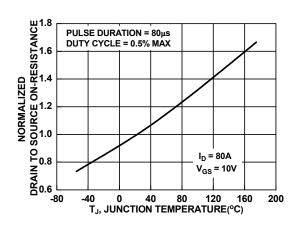


Figure 12. Normalized R_{DSON} vs. Junction Temperature

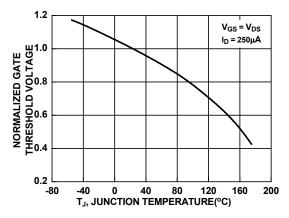


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

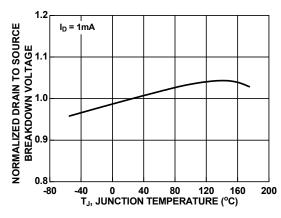


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

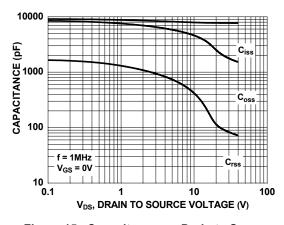


Figure 15. Capacitance vs. Drain to Source Voltage

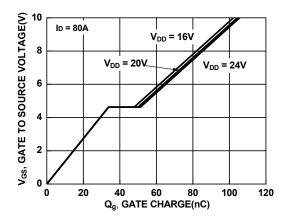


Figure 16. Gate Charge vs. Gate to Source Voltage





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