DATASHEET

Description

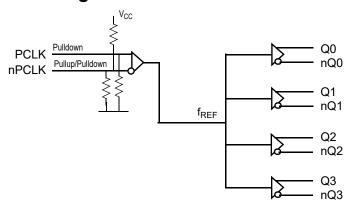
The IDT8SLVP1104I is a high-performance differential LVPECL fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The IDT8SLVP1104I is characterized to operate from a 3.3V or 2.5V power supply.

Guaranteed output-to-output and part-to-part skew characteristics make the IDT8SLVP1104I ideal for those clock distribution applications demanding well-defined performance and repeatability. Four low skew outputs are available. The integrated bias voltage reference enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

Features

- Four low skew, low additive jitter LVPECL differential output pairs
- Differential LVPECL input pair can accept the following differential input levels: LVDS, LVPECL, CML
- Differential PCLKx pairs can also accept single-ended LVCMOS levels. See the Applications section Writing the Differential Input Levels to Accept Single-ended Levels (Figures 1 and 2)
- · Maximum input clock frequency: 2GHz
- LVCMOS interface levels for the control input (input select)
- Output skew: 5ps (typical)
- Propagation delay: 320ps (maximum)
- Low additive phase jitter, RMS; f_{REF} = 156.25MHz, V_{PP} = 1V, 12kHz - 20MHz: 40fs (maximum)
- Maximum device current consumption (I_{EE}): 60mA (maximum)
- Full 3.3V or 2.5V supply voltage
- · Lead-free (RoHS 6) packaging
- -40°C to 85°C ambient operating temperature

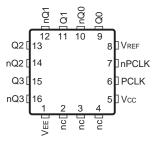
Block Diagram





Pin Assignment

1



IDT8SLVP1104I 16 lead VFQFPN

3.0mm x 3.0mm x 0.925mm package body 1.7mm x 1.7mm Epad Size

NL Package Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Ту	pe	Description
1	V _{EE}	Power		Negative supply pin.
2	nc	Unused		Do not connect.
3	nc	Unused		Do not connect.
4	nc	Unused		Do not connect.
5	V _{CC}	Power		Power supply pin.
6	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock/data input.
7	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock/data input. $V_{CC}/2$ default when left floating.
8	V_{REF}	Output		Bias voltage reference for the PCLK inputs.
9, 10	Q0, nQ0	Output		Differential output pair 0. LVPECL interface levels.
11, 12	Q1, nQ1	Output		Differential output pair 1. LVPECL interface levels.
13, 14	Q2, nQ2	Output		Differential output pair 2. LVPECL interface levels.
15, 16	Q3, nQ3	Output		Differential output pair 3. LVPECL interface levels.

NOTE: Pulldown and Pullup refers to an internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			2		pF
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating	
Supply Voltage, V _{CC}	4.6V	
Inputs, V _I	-0.5V to V _{CC} + 0.5V	
Outputs, I _O (LVPECL)		
Continuous Current	50mA	
Surge Current	100mA	
Input Sink/Source, I _{REF}	±2mA	
Maximum Junction Temperature, T _{J,MAX}	125°C	
Storage Temperature, T _{STG}	-65°C to 150°C	
ESD - Human Body Model, NOTE 1	2000V	
ESD - Charged Device Model, NOTE 1	1500V	

NOTE 1: According to JEDEC/JESD 22-A114/22-C101.

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40$ °C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V _{CC}	Power Supply Voltage		3.135	3.3V	3.465	V
I _{EE}	Power Supply Current			53	60	mA
I _{CC}	Power Supply Current	Q0 to Q3 terminated 50Ω to V_{CC} – $2V$		170	204	mA

Table 3B. Power Supply DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V _{CC}	Power Supply Voltage		2.375	2.5V	2.625	V
I _{EE}	Power Supply Current			49	55	mA
I _{CC}	Power Supply Current	Q0 to Q3 terminated 50Ω to $V_{CC}-2V$		170	199	mA

Table 3C. LVPECL DC Characteristics, V_{CC} = 3.3V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I _{IH}	Input High Current	PCLK, nPCLK	V _{CC} = V _{IN} = 3.465V			150	μA
1	Input Low	PCLK	V _{CC} = 3.465V, V _{IN} = 0V	-10			μA
Current	nPCLK	V _{CC} = 3.465V, V _{IN} = 0V	-150			μA	
V _{REF}	Reference Vo Bias	oltage for Input	I _{REF} = ±1mA	V _{CC} – 1.6	V _{CC} – 1.3	V _{CC} – 1.1	V
V _{OH}	Output High Voltage; NOTE 1			V _{CC} – 1.1	V _{CC} - 0.9	V _{CC} - 0.7	V
V _{OL}	Output Low V	oltage; NOTE 1		V _{CC} – 2.0	V _{CC} – 1.65	V _{CC} – 1.5	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

Table 3D. LVPECL DC Characteristics, V_{CC} = 2.5V ± 5%, V_{EE} = 0V, TA = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I _{IH}	Input High Current	PCLK, nPCLK	V _{CC} = V _{IN} = 2.625V			150	μA
	Input Low	PCLK	V _{CC} = 2.625V, V _{IN} = 0V	-10			μA
I _{IL}	Current	nPCLK	V _{CC} = 2.625V, V _{IN} = 0V	-150			μA
V _{REF}	Reference Voltage for Input Bias		I _{REF} = ±1mA	V _{CC} – 1.6	V _{CC} – 1.3	V _{CC} – 1.1	V
V _{OH}	Output High V	oltage; NOTE 1		V _{CC} – 1.1	V _{CC} - 0.9	V _{CC} - 0.7	V
V _{OL}	Output Low Voltage; NOTE 1			V _{CC} - 2.0	V _{CC} – 1.6	V _{CC} – 1.5	V

NOTE 1: Outputs terminated with 50Ω to $\mbox{V}_{\mbox{CC}}$ – 2V.

AC Electrical Characteristics

Table 4. AC Electrical Characteristics, V_{CC} = 3.3V ± 5% or 2.5V ± 5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f _{REF}	Input PCLK, Prequency PCLK				2	GHz
ΔV/Δt	Input PCLK, Edge Rate nPCLK		1.5			V/ns
t _{PD}	Propagation Delay; NOTE 1	PCK, nPCLK to any Q[0:3], nQ[0:3] for V _{PP} = 0.1V or 0.3V	120	200	320	ps
tsk(o)	Output Skew; NOTE 2, 3			5	25	ps
<i>t</i> sk(p)	Pulse Skew	f _{REF} = 100MHz		5	20	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4			100	200	ps
		f _{REF} = 122.88MHz Sine Wave, V _{PP} = 1V, Integration Range: 1kHz – 40MHz		170		fs
		f _{REF} = 122.88MHz Sine Wave, V _{PP} = 1V, Integration Range: 10kHz – 20MHz		114		fs
		f _{REF} = 122.88MHz Sine Wave, V _{PP} = 1V, Integration Range: 12kHz – 20MHz		114		fs
	Buffer Additive Phase	f _{REF} = 156.25MHz Square Wave, V _{PP} = 1V, Integration Range: 1kHz – 40MHz		42	51	fs
$t_{\sf JIT}$	Jitter, RMS; refer to Additive Phase Jitter	f _{REF} = 156.25MHz Square Wave, V _{PP} = 1V, Integration Range: 10kHz – 20MHz		32	40	fs
	Section	f _{REF} = 156.25MHz Square Wave, V _{PP} = 1V, Integration Range: 12kHz – 20MHz		32	40	fs
		f _{REF} = 156.25MHz Square Wave, V _{PP} = 0.5V, Integration Range: 1kHz – 40MHz		51	71	fs
		f _{REF} = 156.25MHz Square Wave, V _{PP} = 0.5V, Integration Range: 10kHz – 20MHz		38	52	fs
		f _{REF} = 156.25MHz Square Wave, V _{PP} = 0.5V, Integration Range: 12kHz – 20MHz		38	52	fs
t _R / t _F	Output Rise/ Fall Time	20% to 80%	35		180	ps
V	Peak-to-Peak Input	f _{REF} < 1.5 GHz	0.1		1.5	V
V _{PP}	Voltage; NOTE 5, 6	f _{REF} > 1.5 GHz	0.2		1.5	V
V _{CMR}	Common Mode Input Voltage; NOTE 5, 6, 7		1.0		V _{CC} - 0.6	V
V - (nn)	Output Voltage Swing,	V_{CC} = 3.3V, $f_{REF} \le 2GHz$	0.45	0.75	1.0	V
V _O (pp)	Peak-to-Peak	V_{CC} = 2.5V, $f_{REF} \le 2GHz$	0.4	0.65	1.0	V
	Differential Output	V_{CC} = 3.3V, $f_{REF} \le 2GHz$	0.9	1.5	2.0	V
V _{DIFF_OUT}	Voltage Swing, Peak-to-Peak	V_{CC} = 2.5V, $f_{REF} \le 2GHz$	0.8	1.3	2.0	V

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

- NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
- NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.
- NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTES continued on next page.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 5: For single-ended LVCMOS input applications, refer to the Applications section *Writing the Differential Input Levels to Accept Single-ended Levels* (Figures 1 and 2).

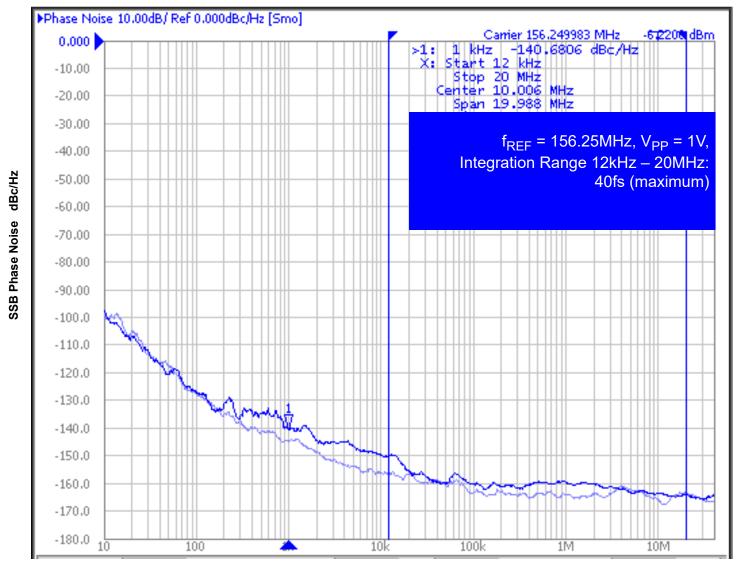
NOTE 6: V_{IL} should not be less than -0.3V.

NOTE 7: Common mode input voltage is defined as the crosspoint.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the *dBc Phase Noise*. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

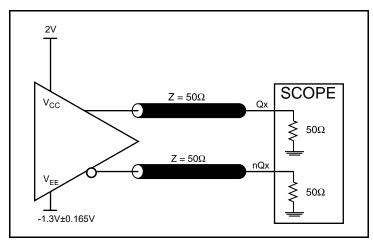


Offset from Carrier Frequency (Hz)

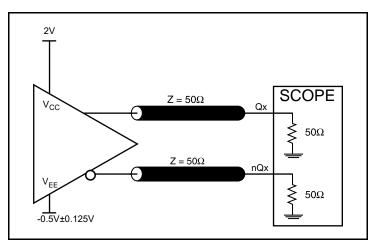
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Wenzel 156.25MHz Oscillator as the input source.

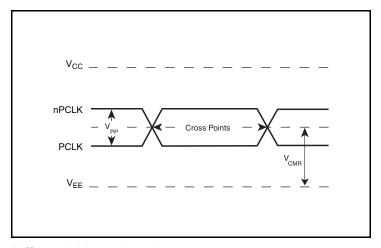
Parameter Measurement Information



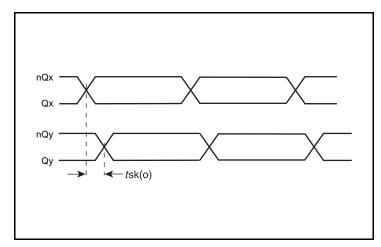
3.3V LVPECL Output Load Test Circuit



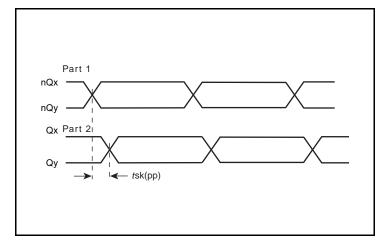
2.5V LVPECL Output Load Test Circuit



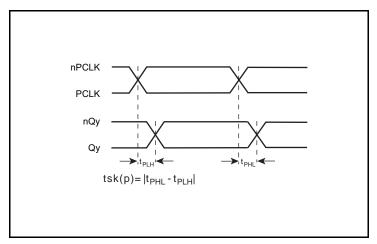
Differential Input Level



Output Skew

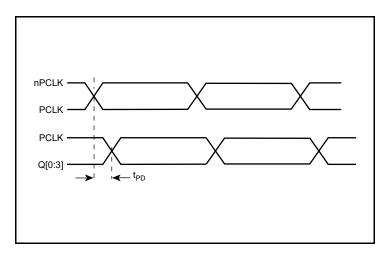


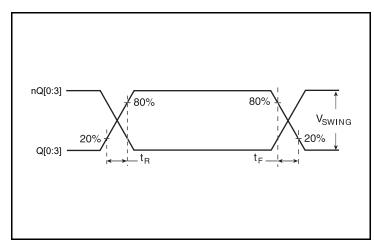
Part-to-Part Skew



Pulse Skew

Parameter Measurement Information, continued





Propagation Delay

Output Rise/Fall Time

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

The IDT8SLVP1104I inputs can be interfaced to LVPECL, LVDS, CML or LVCMOS drivers. *Figure 1A* illustrates how to dc couple a single LVCMOS input to the IDT8SLVP1104I. The value of the series resistance RS is calculated as the difference between the transmission line impedance and the driver output impedance. This resistor should be placed close to the LVCMOS driver. To avoid cross-coupling of single-ended LVCMOS signals, apply the LVCMOS signals to no more than one PCLK input.

A practical method to implement Vth is shown in *Figure 1B* below. The reference voltage Vth = V1 = $V_{CC}/2$, is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible.

The ratio of R1 and R2 might need to be adjusted to position the V1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V1 at 1.25V. The values below apply when both the single-ended swing and V_{CC} are at the same voltage.

When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced, particularly if both input references are LVCMOS to minimize cross talk. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{\rm IL}$ cannot be less than -0.3V and $V_{\rm IH}$ cannot be more than $V_{\rm CC}$ + 0.3V.

Figure 1B shows a way to attenuate the PCLK input level by a factor of two as well as matching the transmission line between the LVCMOS driver and the IDT8SLVP1104I at both the source and the

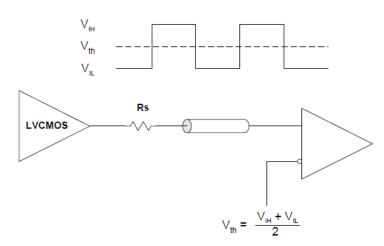


Figure 1A. DC-Coupling a Single LVCMOS Input to the IDT8SLVP1104I

load. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. R3 and R4 in parallel should equal the transmission line impedance; for most 50Ω applications, R3 and R4 will be $100\Omega.$ The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Though some of the recommended components of Figure 1B might not be used, the pads should be placed in the layout so that they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

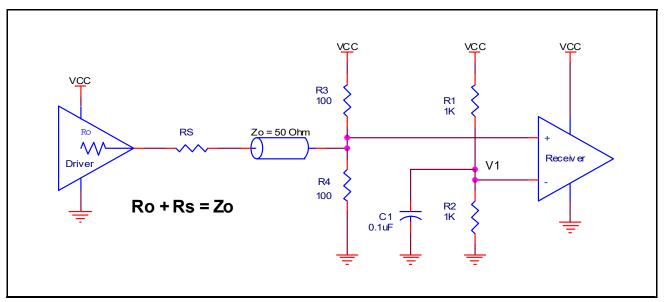


Figure 1B. Alternative DC Coupling a Single LVCMOS Input to the IDT8SLVP1104I

3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

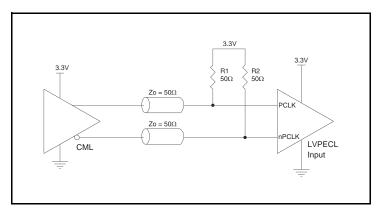


Figure 2A. PCLK/nPCLK Input Driven by a CML Driver

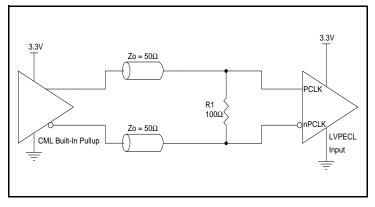


Figure 2B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

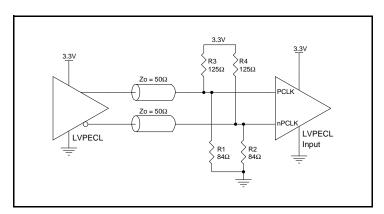


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

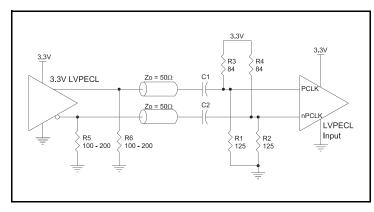


Figure 2D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

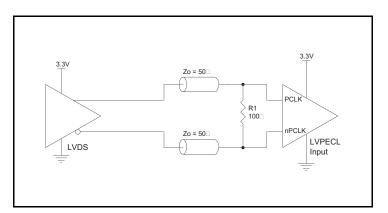


Figure 2E. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

2.5V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The

input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

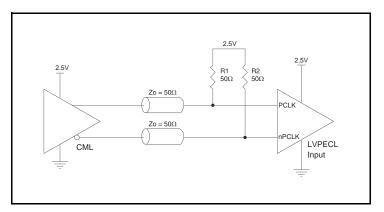


Figure 3A. PCLK/nPCLK Input Driven by a CML Driver

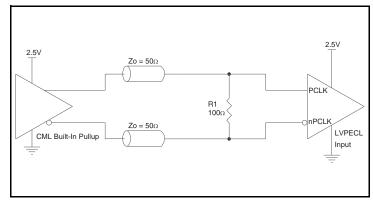


Figure 3B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

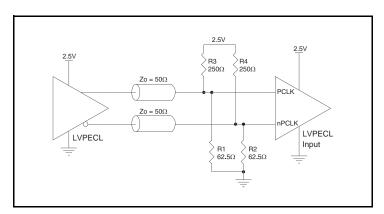


Figure 3C. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

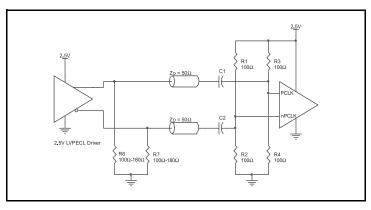


Figure 3D. PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

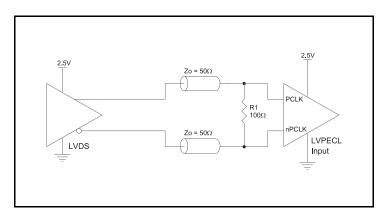


Figure 3E. PCLK/nPCLK Input Driven by a 2.5V LVDS Driver

Recommendations for Unused Output Pins

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

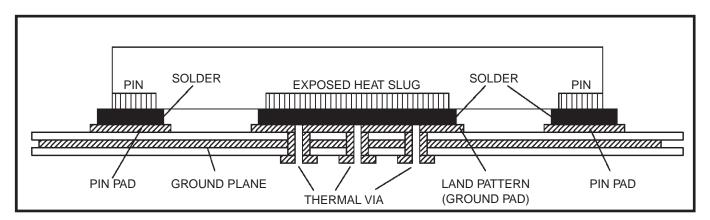


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

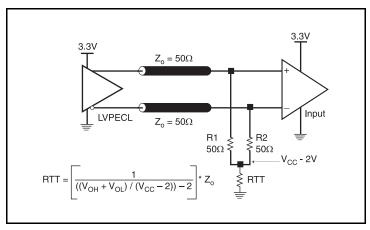


Figure 5A. 3.3V LVPECL Output Termination

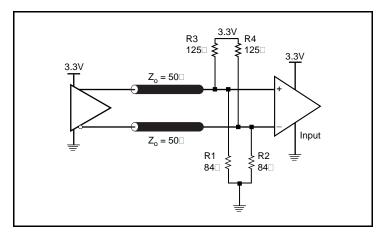


Figure 5B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 6A and Figure 6B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground

level. The R3 in Figure 6B can be eliminated and the termination is shown in *Figure 6C*.

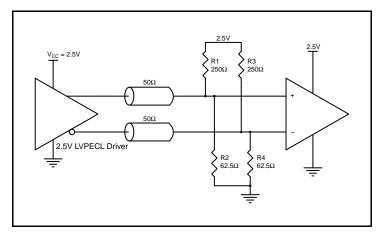


Figure 6A. 2.5V LVPECL Driver Termination Example

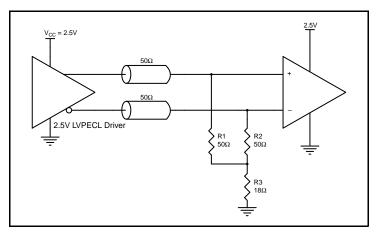


Figure 6B. 2.5V LVPECL Driver Termination Example

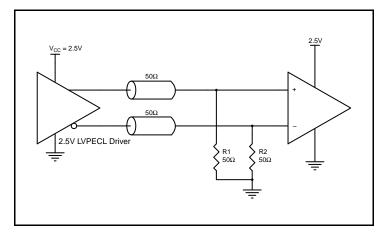


Figure 6C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8SLVP1104I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8SLVP1104I is the sum of the core power plus the power dissipated due to loading. The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

The maximum current at 85° is as follows:

 $I_{EE\ MAX} = 60 \text{mA}$

- Power (core)_{MAX} = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 60mA = 207.9mW
- Power (outputs)_{MAX} = 33.2mW/Loaded Output pair
 If all outputs are loaded, the total power is 4 * 33.2mW = 132.8mW

Total Power_MAX (3.465V, with all outputs switching) = 207.9mW + 132.8mW = 340.7mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

 θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 5 below.

Therefore, Ti for an ambient temperature of 85°C with all outputs switching is:

 $85^{\circ}\text{C} + 0.341\text{W} * 74.7^{\circ}\text{C/W} = 110.5^{\circ}\text{C}$. This is below the limit of 125°C .

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 16-Lead VFQFPN, Forced Convection

θ_{JA} by Velocity					
Meters per Second	0	1	2.5		
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W		

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in Figure 7.

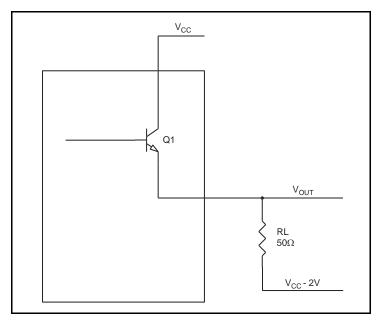


Figure 7. LVPECL Driver Circuit and Termination

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V. These are typical calculations.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} 0.7V$ $(V_{CC_MAX} - V_{OH_MAX}) = 0.7V$
- For logic low, V_{OUT} = V_{OL_MAX} = V_{CC_MAX} 1.5V
 (V_{CC_MAX} V_{OL_MAX}) = 1.5V

Pd H is power dissipation when the output drives high.

Pd L is the power dissipation when the output drives low.

$$Pd_{-}H = [(V_{OH_MA} - (V_{CC_MA} - 2V))/R_{L}] * (V_{CC_MA} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_{L}] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.7V)/50\Omega] * 0.7V = 18.2mW$$

$$Pd_{L} = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_{L}] * (V_{CC_MA} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_{L}] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.5V)/50\Omega] * 1.5V = 15mW$$

Total Power Dissipation per output pair = Pd_H + Pd_L = 33.2mW

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 16-Lead VFQFPN

θ _{JA} at 0 Air Flow				
Meters per Second	0	1	2.5	
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W	

Transistor Count

The transistor count for the IDT8SLVP1104I is: 258

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/16-vfqfpn-package-outline-drawing-30-x-30-x-09-mm-05-mm-170-x-170-mm-epad-nlnlg16p2

Ordering Information

Table 7. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8SLVP1104ANLGI	104AI	"Lead-Free" 16-Lead VFQFPN	Tube	-40°C to 85°C
8SLVP1104ANLGI8	104AI	"Lead-Free" 16-Lead VFQFPN	Tape & Reel	-40°C to 85°C

Revision History

Revision Date	Description of Change
March 13, 2018	Updated the package outline drawings; however, no technical changes Completed other minor changes
February 25, 2014	Ordering Information: changed Tray to Tube.



Corporate Headquarters 6024 Silver Creek Valley Road San Jose, CA 95138 USA www.IDT.com Sales 1-800-345-7015 or 408-284-8200 Fax: 408-284-2775 www.IDT.com/go/sales Tech Support www.idt.com/go/support

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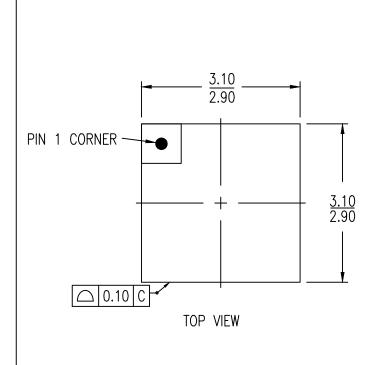
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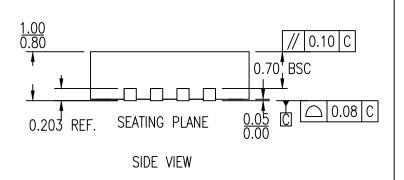
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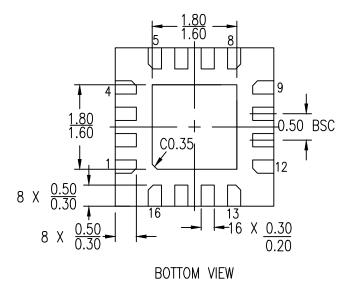


16-VFQFPN Package Outline Drawing

3.0 x 3.0 x 0.9 mm, 0.5mm Pitch, 1.70 x 1.70 mm Epad NL/NLG16P2, PSC-4169-02, Rev 05, Page 1





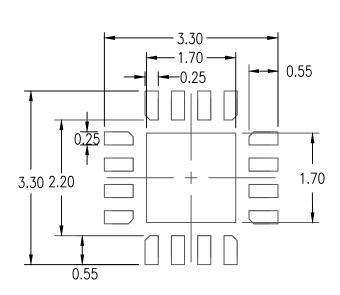


NOTES: 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES



16-VFQFPN Package Outline Drawing

3.0 x 3.0 x 0.9 mm, 0.5mm Pitch, 1.70 x 1.70 mm Epad NL/NLG16P2, PSC-4169-02, Rev 05, Page 2



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

- 1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
- 2. TOP DOWN VIEW-AS VIEWED ON PCB
- 3. LAND PATTERN RECOMMENDATION IS PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 25, 2017	Rev 04	Remove Bookmak at Pdf Format & Update Thickness Tolerance
Jan 18, 2018	Rev 05	Change QFN to VFQFPN

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Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

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