NB3N3020DTGEVB

NB3N3020DTGEVB Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Device Name: NB3N3020DTG (TSSOP−16)
Board Name: NB3302DTGEVB

Description

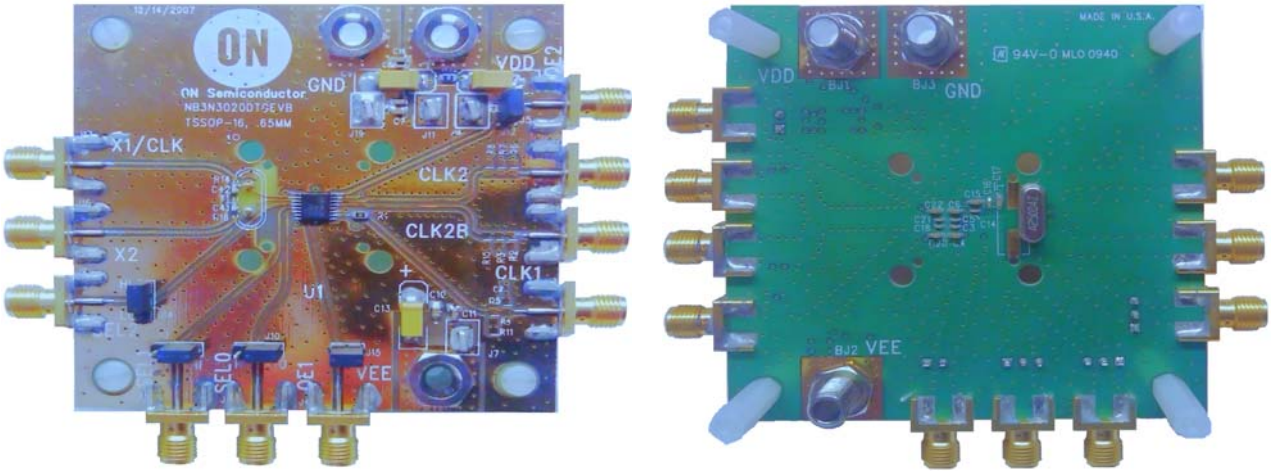
The NB3N3020DTG is a high precision, low phase noise selectable clock multiplier. The device takes a 5 – 27 MHz fundamental mode parallel resonant crystal or a 2 – 210 MHz LVCMOS single ended clock source and generates a differential LVPECL output and a single ended LVCMOS/LVTTL output at a selectable clock output frequency which is a multiple of the input clock frequency. Three tri − level (Low, Mid, High) LVCMOS/LVTTL single ended select pins set one of 26 possible clock multipliers. An LVCMOS/LVTTL output enable (OE) tri − states clock outputs when low. This device is housed in 5 mm x 4.4 mm narrow body TSSOP−16 pin package.

See datasheet NB3N3020/D (www.onsemi.com).The NB3N3020DTGEVB Evaluation board is designed to provide a flexible and convenient platform to quickly program, evaluate and verify the performance and operation of the NB3N3020DTG TSSOP − 16 device under test: With the device removed, this NB3N5573DTGEVB Evaluation board is designed to accept a 16 Lead TSSOP Socket (M&M Specialties, Inc., 1−800−892−8760, www.mmspec.com , M&M #50−000−00809) to permit use as an insertion test fixture.

Board Features

- Crystal mount source, or input external clock source (SMA). One 25 MHz crystal is supplied.
- A TSSOP−16 NB3N3020DTG device is solder mounted or the board may be adapted for insertion testing by adding a TSSOP−16 socket.
- Separate supply connectors for VDD, GND, and VEE (banana jacks and Anvil Clips)

Contents



FRONT BACK

Figure 1. NB3N3020DTGEVB Evaluation Board

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BOARD LAYOUT

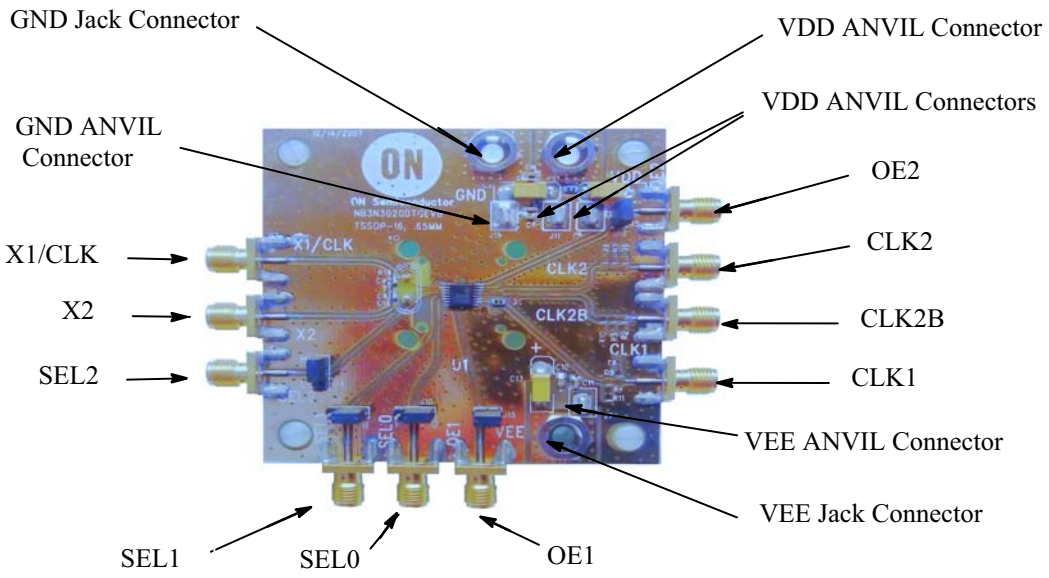

Figure 2. FRONT Board Layout

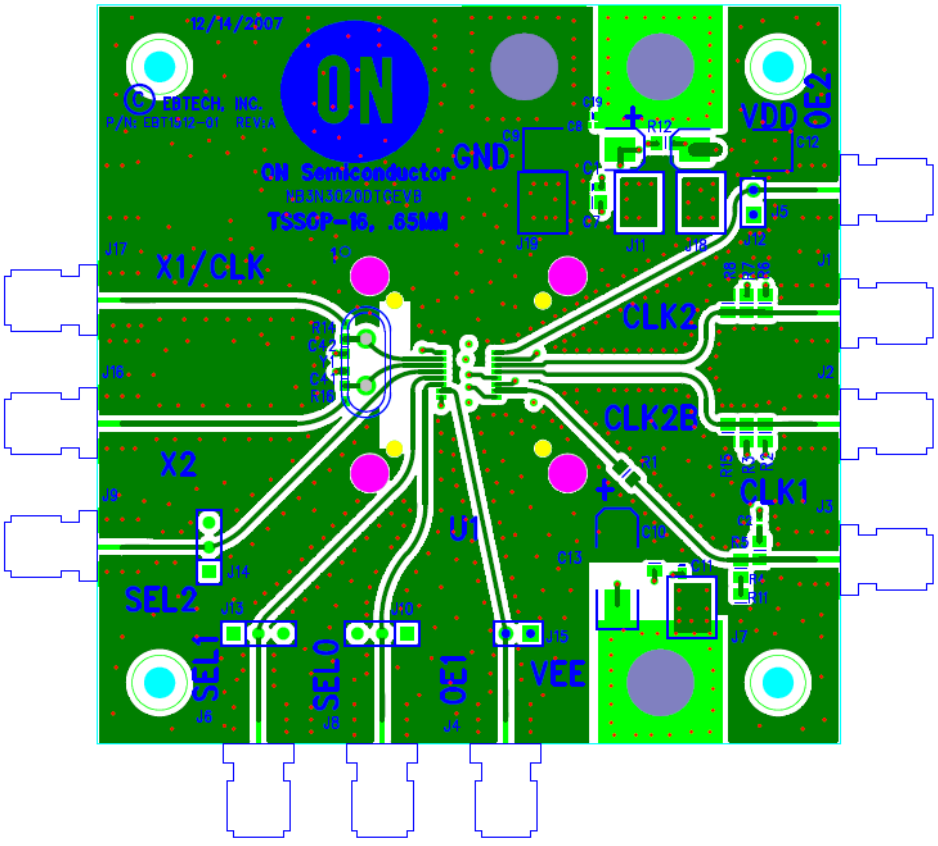

Figure 3. FRONT Layer Design

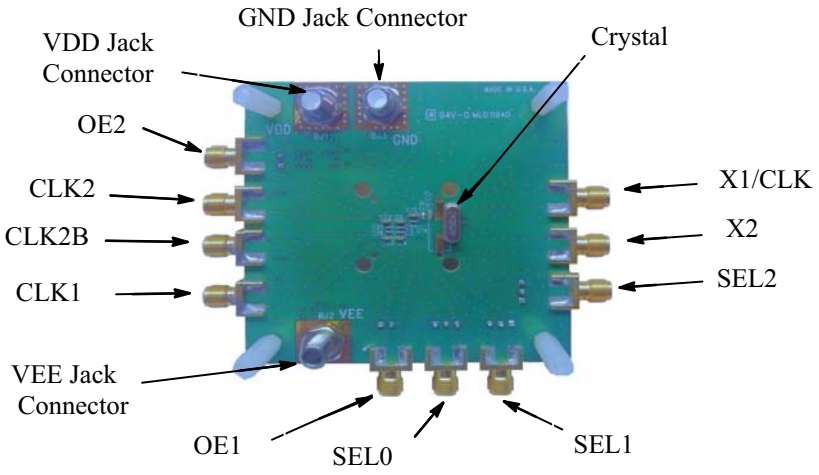

Figure 4. BACK Board Layout

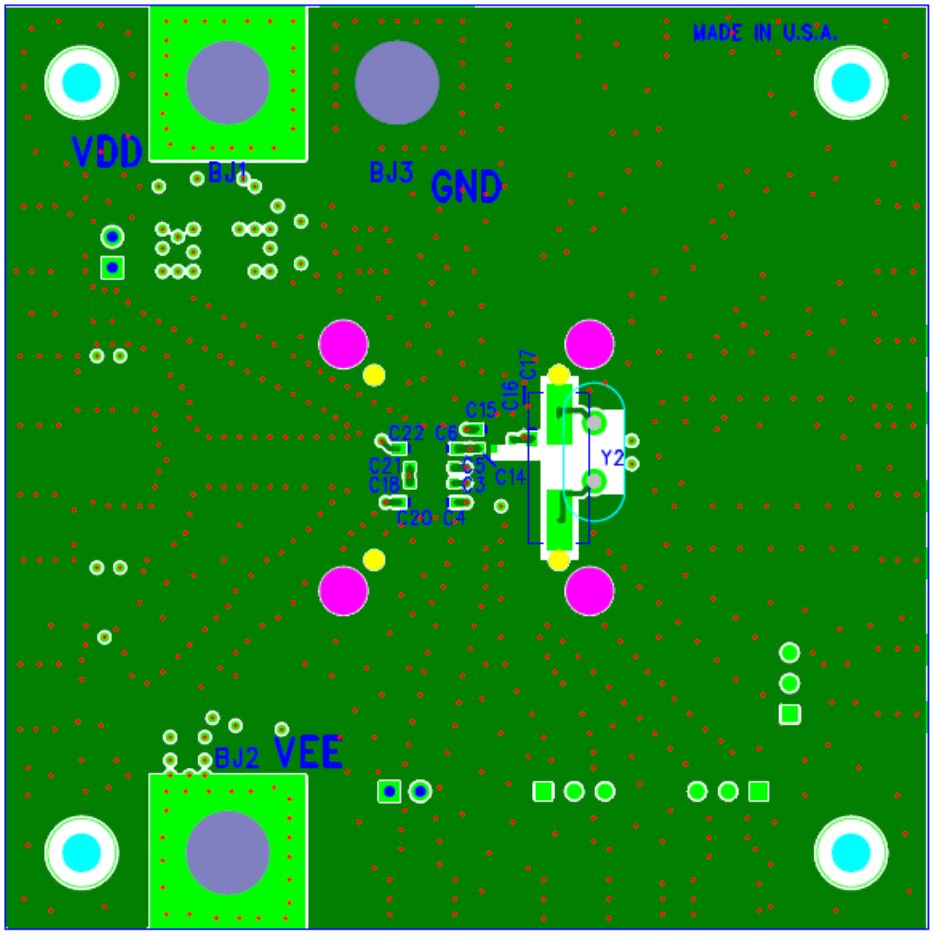

Figure 5. BACK Layer Design

TEST AND MEASUREMENT SET−UP AND PROCEDURE

Step 1: Equipment

1. Signal Generator: Agilent #33250A or HP8133 (or equivalent)
2. Tektronix TDS8000 Oscilloscope
3. Power Supply: Agilent #6624A or AG6626A DC (or equivalent)
4. Digital Voltmeter: Agilent 34410A or 34401 (or equivalent)
5. Matched Cables (> 20 GHz, SMA connectors): Storm or Semflex (or equivalent)
6. Time Transition Convertor: Agilent 14534 250 ps (or equivalent)
7. Phase noise Analyzer: Agilent E5052B (or equivalent)

Step 2: Lab Set−Up Procedure

1. Test Supply Setup:
   Board and Device Power Supply Connections are shown in Table 1. VDD, VEE, and GND and may be connected by banana jacks or anvil clip test points.

Table 1. POWER SUPPLY CONNECTIONS

Device	Board	Banana Jack	Anvil Clip Test Point	Comments
VDD	VDD	BJ1	J11	VDD, VDD1, and VDD2 are shorted by R12
VDD	VDD2	BJ1	J18	
VDD	VDD3	BJ1	J18	
GND	VEE	BJ2	J7	DUTGND
	SMAGND	BJ3	J19	Shield GND

SINGLE SUPPLY OPERATION (V_{DD} = 3.3 V; GND =0.0 V' V_{EE} = 0.0 V)

Single supply operation may be accomplished by shunting GND (SMAGND) and VEE (DUTGND). Input and output levels are not shifted, but High Impedance Probes must be used to sense the outputs. LVPECL outputs CLK2 and CLK2b must be terminated with 50 Ω into a VTT type current sinking supply of V_{DD} − 2.0 V per Figure 6. High Impedance probes must be used to sense the signal levels.

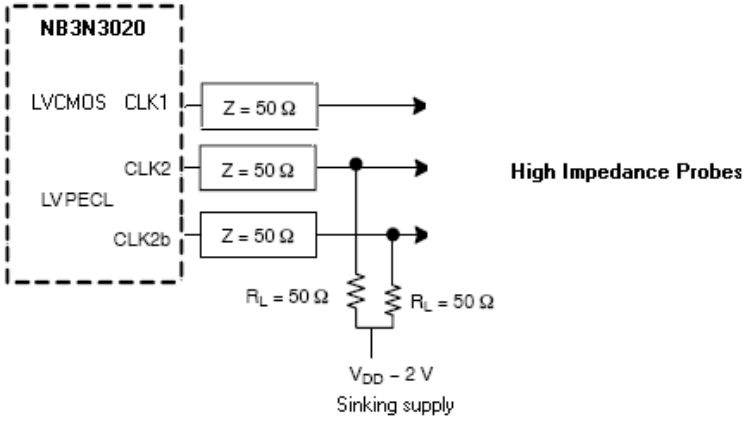

Figure 6. Typical Device Termination Setup and Termination for Single Ended Operation (High Impedance Scope or Probes)

SPLIT SUPPLY OPERATION (VDD = 2.0 V; GND = 0.0 V; VEE = −1.3 V)

For offset or split supply operation, the VDD supply is offset −1.3 V to 2.0 V with respect to GND (SMAGND) and VEE is set to −1.3 V for 3.3 V supply span operation. Supply variance is done by adjusting the VEE supply (±5%). Split supply operation offers the advantage of connecting the LVPECL outputs (CLK2 and CLK2b) directly to a 50 Ω input impedance counter or oscilloscope (or use of Low Impedance probes) per Figure 7. All input and output levels will be offset or shifted −1.3 V. The LVCMOS output CLK1 will be properly terminated but also offset or shifted −1.3 V. Low Impedance (50 Ω) probes must be used to sense the signal levels.

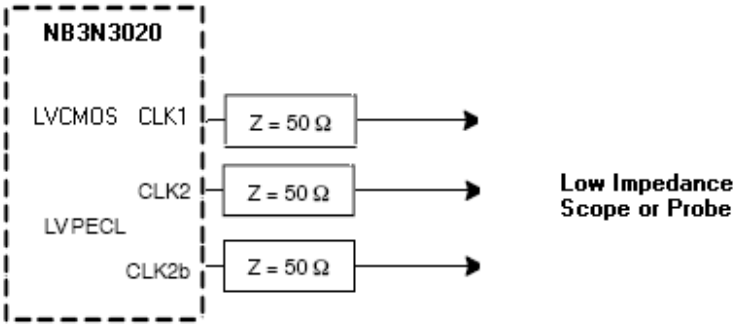

Figure 7. Typical Device Termination Setup and Termination for Split Supply Operation (50 Ω Low Impedance Scope or Probes)

2. Inputs: (see Appendix 1, Device Pin to Board Connection Information)

SINGLE SUPPLY OPERATION (VDD = 3.3 V; GND = 0.0 V' VEE = 0.0 V)

For a Single Ended input to X1/CLK operation, remove the crystal loading caps C41 and C42 and bridge the small topside trace gap from the device input pin to the SMA connector by installing R14 (a Zero Ω resistor). Do not install R16. Do not drive X2. Use a LVCMOS Clock amplitude signal from 2 MHz to 210 MHz which satisfies datasheet VIH and VIL to drive X1/CLK. Input tr/tf transition edges should be about 250 ps. Use a TTC (Time transition Convertor) such as Agilent 14534 (250 ps) or equivalent, if needed, to slow faster edges. Termination of a signal generator may be accomplished by placing a 50 Ω resistor (to GND) at location C42. The mounted crystal does not need to be removed for Single Ended input operation.

For Crystal operation use a fundamental Parallel Resonant crystal (see Datasheet section on "Recommended Crystal Parameters") from 5 MHz to 27 MHz. The board is supplied with a thru–hole 25 MHz crystal installed, but alternatively has the tabs for a surface mount crystal. The Crystal mount is located on the back (underside) of the board and is permanently connected to the device inputs by traces. Crystal Load capacitors (C41 and C42) of 27 mF are mounted.

Device frequency is selected by three level inputs SEL0, SEL1, SEL2. Jumpers J10 (SEL0), J13 (SEL1), and J14 (SEL2) may be set to either VDD (HI), VEE (LO), or floated open (MID) to program the output frequency of operation per datasheet Table 2. Jumpers may be removed to drive SEL0/1/2 directly with spec VIH, VIL, or VIM levels. Note SEL0/1/2 inputs will default to VDD/2 (MID) when left floating open. High Impedance probes must be used to sense the signal levels.

Inputs OE1 and OE2 may be jumpered to VEE (GND) for a LOW level (DISABLED) using J15 (OE1) or J12 (OE2). If floated open (jumper removed), pin will default to a HIGH level (ENABLED). High Impedance probes must be used to sense the signal levels.

SPLIT SUPPLY OPERATION (VDD = 2.0 V; GND = 0.0 V; VEE = −1.3 V)

For a Single Ended input to X1/CLK operation, remove the crystal loading caps C41 and C42 and bridge the small topside trace gap from the device input pin to the SMA connector by installing R14 (a Zero Ω resistor). Do not install R16. Do not drive X2. Use −1.3 V offset LVCMOS Clock amplitude signal from 2 MHz to 210 MHz which satisfies datasheet VIH and VIL to drive X1/CLK. Input tr/tf transition edges should be about 250 ps. Use a TTC (Time Transition Convertor) such as Agilent 14534 (250 ps) or equivalent, if needed to supply proper edges. Termination of a signal generator may be accomplished by placing a 50 Ω resistor (to GND) at location C42. The mounted crystal does not need to be removed for Single Ended input operation.

For Crystal operation use a fundamental Parallel Resonant crystal (see Datasheet section on "Recommended Crystal Parameters") from 5 MHz to 27 MHz. The board is supplied with a thru–hole 25 MHz crystal installed, but alternatively has the tabs for a surface mount crystal. The Crystal mount is located on the back (underside) of the board and is permanently connected to the device inputs by traces. Crystal Load capacitors (C41 and C42) of 27 mF are mounted.

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Inputs OE1 and OE2 may be jumpered to VEE (GND) for a LOW level (DISABLED) using J15 (OE1) or J12 (OE2). If floated open (jumper removed), pin will default to a HIGH level (ENABLED). High Impedance probes must be used to sense the signal levels. All input and output levels will be offset or shifted −1.3 V.

3. Outputs: LVPECL outputs (CLK2, CLK2b):

SINGLE SUPPLY OPERATION (VDD = 3.3 V; GND = 0.0 V' VEE = 0.0 V)

Externally connect LVPECL outputs CLK2 and CLK2b through a 50 Ω terminating resistor to a VTT current sinking regulated supply set to VDD−2V per Figure 6. High Impedance probes must be used to sense the signal levels.

Alternatively, use of a VTT current sinking regulated supply may be avoided by populating R6 (82 Ω) and R7 (130 Ω) to terminate CLK2 and populating R2 (82 Ω) and R3 (130 Ω) to terminate CLK2b as per Figure 8 Alternative Device Termination Setup for On−Board Termination. High Impedance probes must be used to sense the signal levels.

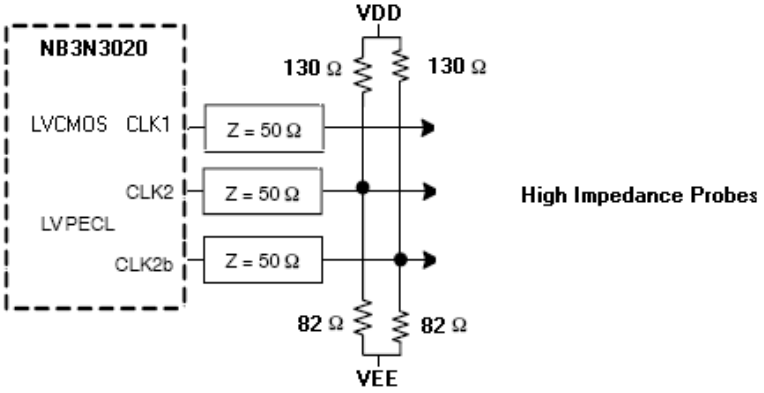

Figure 8. Alternative Device Termination Setup for On−Board Termination

SPLIT SUPPLY OPERATION (VDD = 2.0 V; GND = 0.0 V; VEE = −1.3 V)

Externally connect LVPECL outputs CLK2 and CLK2b directly to a counter or scope (with 50 Ω input impedance) or use Low Impedance Probes (50 Ω) per Figure 7.
NOTE: THE READINGS OF THE OUTPUT VOLTAGE LEVELS WILL BE OFFSET −1.3 V.

Alternatively, LVPECL outputs CLK2 and CLK2b may be terminated on the board by populating R6 (82 Ω) and R7 (130 Ω) to terminate CLK2 and populating R2 (82 Ω) and R3 (130 Ω) to terminate CLK2b as per Figure 6. High Impedance probes must be used to sense the signal levels.
NOTE: THE READINGS OF THE OUTPUT VOLTAGE LEVELS WILL BE OFFSET − 1.3 V.

APPENDIX 1: DEVICE PIN TO BOARD CONNECTION INFORMATION (SEE CURRENT DATASHEET)

Table 2. DEVICE PINS TO BOARD CONNECTION

Device Pin	Device Pin Name	Board Connection	I/O	Description
1	VDD	VDD	Positive Supply	Positive Supply pin. All Supply pins must be connected for proper operation
2	X1/CLK	X1/CLK	Crystal Interface	Oscillator Input from Crystal. Single ended Clock Input.
3	X2	X2	Crystal Interface	Oscillator Output to drive Crystal
4	SEL2	SEL2	Tri – Level Input	Frequency select input 2.
5	SEL1	SEL1	Tri – Level Input	Frequency select input 1
6	SEL0	SEL0	Tri – Level Input	Frequency select input 0
7	OE1	OE1	LVCMOS Input	Input pin OE1 accepts LVCMOS levels to control CLK1 (tri–states CLK1 when LOW, open pin defaults to HIGH)
8/	GND	VEE	Negative Supply	DUT GND. All Supply pins must be connected for proper operation
9	GND	VEE	Negative Supply	DUT GND. All Supply pins must be connected for proper operation
10	CLK1	CLK1	LVCMOS Output	LVCMOS Output
11	VDD	VDD2,	POWER	Positive Supply pin. All Supply pins must be connected for proper operation
12	GND	VEE	Negative Supply	DUT GND
13	CLK2	CLK2	LVPECL Output	True LVPECL Output
14	CLK2b	CLK2b	LVPECL Output	Invert LVPECL Output
15	VDD	VDD3	POWER	Positive Supply pins. All Supply pins must be connected for proper operation
16	OE2	OE2	LVCMOS Input	Input pin OE2 accepts LVCMOS levels to control LVPECL Output CLK2 and CLK2b (when LOW forces CLK1 LOW and CLK2b HIGH, open pin defaults to HIGH)

APPENDIX 2: SCHEMATIC

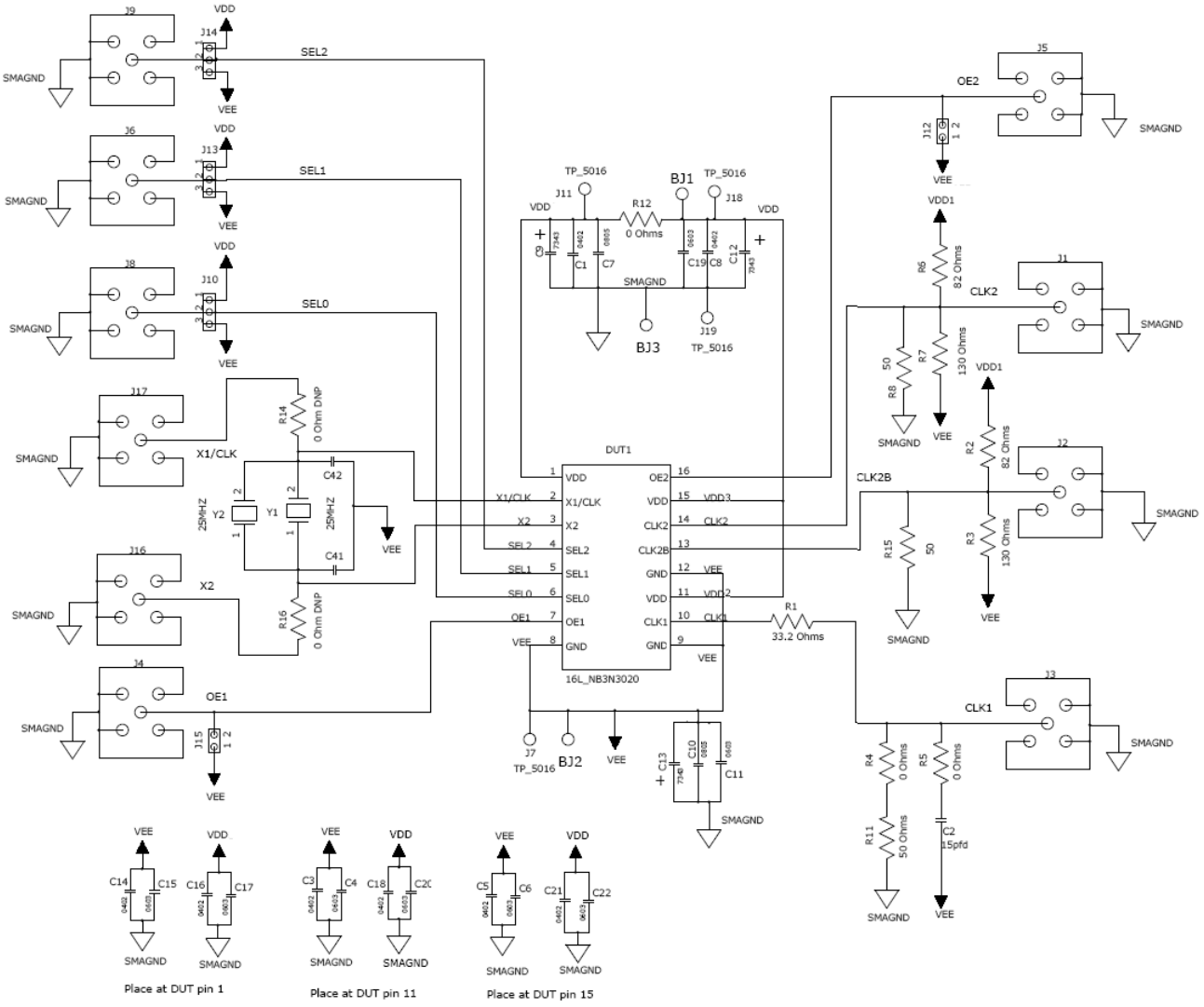

Figure 9. Schematic

APPENDIX 3: BILL OF MATERIALS, LAMINATION STACKUP, AND ASSEMBLY NOTES

Table 3. BILL OF MATERIAL

Item	Qty	Schematic	Value	Size	MFG	P/N	Description
1	3	BJ1−BJ3			ITT POMONA ELECTRONICS	B−JACK 1/4−32 THREAD	BANANAJACK
2	8	C2,C3,C5,C8,C14,C 16,C18,C21	.01ufd	0402	AVX Corporation	04023C103KAT2A	CAP CERM .01UF 10% 25V X7R
3	9	C1,C4,C6,C11,C15, C17,C19,C20,C22	.01ufd	0603	Murata	GRM188R71H103KA01D	CAP CER 10000PF 50V 10% X7R
4	2	C7, C10	.01ufd	0805	TDK	C2012X7R1H103K	CAP CER .01UF 50V X7R 10%
5	2	C41,C42	27pfd	0603	AVX Corporation	06031A270FAT2A	CAP CERM 27PF 1% 100V NP0
6	3	C9,C12,C13	10ufd	7343	Kemet	T491C106K016AT	CAPACITOR TANT 10UF 16V 10% SMD
7	2	J12,J15	2 Pin		Sullins	PEC36SACN	CONN HEADER .100 SINGL STR 36POS
8	5	J10,J12,J13,J14,J15			SULLINS ELECTRONICS CORP	STC02SYAN	CONN JUMPER SHORTING TIN
9	3	J10,J13,J14	3 Pin		Sullins	PEC36SACN	CONN HEADER .100 SINGL STR 36POS
10	1	R1	33.2	0805	Panasonic − ECG	ERJ−2RKF33R2X	RES 33.2 Ω 1/16W 1% 0805 SMD
11	1	R12	0	0805			
12	10	J1,J2,J3,J4,J5,J6,J8 ,J9,J16,J17			Emerson Network Power Connectivity Solutions	142−0701−801	CONN JACK END LAUNCH PCB .187” G
13	4	J7,J11,J18,J19	SMT		KEYSTONE ELECTRONICS	5016	PC TEST POINT COMPACT SMT
14	2	Y1 Crystal Socket Receptacle	BOTTOM		Ampere	2−330808−8	CONN SOCKET RCPT .013−0.21 30AU
15	4	Standoff					Nylon Standoff
16	4	Screw					Nylon Screw
17	1	C2		0402			NOT INSTALLED
18	9	R2,R3,R4,R5,R6,R7 ,R8,R11,R15		0805			NOT INSTALLED
19	2	R14,R16		0603			NOT INSTALLED
20	1	Y1	25 MHz		Abracon	ABL−25.000MHZ−B2F	Through Hole Crystal
21	1	SOCKET			M&M	50−000−00809	NOT INSTALLED
22	1	U1			On Semi	NB3N3020	16 lead TSSOP Dut

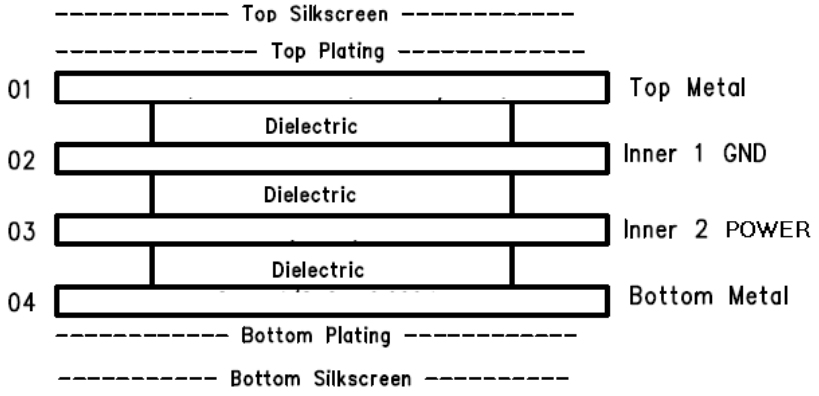

Figure 10. Lamination Stack

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
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