

LTC6416

2 GHz Low Noise Differential 16-Bit ADC Buffer

DESCRIPTION

Demonstration circuit 1257B features the LTC®6416, a 2GHz low noise differential 16-Bit ADC buffer driving the LTC2208, a 16-bit 130Msps ADC. The DC1257B is supplied with a bandpass filter centered at 140MHz between the buffer and the ADC. The filter center frequency can be changed to optimize performance at different analog input frequencies. Both single-ended and differential configurations are supported at the inputs. The DC1257B has been

developed from the DC996B-B, used to characterize the LTC2208 family of ADCs.

Use the DC1257B with a DC890 FastDAACS and PScope™ software to collect time and frequency data.

Design files for this circuit board are available at <http://www.linear.com/demo>

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QUICK START PROCEDURE

Demonstration circuit 1257B is easy to set up. Refer to Figure 1 for proper measurement equipment setup. Table 1

describes the function of each SMA connector and default settings for the jumpers on the board.

Table 1: DC1257B SMA Connector and Jumper Descriptions

J2 (A _{IN} ⁺)	Single-Ended/Differential Input. By default, this is configured as a single-ended input. Use this connector to supply an input to the DC1257B. When driven from a 50Ω signal source, no external termination necessary.
J3 (A _{IN} ⁻)	Differential Input. Not connected by default. Capacitor C23 can be installed and C25 removed to drive the DC1257B differentially.
J4 (CLK)	Single-Ended Input. This input is designed to be driven by an extremely low jitter 50Ω source. A sinusoidal input of up to 13dBm is recommended.
JP1 (PGA)	Programmable gain amplifier. Default to LOW Gain Mode. This sets the gain of the ADC amplifier to 1.0.
JP2 (RAND)	ADC Digital Output Randomization. Default to OFF. This disables randomization.
JP3 (SHDN ADC)	ADC Power Shutdown ADC. Default to EN. This results in normal operation.
JP4 (DITH)	ADC Internal Dither Enable. Default to OFF. This disables internal dither.

HARDWARE SETUP

The DC1257B requires DC890 FastDAACS data acquisition board with PScope System Software. The PScope System Software is available from the Linear Technology website at <http://www.linear.com/software/>.

Apply power to the DC1257B Demonstration Circuit. Apply +3.6V across the pins marked OPT and GND, VS and GND. The DC1257B demonstration circuit requires up to 100mA from the OPT pin, and up to 700 mA from the VS pin.

Supply power to the DC890B FastDAACS Board with an external 6V ±0.5V 1A supply on turrets on G7(+) and G1(–) or the adjacent 2.1mm power jack. Unless the DC890B detects external power it will not activate the LVDS mode of the Xilinx Spartan-III FPGA. The FPGA actively terminates the LVDS repeaters at the outputs of the LTC2208.

HARDWARE SETUP

Apply Encode Clock to the DC1257B on the SMA connector marked "(J4) CLK". This transformer coupled input is terminated with a 100Ω at the secondary and a 100Ω at the ADC clock inputs. For best noise performance the clock input must be driven with a very low jitter source. The amplitude of the sinusoidal generator should be as large as possible, up to 13dBm. Bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. Data sheet FFT plots were taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, non-harmonically related spurs and broad band noise. Low phase noise (jitter) Agilent 8644B generators are used with TTE band pass filters for the CLK input and Analog input.

Apply the Analog Input to the DC1257B on the SMA connector marked "(J2) A_{IN}⁺". This input is capacitively coupled to a 1:4 Balun transformer TCM4-19+.

Start and Configure the PScope data collection software for the FastDAACS DC890 by selecting AutoConfigure. If the board is not detected, up-date PScope for latest software and device list, and then select LTC2208 from the Configure→Device menu. You can also manually configure PScope for the LTC2208 by setting the parameters listed in Table 2.

Table 2: PScope User Configuration for LTC2208

USER CONFIGURE	
Bits	16
Channels	1
Alignment	16
FPGA Ld	LVDS
Bipolar	[x]
Positive Egde Clk	[x]

Collect Data by clicking on the "Collect" button. Time and frequency plots will be displayed in the PScope window. Consult the DC890 Quick Start Guide for additional information.

Buffer ADC Interface

The LTC6416 has been specifically designed to interface directly with high speed A/D converters. It is possible to drive the ADC directly from the LTC6416. In practice, however, better SFDR may be obtained by adding a few external components at the output of the LTC6416.

Figure 2 shows the LTC6416 being driven by a 1:4 transformer which provides 6 dB of voltage gain while also performing single-ended to differential conversion. The differential outputs of the LTC6416 are lowpass filtered to drive the differential inputs of the LTC2208 ADC. In many applications, an anti-alias filter like this is desirable to limit the wideband noise of the amplifier. This is especially true in high performance 16-bit designs. The minimum recommended network between the LTC6416 and the ADC is simply two 5Ω series resistors, which are used to help eliminate resonances associated with the stray capacitances of PCB traces and the stray inductance of the internal bond wires at the ADC input, and the driver output pins. Table 3 suggests filter components for different input frequencies.

Table 3. Suggested Components for the Filter

INPUT FREQUENCY	LTC6416 OUTPUT RESISTORS R13 = R15	FILTERING CAPACITORS C20/C22/C24
30MHz	50Ω	5.6pF/6.8pF/5.6pF
70MHz	25Ω	5.6pF/6.8pF/5.6pF
140MHz	25Ω	1.5pF/1pF/1.5pF
250MHz	5Ω	-/-/-

HARDWARE SETUP

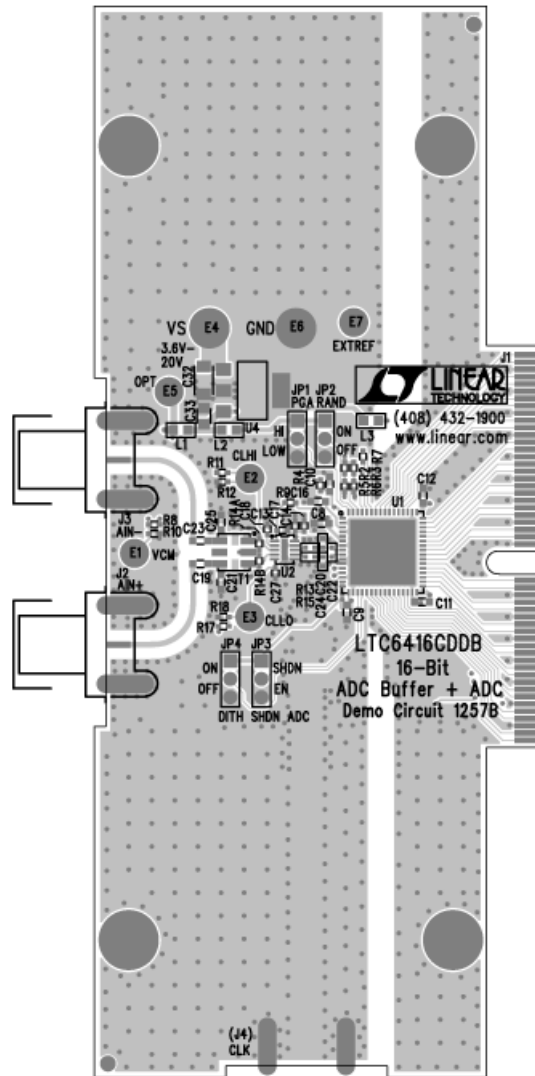


Figure 1. Demo Board DC1257B Layout

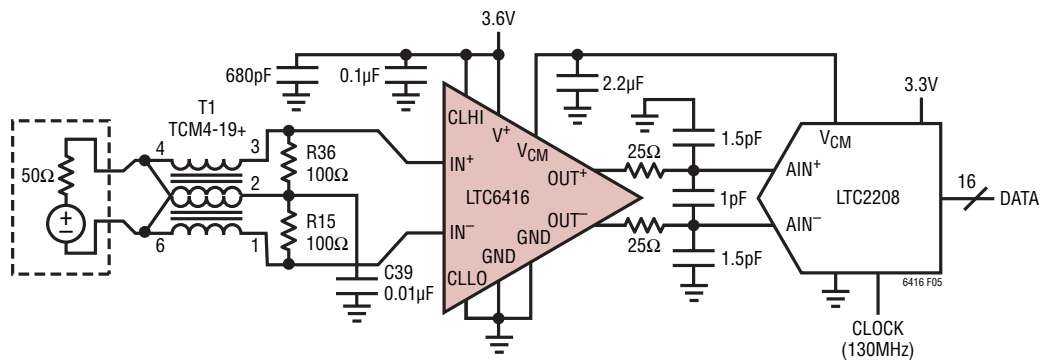


Figure 2. DC1257B Simplified Schematic with Recommended Output Termination for Driving an LTC2208 16-Bit ADC at 140MHz

DEMO MANUAL DC1257B

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	12	C8-C12, C19, C25, C26, C28-C31	CAP., X7R, 0.1µF, 25V, 20% 0603	AVX, 06033C104MAT2A
2	4	C13, C14, C18, C27	CAP., X5R, 0.1µF, 16V, 10% 0402	AVX, 0402YD104KAT2A
3	1	C16	CAP., X5R, 2.2µF, 6.3V, 10% 0603	AVX, 06036D225KAT2A
4	1	C17	CAP., C0G, 220pF, 16V, 10% 0402	AVX, 0402YA221KAT2A
5	2	C20, C24	CAP., C0G, 1.5pF, 50V, ±.25pf 0402	AVX, 04025A1R5CAT2A
6	1	C22	CAP., C0G, 1.0pF, 50V, ±.25pf 0402	AVX, 04025A1R0CAT2A
7	0	C21, C23 (OPT)	CAP., 0603	(OPT)
8	1	C32	CAP., X5R, 10µF, 25V, 20% 1206	Taiyo Yuden, TMK316BJ106ML
9	1	C33	CAP., X5R, 10µF, 6.3V, 20% 0805	Taiyo Yuden, JMK212BJ106MG
10	5	E1, E2, E3, E5, E7	TESTPOINT, TURRET, .061" pbf	MILL-MAX, 2308-2-00-80-00-00-07-0
11	2	E4, E6	TESTPOINT, TURRET, .094" pbf	MILL-MAX, 2501-2-00-80-00-00-07-0
12	4	JP1, JP2, JP3, JP4	HEADER 3-PIN 0.079 SINGLE ROW	SAMTEC, TMM103-02-L-S
13	4	JP1, JP2, JP3, JP4	SHUNT, .079" CENTER	SAMTEC, 2SN-BK-G
14	3	J2, J3, J4	CON., SMA 50Ω EDGE-LAUNCH	E.F. JOHNSON, 142-0701-851
15	0	L1	INDUCTOR, Ferrite Bead	(OPT)
16	2	L2, L3	INDUCTOR, Ferrite Bead	Murata, BLM18PG221SN1D
17	2	R3, R2	RES., CHIP, 10, 1/16W, 5% 0402	VISHAY, CRCW040210R0JNED
18	1	R4	RES., CHIP, 1k, 1/16W, 5% 0402	VISHAY, CRCW04021K00FKED
19	0	R5, R6, R8, R10-R12, R17, R18 (OPT)	RES., CHIP, 0402	(OPT)
20	1	R7	RES., CHIP, 100, 1/16W, 5% 0402	VISHAY, CRCW0402100RJNED
21	2	R13, R15	RES., CHIP, 24.9, 1/16W, 1% 0402	VISHAY, CRCW040224R9FKED
22	2	R14A, R14B	RES., CHIP, 100, 1/16W, 1% 0402	VISHAY, CRCW0402100FKED
23	1	R9, (Bal to#1450A)	RES., CHIP, 10.0, 1/16W, 1% 0402	VISHAY, CRCW040210R0FKED
24	1	R16	RES., CHIP, 5.1k, 1/16W, 5% 0603	VISHAY, CRCW06035K10JNEA
25	2	R26, R19	RES., CHIP, 51.1, 1/16W, 1% 0402	VISHAY, CRCW040251R1FKED
26	1	R21	RES., CHIP, 100, 0.05W, 5% 0201	VISHAY, CRCW0201J100JNTD
27	3	R24, R25, R28	RES., CHIP, 4.99k, 1/16W, 1% 0603	VISHAY, CRCW06034K99FKEA
28	1	R27	RES., CHIP, 2k, 1/16W, 5% 0603	VISHAY, CRCW06032K00JNEA
29	0	R29 (OPT)	RES., CHIP, 0603	(OPT)
30	1	T1	TRANSFORMER, TCM4-19+	Mini-Circuits, TCM4-19+
31	1	T2	TRANSFORMER, ETC1-1-13, SM-22	M/A-COM, MABA-001759-000000
32	1	U1 lot#T28918.2 DC=0837	I.C. LTC2208CUP 9 × 9 QFN	LINEAR, LTC2208CUP#PBF
33	1	U2 lot#J20129.1 DC=0808	I.C. LTC6416CDDDB DFN 10-PIN (3 × 2)	LINEAR, LTC6416CDDDB#PBF
34	1	U3	I.C., 24LC025, TSSOP-8	MICROCHIP, 24LC025 I/ST
35	1	U4 see file for #'s	IC., LT1963AEST-3.3 SOT-223	LINEAR, LT1963AEST-3.3#PBF
36	4	(STAND-OFF)	STAND-OFF, NYLON 0.25"	KEYSTONE, 8831(SNAP ON)
37	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1257B
38	1		STENCIL	STENCIL 1257B

SCHEMATIC DIAGRAM

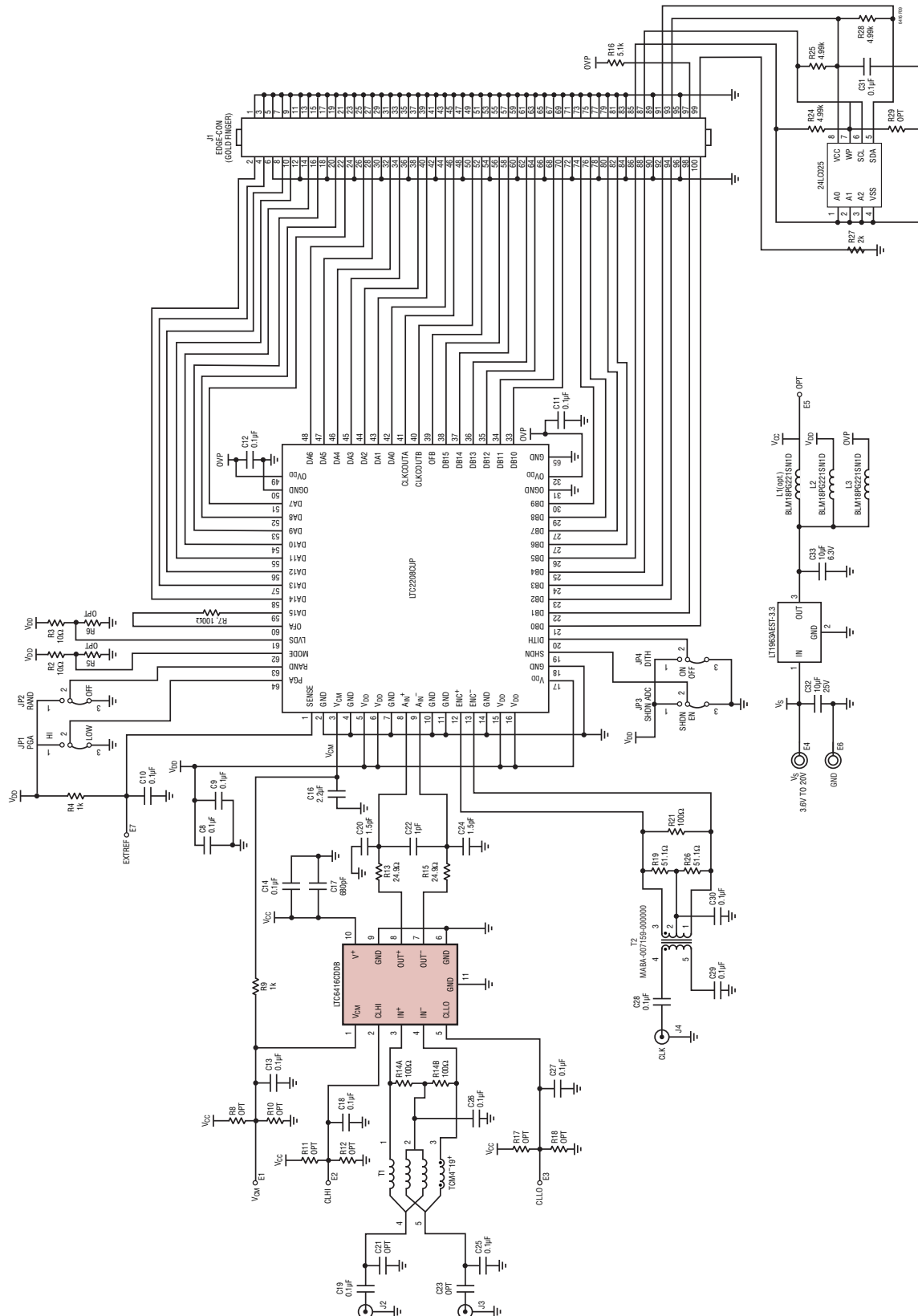


Figure 3. Demo Board DC1257B Schematic (Test Circuit B)

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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