3 MSPS, 12-/10-/8-Bit ADCs in 6-Lead TSOT

Data Sheet

AD7276/AD7277/AD7278

FEATURES

Throughput rate: 3 MSPS
Specified for V_{DD} of 2.35 V to 3.6 V
Power consumption
12.6 mW at 3 MSPS with 3 V supplies
Wide input bandwidth
70 dB SNR at 1 MHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface
SPI-/QSPI™-/MICROWIRE™-/DSP compatible
Temperature range: −40°C to +125°C
Power-down mode: 0.1 µA typical
6-lead TSOT package
8-lead MSOP package
AD7476 and AD7476A pin compatible

GENERAL DESCRIPTION

The AD7276/AD7277/AD7278 are 12-/10-/8-bit, high speed, low power, successive approximation analog-to-digital converters (ADCs), respectively. The parts operate from a single 2.35 V to 3.6 V power supply and feature throughput rates of up to 3 MSPS. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 55 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$, and the conversion is initiated at this point. There are no pipeline delays associated with the part.

The AD7276/AD7277/AD7278 use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the part is taken internally from VDD. This allows the widest dynamic input range to the ADC; therefore, the analog input range for the part is 0 to VDD. The conversion rate is determined by the SCLK.

FUNCTIONAL BLOCK DIAGRAM

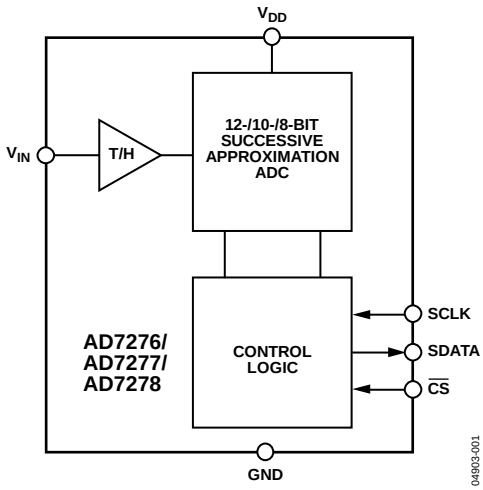

Figure 1.

Table 1.

Part Number	Resolution	Package	
AD7276	12	8-Lead MSOP	6-Lead TSOT
AD7277	10	8-Lead MSOP	6-Lead TSOT
AD7278	8	8-Lead MSOP	6-Lead TSOT
AD7274[1]	12	8-Lead MSOP	8-Lead TSOT
AD7273[1]	10	8-Lead MSOP	8-Lead TSOT

[1] Part contains external reference pin.

PRODUCT HIGHLIGHTS

1. 3 MSPS ADCs in a 6-lead TSOT package.
2. AD7476/AD7477/AD7478 and AD7476A/AD7477A/AD7478A pin compatible.
3. High throughput with low power consumption.
4. Flexible power/serial clock speed management. This allows maximum power efficiency at low throughput rates.
5. Reference derived from the power supply.
6. No pipeline delay. The parts feature a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

Rev. D
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REVISION HISTORY

7/15—Rev. C. to Rev. D

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7/05—Revision 0: Initial Version

SPECIFICATIONS

AD7276 SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V, B Grade and A Grade: f_{SCLK} = 48 MHz, f_{SAMPLE} = 3 MSPS, Y Grade:[1] f_{SCLK} = 16 MHz, f_{SAMPLE} = 1 MSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Grade[2, 3]	B, Y Grade[2, 3]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 1 MHz sine wave, B Grade f_{IN} = 100 kHz sine wave, Y Grade
Signal-to-Noise + Distortion (SINAD)[4]	68	68	dB min	
Signal-to-Noise Ratio (SNR)	69	69	dB min	
	70	70	dB typ	
Total Harmonic Distortion (THD)[4]	−73	−73	dB max	
	−78	−78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[4]	−80	−80	dB typ	
Intermodulation Distortion (IMD)[4]				
Second-Order Terms	−82	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Third-Order Terms	−82	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Aperture Delay	5	5	ns typ	
Aperture Jitter	18	18	ps typ	
Full Power Bandwidth	55	55	MHz typ	@ 3 dB
	8	8	MHz typ	@ 0.1 dB
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity[4]	±1.5	±1	LSB max	
Differential Nonlinearity[4]	+1.2/−0.99	+1.2/−0.99	LSB max	Guaranteed no missed codes to 12 bits
Offset Error[4]	±4	±3	LSB max	
Gain Error[4]	±3.5	±3.5	LSB max	
Total Unadjusted Error[4] (TUE)	±5	±3.5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	µA max	−40°C to +85°C
	±5.5	±5.5	µA max	85°C to 125°C
Input Capacitance	42	42	pF typ	When in track
	10	10	pF typ	When in hold
LOGIC INPUTS				
Input High Voltage, V_{INH}	1.7	1.7	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	2	V min	2.7 V < V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}	0.7	0.7	V max	2.35 V ≤ V_{DD} ≤ 2.7 V
	0.8	0.8	V max	2.7 V < V_{DD} ≤ 3.6 V
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[5]	2	2	pF typ	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} − 0.2	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±2.5	±2.5	µA max	
Floating-State Output Capacitance[5]	4.5	4.5	pF typ	
Output Coding	Straight (natural) binary			

Parameter	A Grade[2, 3]	B, Y Grade[2, 3]	Unit	Test Conditions/Comments
CONVERSION RATE				
Conversion Time	291	291	ns max	14 SCLK cycles with SCLK at 48 MHz, B Grade
	875	875	ns max	14 SCLK cycles with SCLK at 16 MHz, Y Grade
Track-and-Hold Acquisition Time[4]	60	60	ns min	
Throughput Rate	3	3	MSPS max	See the Serial Interface section
POWER REQUIREMENTS				
V_{DD}	2.35/3.6	2.35/3.6	V min/max	
I_{DD}				Digital I/Ps 0 V or V_{DD}
Normal Mode (Static)	1	1	mA typ	V_{DD} = 3.6 V, SCLK on or off
Normal Mode (Operational)	5.5	5.5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 3 MSPS, B Grade
	2.5	2.5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 1 MSPS, Y Grade
	4.2	4.2	mA typ	V_{DD} = 3 V, f_{SAMPLE} = 3 MSPS, B Grade
	1.6	1.6	mA typ	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, Y Grade
Partial Power-Down Mode (Static)	34	34	µA typ	
Full Power-Down Mode (Static)	2	2	µA max	−40°C to +85°C, typically 0.1 µA
	10	10	µA max	85°C to 125°C
Power Dissipation[6]				
Normal Mode (Operational)	19.8	19.8	mW max	V_{DD} = 3.6 V, f_{SAMPLE} = 3 MSPS, B Grade
	9	9	mW max	V_{DD} = 3.6 V, f_{SAMPLE} = 1 MSPS, Y Grade
	12.6	12.6	mW typ	V_{DD} = 3 V, f_{SAMPLE} = 3 MSPS, B Grade
	4.8	4.8	mW typ	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, Y Grade
Partial Power-Down	102	102	µW typ	V_{DD} = 3 V
Full Power-Down	7.2	7.2	µW max	V_{DD} = 3.6 V, −40°C to +85°C

[1] Y grade specifications are guaranteed by characterization.
[2] Temperature range from −40°C to +125°C.
[3] Typical specifications are tested with V_{DD} = 3 V and at 25°C.
[4] See the Terminology section.
[5] Guaranteed by characterization.
[6] See the Power vs. Throughput Rate section.

AD7277 SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V, f_{SCLK} = 48 MHz, f_{SAMPLE} = 3 MSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	A Grade[1, 2]	B Grade[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 1 MHz sine wave
Signal-to-Noise + Distortion (SINAD)[3]	60.5	60.5	dB min	
Total Harmonic Distortion (THD)[3]	−70	−1	dB max	
	−76	−76	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	−80	−80	dB typ	
Intermodulation Distortion (IMD)[3]				
Second-Order Terms	−82	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Third-Order Terms	−82	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Aperture Delay	5	5	ns typ	
Aperture Jitter	18	18	ps typ	
Full Power Bandwidth	74	74	MHz typ	@ 3 dB
	10	10	MHz typ	@ 0.1 dB
DC ACCURACY				
Resolution	10	10	Bits	
Integral Nonlinearity[3]	±0.5	±0.5	LSB max	
Differential Nonlinearity[3]	±0.5	±0.5	LSB max	Guaranteed no missed codes to 10 bits
Offset Error[3]	±1.5	±1	LSB max	
Gain Error[3]	±2	±1.5	LSB max	
Total Unadjusted Error (TUE)[3]	±2.5	±2.5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	µA max	−40°C to +85°C
	±5.5	±5.5	µA max	85°C to 125°C
Input Capacitance	42	42	pF typ	When in track
	10	10	pF typ	When in hold
LOGIC INPUTS				
Input High Voltage, V_{INH}	1.7	1.7	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	2	V min	2.7 V < V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}	0.7	0.7	V max	2.35 V ≤ V_{DD} ≤ 2.7 V
	0.8	0.8	V max	2.7 V < V_{DD} ≤ 3.6 V
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	2	2	pF typ	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} − 0.2	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±2.5	±2.5	µA max	
Floating-State Output Capacitance[4]	4.5	4.5	pF typ	
Output Coding	Straight (natural) binary			
CONVERSION RATE				
Conversion Time	250	250	ns max	12 SCLK cycles with SCLK at 48 MHz
Track-and-Hold Acquisition Time[3]	60	60	ns min	
Throughput Rate	3.45	3.45	MSPS max	SCLK at 48 MHz

Parameter	A Grade[1, 2]	B Grade[1, 2]	Unit	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	2.35/3.6	2.35/3.6	V min/max	
I_{DD}				Digital I/Ps 0 V or V_{DD}
Normal Mode (Static)	0.6	0.6	mA typ	V_{DD} = 3.6 V, SCLK on or off
Normal Mode (Operational)	5.5	5.5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 3 MSPS
	3.5	3.5	mA typ	V_{DD} = 3 V
Partial Power-Down Mode (Static)	34	34	µA typ	
Full Power-Down Mode (Static)	2	2	µA max	−40°C to +85°C, typically 0.1 µA
	10	10	µA max	85°C to 125°C
Power Dissipation[5]				
Normal Mode (Operational)	19.8	19.8	mW max	V_{DD} = 3.6 V, f_{SAMPLE} = 3 MSPS
	10.5	10.5	mW typ	V_{DD} = 3 V
Partial Power-Down	102	102	µW typ	V_{DD} = 3 V
Full Power-Down	7.2	7.2	µW max	V_{DD} = 3.6 V, −40°C to +85°C

[1] Temperature range from −40°C to +125°C.
[2] Typical specifications are tested with V_{DD} = 3 V and at 25°C.
[3] See the Terminology section.
[4] Guaranteed by characterization.
[5] See the Power vs. Throughput Rate section.

AD7278 SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V, f_{SCLK} = 48 MHz, f_{SAMPLE} = 3 MSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	A Grade[1, 2]	B Grade[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 1 MHz sine wave
Signal-to-Noise + Distortion (SINAD)[3]	49	49	dB min	
Total Harmonic Distortion (THD)[3]	−66	−67	dB max	
	−73	−73	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	−69	−69	dB typ	
Intermodulation Distortion (IMD)[3]				
Second-Order Terms	−76	−76	dB typ	fa = 1 MHz, fb = 0.97 MHz
Third-Order Terms	−76	−76	dB typ	fa = 1 MHz, fb = 0.97 MHz
Aperture Delay	5	5	ns typ	
Aperture Jitter	18	18	ps typ	
Full Power Bandwidth	74	74	MHz typ	@ 3 dB
Full Power Bandwidth	10	10	MHz typ	@ 0.1 dB
DC ACCURACY				
Resolution	8	8	Bits	
Integral Nonlinearity[3]	±0.2	±0.2	LSB max	
Differential Nonlinearity[3]	±0.3	±0.3	LSB max	Guaranteed no missed codes to 8 bits
Offset Error[3]	±0.9	±0.5	LSB max	
Gain Error[3]	±1.2	±1	LSB max	
Total Unadjusted Error (TUE)[3]	±1.5	±1.5	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	µA max	−40°C to +85°C
	±5.5	±5.5	µA max	85°C to 125°C
Input Capacitance	42	42	pF typ	When in track
	10	10	pF typ	When in hold
LOGIC INPUTS				
Input High Voltage, V_{INH}	1.7	1.7	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	2	V min	2.7 V < V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}	0.7	0.7	V max	2.35 V ≤ V_{DD} ≤ 2.7 V
	0.8	0.8	V max	2.7 V < V_{DD} ≤ 3.6 V
Input Current, I_{IN}	±1	±1	µA max	
Input Capacitance, C_{IN}[4]	2	2	pF typ	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} − 0.2	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±2.5	±2.5	µA max	
Floating-State Output Capacitance[4]	4.5	4.5	pF typ	
Output Coding	Straight (natural) binary			
CONVERSION RATE				
Conversion Time	208	208	ns max	10 SCLK cycles with SCLK at 48 MHz
Track-and-Hold Acquisition Time[3]	60	60	ns min	
Throughput Rate	4	4	MSPS max	SCLK at 48 MHz

Parameter	A Grade[1, 2]	B Grade[1, 2]	Unit	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	2.35/3.6	2.35/3.6	V min/max	
I_{DD}				Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	0.5	0.5	mA typ	V_{DD} = 3.6 V, SCLK on or off
Normal Mode (Operational)	5.5	5.5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 3 MSPS
	3.5	3.5	mA typ	V_{DD} = 3 V
Partial Power-Down Mode (Static)	34	34	µA typ	
Full Power-Down Mode (Static)	2	2	µA max	−40°C to +85°C, typically 0.1 µA
	10	10	µA max	+85°C to +125°C
Power Dissipation[5]				
Normal Mode (Operational)	19.8	19.8	mW max	V_{DD} = 3.6 V, f_{SAMPLE} = 3 MSPS
	10.5	10.5	mW typ	V_{DD} = 3 V
Partial Power-Down	102	102	µW typ	V_{DD} = 3 V
Full Power-Down	7.2	7.2	µW max	V_{DD} = 3.6 V, −40°C to +85°C

[1] Temperature range from −40°C to +125°C.
[2] Typical specifications are tested with V_{DD} = 3 V and at 25°C.
[3] See the Terminology section.
[4] Guaranteed by characterization.
[5] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS—AD7276/AD7277/AD7278

V_{DD} = 2.35 V to 3.6 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1]

Table 5.

Parameter[2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCLK}[3]	500	kHz min[4]	
	48	MHz max	B grade
	16	MHz max	Y grade
$t_{CONVERT}$	14 × t_{SCLK}		AD7276
	12 × t_{SCLK}		AD7277
	10 × t_{SCLK}		AD7278
t_{QUIET}	4	ns min	Minimum quiet time required between the bus relinquish and the start of the next conversion
t_1	3	ns min	Minimum $\overline{CS}$ pulse width
t_2	6	ns min	$\overline{CS}$ to SCLK setup time
t_3[5]	4	ns max	Delay from $\overline{CS}$ until SDATA three-state disabled
t_4[5]	15	ns max	Data access time after SCLK falling edge
t_5	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_7[5]	5	ns min	SCLK to data valid hold time
t_8	14	ns max	SCLK falling edge to SDATA three-state
	5	ns min	SCLK falling edge to SDATA three-state
t_9	4.2	ns max	$\overline{CS}$ rising edge to SDATA three-state
$T_{POWER-UP}$[6]	1	µs max	Power-up time from full power-down

[1] Sample tested during initial release to ensure compliance. All timing specifications given are with a 10 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used.
[2] Guaranteed by characterization. All input signals are specified with tr = tf = 2 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[3] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[4] Minimum f_{SCLK} at which specifications are guaranteed.
[5] The time required for the output to cross the V_{IH} or V_{IL} voltage.
[6] See the Power-Up Times section.

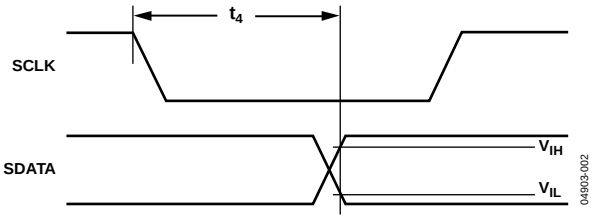

Figure 2. Access Time After SCLK Falling Edge

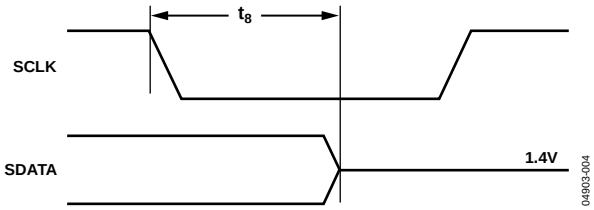

Figure 4. SCLK Falling Edge SDATA Three-State

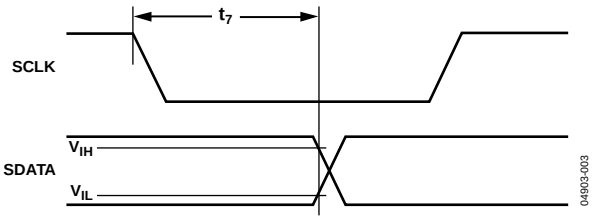

Figure 3. Hold Time After SCLK Falling Edge

TIMING EXAMPLES

For the AD7276, if $\overline{CS}$ is brought high during the 14th SCLK rising edge after the two leading zeros and 12 bits of the conversion have been provided, the part can achieve the fastest throughput rate, 3 MSPS. If $\overline{CS}$ is brought high during the 16th SCLK rising edge after the two leading zeros and 12 bits of the conversion and two trailing zeros have been provided, a throughput rate of 2.97 MSPS is achievable. This is illustrated in the following two timing examples.

Timing Example 1

In Figure 6, using a 14 SCLK cycle, f_{SCLK} = 48 MHz and the throughput is 3 MSPS. This produces a cycle time of t_2 + 12.5(1/f_{SCLK}) + t_{ACQ} = 333 ns, where t_2 = 6 ns minimum and t_{ACQ} = 67 ns.

This satisfies the requirement of 60 ns for t_{ACQ}. Figure 6 also shows that t_{ACQ} comprises 0.5(1/f_{SCLK}) + t_8 + t_{QUIET}, where t_8 = 14 ns max. This allows a value of 43 ns for t_{QUIET}, satisfying the minimum requirement of 4 ns.

Timing Example 2

The example in Figure 7 uses a 16 SCLK cycle, f_{SCLK} = 48 MHz, and the throughput is 2.97 MSPS. This produces a cycle time of t_2 + 12.5(1/f_{SCLK}) + t_{ACQ} = 336 ns, where t_2 = 6 ns minimum and t_{ACQ} = 70 ns. Figure 7 shows that t_{ACQ} comprises 2.5(1/f_{SCLK}) + t_8 + t_{QUIET}, where t_8 = 14 ns max. This satisfies the minimum requirement of 4 ns for t_{QUIET}.

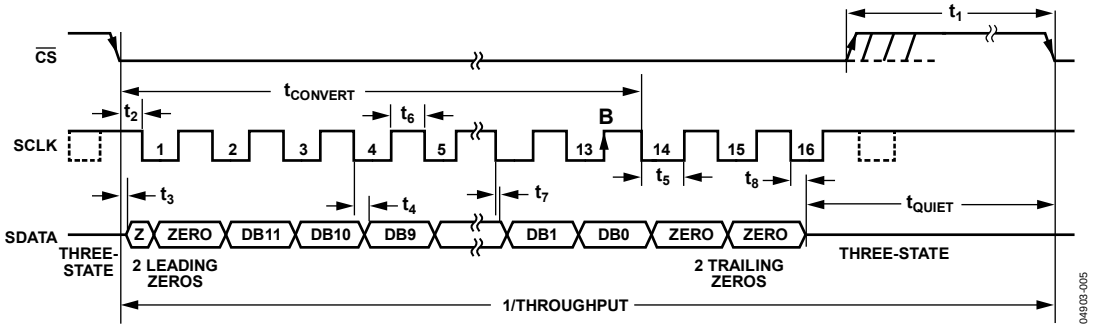

Figure 5. AD7276 Serial Interface Timing Diagram

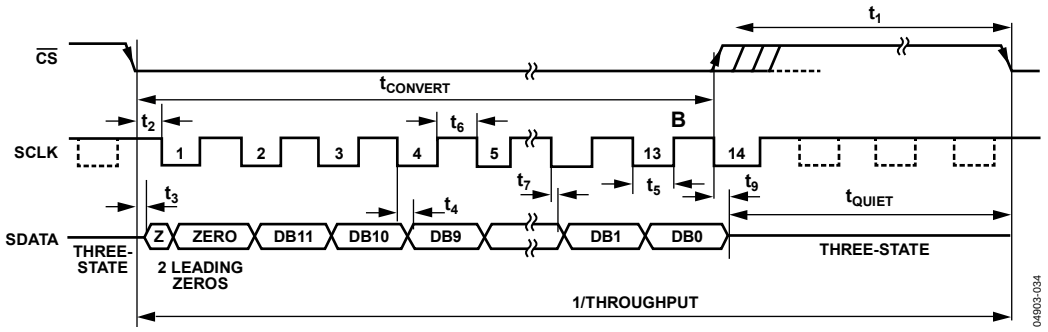

Figure 6. AD7276 Serial Interface Timing 14 SCLK Cycle

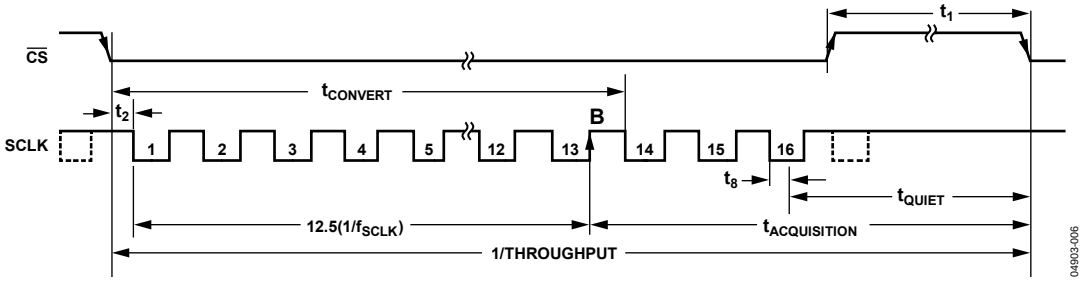

Figure 7. AD7276 Serial Interface Timing 16 SCLK Cycle

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameters	Ratings
V_{DD} to GND	−0.3 V to +6 V
Analog Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to +6 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B grade)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
6-Lead TSOT Package	
θ_{JA} Thermal Impedance	230°C/W
θ_{JC} Thermal Impedance	92°C/W
8-Lead MSOP Package	
θ_{JA} Thermal Impedance	205.9°C/W
θ_{JC} Thermal Impedance	43.74°C/W
Lead Temperature Soldering	
Reflow (10 sec to 30 sec)	255°C
Lead Temperature Soldering	
Reflow (10 sec to 30 sec)	260°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA cause SCR latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

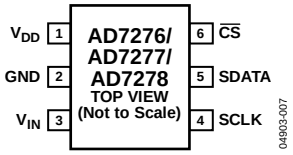

Figure 8. 6-Lead TSOT Pin Configuration

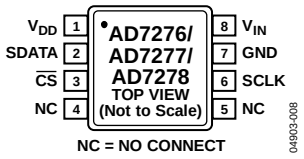

Figure 9. 8-Lead MSOP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
6-Lead TSOT	**8-Lead MSOP**	**Mnemonic**	**Description**
1	1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7276/AD7277/AD7278 is 2.35 V to 3.6 V.
2	7	GND	Analog Ground. Ground reference point for all circuitry on the AD7276/AD7277/AD7278. All analog input signals should be referred to this GND voltage.
3	8	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to V_{DD}.
4	6	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process of the AD7276/AD7277/AD7278.
5	2	SDATA	Data Out. Logic output. The conversion result from the AD7276/AD7277/AD7278 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7276 consists of two leading zeros followed by 12 bits of conversion data and two trailing zeros, provided MSB first. The data stream from the AD7277 consists of two leading zeros followed by 10 bits of conversion data and four trailing zeros, provided MSB first. The data stream from the AD7278 consists of two leading zeros followed by 8 bits of conversion data and six trailing zeros, provided MSB first.
6	3	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversion on the AD7276/AD7277/AD7278 and framing the serial data transfer.
	4, 5	NC	No Connect.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

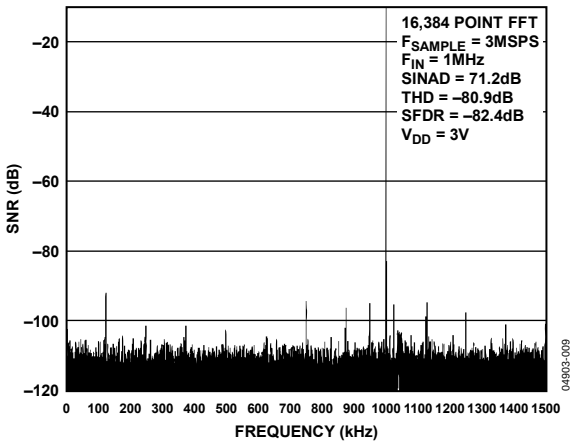

Figure 10. AD7276 Dynamic Performance at 3 MSPS, Input Tone = 1 MHz

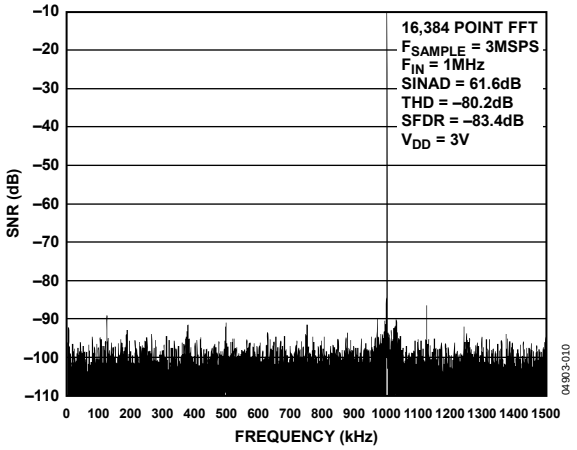

Figure 11. AD7277 Dynamic Performance at 3 MSPS, Input Tone = 1 MHz

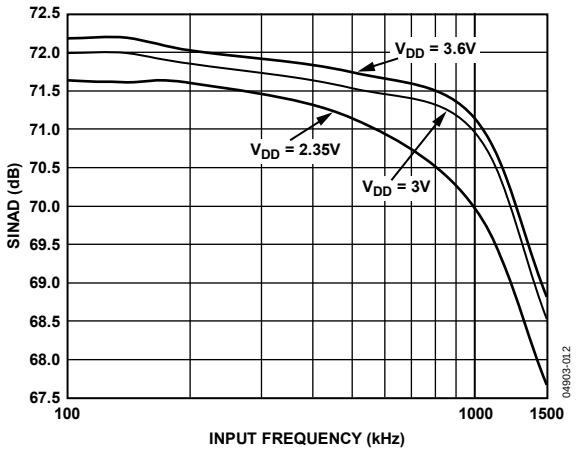

Figure 12. AD7276 SINAD vs. Analog Input Frequency at 3 MSPS for Various Supply Voltages, SCLK Frequency = 48 MHz

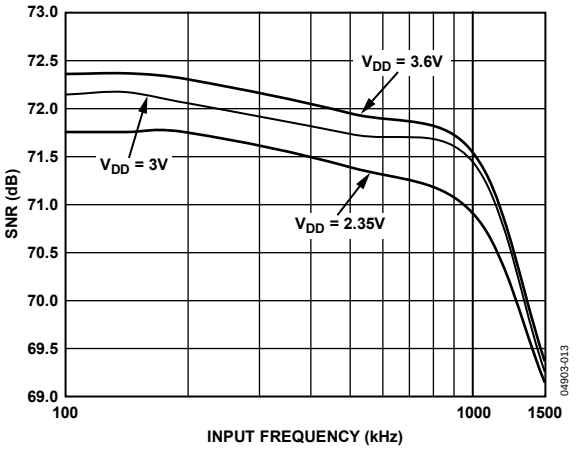

Figure 13. AD7276 SNR vs. Analog Input Frequency at 3 MSPS for Various Supply Voltages, SCLK Frequency = 48 MHz

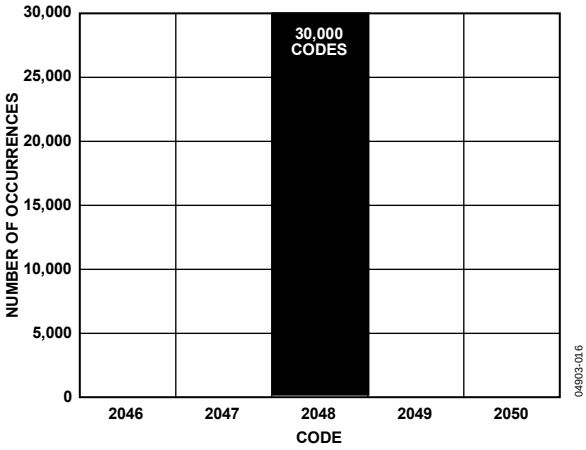

Figure 14. Histogram of Codes for 30,000 Samples

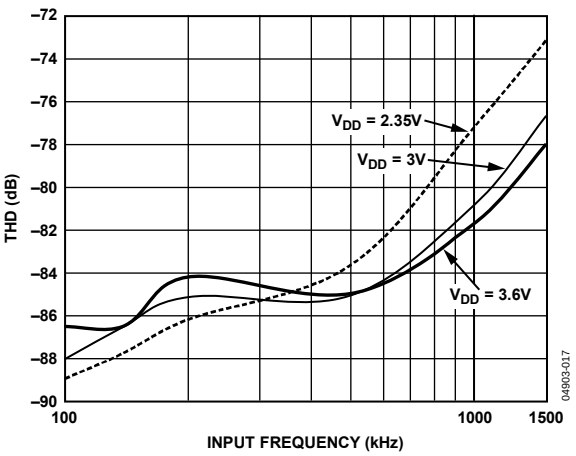

Figure 15. THD vs. Analog Input Frequency at 3 MSPS for Various Supply Voltages, SCLK Frequency = 48 MHz

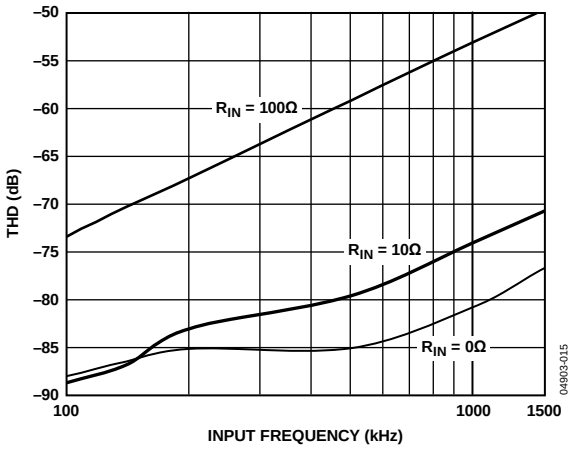

Figure 16. THD vs. Analog Input Frequency at 3 MSPS for Various Source Impedances, SCLK Frequency = 48 MHz, Supply Voltage = 3 V

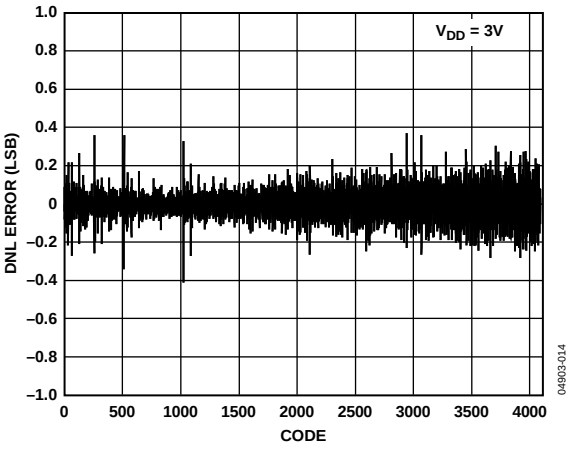

Figure 18. AD7276 DNL Performance

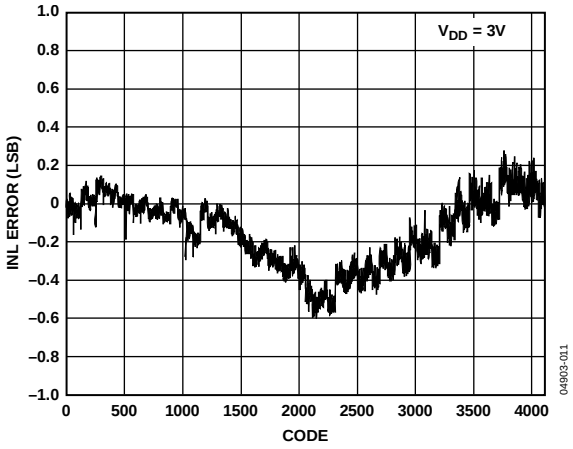

Figure 17. AD7276 INL Performance

TERMINOLOGY

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7276/AD7277/AD7278, the endpoints of the transfer function are zero scale at 0.5 LSB below the first code transition and full scale at 0.5 LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, that is, AGND + 0.5 LSB.

Gain Error
The deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal after adjusting for the offset error, that is, V_{REF} − 1.5 LSB.

Total Unadjusted Error
A comprehensive specification that includes gain, linearity, and offset errors.

Track-and-Hold Acquisition Time
The time required after the conversion for the output of the track-and-hold amplifier to reach its final value within ±0.5 LSB. See the Serial Interface section for more details.

Signal-to-Noise + Distortion Ratio (SINAD)
The measured ratio of signal to noise plus distortion at the output of the ADC. The signal is the rms amplitude of the fundamental, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), including harmonics but excluding dc. The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. For an ideal N-bit converter, the SINAD is defined as

$$SINAD = 6.02\ N + 1.76\ \text{dB}$$

According to this equation, the SINAD is 74 dB for a 12-bit converter and 62 dB for a 10-bit converter. However, various error sources in the ADC, including integral and differential nonlinearities and internal ac noise sources, cause the measured SINAD to be less than its theoretical value.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. It is defined as:

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum; however, for ADCs with harmonics buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, …. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7276/AD7277/AD7278 are tested using the CCIF standard in which two input frequencies are used (see fa and fb in the specifications). In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The intermodulation distortion is calculated in a similar manner to the THD specification, that is, the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Aperture Delay
The measured interval between the leading edge of the sampling clock and the point at which the ADC takes the sample.

Aperture Jitter
The sample-to-sample variation when the sample is taken.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7276/AD7277/AD7278 are fast, micropower, 12-/10-/8-bit, single-supply ADCs, respectively. The parts can be operated from a 2.35 V to 3.6 V supply. When operated from a supply voltage within this range, the AD7276/AD7277/AD7278 are capable of throughput rates of 3 MSPS when provided with a 48 MHz clock.

The AD7276/AD7277/AD7278 provide the user with an on-chip track-and-hold ADC and a serial interface housed in a tiny 6-lead TSOT or an 8-lead MSOP package, which offers the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part and provides the clock source for the successive approximation ADC. The analog input range is 0 V to V_{DD}. An external reference is not required for the ADC, and there is no reference on-chip. The reference for the AD7276/AD7277/AD7278 is derived from the power supply, resulting in the widest dynamic input range.

The AD7276/AD7277/AD7278 also feature a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7276/AD7277/AD7278 are successive approximation ADCs that are based on a charge redistribution DAC. Figure 19 and Figure 20 show simplified schematics of the ADC. Figure 19 shows the ADC during its acquisition phase, where SW2 is closed, SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

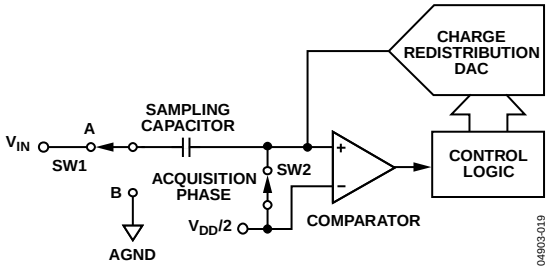

Figure 19. ADC Acquisition Phase

When the ADC starts a conversion, SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced (see Figure 20). The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code.

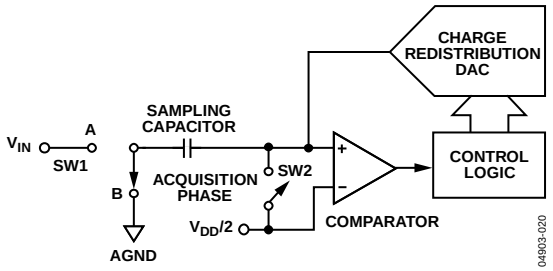

Figure 20. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7276/AD7277/AD7278 is straight binary. The designed code transitions occur midway between successive integer LSB values, such as 0.5 LSB and 1.5 LSB. The LSB size is V_{DD}/4,096 for the AD7276, V_{DD}/1,024 for the AD7277, and V_{DD}/256 for the AD7278. The ideal transfer characteristic for the AD7276/AD7277/AD7278 is shown in Figure 21.

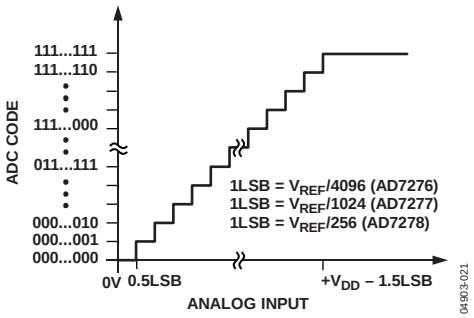

Figure 21. AD7276/AD7277/AD7278 Transfer Characteristics

TYPICAL CONNECTION DIAGRAM

Figure 22 shows a typical connection diagram for the AD7276/AD7277/AD7278. V_{REF} is taken internally from V_{DD}; therefore, V_{DD} should be decoupled. This provides an analog input range of 0 V to V_{DD}. The conversion result is output in a 16-bit word with two leading zeros followed by the 12-bit, 10-bit, or 8-bit result. The 12-bit result from the AD7276 is followed by two trailing zeros; the 10-bit and 8-bit results from the AD7277 and AD7278 are followed by four and six trailing zeros, respectively.

Alternatively, because the supply current required by the AD7276/AD7277/AD7278 is so low, a precision reference can be used as the supply source for the AD7276/AD7277/AD7278. A REF192 or REF193 voltage reference (REF193 for 3 V) can be used to supply the required voltage to the ADC (see Figure 22). This configuration is especially useful if the power supply is noisy or the system supply voltage is a value other than 3 V (for example, 5 V or 15 V). The REF192 or REF193 outputs a steady voltage to the AD7276/AD7277/AD7278. If the low dropout REF193 is used, it must supply a current of typically 1 mA to the AD7276/AD7277/AD7278. When the ADC is converting at a rate of 3 MSPS, the REF193 must supply a maximum of 5 mA to the AD7276/AD7277/AD7278.

The load regulation of the REF193 is typically 10 ppm/mA (REF193, V_S = 5 V), which results in an error of 50 ppm (150 µV) for the 5 mA drawn from it. When V_{DD} = 3 V from the REF193, it corresponds to an error of 0.204 LSB, 0.051 LSB, and 0.0128 LSB for the AD7276, AD7277, and AD7278, respectively. For applications where power consumption is of concern, use the power-down mode of the ADC and the sleep mode of the REF193 reference to improve power performance. See the Modes of Operation section.

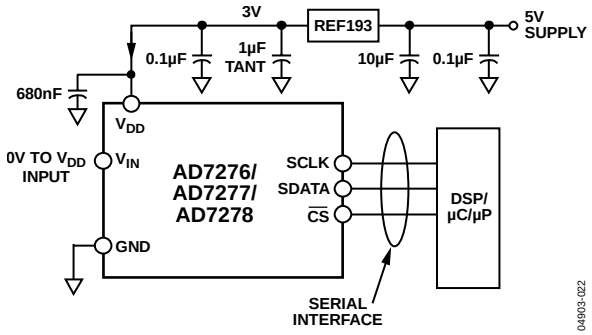

Figure 22. REF193 as Power Supply to the AD7276/AD7277/AD7278

Table 8 provides typical performance data with various references used as a V_{DD} source with the same setup conditions.

Table 8. AD7276 Performance (Various Voltage References IC)

Reference Tied to V_{DD}	SNR Performance, 1 MHz Input
AD780 @ 3 V	71.3 dB
AD780 @ 2.5 V	70.1 dB
REF193	70.9 dB

Analog Input

Figure 23 shows an equivalent circuit of the analog input structure of the AD7276/AD7277/AD7278. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. Signals exceeding this value cause these diodes to become forward biased and to start conducting current into the substrate. These diodes can conduct a maximum current of 10 mA without causing irreversible damage to the part. Capacitor C1 in Figure 23 is typically about 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 75 Ω. Capacitor C2 is the ADC sampling capacitor and has a capacitance of 4 pF typically when in hold mode and 32 pF typically when in track mode. For ac applications, removing high frequency components from the analog input signal is recommended by using a band-pass filter on the relevant analog input pin. In applications where the harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source.

Large source impedances significantly affect the ac performance of these ADCs and can necessitate the use of an input buffer amplifier. The AD8021 op amp is compatible with these devices; however, the choice of the op amp is a function of the particular application.

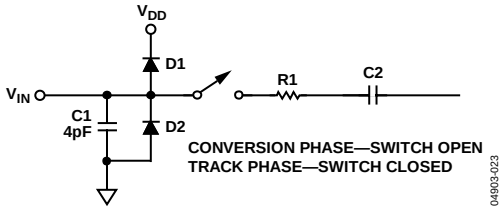

Figure 23. Equivalent Analog Input Circuit

When no amplifier is used to drive the analog input, the source impedance should be limited to a low value. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 16 shows a graph of the THD vs. the analog input frequency for different source impedances when using a supply voltage of 3 V and sampling at a rate of 3 MSPS.

Digital Inputs

The digital inputs applied to the AD7276/AD7277/AD7278 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs applied to the AD7276/AD7277/AD7278 can be 6 V and are not restricted by the V_{DD} + 0.3 V limit of the analog inputs. For example, if the AD7276/AD7277/AD7278 are operated with a V_{DD} of 3 V, then 5 V logic levels can be used on the digital inputs. However, it is important to note that the data output on SDATA still has 3 V logic levels when V_{DD} = 3 V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. For example, unlike with the analog inputs, with the digital inputs, if $\overline{CS}$ or SCLK is applied before V_{DD}, there is no risk of latch-up.

MODES OF OPERATION

The mode of operation of the AD7276/AD7277/AD7278 is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated determines which power-down mode, if any, the device enters. Similarly, if the device is already in power-down mode, $\overline{CS}$ can control whether the device returns to normal operation or remains in power-down mode. These modes of operation are designed to provide flexible power management options, which can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance because the device remains fully powered at all times, eliminating worry about power-up times. Figure 24 shows the general diagram of AD7276/AD7277/AD7278 operation in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges elapse after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high after the 10th SCLK falling edge but before the 16th SCLK falling edge, the part remains powered up, but the conversion is terminated and SDATA goes back into three-state.

For the AD7276, a minimum of 14 serial clock cycles are required to complete the conversion and access the complete conversion result. For the AD7277 and AD7278, a minimum of 12 and 10 serial clock cycles are required to complete the conversion and to access the complete conversion result, respectively.

$\overline{CS}$ can idle high until the next conversion or low until $\overline{CS}$ returns high before the next conversion (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

Partial Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required. An example of this is when either the ADC is powered down between each conversion or a series of conversions is performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7276/AD7277/AD7278 are in partial power-down mode, all analog circuitry is powered down except the bias-generation circuit.

To enter partial power-down mode, interrupt the conversion process by bringing $\overline{CS}$ high between the second and 10th falling edges of SCLK, as shown in Figure 25.

Once $\overline{CS}$ is brought high in this window of SCLKs, the part enters partial power-down mode, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and SDATA goes back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This prevents accidental power-down due to glitches on the $\overline{CS}$ line.

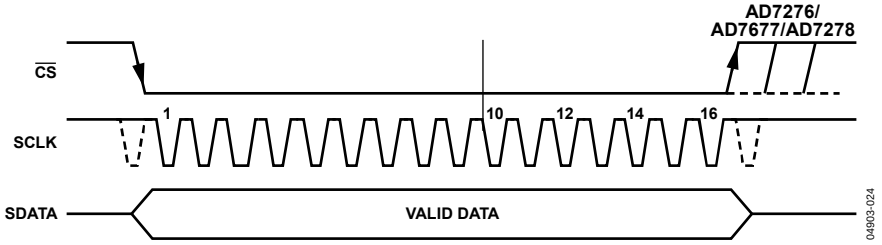

Figure 24. Normal Mode Operation

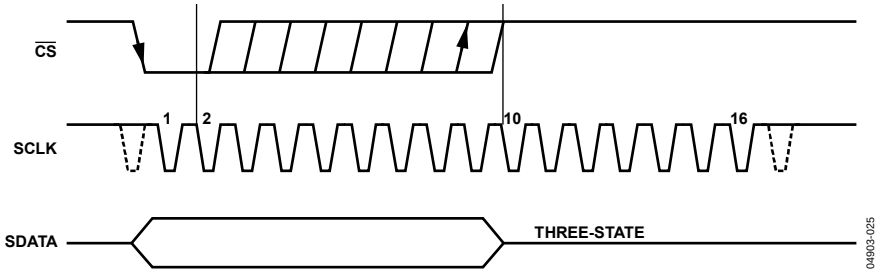

Figure 25. Entering Partial Power-Down Mode

To exit this mode of operation and power up the AD7276/AD7277/AD7278, users should perform a dummy conversion. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device is fully powered up once 16 SCLKs elapse; valid data results from the next conversion, as shown in Figure 26. If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, the AD7276/AD7277/AD7278 go into full power-down mode. Therefore, although the device can begin to power up on the falling edge of $\overline{CS}$, it powers down on the rising edge of $\overline{CS}$ as long as this occurs before the 10th SCLK falling edge.

If the AD7276/AD7277/AD7278 are already in partial power-down mode and $\overline{CS}$ is brought high before the 10th falling edge of SCLK, the device enters full power-down mode. For more information on the power-up times associated with partial power-down mode in various configurations, see the Power-Up Times section.

Full Power-Down Mode

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required because power-up from a full power-down takes substantially longer than that from a partial power-down. This mode is suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus, power down.

When the AD7276/AD7277/AD7278 are in full power-down mode, all analog circuitry is powered down. To enter full power-down mode, put the device into partial power-down mode by bringing $\overline{CS}$ high between the second and 10th falling edges of SCLK. In the next conversion cycle, interrupt the conversion process in the same way as shown in Figure 27 by bringing $\overline{CS}$ high before the 10th SCLK falling edge. Once $\overline{CS}$ is brought high in this window of SCLKs, the part powers down completely. Note that it is not necessary to complete the 16 SCLKs once $\overline{CS}$ is brought high to enter either of the power-down modes. Glitch protection is not available when entering full power-down mode.

To exit full power-down mode and to power up the AD7276/AD7277/AD7278, users should perform a dummy conversion, similar to when powering up from partial power-down mode. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The required power-up time must elapse before a conversion can be initiated, as shown in Figure 28. See the Power-Up Times section for the power-up times associated with the AD7276/AD7277/AD7278.

Power-Up Times

The AD7276/AD7277/AD7278 have two power-down modes, partial power-down and full power-down, which are described in detail in the Modes of Operation section. This section deals with the power-up time required when coming out of either of these modes.

To power up from partial power-down mode, one cycle is required. Therefore, with an SCLK frequency of up to 48 MHz, one dummy cycle is sufficient to allow the device to power up from partial power-down mode. Once the dummy cycle is complete, the ADC is fully powered up and the input signal is acquired properly. The quiet time, t_{QUIET}, must still be allowed from the point where the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{CS}$.

To power up from full power-down, approximately 1 µs should be allowed from the falling edge of $\overline{CS}$, shown in Figure 28 as $t_{POWER\ UP}$.

Note that during power-up from partial power-down mode, the track-and-hold, which is in hold mode while the part is powered down, returns to track mode after the first SCLK edge, following the falling edge of $\overline{CS}$. This is shown as Point A in Figure 26.

When power supplies are first applied to the AD7276/AD7277/AD7278, the ADC can power up in either of the power-down modes or in normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure that the part is fully powered up before attempting a valid conversion. Likewise, if the part is to be kept in partial power-down mode immediately after the supplies are applied, then two dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th SCLK falling edge; in the second cycle, $\overline{CS}$ must be brought high between the second and 10th SCLK falling edges (see Figure 25).

Alternatively, if the part is to be placed into full power-down mode when the supplies are applied, three dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th SCLK falling edge; the second and third dummy cycles place the part into full power-down mode (see Figure 27). See the Modes of Operation section.

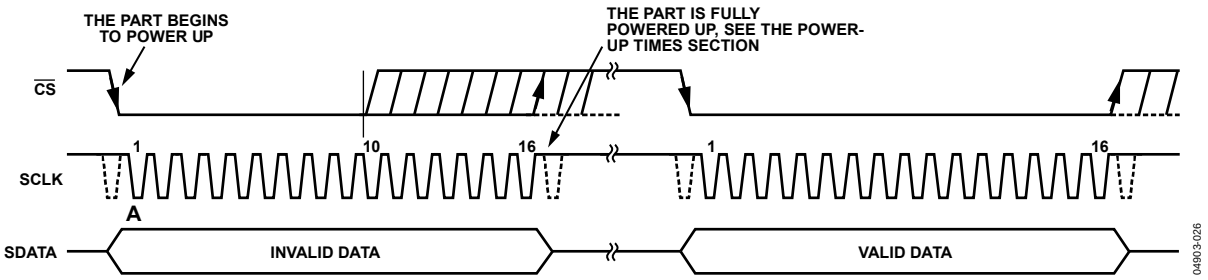

Figure 26. Exiting Partial Power-Down Mode

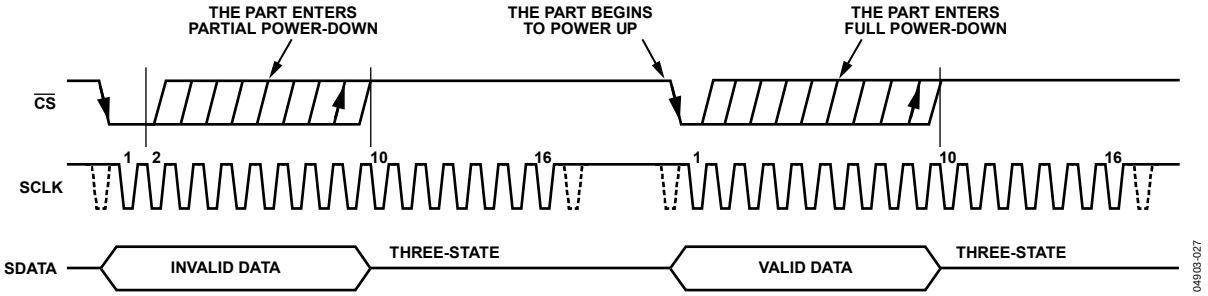

Figure 27. Entering Full Power-Down Mode

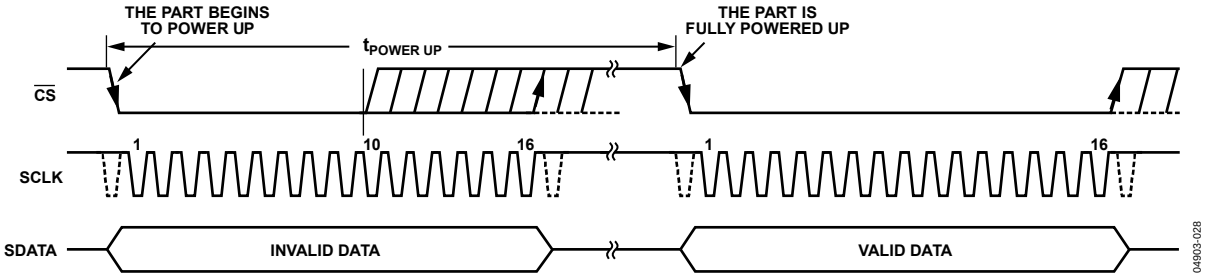

Figure 28. Exiting Full Power-Down Mode

POWER VS. THROUGHPUT RATE

Figure 29 shows the power consumption of the device in normal mode, in which the part is never powered down. By using the power-down mode of the AD7276/AD7277/AD7278 when not performing a conversion, the average power consumption of the ADC decreases as the throughput rate decreases. Figure 30 shows that as the throughput rate is reduced, the device remains in its power-down state longer, and the average power consumption over time drops accordingly. For example, if the AD7276/AD7277/AD7278 are operated in continuous sampling mode with a throughput rate of 200 kSPS and an SCLK of 48 MHz (V_{DD} = 3 V) and the devices are placed into power-down mode between conversions, then the power consumption is calculated as follows. The power dissipation during normal operation is 12.6 mW (V_{DD} = 3 V). If the power-up time is one dummy cycle, that is, 333 ns, and the remaining conversion time is 290 ns, then the AD7276/AD7277/AD7278 can be said to dissipate 12.6 mW for 623 ns during each conversion cycle. If the throughput rate is 200 kSPS, then the cycle time is 5 µs and the average power dissipated during each cycle is 623/5,000 × 12.6 mW = 1.56 mW. Figure 29 shows the power vs. throughput rate when using the partial power-down mode between conversions at 3 V. The power-down mode is intended for use with throughput rates of less than 600 kSPS, because at higher sampling rates, there is no power saving achieved by using the power-down mode.

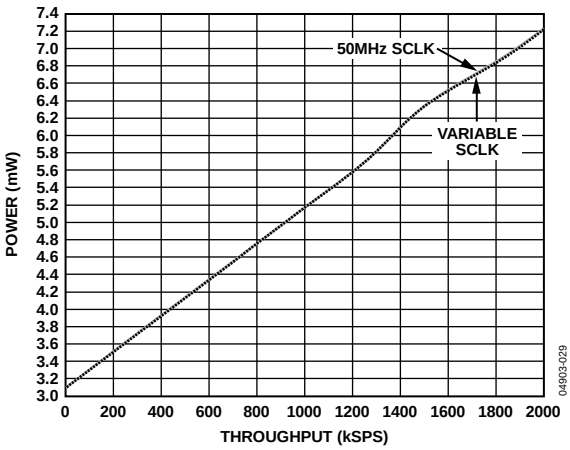

Figure 29. Power vs. Throughput Normal Mode

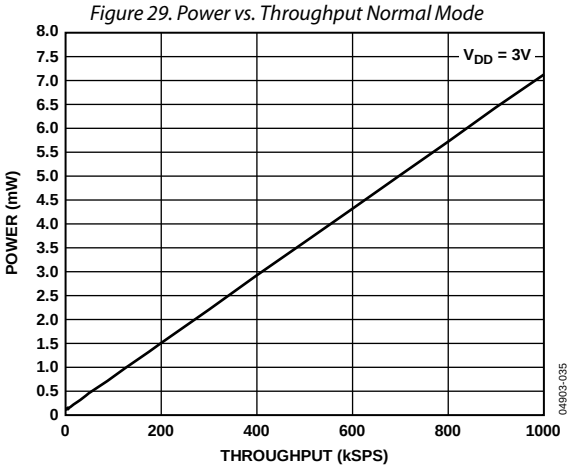

Figure 30. Power vs. Throughput Partial Power-Down Mode

SERIAL INTERFACE

Figure 31 through Figure 34 show the detailed timing diagrams for serial interfacing to the AD7276, AD7277, and AD7278. The serial clock provides the conversion clock and controls the transfer of information from the AD7276/AD7277/AD7278 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state. The analog input is sampled and the conversion is initiated at this point.

For the AD7276, the conversion requires completing 14 SCLK cycles. Once 13 SCLK falling edges have elapsed, the track-and-hold goes back into track mode on the next SCLK rising edge, as shown in Figure 31 at Point B. If the rising edge of $\overline{CS}$ occurs before 14 SCLKs have elapsed, the conversion is terminated and the SDATA line goes back into three-state. If 16 SCLKs are considered in the cycle, the last two bits are zeros and SDATA returns to three-state on the 16th SCLK falling edge, as shown in Figure 32.

For the AD7277, the conversion requires completing 12 SCLK cycles. Once 11 SCLK falling edges elapse, the track-and-hold goes back into track mode on the next SCLK rising edge, as shown in Figure 33 at Point B. If the rising edge of $\overline{CS}$ occurs before 12 SCLKs elapse, the conversion is terminated and the SDATA line goes back into three-state. If 16 SCLKs are considered in the cycle, the AD7277 clocks out four trailing zeros for the last four bits and SDATA returns to three-state on the 16th SCLK falling edge, as shown in Figure 33.

For the AD7278, the conversion requires completing 10 SCLK cycles. Once 9 SCLK falling edges elapse, the track-and-hold goes back into track mode on the next rising edge. If the rising edge of $\overline{CS}$ occurs before 10 SCLKs elapse, the part enters power-down mode.

If 16 SCLKs are considered in the cycle, then the AD7278 clocks out six trailing zeros for the last six bits and SDATA returns to three-state on the 16th SCLK falling edge, as shown in Figure 34.

If the user considers a 14 SCLK cycle serial interface for the AD7276/AD7277/AD7278, then $\overline{CS}$ must be brought high after the 14th SCLK falling edge. Then the last two trailing zeros are ignored, and SDATA goes back into three-state. In this case, the 3 MSPS throughput can be achieved by using a 48 MHz clock frequency.

$\overline{CS}$ going low clocks out the first leading zero to be read by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the second leading zero. Therefore, the first falling clock edge on the serial clock provides the first leading zero and clocks out the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, because it is clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it is possible to read data on each SCLK rising edge. In such cases, the first falling edge of SCLK clocks out the second leading zero and can be read on the first rising edge. However, the first leading zero clocked out when $\overline{CS}$ goes low is missed if read within the first falling edge. The 15th falling edge of SCLK clocks out the last bit and can be read on the 15th rising SCLK edge.

If $\overline{CS}$ goes low just after one SCLK falling edge elapses, then $\overline{CS}$ clocks out the first leading zero and can be read on the SCLK rising edge. The next SCLK falling edge clocks out the second leading zero and can be read on the following rising edge.

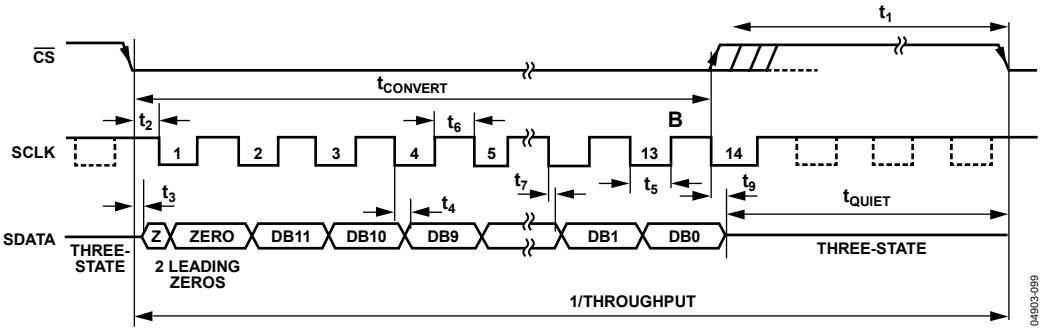

Figure 31. AD7276 Serial Interface Timing Diagram 14 SCLK Cycle

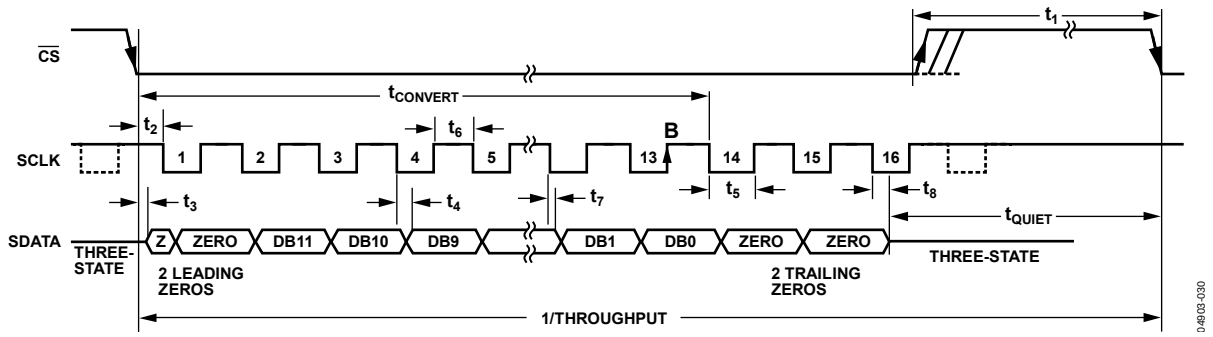

Figure 32. AD7276 Serial Interface Timing Diagram 16 SCLK Cycle

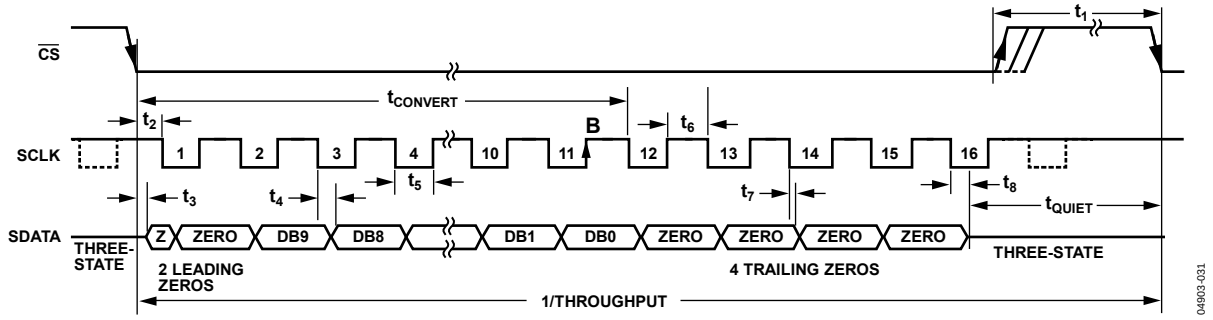

Figure 33. AD7277 Serial Interface Timing Diagram

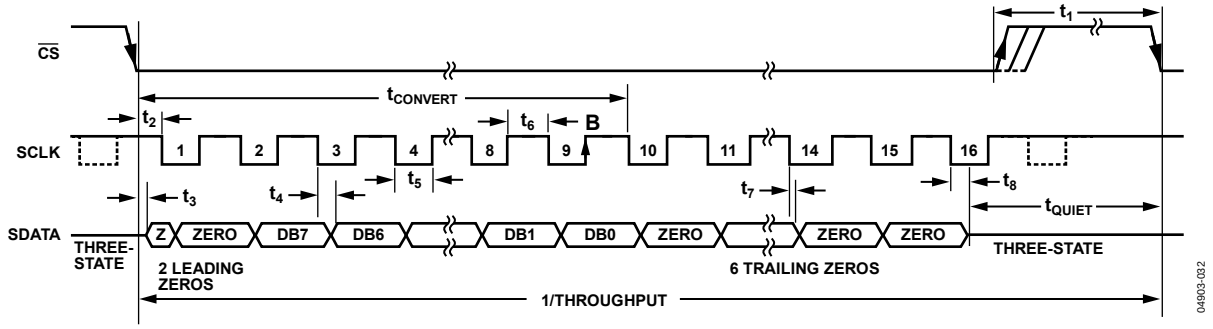

Figure 34. AD7278 Serial Interface Timing Diagram

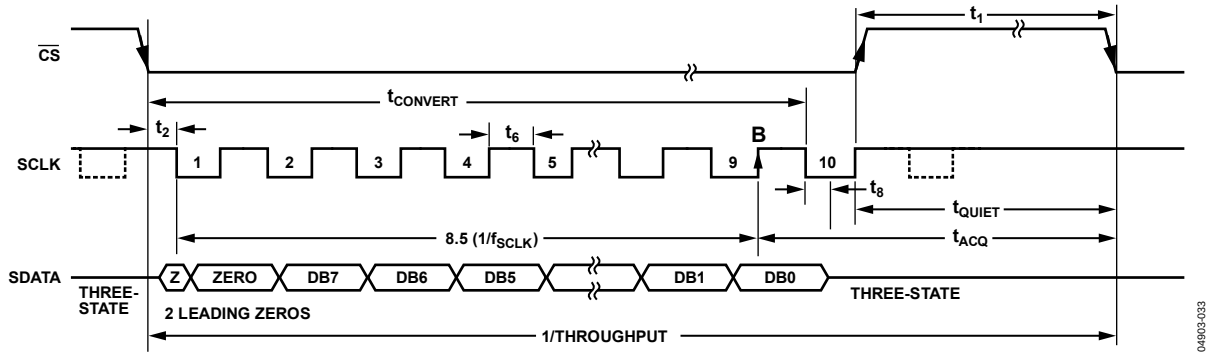

Figure 35. AD7278 in a 10 SCLK Cycle Serial Interface

AD7278 IN A 10 SCLK CYCLE SERIAL INTERFACE

For the AD7278, if $\overline{CS}$ is brought high during the 10th rising edge after the two leading zeros and eight bits of the conversion are provided, then the part can achieve a 4 MSPS throughput rate. For the AD7278, the track-and-hold goes back into track mode on the ninth rising edge. In this case, a f_{SCLK} = 48 MHz and throughput of 4 MSPS result in a cycle time of $t_2 + 8.5(1/f_{SCLK}) + t_{ACQ}$ = 250 ns, where t_2 = 6 ns minimum and t_{ACQ} = 67 ns. This satisfies the requirement of 60 ns for t_{ACQ}. Figure 35 shows that t_{ACQ} comprises $0.5(1/f_{SCLK}) + t_8 + t_{QUIET}$, where t_8 = 14 ns max. This allows a value of 43 ns for t_{QUIET}, satisfying the minimum requirement of 4 ns.

MICROPROCESSOR INTERFACING

AD7276/AD7277/AD7278 to Blackfin Processor

The Analog Devices, Inc., family of Blackfin DSPs, including the ADSP-BF531, ADSP-BF532, ADSP-BF533, ADSP-BF534, ADSP-BF535, ADSP-BF536, ADSP-BF537, ADSP-BF538, ADSP-BF538F, ADSP-BF539, and ADSP-BF539F, interfaces directly to the AD7276/AD7277/AD7278 without requiring glue logic. (These DSPs are represented by the ADSP-BF531 in Figure 36.) Set up the SPORT0 Receive Configuration 1 Register up as outlined in Table 9.

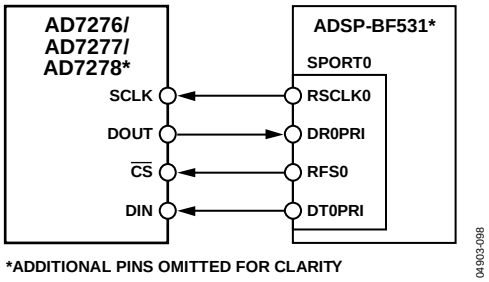

Figure 36. Interfacing with the ADSP-BF531

Table 9. The SPORT0 Receive Configuration 1 Register (SPORT0_RCR1)

Setting	Description
RCKFE = 1	Sample data with falling edge of RSCLK
LRFS = 1	Active low frame signal
RFSR = 1	Frame every word
IRFS = 1	Internal RFS used
RLSBIT = 0	Receive MSB first
RDTYPE = 00	Zero fill
IRCLK = 1	Internal receive clock
RSPEN = 1	Receive enabled
SLEN = 1111	16-bit data-word (or can be set to 1101 for 14-bit data-word)
TFSR = RFSR = 1	

To implement the power-down modes, SLEN should be set to 1001 to issue an 8-bit SCLK burst.

APPLICATION HINTS

GROUNDING AND LAYOUT

The printed circuit board that houses the AD7276/AD7277/AD7278 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates using ground planes that can easily be separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All AGND pins of the AD7276/AD7277/AD7278 should be sunk into the AGND plane. Digital and analog ground planes should be joined in one place only. If the AD7276/AD7277/AD7278 are in a system where multiple devices require an AGND-to-DGND connection, the connection should still be made at only one point, a star ground point established as close as possible to the ground pin on the AD7276/AD7277/AD7278.

Avoid running digital lines under the device because this couples noise onto the die. However, the analog ground plane should be allowed to run under the AD7276/AD7277/AD7278 to avoid noise coupling. The power supply lines to the AD7276/AD7277/AD7278 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, components with fast-switching signals, such as clocks, should be shielded with digital ground, and they should never be run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces on opposite sides of the board should run at right angles to each other. A microstrip technique is by far the best method, but it is not always possible to use this approach with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 µF ceramic capacitors in parallel with 0.1 µF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 µF capacitors should have low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic or surface-mount types of capacitors. Capacitors with low ESR and low ESI provide a low impedance path to ground at high frequencies, which allow them to handle transient currents due to internal logic switching.

EVALUATING PERFORMANCE

The recommended layout for the AD7276/AD7277/AD7278 is outlined in the evaluation board documentation. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the evaluation board controller. To demonstrate/evaluate the ac and dc performance of the AD7276/AD7277, the evaluation board controller can be used in conjunction with the AD7276/AD7277 evaluation board, as well as with many other Analog Devices evaluation boards ending in the CB designator,

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7276/AD7277. The software and documentation are on a CD shipped with the evaluation board.

OUTLINE DIMENSIONS

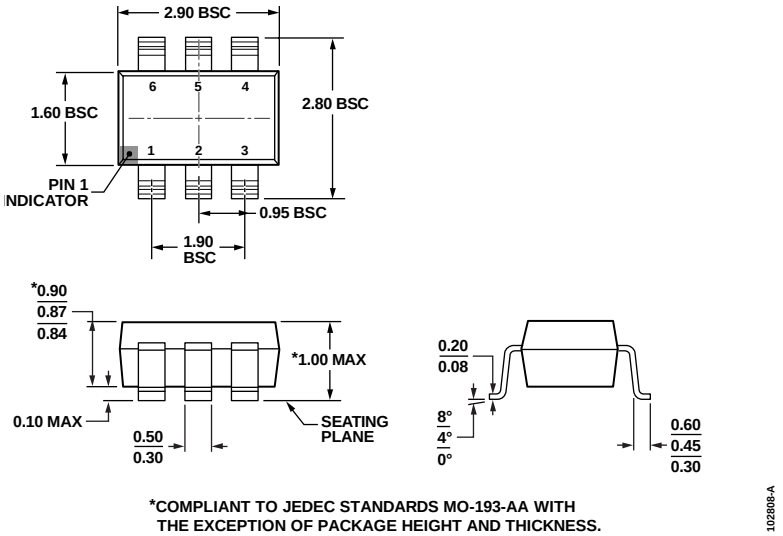

Figure 37. 6-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-6)
Dimensions shown in millimeters

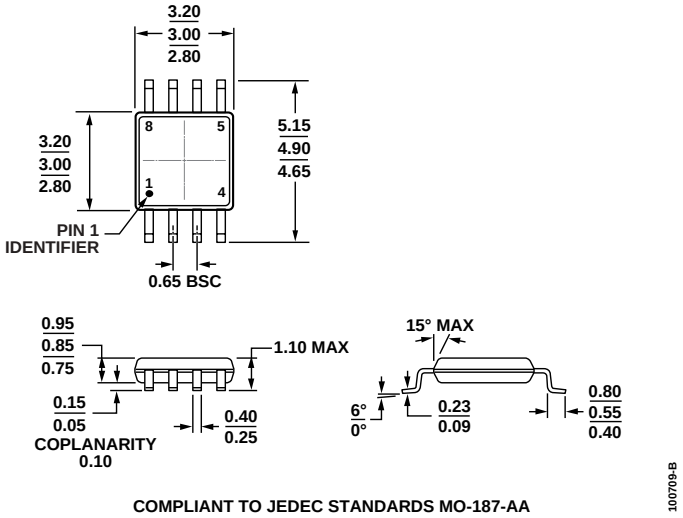

Figure 38. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Notes	Temperature Range	Linearity Error (LSB)[3]	Package Description	Package Option	Branding
AD7276BRM		−40°C to +125°C	±1 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C1W
AD7276BRMZ		−40°C to +125°C	±1 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C30
AD7276BRMZ-REEL		−40°C to +125°C	±1 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C30
AD7276BUJZ-REEL7		−40°C to +125°C	±1 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C30
AD7276BUJZ-500RL7		−40°C to +125°C	±1 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C30
AD7276YUJZ-500RL7		−40°C to +125°C	±1 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C4W
AD7276YUJZ-REEL7		−40°C to +125°C	±1 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C4W
AD7276ARMZ		−40°C to +125°C	±1.5 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C6S
AD7276ARMZ-REEL		−40°C to +125°C	±1.5 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C6S
AD7276AUJZ-500RL7		−40°C to +125°C	±1.5 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C6S
AD7276AUJZ-REEL7		−40°C to +125°C	±1.5 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C6S
AD7277BRMZ		−40°C to +125°C	±0.5 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C31
AD7277BRMZ-REEL		−40°C to +125°C	±0.5 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C31
AD7277BUJZ-500RL7		−40°C to +125°C	±0.5 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C31
AD7277BUJZ-REEL7		−40°C to +125°C	±0.5 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C31
AD7277ARMZ		−40°C to +125°C	±0.5 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C6T
AD7277ARMZ-RL		−40°C to +125°C	±0.5 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C6T
AD7277AUJZ-500RL7		−40°C to +125°C	±0.5 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C6T
AD7278BRMZ		−40°C to +125°C	±0.3 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C32
AD7278BRMZ-REEL		−40°C to +125°C	±0.3 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C32
AD7278BUJZ-500RL7		−40°C to +125°C	±0.3 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C32
AD7278BUJZ-REEL7		−40°C to +125°C	±0.3 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C32
AD7278ARMZ		−40°C to +125°C	±0.3 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C6U
AD7278ARMZ-RL		−40°C to +125°C	±0.3 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C6U
AD7278AUJZ-500RL7		−40°C to +125°C	±0.3 max	6-Lead Thin Small Outline Transistor Package (TSOT)	UJ-6	C6U
EVAL-AD7276SDZ				Evaluation Board		
EVAL-CONTROL BRD2				Control Board		

[1] Z = RoHS Compliant Part.
[2] For Y grade devices, f_{SAMPLE} = 1 MSPS.
[3] Linearity error refers to integral nonlinearity.

NOTES

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D04903-0-7/15(D)

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