# **BUK9M6R7-40H**

N-channel 40 V, 6.7 mΩ logic level MOSFET in LFPAK33
29 January 2019 Product data sheet

## 1. General description

Automotive qualified logic level N-channel MOSFET in an LFPAK33 package using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101 for use in high performance automotive applications.

### 2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Trench 9 superjunction technology:
  - · Low power losses, high power density
- · LFPAK copper clip package technology:
  - · High robustness and reliability
  - · Gull wing leads for high manufacturability and AOI
- Repetitive avalanche rated

## 3. Applications

- 12 V automotive systems
- · Powertrain, chassis, body and infotainment applications
- · Medium/Low power motor drive
- · DC-DC systems
- LED lighting

### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	40	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	-	50	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	65	W
Static characte	eristics						
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 11		3.8	5.5	6.7	mΩ
Dynamic chara	cteristics				•		
$Q_{GD}$	gate-drain charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; Fig. 13; Fig. 14		-	2.5	5	nC
Source-drain diode							
Q <sub>r</sub>	recovered charge	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 ^{\circ}\text{C}$		-	16	-	nC



Symbol	Parameter	Conditions	Min	Тур	Max	Unit
S		$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 17$	-	0.6	-	

<sup>[1] 50</sup>A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

#### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		D -
2	S	source		
3	S	source		G (F)
4	G	gate		mbb076 S
mb	D	Mounting base; connected to drain	1 2 3 4 LFPAK33 (SOT1210	<b>)</b>

## 6. Ordering information

### **Table 3. Ordering information**

Type number	Package	ackage					
	Name	Description	Version				
BUK9M6R7-40H	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210				

## 7. Marking

## Table 4. Marking codes

Type number	Marking code
BUK9M6R7-40H	96H740

## 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit	
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	40	V	
$V_{GS}$	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C		-10	16	V	
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	65	W	
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	50	А	
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>		-	50	А	
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 °C$ ; Fig. 3		-	282	А	
T <sub>stg</sub>	storage temperature			-55	175	°C	
Tj	junction temperature			-55	175	°C	
Source-drain o	Source-drain diode						

Symbol	Parameter	Conditions		Min	Max	Unit
Is	source current	T <sub>mb</sub> = 25 °C		-	50	А
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$		-	282	А
Avalanche rugg	edness					
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 50 A; $V_{sup} \le 40$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[2] [3]	-	28	mJ

- [1] 50A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.

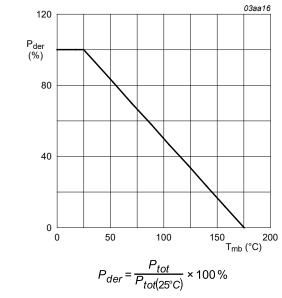
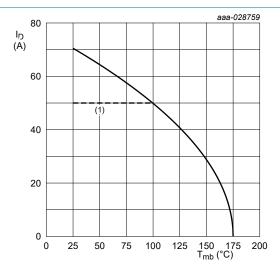


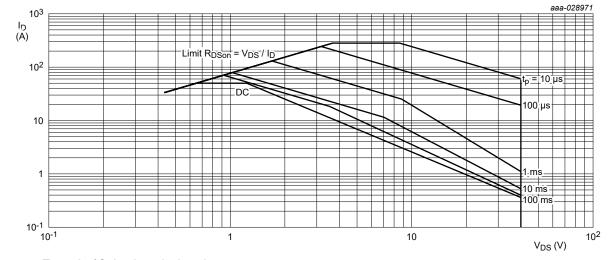
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V<sub>GS</sub> ≥ 10 V

(1) 50A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

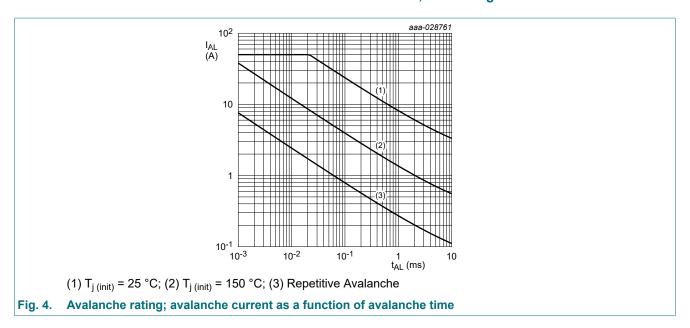


T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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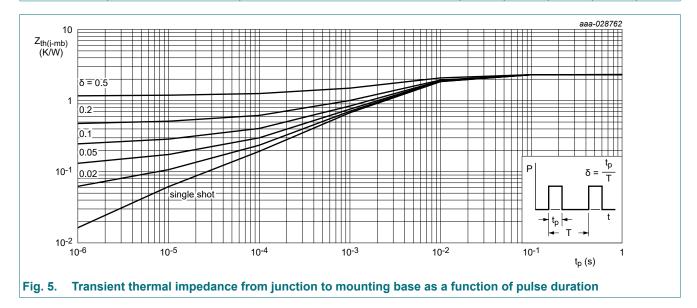
### N-channel 40 V, 6.7 m $\Omega$ logic level MOSFET in LFPAK33



## 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. 5	-	2.09	2.32	K/W



## 10. Characteristics

**Table 7. Characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static chara	cteristics		•		·		
V <sub>(BR)DSS</sub>	drain-source	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		40	43	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 ^{\circ}C$		-	40.5	-	V

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	36	40	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 1 \text{ mA; } V_{DS} = V_{GS}; T_j = 25 \text{ °C; } Fig. 9; Fig. 10$	1.45	1.77	2.15	V
	-	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>i</sub> = -55 °C; <u>Fig. 10</u>	-	-	2.6	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; Fig. 10	0.7	-	-	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	5	μΑ
		V <sub>DS</sub> = 16 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 125 °C	-	0.51	10	μΑ
		V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	44	500	μΑ
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -10 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_{D}$ = 20 A; $T_{j}$ = 25 °C; Fig. 11	3.8	5.5	6.7	mΩ
		$V_{GS}$ = 10 V; $I_D$ = 20 A; $T_j$ = 105 °C; Fig. 12	5.2	8	10	mΩ
		$V_{GS}$ = 10 V; $I_D$ = 20 A; $T_j$ = 125 °C; Fig. 12	5.7	8.7	10.8	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 175 °C; Fig. 12	6.9	10.5	13	mΩ
		$V_{GS}$ = 4.5 V; $I_{D}$ = 15 A; $T_{j}$ = 25 °C; Fig. 11	4.9	7	8.6	mΩ
		$V_{GS}$ = 4.5 V; $I_D$ = 15 A; $T_j$ = 105 °C; Fig. 12	6.7	9.9	12.9	mΩ
		$V_{GS}$ = 4.5 V; $I_{D}$ = 15 A; $T_{j}$ = 125 °C; Fig. 12	7.4	10.8	13.9	mΩ
		$V_{GS}$ = 4.5 V; $I_D$ = 15 A; $T_j$ = 175 °C; Fig. 12	9	13	16.7	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	0.3	0.8	1.9	Ω
Dynamic ch	aracteristics			'		
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; Fig. 13; Fig. 14	-	22	31	nC
		I <sub>D</sub> = 20 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V;	-	10	14	nC
Q <sub>GS</sub>	gate-source charge	Fig. 13; Fig. 14	-	4.1	6.2	nC
Q <sub>GD</sub>	gate-drain charge	1	-	2.5	5	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	-	1467	2054	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	-	390	546	pF
C <sub>rss</sub>	reverse transfer capacitance	-	-	59	130	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 20 \text{ V}; R_L = 1 \Omega; V_{GS} = 4.5 \text{ V};$	-	15	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega$	-	21	-	ns
$t_{d(off)}$	turn-off delay time	1	-	14	-	ns
t <sub>f</sub>	fall time	1	-	10	-	ns
Source-dra	in diode					
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 20 A; V <sub>GS</sub> = 0 V; T <sub>i</sub> = 25 °C; <u>Fig. 16</u>	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C; Fig. 17	-	23	-	ns
Q <sub>r</sub>	recovered charge	$I_S = 20 \text{ A}$ ; $dI_S/dt = -100 \text{ A/µs}$ ; $V_{GS} = 0 \text{ V}$ ; $V_{DS} = 20 \text{ V}$ ; $T_i = 25 \text{ °C}$	-	16	-	nC

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
S	softness factor	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 17$	-	0.6	-	
		$I_S$ = 20 A; $dI_S/dt$ = -500 A/ $\mu$ s; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C; Fig. 17	-	0.43	-	

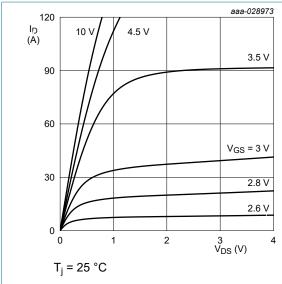


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

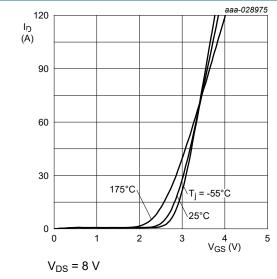


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

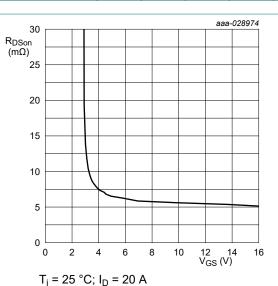


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

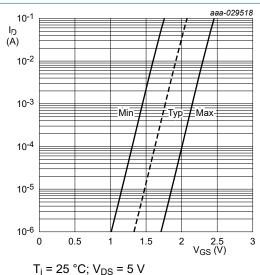


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

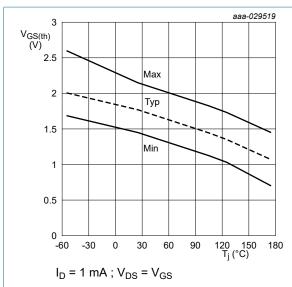


Fig. 10. Gate-source threshold voltage as a function of junction temperature

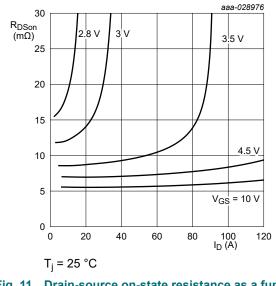


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

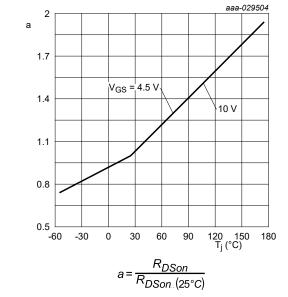


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

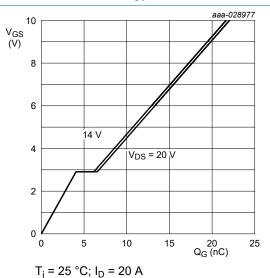


Fig. 13. Gate-source voltage as a function of gate charge; typical values

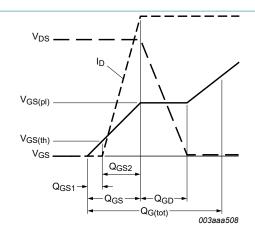
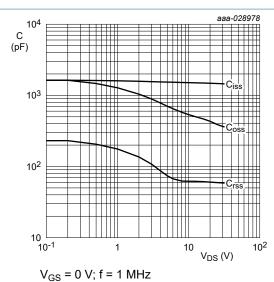


Fig. 14. Gate charge waveform definitions



VGS = 0 V, I = I WHZ

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

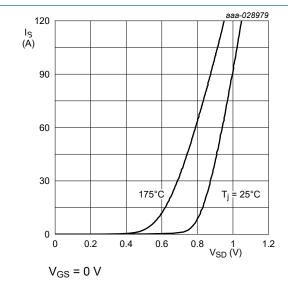


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

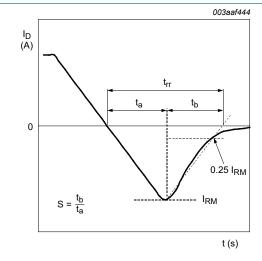


Fig. 17. Reverse recovery timing definition

## 11. Package outline

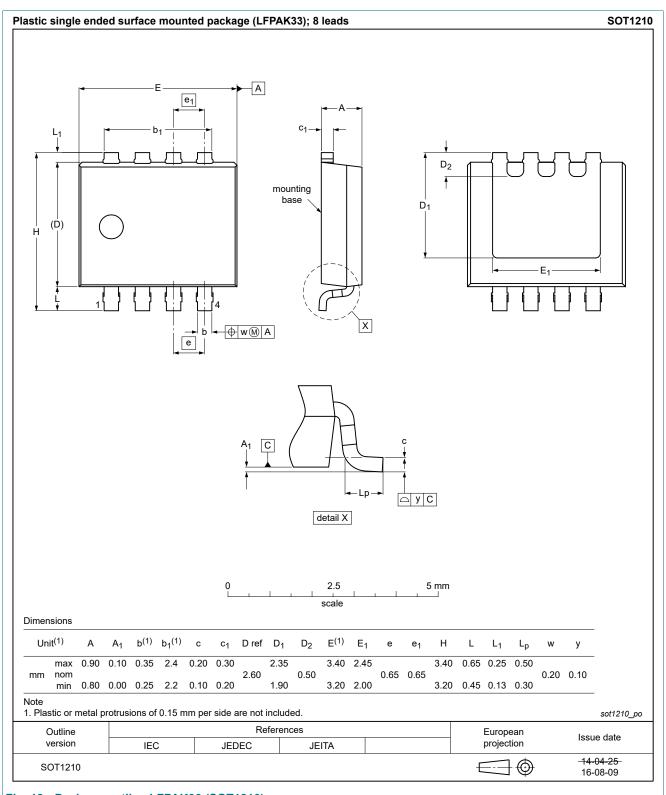


Fig. 18. Package outline LFPAK33 (SOT1210)

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Document status [1][2]	Product status [3]	Definition
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## **Contents**

1.	General description	1
2.	Features and benefits	1
3.	Applications	1
4.	Quick reference data	1
5.	Pinning information	2
6.	Ordering information	2
7.	Marking	2
8.	Limiting values	2
9.	Thermal characteristics	4
10.	. Characteristics	4
11.	Package outline	9
12.	. Legal information	10

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Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

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