MIC2155/2156

Two-Phase, Single-Output, PWM Synchronous Buck Control IC

General Description

The MIC2155 and MIC2156 are a family of two-phase, single-output synchronous buck control ICs featuring small size, high efficiency, and a high level of flexibility. The ICs implement a 500kHz (MIC2155) and 300kHz (MIC2156) voltage mode PWM control, with the outputs switching 180° out of phase. The result of the out-of-phase operation is 1MHz (or 600kHz) input ripple with ripple current cancellation, minimizing the required input filter capacitance. A 1% output voltage tolerance allows the maximum level of system performance. Internal drivers with adaptive gate drive allow the highest efficiency with the minimum external components.

Two independent enable pins and a power good output are provided, allowing a high level of control and sequencing capability.

The MIC215x family has a junction operating range from -40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

Features

- Synchronous buck control ICs with outputs switching 180° out-of-phase
- Remote sensing with internal differential amplifier
- 4.5V to 14.5V input voltage range
- Adjustable output voltages down to 0.7V
- 1% output voltage accuracy
- Starts up into a pre-biased output
- 500kHz PWM operation (MIC2155)
- 300kHz PWM operation (MIC2156)
- Adaptive gate drive allows efficiencies over 95%
- Adjustable current limit with no sense resistor
- Senses low-side MOSFET current
- Internal drivers allow 25A per phase
- Power Good output allow simple sequencing
- Dual enables with micro-power shutdown and UVLO
- Programmable soft-start pin
- Output over-voltage protection
- Works with ceramic output capacitors
- Multi-input supply capability
- Single-output high-current capability with master/slave current sharing
- External synchronization
- Small footprint 32-pin 5mm × 5mm MLF®
- Junction temperature range of -40°C to +125°C

Applications

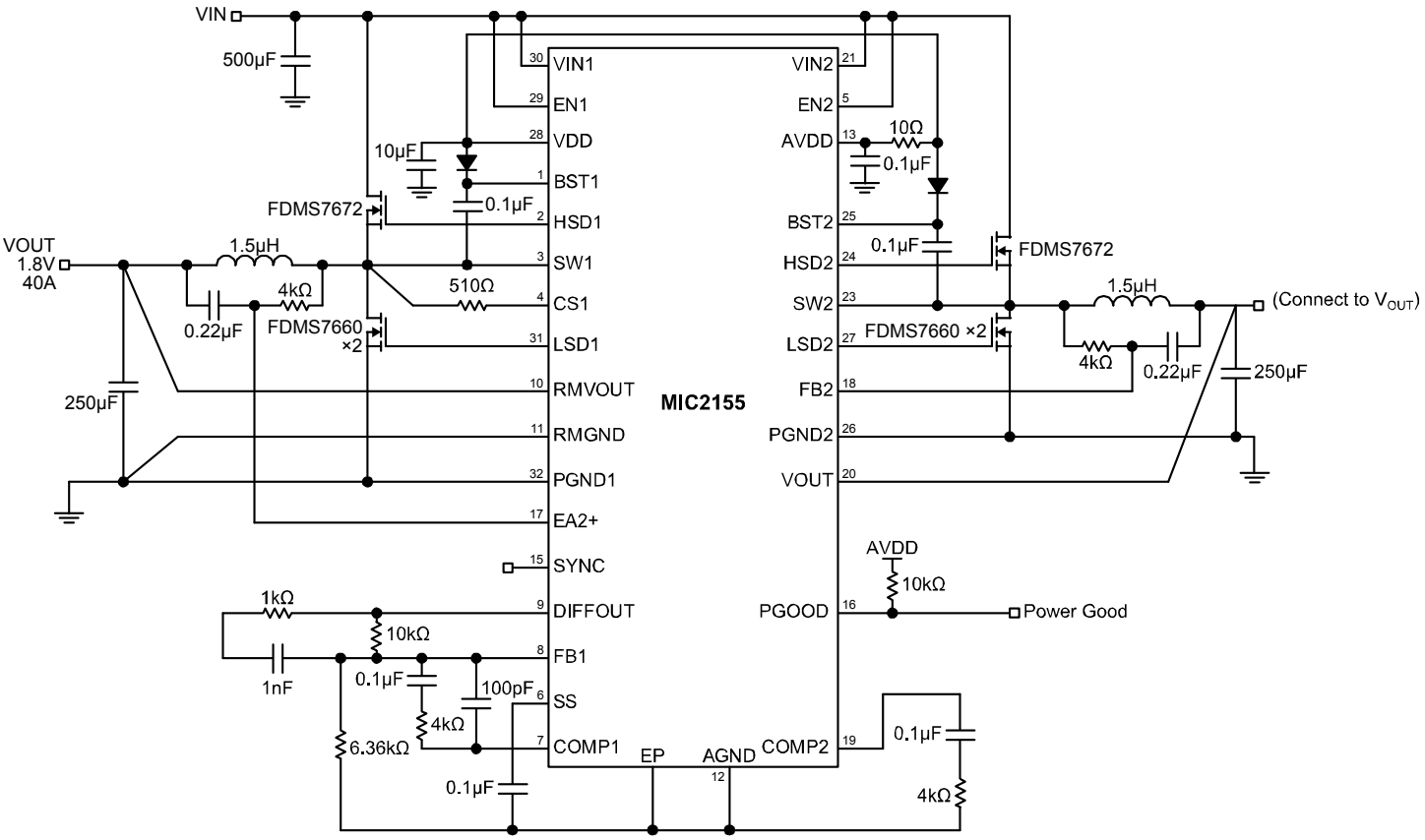
- Multi-output power supplies with sequencing
- DSP, FPGA, CPU and ASIC power supplies
- DSL modems
- Telecom and networking equipment
- Servers

Contents

Ordering Information

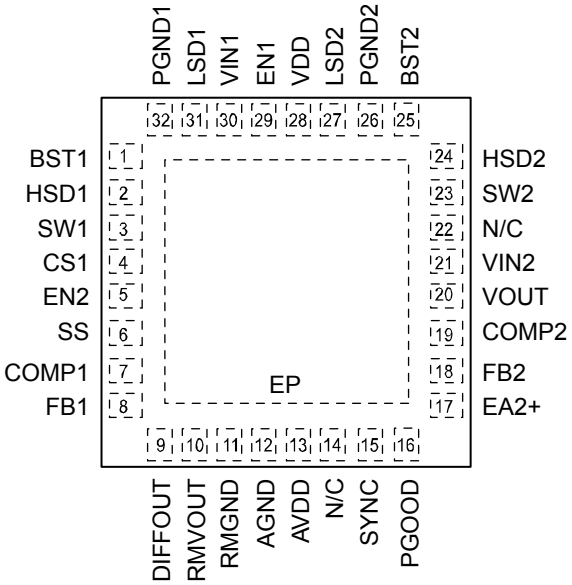
Part Number	Frequency	Voltage	Junction Temp. Range[1]	Package	Lead Finish
MIC2155YML	500kHz	Adj.	-40°C to +125°C	32-Pin 5mm × 5mm MLF	Pb-Free
MIC2156YML	300kHz	Adj.	-40°C to +125°C	32-Pin 5mm × 5mm MLF	Pb-Free

Typical Application



40A Two-Phase Converter

Pin Configuration



32-Pin MLF® (ML)

Pin Description

Pin Number	Pin Name	Pin Function
1	BST1	Boost 1 (Input): Provides voltage for high-side MOSFET driver 1. The gate drive voltage is higher than the source voltage by V_{DD} minus a diode drop.
2	HSD1	High-Side Drive 1 (Output): High-current output-driver for external high-side MOSFET.
3	SW1	Switch Node 1 (Output): Return for HSD1
4	CS1	Current Sense 1 (Input). Current-limit comparator non-inverting input. Current is sensed across the side 1 low-side FET during the off-time. Current limit is set by the resistor in series with the CS1 pin.
5	EN2	Enable 2 (Input): Channel 2 enable. Pull high to enable. Pull low to disable.
6	SS	Soft Start (Input): Controls the turn-on time of the output voltage. Active at Power-up, Enable, and Current Limit recovery.
7	COMP1	Compensation 1 (Input): Output of the internal error amplifier for Channel 1.
8	FB1	Feedback 1 (Input): Negative input to the error amplifier of Channel 1.
9	DIFFOUT	Output of remote sense differential amplifier.
10	RMVOUT	Remote V_{OUT}: Connect to V_{OUT} at the remote sense point. Input to precision differential amplifier.
11	RMGND	Remote Ground: Connect to Ground at the remote sense point. Input to precision differential amplifier.
12	AGND	Analog Ground
13	AVDD	Analog supply voltage (input). Connect to V_{DD} through an RC filter network
14	N/C	No Connect
15	SYNC	Sync (Input): Synchronizes switching to an external source. Leave floating when not used.

Pin Description cont.

Pin Number	Pin Name	Pin Function
16	PGOOD	Power Good (Output): Asserts high when voltage on the FB pin rises above Power Good threshold.
17	EA2+	(input) Positive input to Channel 2 (current sharing) Error Amplifier. Connect to Channel 1 current sense.
18	FB2	Negative Input to Channel 2 (current sharing) Error Amplifier (Input). Connect to Channel 2 current sense.
19	COMP2	Compensation 2 (Input): Pin for external compensation of Channel 2.
20	VOUT	Output Sense (input): Connect to output side of inductors. Used for current sharing.
21	VIN2	Supply Voltage for Channel 2 (Input). Used for Channel 2 UVLO circuit.
22	N/C	No Connect
23	SW2	Switch node 2 (Output): Return for HSD2.
24	HSD2	High-Side Drive 2 (Output): High-current output-driver for the high-side MOSFET.
25	BST2	Boost 2 (Input): Provides voltage for high-side MOSFET driver in Channel 2. The gate drive voltage is higher than the source voltage by V_{DD} minus a diode drop.
26	PGND2	Power Ground 2. High current return for low-side driver 2.
27	LSD2	Low-Side Drive 2 (Output): High-current driver output for Channel 2 low-side external MOSFET.
28	VDD	5V Internal Linear Regulator from $V_{IN}1$ (Output): V_{DD} is the ext. MOSFET gate drive supply voltage and an internal supply bus for the IC. When $V_{IN}1$ is <5V, this regulator operates in drop-out mode. Connect external bypass capacitor.
29	EN1	Enable 1 (Input): Output enable. Turns off both sides. Pull high to enable. Pull low to disable.
30	VIN1	Supply voltage Channel 1 (Input): Used for UVLO and V_{DD} circuits.
31	LSD1	Low-Side Drive 1 (Output): High-current driver output for Channel 1 low-side external MOSFET.
32	PGND1	Power Ground 1. High current return for low-side driver 1.
EPAD	EP	Exposed Pad (Power): Must make a full connection to the GND plane to maximize thermal performance of the package.

Absolute Maximum Ratings[1]

Supply Voltage (V_{IN} 1, 2) ..... -0.3V to 15V
Bootstrapped Voltage (V_{BST}) ..... V_{IN} + 6V
SS, FB1, RMV_{OUT}, RM_{GND}, A_{VDD}, Sync, EA2+, FB2, V_{OUT} ..... -0.3V to 6V
CS1, EN1, EN2 ..... -0.3V to 15V
Junction Temperature Range..... $-40°C \le T_J \le +125°C$
Ambient Storage Temperature..... -65°C to +150°C
ESD ..... 100V Machine Model
1500V Human Body Model
Lead Temperature (soldering 10sec)..... 260°C

Operating Ratings[2]

Supply Voltage (V_{IN} 1, 2)..... +4.5V to +14.5V
Output Voltage Range..... 0.7V to 3.6V
Package Thermal Resistance
5mm × 5mm MLF® (θ_{JA}) .....50°C/W
5mm × 5mm MLF® (θ_{JC}).....5°C/W

Electrical Characteristics[3]

T_J = 25°C; V_{EN} = V_{IN1} = V_{IN2} =12V; unless otherwise specified. **Bold** values indicate -40°C≤T_J≤+125°C

Parameter	Condition		Min	Typ	Max	Units
V_{IN} , V_{DD} and V_{REF} Supply						
Total Supply Current, I_{VIN1} + I_{VIN2} PWM Mode Supply Current	V_{FB} = 0.8V (both O/Ps; non-switching)			6	**10**	mA
Shutdown Current	V_{EN1} = V_{EN2} = 0V			210	**300**	µA
CH1 V_{IN} UVLO Start Voltage	V_{DD} = Open		**3.6**	4	**4.4**	V
CH1 V_{IN} UVLO Stop Voltage	V_{DD} = Open		**3.4**	3.97	**4.2**	V
CH2 V_{IN} UVLO Start Voltage	V_{DD} = Open		**2.5**	2.7	**2.9**	V
CH2 V_{IN} UVLO Stop Voltage	V_{DD} = Open		**2.3**	2.5	**2.7**	V
V_{DD} UVLO Start Voltage	V_{IN1} = V_{DD} for V_{IN} < 6V			3.6		
V_{DD} UVLO Stop Voltage	V_{IN1} = V_{DD} for V_{IN} < 6V			3.3		
V_{IN} UVLO Hysteresis	V_{DD} = open			40		mV
V_{EN} Shutdown Threshold	(Each Channel)		**0.6**	1	**1.6**	V
V_{EN} Hysteresis	(Each Channel)			30		mV
Internal Bias Voltage (V_{DD})	I_{VDD} = -75mA I_{VDD} = -50mA V_{IN} = 6V		4.9 4.9	5.25 5	5.6 5.6	V
Oscillator / PWM Section						
PWM Frequency		MIC2155 MIC2156	450 270	510 310	550 330	kHz
Sync Range	Sync Input is 2x PWM Frequency	MIC2155 MIC2156	860 500		1200 680	kHz
Sync Level			**0.5**		**3**	V
Maximum Duty Cycle (each Channel)			**80**			%
Minimum Headroom between VDD and VOUT	Required for remote sense amplifier use				**1.3**	V

Electrical Characteristics[3] cont.

T_J = 25°C; V_{EN} = V_{IN1} = V_{IN2} =12V; unless otherwise specified. **Bold** values indicate -40°C≤T_J≤+125°C

Parameter	Condition	Min	Typ	Max	Units
Minimum On-Time	(each Channel) **Note 4**		30		ns
Regulation					
CH1 Feedback Voltage Reference	(+/- 1%) (+/- 2%)	693 **686**	697	707 **714**	mV
CH1 Feedback Bias Current	VFB=0.7V		30		nA
Output Voltage Line Regulation	4.5 ≤ V_{IN} ≤ 14.5		0.08		%
Output Voltage Load Regulation			0.5		%
Output Voltage Total Regulation	4.5V ≤ V_{IN} ≤ 14.5V; 1A ≤ I_{OUT} ≤ 10A (V_{OUT} = 2.5V)		0.6		%
Channel Current Balancing					
Asynchronous Mode V_{TH} for Slave Output			10		mV
Error Amplifier (CH1)					
DC Gain			70		dB
Output Sourcing/Sinking Current			1		mA
Error Amplifier (CH2)					
DC Gain			70		dB
Transconductance			1.25		mS
Differential Amplifier					
Voltage Gain			1		
Offset Voltage		**-20**		**+20**	mV
Output Sourcing Current Range		0		500	µA
Output Over Voltage Protection					
V_{FB} Threshold	(Latches LSD High)	**106**	109	**114**	%Nom
Delay Blanking time			1		µs
Soft Start					
Internal Soft-Start Source Current		1.25 **1**	2	2.75 **3**	µA

Electrical Characteristics[3] cont.

T_J = 25°C; V_{EN} = V_{IN1} = V_{IN2} =12V; unless otherwise specified. **Bold** values indicate -40°C≤T_J≤+125°C

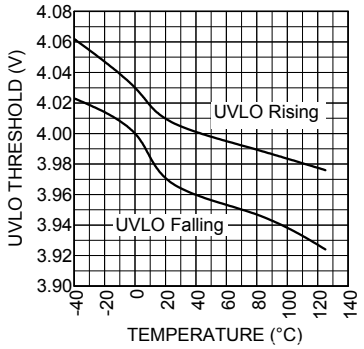
Parameter	Condition	Min	Typ	Max	Units
Current Sense					
CS Over Current Trip Point Program Current		180	195	220	µA
CS Comparator Sense Threshold	(Senses drop across low-side FET)	**-10**	0	**+10**	mV
Power Good					
V_{FB} Threshold		**86**	88.5	**91**	%Nom
PGOOD Voltage Low	V_{FB} = 0 V; I_{PGOOD} = 1mA		0.225	**0.3**	V
Gate Drivers					
Rise/Fall Time	Into 3000pF Source Sink		23 16		ns
High-Side Drive Resistance	V_{DD} = V_{IN} = 5V Source Sink		1.6 1.7	**3.5** **2.5**	Ω Ω
Low-Side Drive Resistance	V_{DD} = V_{IN} = 5V Source Sink		2 1.4	**3.5** **2.5**	Ω Ω
Driver Non-Overlap Time (adaptive)			60		ns

Notes:

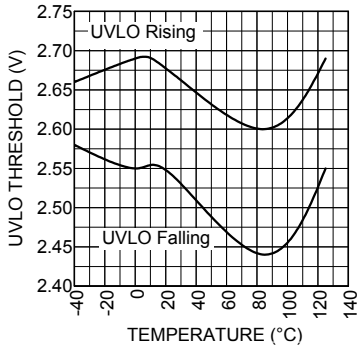
1. Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its operating ratings. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(Max)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
2. The device is not guaranteed to function outside its operating rating.
3. Specification for packaged product only.
4. Minimum on-time before automatic cycle skipping begins. See applications section.

Typical Characteristics

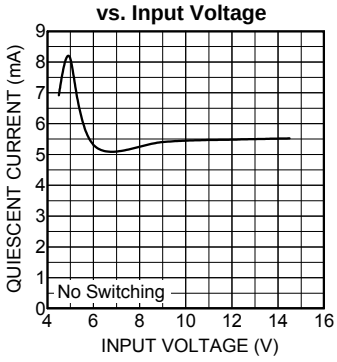
VIN1 UVLO Threshold



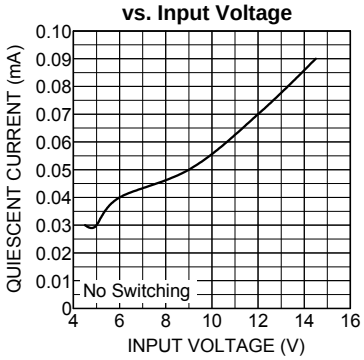
VIN2 UVLO Threshold



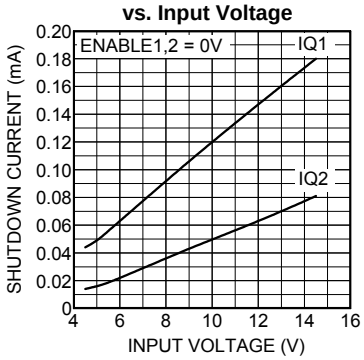
Quiescent Current 1 vs. Input Voltage



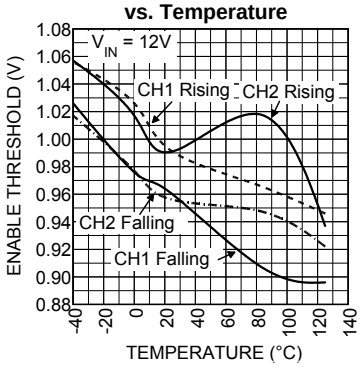
Quiescent Current 2 vs. Input Voltage



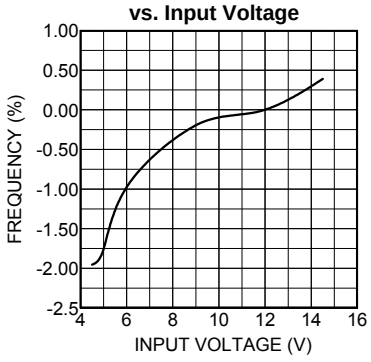
Shutdown Current vs. Input Voltage



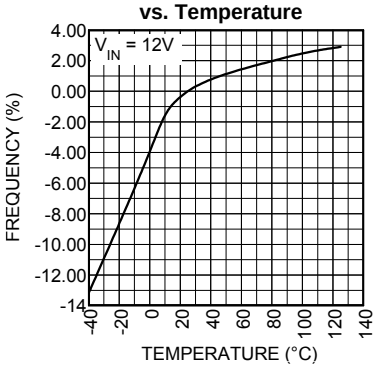
Enable Threshold vs. Temperature



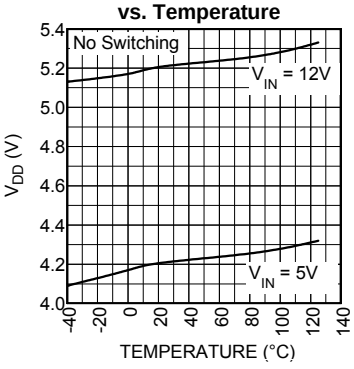
Change in Switching Frequency vs. Input Voltage



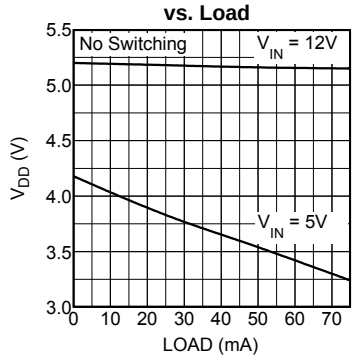
Change in Switching Frequency vs. Temperature



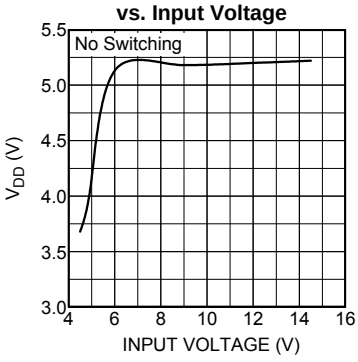
V_{DD} vs. Temperature



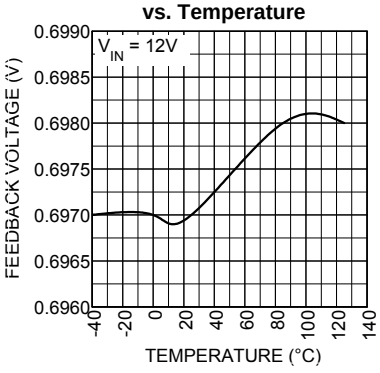
V_{DD} vs. Load



V_{DD} vs. Input Voltage

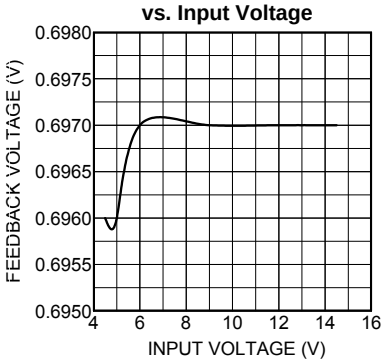


Feedback Voltage vs. Temperature

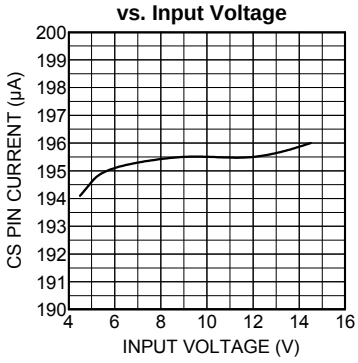


Typical Characteristics (cont.)

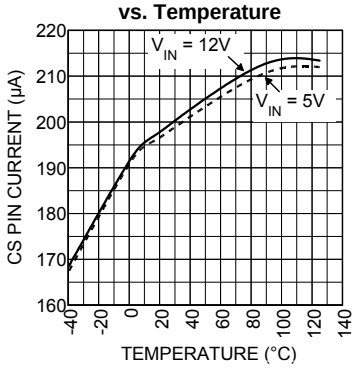
Feedback Voltage vs. Input Voltage



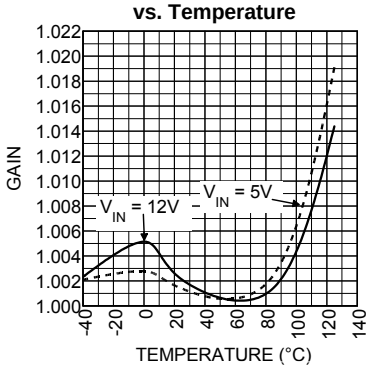
CS Pin Current vs. Input Voltage



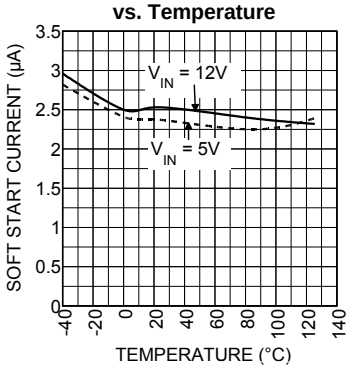
CS Pin Current vs. Temperature



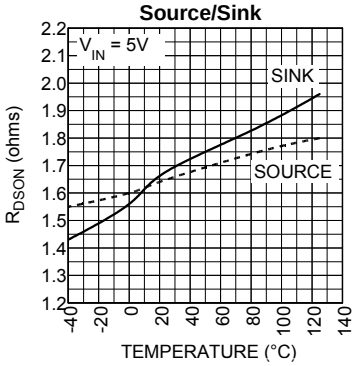
Differential Amplifier Gain vs. Temperature



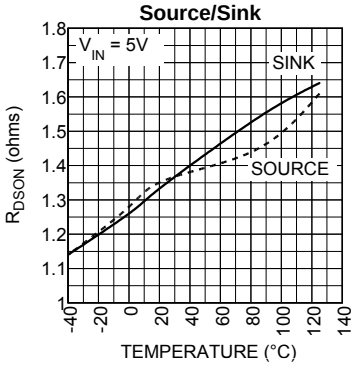
Soft Start Current vs. Temperature



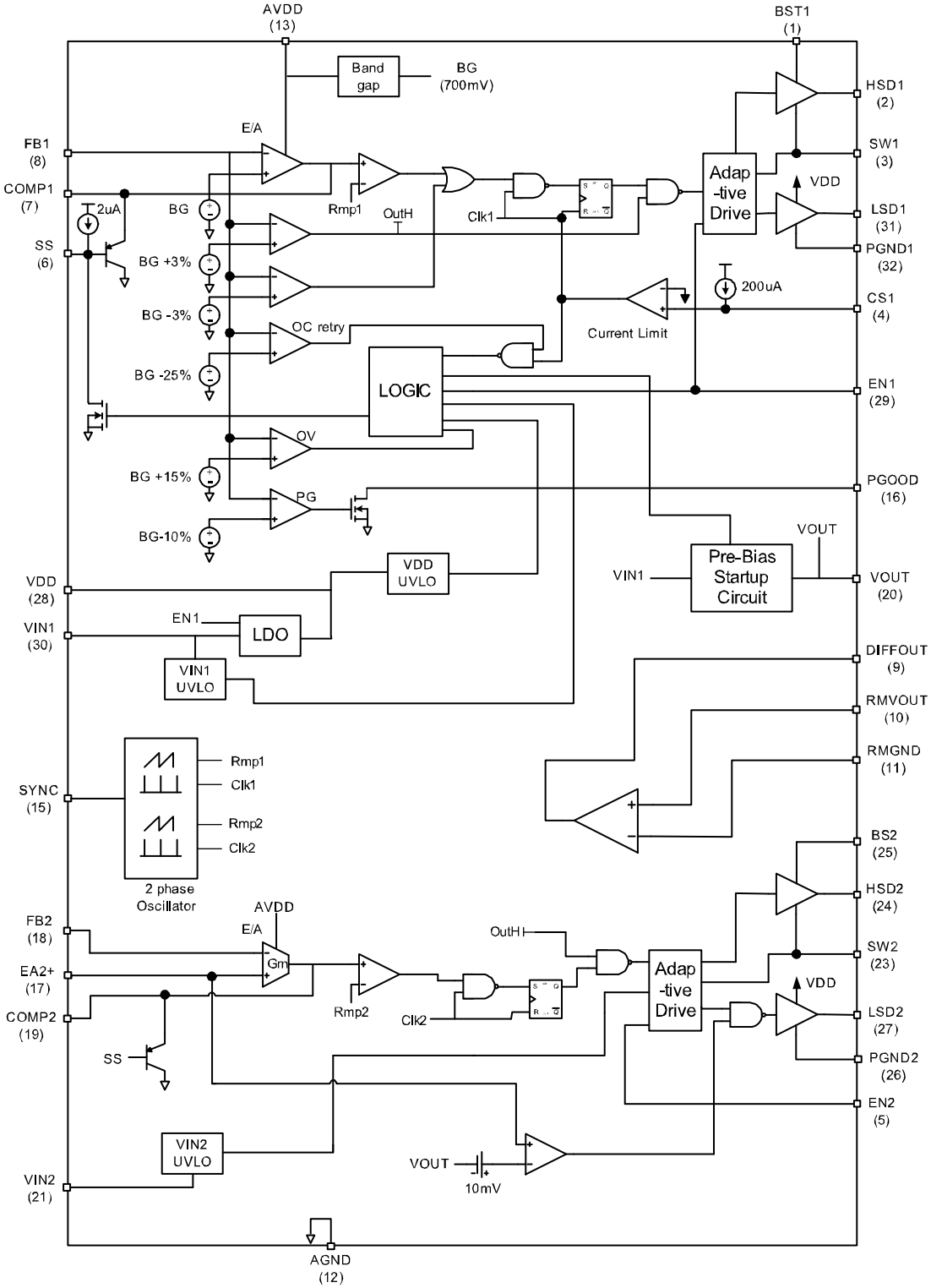
R_{DSON} High Side Drive Source/Sink



R_{DSON} LowSide Drive Source/Sink



Functional Diagram



MIC2155/6 Block Diagram

Functional Description

The MIC2155 and MIC2156 are two-phase, synchronous buck controllers operating at a fixed frequency. The two controllers differ only in switching frequency with the MIC2155 switching at 500kHz per phase (1MHz at the input and output) and the MIC2156 switches at 300kHz per phase.

Some of the advantages of multi-phase operation are:

- Smaller input and output filtering components are required because of current cancelation and higher input and output frequency.
- Faster transient response is possible with smaller output filter component values.
- Load current through each phase is one half the total output current, which allows for even heat distribution and smaller components.
- Control circuitry forces better current sharing in the MOSFETs than paralleling FETs in a single phase application.

The controller utilizes a voltage-mode control scheme (VMC). Lossless current sharing is accomplished by sensing the DC voltage across each inductor winding. Lossless overcurrent protection is performed by sensing the voltage across the low-side MOSFET on-resistance during the off-time.

Other features of the controller are:

- Overvoltage protection
- Soft start
- UVLO
- Enable
- Remote sensing
- Pre-biased output startup
- Multiple input supplies
- Power Good signal
- Frequency synchronization

Startup

A typical startup sequence is shown in **Error! Reference source not found.** (also refer to the block diagram). The enable pins are asserted after V_{IN} is applied. V_{DD} is immediately turned on and an internal FET releases the soft start pin. The soft start pin controls the error amplifier voltage. As V_{SS} ramps up, it reaches a threshold where the gate drive is enabled and the MOSFETs start to switch at a very low duty cycle. The rise of the soft start voltage controls the increase in V_{OUT} by gradually allowing the COMP1 pin voltage to rise. A 10mV offset in the current controller keeps the Channel 2 low-side drive off when the output current is low to prevent current from circulating between the phases. PGOOD is asserted when V_{OUT} reaches the PGOOD threshold.

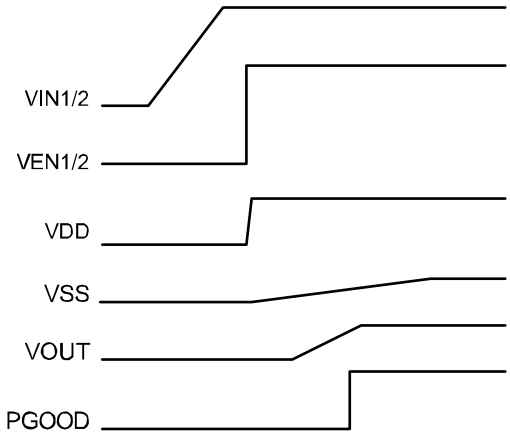


Figure 1. Startup Sequence

A typical output voltage and inductor current startup is shown in Figure 2.

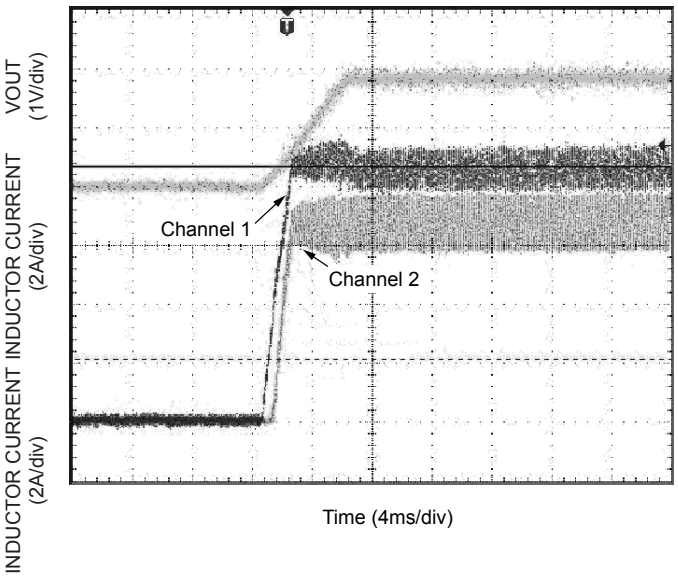


Figure 2. Turn On

Soft Start

The soft-start capacitor controls how fast the output voltage rises by controlling the COMP pin risetime. Without soft start a fast or uncontrolled turn-on requires a higher current from the input source to charge up the output capacitance.

The soft-start capacitor also controls the delay time between the enable pin assertion to when V_{OUT} starts to rise. Figures 3 and 4 show the soft-start circuitry and waveform timing.

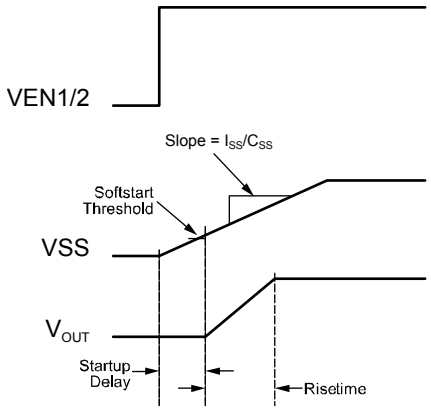


Figure 3. Soft Start Waveforms

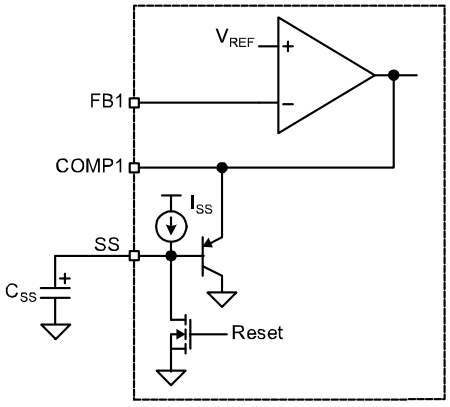


Figure 4. Soft Start Circuit

The output voltage starts to rise when V_{SS} is approximately 1 diode drop above ground, 0.6V.

The startup delay and output voltage risetime can be approximated using the formula shown below:

Delay

$$t_d = \frac{C_{SS} \times 0.6V}{I_{SS}}$$

Risetime

$$t_R = \frac{C_{SS} \times V_{OUT}}{14 \times I_{SS}}$$

The soft start pin is discharged under the following conditions:

- EN1 pin de-asserted
- UVLO on the VIN1 or VDD pins
- Overcurrent
- Overvoltage (latched off)

Enable

There is an enable pin for each of the two channels. Asserting EN1 will enable Channel 1 gate drive and release the soft start circuit. De-asserting EN1 will disable the gate drive, discharge C_{SS} and disable V_{DD}. It will bring the controller into a low current off state.

Enable 2 only controls switching of Channel 2. Disabling Channel 2 stops the switching of the power FETs on Channel 2 which reduces the V_{DD} current draw. This can improve efficiency when operating at low output current, especially when large MOSFETs are used.

Supply Voltages and Internal References

The MIC2155/6 is powered from a 4.5V to 14.5V supply. The two input supply pins (VIN1 and VIN2) are connected together in most applications. They are powered separately in configurations with two input supply voltages.

VIN1 supplies an internal LDO, which generates the VDD supply voltage. V_{DD} is used to power the gate drive circuitry and must be externally decoupled to the power ground pins (PGND1 and PGND2). A 10µF Ceramic capacitor is recommended for most applications. The AVDD pin is the supply pin for the Bandgap reference and internal analog circuits. A small RC filter (10Ω/0.1µF) connected to AVDD is recommended to help attenuate switching noise from the VDD supply.

The dropout of the internal VDD regulator causes VDD to drop if VIN1 is below 6V. When operating below 6V, VDD may be jumpered to VIN1. This bypasses the internal LDO and prevents VDD from dropping out.

An LDO or simple series pass regulator can be used to limit the VDD voltage for applications with an input voltage that spans above and below the 6V maximum V_{DD} limit. Figures 5 and 6 illustrate two examples of regulating VDD with external circuitry.

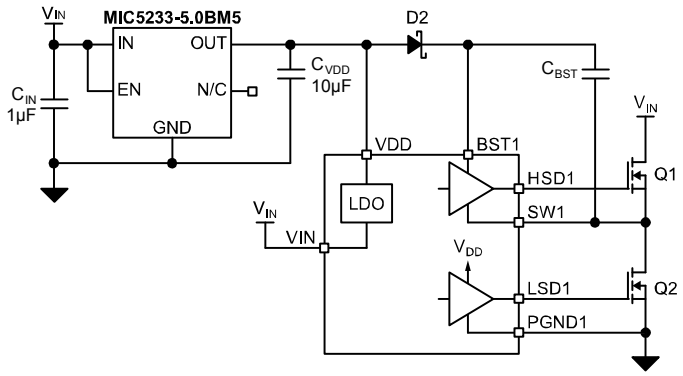


Figure 5. LDO Regulator

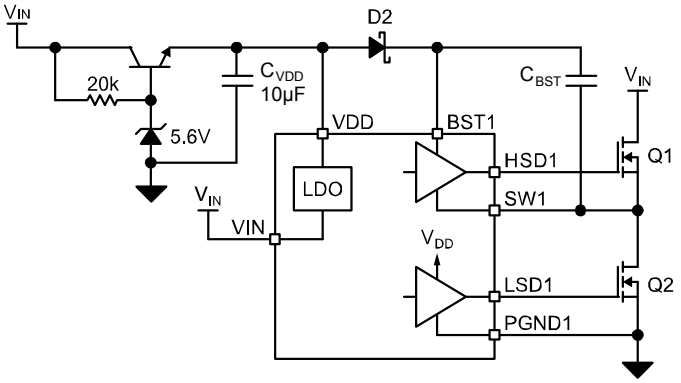


Figure 6. Emitter Follower Regulator

The internal VDD regulator can supply up to 75mA of current to drive the external MOSFETs. Power dissipation inside the MIC2155/6 control IC is divided between power dissipated in the controller's analog circuitry and power dissipated in the drive circuitry. Drive circuitry power is almost always much greater than analog circuitry power. Total regulator power dissipation is calculated using the following formula:

$$P_{DISS} = V_{IN1} \times I_{IN1} = V_{IN1} \times (f_S \times Qg + I_Q)$$

Where:

Qg = total gate charge of all MOSFETs
f_S = switching frequency of each stage (500kHz for the MIC2155 and 300kHz for the MIC2156)
I_Q = Controller quiescent current (non-switching supply current)

In some instances, power dissipation inside the control IC may limit the controller's maximum ambient temperature. For example, if the MIC2155 is powered from a 12V source and is driving 4 FETs. If each FET has a Qg=37nC, the total power dissipation in the MIC2155 is:

$$P_{DISS} = 12V \times (37nC \times 4) \times 500kHz = 0.888W$$

The maximum operating ambient temperature is:

$$T_{A(MAX)} = T_{J(MAX)} - P_{DISS} \times \theta_{JC}$$
$$T_{A(MAX)} = 125°C - 0.888W \times 50\,{}^{°C}/_{W}$$
$$T_{A(MAX)} = 81°C$$

Using an external LDO to supply VDD (as in Figure 5) can lower power dissipation in the controller and reduce junction temperature by supplying VDD externally. Using an external regulator, the power dissipated in the controller is reduced to:

$$P_{DISS} = (5V \times (37nC \times 4) \times 500kHz = 0.37W$$

Careful selection and temperature rise calculations of the external LDO should be done to prevent an excessively high LDO junction temperature.

UVLO

Separate UVLO circuits monitor VIN1, VIN2 and VDD. Switching on Channel 1 is inhibited until the voltage on the VIN1 and VDD pins is greater than their respective UVLO thresholds. The gate drive on Channel 2 is inhibited until the VIN2 pin voltage exceeds its UVLO threshold.

Individual UVLO thresholds are necessary to allow proper operation from separate input supplies. The VIN1 threshold prevents the IC from switching if the input voltage is too low to properly source the VDD voltage. The VIN2 UVLO threshold is lower than VIN1 to allow operation from a low voltage input.

Channel 1 will switch and provide a regulated output voltage even if the VIN2 UVLO prevents Channel 2 from switching.

Power Good

The power good signal asserts high when the output voltage is greater than the power good threshold. The power good circuit compares a portion of the reference voltage to the voltage on the feedback pin. The output is an open drain FET as shown in Figure 7. To assert high it must be pulled up to A_{VDD} through a resistor.

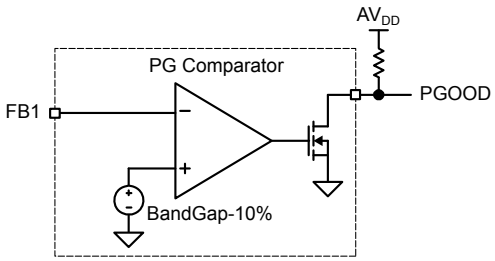


Figure 7. Power Good

The power good signal may be connected to the enable pin of other power supplies and used to sequence the other outputs.

Oscillator and Frequency Synchronization

The internal oscillator free runs at a fixed frequency and requires no external components. The oscillator generates two clock signals that are 180° out of phase with each other. This forces each channel of the controller to switch 180° out of phase, which reduces input and output ripple current.

The internal oscillator generates a clock signal and ramp signal. The clock signal terminates the switching cycle for each channel. The ramp voltage for Channel 1 is compared with the output of the error amplifier and regulates the output voltage. The ramp signal for Channel 2 is compared with the Channel 2 error amplifier output and forces the output current of Channel 2 to match Channel 1.

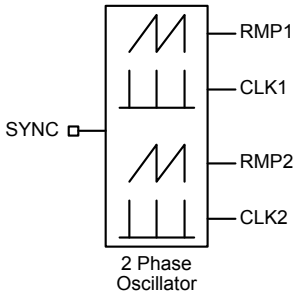


Figure 8. Oscillator and Sync Diagram

The SYNC input (pin 15) allows the MIC2155/6 to synchronize to an external clock signal. When synchronized, each channel switches at half of the synchronization frequency. Limitations on the synchronization frequency and signal amplitude are listed in the electrical characteristics section of the spec. When not used, the sync pin should be left open (no connect).

MOSFET Gate-Drive Circuitry

The high-side drive circuit is designed to switch an N-channel MOSFET. Figure 9 shows a diagram of the gate drive and bootstrap circuit. D2 and C_{BST} comprise the bootstrap circuit, which is used to supply drive voltage to the high-side FET. Bootstrap capacitor C_{BST} is charged through diode D2 while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to charge the MOSFET gate, turning on the FET. As the MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D2 is reversed biased and C_{BST} is pulled high while continuing to keep the high-side MOSFET on. The high-side drive voltage, which is derived from V_{DD}, is approximately 4.5V due the voltage drop across D2. When operating at $4.5V_{IN}$, without connecting V_{DD} to V_{IN}, the gate drive voltage to the high-side FET could be as low as 3.2V. MOSFETs with an appropriate V_{GS} threshold should be used in this situation.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge vs. V_{GS} voltage. Based on this information and a recommended ΔVHB of less than 0.1V, the minimum value of bootstrap capacitance is calculated as:

$$C_{BST} \geq \frac{Q_{GATE}}{\Delta V_{BST}}$$

Where:
Q_{GATE} = Total Gate Charge a V_{BST}
ΔV_{BST} = Voltage drop at the BST pin

A minimum value of 0.1µF is required for each of the bootstrap capacitors, regardless of the MOSFETs being driven. Larger or paralleled MOSFETs may require larger capacitance values for proper operation. Placement is critical. The bypass capacitor (C_{BST}) for the BST supply pins must be located close between the BST and SW1 pins. The etch connections should be short, wide and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the section on layout and component placement for more information.

A delay between the switching of the two MOSFETs is necessary to prevent both MOSFETs from being on at the same time and shorting V_{IN} to ground. An adaptive gate drive in the controller monitors the switch node (SW1) and low-side driver (LSD1) to minimize dead time while preventing both MOSFETs from being on at the same time. This enables the use of a broad range of MOSFETS without requiring excessive deadtime.

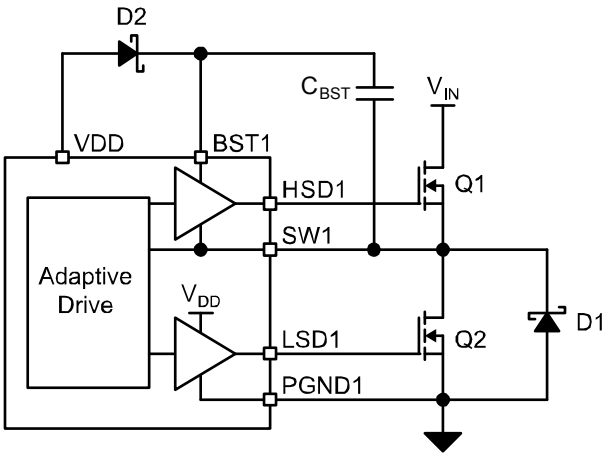


Figure 9. Gate Drive

dv/dt Induced Turn On of the Low-Side MOSFET

As the high-side MOSFET turns on, the rising dv/dt on the switch-node forces current through C_{GD} of the low-side FET causing a glitch on the FET's gate. Figure 10 illustrates the basic mechanism causing this issue. If the glitch on the gate is greater than the FET's turn-on threshold, it may cause an unwanted turn-on of the low-side FET while the high-side FET is on. A short circuit between input and ground would occur that lowers efficiency and increases power dissipation in both FETs. Additionally, turning on the low-side FET during the off-time could interfere with overcurrent sensing.

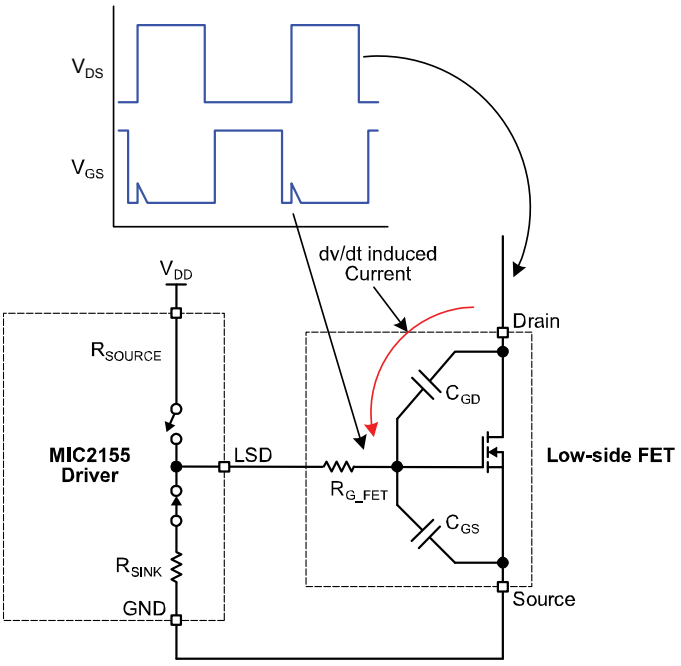


Figure 10. dv/dt Induced Turn-On

The following steps can be taken to lower the gate drive impedance, minimize the dv/dt induced current and lower the FETs susceptibility to the induced glitch:

1) Chose a MOSFET with:
   a) a high C_{GS}/C_{GD} ratio
   b) a low internal gate resistance
2) Do not put a resistor between the LSD output and the gate.
3) Insure both the gate drive and return etch are short, low inductance connections.
4) Use a 4.5V V_{GS}-rated MOSFET because its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated FET.
5) Connect V_{DD} to V_{IN} or a 5V supply if V_{IN} is below 6V. The R_{DSON} of the internal driver will be lower and a 4.5V rated MOSFET can be used.

Remote Sense

Remote sensing provides accurate output voltage regulation by sensing at the load. Remote sensing makes up for losses in the power distribution path. It uses a unity gain differential amplifier to overcome voltage drops in both the output and return (ground) paths. The amplifier has common mode input range from -0.3V to 3.6V. For proper remote sense operation, V_{IN} must be greater than 6V. If V_{IN} is less than 6V, the V_{DD} pin must be connected to V_{IN} or externally supplied with 5V.

The output of the remote sense amplifier can source up to 500µA. The voltage divider resistors (R1 and R4 in Figure 12) must be chosen to insure the output current of the amplifier does not exceed the maximum of 500µA.

$$R1_{MAX} \geq \frac{V_{OUT} - V_{REF}}{500\mu A}$$

Where:
V_{REF} = 0.7V

A gain/phase plot of the remote sense amplifier in Figure 11 shows a typical 2MHz bandwidth. Phase lag is 45° at 1MHz.

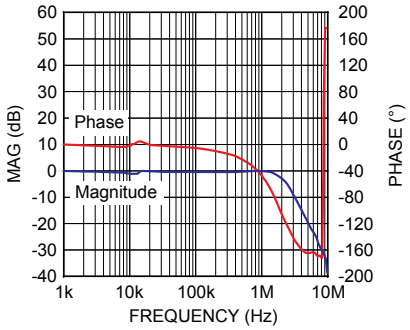


Figure 11. Remote Sense Amplifier Gain/Phase Plot

A typical remote sense configuration is shown in Figure 12. The output of the remote sense amplifier feeds a voltage divider (R1, R4), which is connected to the Channel 1 error amplifier. The divider and compensation network for the remote sense are the same as for a local sense configuration. The 10Ω resistors provide an alternate feedback path if the remote sense connections are removed or opened. The remote sense connections should not be shorted or the output voltage will increase close to V_{IN}. The OVP circuit in the controller will not protect against this type of fault since the feedback pin voltage will be 0V.

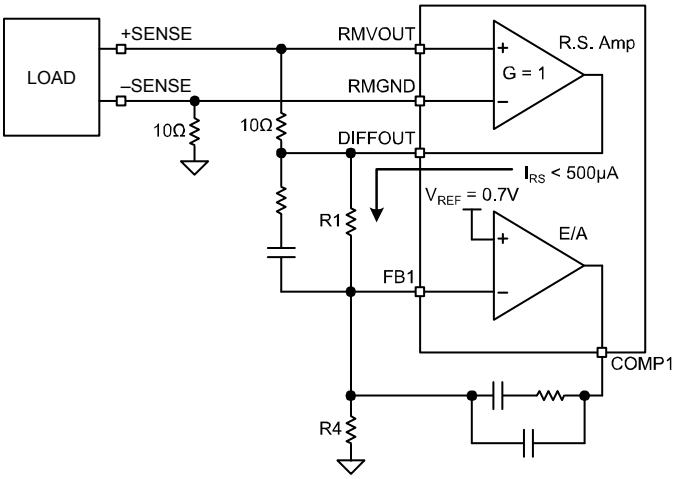


Figure 12. Remote Sense

Setting the Output Voltage

Regardless of whether the remote sensing or local output voltage sensing is used, the output voltage is set with voltage divider resistors R1 and R4 (Figure 12). The equation below is used to calculate V_{OUT}.

$$V_{OUT} = V_{REF} \times \left[1 + \frac{R1}{R4}\right]$$

Where:
V_{REF} = 0.7V

Current Limit and Overcurrent Protection

The MIC2155/6 uses the synchronous (low-side) MOSFETs R_{DSON} to sense an over current condition. The low-side MOSFET is used because it displays lower parasitic oscillations after switching then the upper MOSFET. Additionally, it improves the accuracy and reduces false tripping at lower voltage outputs and narrow duty cycles since the off-time increases as duty cycle decreases.

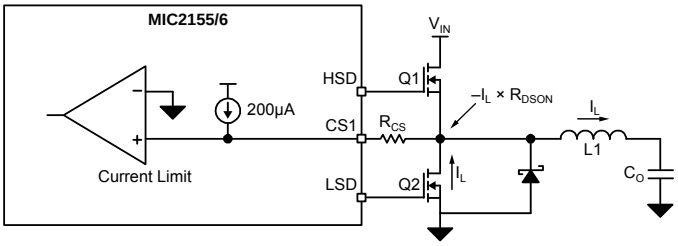


Figure 13. Overcurrent Circuit

Inductor current flows from the lower MOSFET source to the drain during the off-time. The drain voltage becomes negative with respect to ground as the inductor current continues to flow from Source to Drain. This negative voltage is proportional to instantaneous inductor current times the MOSFET R_{DSON}. The voltage across the low-side FET becomes even more negative as the output current increases. The overcurrent circuit operates by passing a known fixed current source (200µA) through a resistor R_{CS}. This sets up an offset voltage (I_{CS} × R_{CS}) that is compared to the VDS of the low-side FET. When I_{SD} (Source to Drain current) × I_L is equal to this voltage, the MIC2155's over current trigger is set, which disables the next high side gate drive pulse. After missing the high side pulse, the overcurrent (OC) trigger is reset. If on the next low-side drive cycle, the current is still too high i.e. V_{CS} is ≤ 0V, another high side pulse is missed and so on. This effectively reduces the overall energy transferred to the output and V_{OUT} starts to fall.

The MIC2155/6 current limit circuit restricts the maximum output current. If the load tries to draw additional current the output voltage drops until it is no longer within regulation limits. At this point (75% of nominal output voltage) a hiccup current mode is initiated to protect down stream loads from excessive current during hard short circuits. This helps reduce the overall power dissipation in the PWM converter components during a fault.

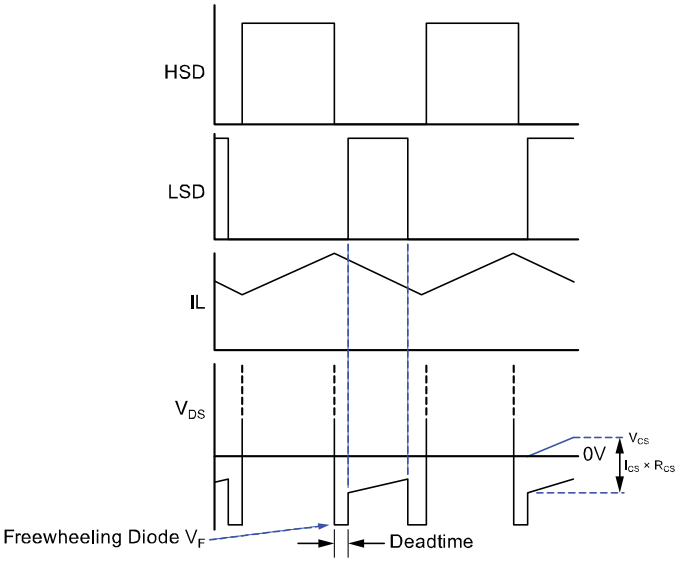


Figure 14. Overcurrent Sense Waveforms

The MIC2155/6 only senses current across the low side MOSFET of Channel 1 since both channels operate in parallel. This means the total output current limit is approximately twice the calculated current limit.

Current Limit Setting

The current limit circuit responds to the peak inductor current flowing through the low-side FET. The value of R_{CS} can be estimated with the "simple" method or can be more accurately calculated by taking the inductor ripple current into account.

The Simple Method

Current limit can be quickly estimated with the following equation:

$R_{CS} = I_{OUT}/2 \times R_{DSON(MAX)}/180\mu A$.
Where: R_{DSON} is the maximum on-resistance of the low side FET at the operating junction temperature

Accurate Method

For designs where ripple current is significant when compared to I_{OUT} or for low duty cycle operation, calculating the current setting resistor R_{CS} should take into account that we are sensing the peak inductor current and that there is a blanking delay of approximately 100ns.

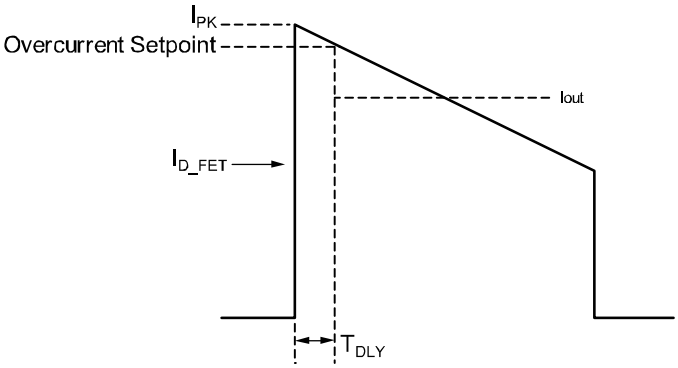


Figure 15. Overcurrent waveform

The equations to accurately calculate the current limit resistor value are shown below:

$$I_{PK} = \frac{I_{OUT}}{2} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{V_{OUT} \times (1 - D)}{F_S \times L}$$

$$I_{SET} = I_{PK} - \frac{V_{OUT} \times T_{DLY}}{L}$$

$$R_{CS} = \frac{I_{SET} \times R_{DSON(MAX)}}{I_{CS(MIN)}}$$

D = Duty Cycle
F_S = Switching Frequency
L = Power inductor value
T_{DLY} = Current limit blanking time ~ 100ns
$I_{CS(min)}$ = 180µA

Example:

Consider a 12V to 3.3V @ 30A converter with 1.5µH power inductor and 90% efficiency at full load. Each channel will supply 15A at a 500kHz (MIC2155) switching frequency. The on-resistance of the low side MOSFET is 6mΩ.

Using the simple method:

$$R_{CS} = \frac{\frac{30A}{2} \times 6m\Omega}{180\mu A} = 500\Omega$$

Using the accurate method:

$$D = \frac{V_{OUT}}{V_{IN} \times Efficiency} = \frac{3.3}{12 \times 0.9} = 0.3$$

$$I_{RIPPLE} = \frac{3.3 \times (1 - 0.3)}{500kHz \times 1.5\mu H} = 3.1A$$

$$I_{PK} = \frac{30}{2} + \frac{3.1}{2} = 16.55A$$

$$I_{SET} = 16.55 - \frac{3.3 \times 100ns}{1.5\mu H} = 16.33A$$

$$R_{CS} = \frac{16.33 \times 6m\Omega}{180\mu A} = 544\Omega$$

Using the simple method here would result in a current limit point lower than expected.

This equation sets the minimum current limit point of the converter, but maximum will depend on the actual inductor value and on resistance of the MOSFET under current limit conditions. This could be in the region of 50% higher and should be considered to ensure that all the power components are within their thermal limits unless thermal protection is implemented separately.

Inductor Current Sensing

Current sharing between the two phases is achieved by sensing the inductor current in each phase. Lossless inductor current sensing is used, which has the advantages of lower power loss and lower cost – over using a discrete resistor in series with the inductor.

The inductor sense circuit is shown in Figure 16. It extracts the voltage drop across the inductor's DC winding resistance.

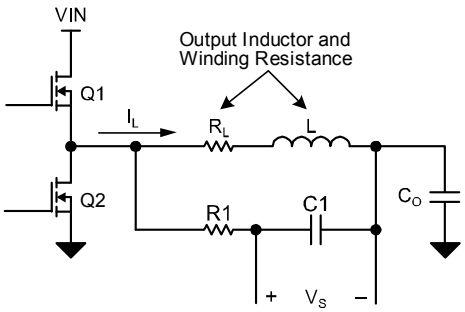


Figure 16. Lossless Inductor Current Sense

The voltage across capacitor C1 is:

$$V_S = I_L \times \left[RL \times \frac{\frac{sLo}{R_L} + 1}{sC1 \times R1 + 1} \right]$$

If the R1 × C1 time constant is equal to the Lo/R_L time constant, the voltage across capacitor C1 equals the R_L × I_L. Figure 17 is a plot of this equation and shows the results graphically. It assumes an inductance of 1.5µH, RL = 0.01Ω (-40dB), C1=0.1µF and R1=1.5k. The time constants are equal and diverge at the same rate. The overall impedance, H(s), equals RL for all frequencies.

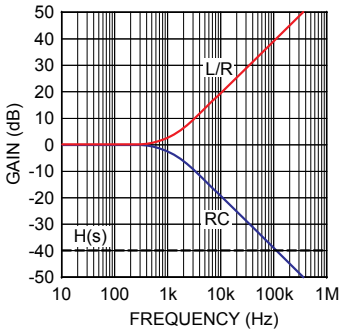


Figure 17. Current Sense Gain/Phase Plot

Current Sharing

The schematic in Figure 18 illustrates the current sharing scheme. The error amplifier in Channel 1, E/A 1, monitors the output voltage and adjusts the duty cycle of Channel 1 to regulate that voltage. The inputs of transconductance error amplifier, E/A 2, are connected to the current sense points of each channel. The error amplifier regulates Channel 2 current by monitoring the current sense point of Channel 1 and forcing the current sense point of Channel 2 to be equal.

Any offset or difference in current between the two channels is caused by tolerances in the inductance, DCR, and tolerances of R1, C1, R2 and C2. Additionally, voltage offset in E/A 2 may cause variations in output current sharing. At lower currents, these variations may force the current of Channel 2 to be 0.

A nominal 10mV offset inhibits the Channel 2 low-side MOSFET until the output current increases to the magnitude where the voltage across C1 is 10mV. This prevents the low-side MOSFET of Channel 2 from sinking current to ground during startup or during low current operation.

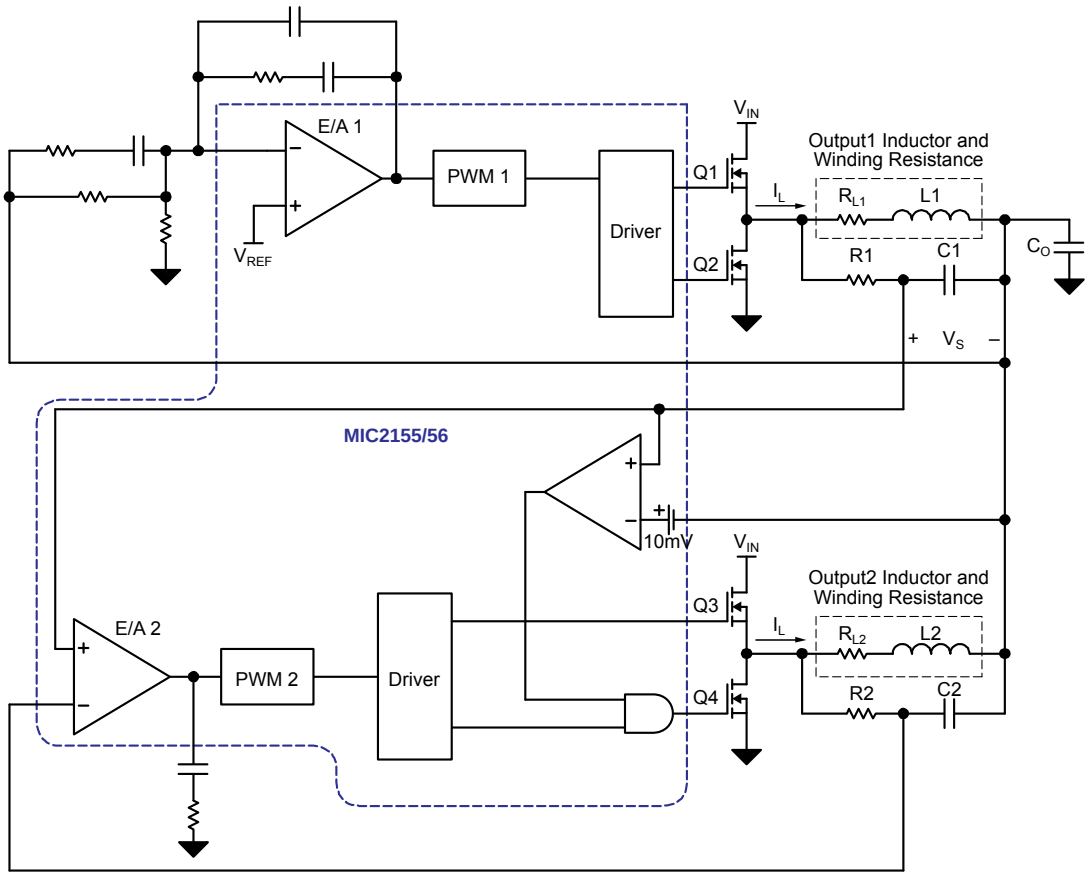


Figure 18. Current Sharing Diagram

Startup into a Pre-Biased Output

Soft start circuitry in a conventional synchronous buck regulator forces the regulator to start up by initially operating at a minimum duty cycle and gradually increasing the duty cycle until the output voltage reaches regulation. In a synchronous buck power supply, a narrow duty cycle means the low-side MOSFET is on for most of the switching period. If the output voltage is not 0V, the wide on time of the low-side MOSFET may discharge the output and cause high reverse current to flow in the inductor.

The MIC2155/6 is designed to turn on into a pre-biased output without discharging the output. Circuitry in the controller monitors the input and output voltage and forces the soft start circuit to initially operate at the proper duty cycle. This allows the output to turn on in a controlled fashion without discharging the output. The minimum output voltage for proper operation of the pre-bias startup circuitry is 0.6V. If V_{OUT} is less than 0.6V, a partial discharge of V_{OUT} may occur.

Separate Input Supplies

The MIC2155/6 can operate from two different input supplies with different voltages. Each of the two channels can have a different input voltage and still share current. This allows the supply to draw power from more than one supply.

The controller will force the output current to be equal. Since the output voltage and currents of the two channels are the same, the input power drawn from each supply will approximately be the same. The input currents will be inversely proportional to the input voltages of each supply. For example, if the total output power is 50W and efficiency is 91%, the total input power from both supplies is:

$$P_{IN} = \frac{P_{OUT}}{\eta} = \frac{50}{0.9} = 55W$$

Each supply contributes approximately half the power:

$$P_{IN1} = P_{IN2} = 27.5W$$

For V_{IN1} = 12V and V_{IN2} = 3.3V

$$I_{IN1} = \frac{27.5W}{12V} = 2.3A$$

and

$$I_{IN2} = \frac{27.5W}{3.3V} = 8.3A$$

Component Selection, Guidelines and Design Example

The following section outlines a procedure for designing a two-phase synchronous buck converter using the MIC2155.

This example will use the following parameters:

V_{IN} = 12V
V_{OUT} = 1.8V
I_{OUT} = 30A
Switching frequency (f_S) = 500kHz/channel (MIC2155)

Output Filter Selection

The output filter is comprised of the output capacitors and the output inductors. The filter is designed to attenuate the output voltage ripple to the desired value. The output filter components also determine how well the supply responds to output current transients. If output transients are significant, the output capacitors should be chosen first to meet the transient specification. The output inductor is then selected to insure the filter attenuates the output ripple to meet the specification.

A second, commonly used method of designing the filter is to select the inductor value to keep the ripple current between 20% and 30% of the output current for that channel. Then select the output capacitance to meet the output voltage ripple specification and output current transient specification.

Values for inductance, peak and RMS currents are required to choose the output inductors. The input and output voltages and the inductance value determine the peak to peak inductor ripple current. Output capacitor selection requires calculation of transient current, RMS capacitor current and output voltage.

There are several tradeoffs to be made when selecting the output inductor. Generally, higher inductance values are used with higher input voltages. Larger peak to peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak to peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor.

Higher switching frequencies allow the use of a small inductance but increase power dissipation in the inductor core and MOSFET switching loss. The MIC2155 switches at 500kHz/channel and is designed to use a smaller inductor at the expense of higher switching losses and slightly lower efficiency. While the 300kHz MIC2156 was optimized for higher efficiency and higher output current but its lower switching frequency requires a larger output inductance to maintain the same peak-to-peak output ripple current.

The peak output ripple current for a two-phase converter is shown in Figure 19. The graph shows that peak ripple current is a function of duty cycle. Since each channel is 180° out of phase with the other, at 50% duty cycle, the output ripple currents from each channel cancel and output ripple current is close to zero.

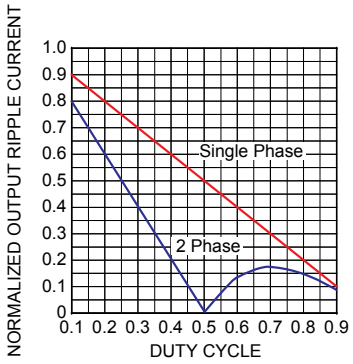


Figure 19. 2 Phase Output Ripple Current vs. Duty Cycle

For this example, with V_{IN} = 12V, V_{OUT} = 1.8V and efficiency = 88%, the duty cycle is:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} = \frac{1.8V}{0.88 \times 12} = 0.17$$

Figure 19 shows the peak-to-peak output ripple current normalized to:

$$\frac{V_{OUT}}{f_S \times L_{OUT}}$$

The peak-to-peak output ripple current is less than for a single phase conversion. If V_{IN} varies, the input voltage that generated the highest ripple current should be used for the calculation.

For this example, assume the output transient loading is small and the filter design is based on output ripple voltage requirement.

The inductance value is calculated by the equation below:

$$L = \frac{V_{OUT} \times (\eta \times V_{IN(MAX)} - V_{OUT})}{\eta \times V_{IN(MAX)} \times f_S \times 0.2 \times I_{OUT}}$$

Where:

f_S is the switching frequency
0.2 is the ratio of AC ripple current to DC output current
$V_{IN(MAX)}$ is the maximum input voltage
I_{OUT} is output current of the each channel or ½ of the total output current
η is the converters efficiency

For this example:

$$L = \frac{1.8V \times (0.88 \times 12V - 1.8V)}{0.88 \times 12V \times 500kHz \times 0.2 \times 15A} = 1\mu H$$

If another inductor value is used, the ripple current for each channel is calculated from the formula below:

$$I_{PP} = \frac{V_{OUT} \times (\eta \times V_{IN(MAX)} - V_{OUT})}{\eta \times V_{IN(MAX)} \times f_S \times L}$$

$$I_{PP} = \frac{1.8V \times (0.88 \times 12V - 1.8V)}{0.88 \times 12V \times 500kHz \times 1\mu H} = 3A$$

The output capacitors see less ripple current than each channel because they are out of phase.

The normalizing factor is:

$$\frac{V_{OUT}}{f_S \times L_{OUT}} = \frac{1.8V}{500kHz \times 1\mu H} = 3.6$$

The output ripple current in the two-phase configuration is approximately:

$$0.65 \times \frac{V_{OUT}}{f_S \times L_{OUT}} = 0.65 \times \frac{1.8V}{500kHz \times 1\mu H} = 2.3A$$

For the input and output voltage in this application, going to a two-phase design decreased the total output ripple current from $3A_{PP}$ to $2.3A_{PP}$.

The peak inductor current in each channel is equal to the average output current plus one half of the peak to peak inductor ripple current:

$$I_{PK} = I_{OUT} + 0.5 \times I_{PP} = 15A + 0.5 \times 3A = 16.5A$$

The RMS inductor current is used to calculate the $I^2 \times R$ losses in the inductor:

$$I_{INDUCTOR(RMS)} = I_{OUT} \times \sqrt{1 + \frac{1}{12}\left(\frac{I_{PP}}{I_{OUT}}\right)^2}$$

$$I_{INDUCTOR(RMS)} = 15A \times \sqrt{1 + \frac{1}{12}\left(\frac{3A}{15}\right)^2} = 15.1A$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2155 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The inductor winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor.

The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor.

For this example a Cooper HCF1305-1R0 inductor was chosen. Core loss for this application was taken from the data sheet and is 15mW. Winding resistance is 1.9mΩs

Copper loss in the inductor is calculated by the equation below:

$$P_{INDUCTOR(COPPER)} = (I_{INDUCTOR(RMS)})^2 \times R_{WINDING} = 15.12 \times 1.9m\Omega = 0.43W$$

The resistance of the copper wire, $R_{WINDING}$, increases with temperature. If so desired, a more accurate calculation can be made if the maximum ambient temperature and temperature rise of the inductor is known. The value of the winding resistance at operating temperature is calculated with the formula below:

$$R_{WINDING(HOT)} = R_{WINDING(20)} \times (1 + 0.0042 \times (Temp_{HOT} - T_{20})$$

Where:

$Temp_{HOT}$ is the temperature of the wire under operating load

T_{20} is the ambient temperature

$R_{WINDING(20)}$ is the resistance of the winding at room temperature, usually specified by the manufacturer.

For this example, the approximate power dissipation is 0.43W. From the manufacturers data sheet this causes a 20°C rise in inductor temperature. Assuming ambient temperature stayed at 20°C, the maximum winding resistance would be increased from 1.9mΩs to:

$$R_{WINDING(HOT)} = 1.9m\Omega \times (1 + 0.0042 \times (40°C - 20°C) = 2.06m\Omega$$

Output Capacitor Selection

In this example, the output capacitors are chosen to keep the output voltage ripple below a specified value. The output ripple voltage is determined by the capacitors ESR (equivalent series resistance) and capacitance. Voltage rating and RMS current capability are two other important factors in selecting the output capacitor.

Ceramic output capacitors and most polymer capacitors have very low ESR and are recommended for use with the MIC2155/6. The output capacitance is usually the primary cause of output ripple in ceramic and very low ESR capacitors. The minimum value of C_{OUT} is calculated below:

$$C_{OUT} \geq \frac{I_{PP}}{8 \times \Delta V_{OPP} \times 2 \times f_S}$$

Where:

ΔV_{OPP} is the peak-to-peak output voltage ripple

I_{PP} is the peak-to-peak ripple current as see by the capacitors

f_S is the per channel switching frequency

Notice the calculation is performed at 2x the switching frequency since the capacitors see ripple current from both phases.

For this example, using ΔV_{OPP} = 10mV, the minimum C_{OUT} is:

$$C_{OUT} \geq \frac{2.3}{8 \times 10mV \times 2 \times 500kHz} = 29\mu F$$

A capacitance value this low is usually not used in high current converters because of transient output current requirements.

For this example, 500µF total capacitance is used. It is split up into (4) 47µF ceramic capacitors and (2) 150µF Aluminum Polymer capacitors

The total output ripple is a combination of the ESR and the output capacitance. The total ripple is calculated below:

$$\Delta V_{OUT} = \sqrt{\left[\frac{I_{PP}}{8 \times C_{OUT} \times 2 \times f_S}\right]^2 + \left[I_{PP} \times R_{ESR}\right]^2}$$

To increase reliability, the recommended voltage rating of capacitor should be twice the output voltage for a tantalum and 20% greater for an aluminum electrolytic or ceramic.

The output capacitor RMS current is calculated below:

$$I_{COUT(RMS)} = \frac{I_{PP}}{\sqrt{12}} = \frac{2.3A}{\sqrt{12}} = 0.66A$$

The power dissipated in the output capacitors can be calculated by the equation below:

$$P_{DISS(COUT)} = \left(I_{COUT(RMS)}\right)^2 \times R_{ESR}$$

Inductor Current Sense Components

The RC circuit values that sense current across the inductor can be calculated once the inductor is selected. The circuit is shown in Figure 20.

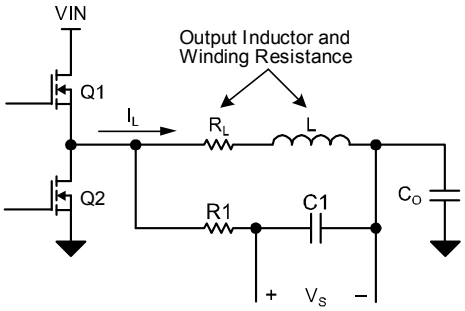


Figure 20. Inductor Current Sense

The inductor has the following values:

$$L = 1.0\mu H,\ R_L = 1.9m\Omega$$

Proper sensing of the DC voltage across the inductor requires the R_L/L time constant be equal to the R1×C1 time constant:

$$\frac{L}{R_L} = C1 \times R1$$

A good range of values for C1 is 0.1µF to 1µF. For this example C1 is chosen as 0.22µF. R1 is:

$$R1 = \frac{L}{R_L \times C1} = \frac{1\mu H}{1.9m\Omega \times 0.22\mu F} = 2.39k$$

Input Capacitor Selection

In addition to high-frequency ceramic capacitors, a larger bulk capacitance, either ceramic or Al. El. should be used to help attenuate ripple on the input and to supply current to the input during large output current transients. The input capacitors must be rated for the RMS input current of the power supply. RMS input capacitor current is determined at the maximum output current. The graph in Figure 21 shows the normalized RMS input ripple current vs. duty cycle. Data is normalized to the output current.

For a two-phase converter operating at 17% duty cycle, the input RMS current is determined from the graph:

$$I_{CIN\_RMS} \approx I_{OUT} \times 0.24 = 7.2A$$

The power dissipated in the input capacitor is:

$$P_{DISS(CIN)} = \left(I_{CIN(RMS)}\right)^2 \times R_{ESR}$$

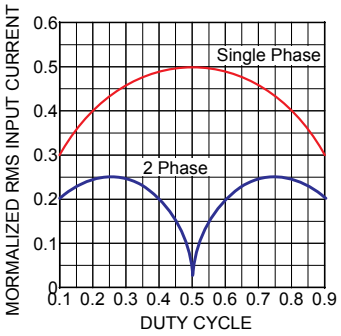


Figure 21. RMS Input Current vs. Duty Cycle

MOSFET Selection

External N-channel logic level power MOSFETs must be used for the high and low side switches. The MOSFET gate to source drive voltage of the MIC2155 is regulated by an internal 5V V_{DD} regulator. Logic level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used. This resistance is used to calculate the losses during the MOSFET's conduction time. If operating at 4.5V_{IN}, without connecting V_{DD} to V_{IN}, the gate drive voltage to the high-side FET could be as low as 3.2V. MOSFETs with low V_{GS} enhanced gates should be used in this situation.

It is important to note the on-resistance of a MOSFET increases at high junction temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 40% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation.

Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2155 gate drive circuit. Gate charge can be a significant source of power dissipation in the controller due to the high switching frequencies and generally large MOSFETs that are driven. At low output load this power dissipation is noticeable as a reduction in efficiency.

The average current required to drive the MOSFETs is:

$$I_{DD} = Qg \times fs$$

Where:

Qg is the total gate charge for all high and low side MOSFETs. This information should be obtained from the manufacturer's data sheet with a 5V V_{GS}.
Since the current from the gate drive comes from the input voltage, the power dissipated in the MIC2155 due to gate drive is:

$$P_{GATE\_DRIVE} = Qg \times f_S \times V_{IN}$$

A convenient figure of merit for switching MOSFETs is the on-resistance times the total gate charge (R_{DSON} × Qg). Lower numbers translate into higher efficiency. Low gate charge, logic level MOSFETs are a good choice for use with the MIC2155. The internal LDO that supplies V_{DD} is rated for 75mA. Exceeding this value could damage the regulator or cause excessive power dissipation in the IC. Refer to the "Supply Voltages and Internal Regulator" section of this specification for additional information.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On resistance
- Total Gate Charge

The V_{DS} voltage rating of the MOSFETs is essentially equal to the input voltage. A safety factor of 20% should be added to the $V_{DS(max)}$ of the MOSFETs to account for voltage spikes due to circuit parasitics.

The power dissipated in the switching transistor is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses that occur during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{SW} = P_{CONDUCTION} + P_{AC}$$

Where:

$$P_{CONDUCTION} = I_{SWITCH(rms)}^2 \times R_{SWITCH}$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)}$$

R_{SWITCH} is the on resistance of the MOSFET switch.

Making the assumption the turn-on and turn-off transition times are equal, the total AC switching loss is:

$$P_{AC} = (V_{IN} + V_D) \times I_{SW\_PEAK} \times T_t \times f_S$$

Where:

T_t is the switching transition time (typically 15ns to 30ns)
f_S it the switching frequency of each phase

RMS Current and MOSFET Power Dissipation Calculation

Under normal operation, the high side MOSFET's RMS current is greatest when V_{IN} is low (maximum duty cycle). The low side MOSFET's RMS current is greatest when V_{IN} is high (minimum duty cycle). However, the MOSFET sees maximum stress during short circuit conditions, where the output current is equal to the maximum overcurrent level. The calculations below are for normal operation. To calculate the stress under short circuit conditions, substitute the maximum overcurrent level for $I_{OUT(max)}$.

The RMS value of the high side switch current is:

$$I_{SW\_RMS(HIGH\_SIDE)} = D\sqrt{(I_{OUT(max)}^2 + \frac{I_{PP}^2}{12})}$$

$$I_{SW\_RMS(LOW\_SIDE)} = (1-D)\sqrt{(I_{OUT(max)}^2 + \frac{I_{PP}^2}{12})}$$

Where:

D is the duty cycle of the converter
I_{PP} is the individual inductor ripple current

$$D = \frac{V_{OUT}}{\eta \times V_{IN}}$$

and η is the efficiency of the converter.

Converter efficiency also depends on other component parameters that have not yet been selected. For design purposes, an efficiency estimate of 85% – 90% can be used. The efficiency can be more accurately calculated once the design is complete. If the assumed efficiency is grossly inaccurate, a second iteration through the design procedure should be made.

For the high-side switch, the maximum DC power dissipation is:

$$P_{SWITCH1(DC)} = R_{DSON1} \times (I_{SW1(rms)})^2$$

For the low-side switch, the DC power dissipation is:

$$P_{SWITCH2(DC)} = R_{DSON2} \times (I_{SW2(rms)})^2$$

The switching loss for each of the high-side MOSFETs is:

$$P_{AC} = V_{IN} \times I_{SW(peak)} \times T_t \times f_S$$

The total power dissipation for each MOSFET is:

$$P_{FET\_total} = P_{SWITCH1(DC)} + P_{AC}$$

External Schottky Diode

A freewheeling diode in parallel with the low-side FET is needed to keep the inductor current flow continuous while both MOSFETs are turned off (dead time). Dead time is necessary to prevent current from flowing unimpeded through both MOSFETs. An external Schottky diode is not necessary for circuit operation since the low-side MOSFET contains a parasitic body diode. An external diode will improve efficiency due to its lower forward voltage drop as compared to the internal parasitic diode in the FET. It may also decrease high frequency noise because the schottky diode junction does not suffer from reverse recovery.

If the MOSFET body diode is used, it must be rated to handle the peak and average current. The body diode may have a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn on. If the internal FET diode is used, power dissipated during the dead time should be added to the P_{DISS} of the low-side MOSFET.

An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes is less ringing and power loss. Depending on the circuit components and operating conditions, an external Schottky diode may give a ½% to 1% improvement in efficiency.

This power dissipation is calculated below:

$$I_{D(ave)} = I_{OUT} \times 2 \times t_d \times f_S$$

Where:

t_d is the dead time when both MOSFETs are off.

The reverse voltage requirement of the diode is:

$$V_{DIODE\_RRM} = V_{IN}$$

The power dissipated by the diode is:

$$P_{DIODE} = I_{D\_AVE} \times V_F$$

Where:

V_F is the forward voltage at the peak diode current.

Snubber Design

A snubber is used to damp out high frequency ringing caused by parasitic inductance and capacitance in the buck converter circuit. A snubber is needed for each of the two phases in the converter. Figure 22 shows a simplified schematic of one of the buck converter phases. Stray capacitance consists mostly of the two MOSFET's output capacitance (C_{OSS}). The stray inductance is mostly package and etch inductance. The arrows show the resonant current path when the high side MOSFET turns on. This ringing causes stress on the semiconductors in the circuit as well as increased EMI.

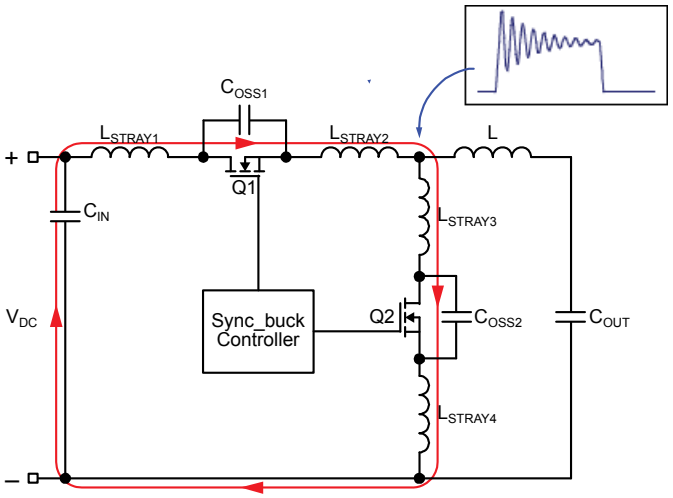


Figure 22. Output Parasitics

One method of reducing the ringing is to use a resistor and capacitor to lower the Q of the resonant circuit. The circuit in Figure 23 shows the resistor in between the switch node and ground. Capacitor Cs is used to block DC and minimize the power dissipation in the resistor. This capacitor value should be between 5 and 10 times the parasitic capacitance of the MOSFET C_{OSS}. A capacitor that is too small will have high impedance and prevent the resistor from damping the ringing. A capacitor that is too large causes unnecessary power dissipation in the resistor, which lowers efficiency.

The snubber components should be placed as close as possible to the low-side MOSFET and/or external schottky diode since in contributes to most of the stray capacitance. Placing the snubber too far from the FET or using etch that is too long or thin will add inductance to the snubber and diminishes its effectiveness.

A proper snubber design requires the parasitic inductance and capacitance be known. A method of determining these values and calculating the damping resistor value is outlined below.

1. Measure the ringing frequency at the switch node which is determined by parasitic L_P and C_P. Define this frequency as f_1.

2. Add a capacitor C_S (normally at least 3 times as big as the C_{OSS} of the FET) from the switch node to ground and measure the new ringing frequency. Define this new (lower) frequency as f_2. L_P and C_P can now be solved using the values of f_1, f_2 and C_S.

3. Add a resistor R_S in series with C_S to generate critical damping.

Step 1: First measure the ringing frequency on the switch node voltage when the high-side MOSFET turns on. This ringing is characterized by the equation:

$$f_1 = \frac{1}{2\pi\sqrt{L_P \times C_P}}$$

Where:
C_P and L_P are the parasitic capacitance and inductance

Step 2: Add a capacitor, C_S, in parallel with the synchronous MOSFET, Q2. The capacitor value should be approximately 3 times the C_{OSS} of Q2. Measure the frequency of the switch node ringing, f_2:

$$f_2 = \frac{1}{2\pi\sqrt{Lp \times (Cs + Cp)}}$$

Define f' as:

$$f' = \frac{f_1}{f_2}$$

Combining the equations for f_1, f_2 and f' to derive C_P, the parasitic capacitance:

$$C_P = \frac{C_S}{2 \times (f')^2 - 1}$$

L_P is solved by re-arranging the equation for f_1:

$$L_P = \frac{1}{(2\pi)^2 \times C_P \times (f_1)^2}$$

Step 3: Calculate the damping resistor.

Critical damping occurs at Q = 1:

$$Q = \frac{1}{R_S}\sqrt{\frac{L_P}{C_S}} = 1$$

Solving for R_S

$$R_S = \sqrt{\frac{L_P}{C_S}}$$

Figure 23 shows the snubber in the circuit and the damped switch node waveform.

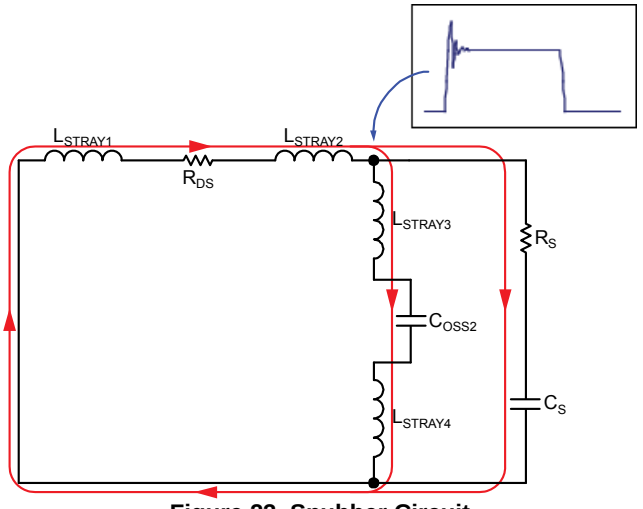


Figure 23. Snubber Circuit

The snubber capacitor, C_S, is charged and discharged each switching cycle. The energy stored in C_S is dissipated by the snubber resistor, R_S, two times per switching period. This power is calculated in the equation below:

$$P_{SNUBBER} = f_S \times C_S \times V_{IN}^2$$

Where:

f_S is the switching frequency for each phase

V_{IN} is the DC input voltage

Compensation of the Output Voltage Loop

The voltage regulation, filter and power stage section is shown in Figure 24. The error amplifier for Channel 1 is used to regulate the output voltage and compensate the voltage regulation loop. It is a voltage output op amp that is designed to use type III (PID) compensation. Type III compensation has two compensating zeros, two poles and a pole at the origin. The figure also shows the transfer function for each section.

Compensation is necessary to insure the control loop has adequate bandwidth and phase margin to properly respond to input voltage and output current transients.

High gain at DC and low frequencies is needed for accurate output voltage regulation. Attenuation near the switching frequency prevents switching frequency noise from interfering with the control loop.

For this analysis, the LC filter in the two phase design is combined into one. The inductances are in parallel and the output capacitance is the total sum of all C_{OUT}. The ESR is the parallel combination of all ESRs. The output load is represented by a resistor R.

The output filter contains a complex double pole formed by the capacitor and inductor and a zero from the output capacitor and it's ESR. The transfer function of the filter is:

$$Gfilter(s) = \frac{1 + \frac{s}{\omega z}}{1 + \frac{s}{2 \times Q \times \omega o} + \left(\frac{s}{\omega o}\right)^2}$$

Where:

$$\omega z = \frac{1}{C_O \times Resr}$$

$$\omega o = \frac{1}{\sqrt{C_O \times L_O}}$$

$$Q = R \times \sqrt{\frac{C_O}{L}}$$

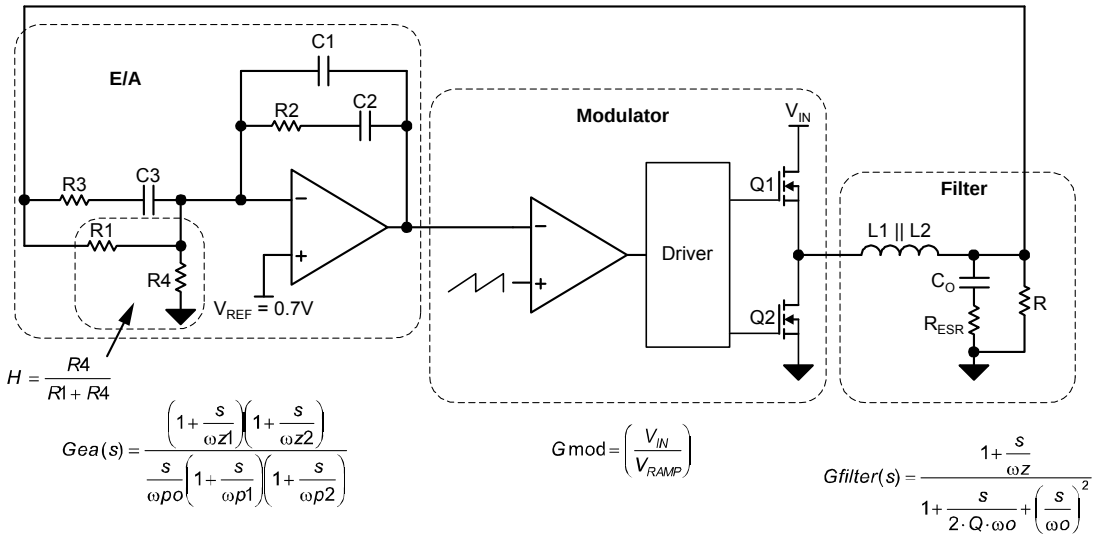


Figure 24. Voltage Loop and Transfer Functions

The Modulator Gain is proportional to the input voltage and inversely proportional to the internal ramp voltage generated by the oscillator. The MIC2155/6 peak-peak ramp voltage is 1V:

$$G_{MOD} = \left(\frac{V_{IN}}{V_{RAMP}} \right)$$

The output voltage divider attenuates V_{OUT} and feeds it back to the error amplifier. The divider gain is:

$$H = \frac{R4}{R1 + R4} = \frac{V_{REF}}{V_{OUT}}$$

The modulator, filter and voltage divider gains can be multiplied together to show the open loop gain of these parts:

$$G_{VD}(s) = G_{FILTER}(s) \times H \times G_{MOD}$$

This transfer function is plotted in Figure 25. At low frequency, the transfer function gain equals the modulator gain times the voltage divider gain. As the frequency increases toward the LC filter resonant frequency, the gain starts to peak. The increase in the gain's amplitude equals Q. Just above the resonant frequency, the gain drops at a -40db/decade rate. The phase quickly drops from 0° to almost 180° before the phase boost of the zero brings it back up to -90°. Higher values of Q will cause the phase to drop quickly. In a well damped, low Q system the phase will change more slowly.

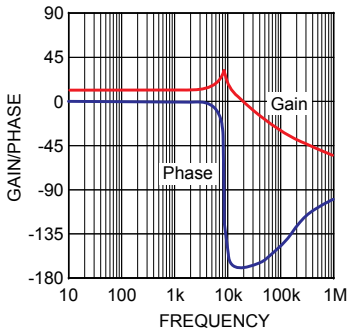


Figure 25. G_{VD} Transfer Function

As the frequency approaches the zero frequency (Fz), formed by Co and it's ESR, the slope of the gain curve changes from -40db/dec. to -20db/dec and the phase increases. The zero causes a 90° phase boost. Ceramic capacitors, with their smaller values of capacitance and ESR, push the zero and its phase boost out to higher frequencies, which allow the phase lag from the LC filter to drop closer to -180°. The system will be close to being unstable if the overall open loop gain crosses 0dB while the phase is close to -180°. If the output capacitance and/or ESR is high, the zero moves lower in frequency and helps to boost the phase, leading to a more stable system.

The error amplifier is a type III which has two zeros, two poles and a pole at the origin. This type of error amplifier works well when Ceramic output capacitors make up the majority of C_{OUT} because it introduces an extra zero that helps improve phase margin:

$$Gea(s) = \frac{\left(1 + \frac{s}{\omega z1}\right)\left(1 + \frac{s}{\omega z2}\right)}{\frac{s}{\omega po}\left(1 + \frac{s}{\omega p1}\right)\left(1 + \frac{s}{\omega p2}\right)}$$

Where:

$$\omega z1 = \frac{1}{R2 \times C2}$$

$$\omega z2 = \frac{1}{(R1 + R3) \cdot C3}$$

$$\omega po = \frac{1}{R1 \times C1}$$

$$\omega p1 = \frac{1}{\frac{C1 \times C2}{C1 + C2} \cdot R2}$$

$$\omega p2 = \frac{1}{R3 \times C3}$$

Figure 26 shows the bode plot of the error amplifier transfer function.

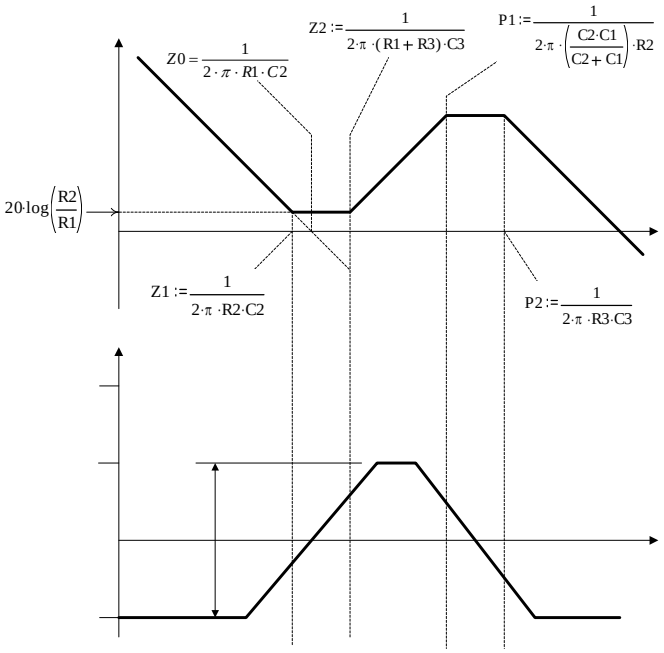


Figure 26. Type III Error Amplifier Gain/Phase

Error Amplifier Design Procedure

Step 1: Decide on the crossover frequency

To maximize transient response, the open loop bandwidth should be made reasonably high. Initially, the bandwidth can be selected to be 1/10 of the output switching frequency. This may be improved once the design is built and measurements are made. An initial bandwidth of 100kHz for the 2155 and 60kHz for the 2156 are good choices.

Step 2: Determine the gain required at the crossover frequency

G_{Boost} is how much gain boost is needed so the open loop transfer function crosses 0dB at the pre-determined crossover frequency. This can be measured by plotting the $G_{VD}(s)$ transfer function or can be estimated with the following formula:

$$G_{Boost} = \frac{1}{\frac{H \times V_{IN}}{V_M} \times \left(\frac{fo}{fc}\right)^2 \times \left(\frac{fc}{fz}\right)}$$

Where: fo = LC filter resonant frequency

fc= open loop bandwidth chosen in Step 1

fz = zero formed by C_{OUT} and its ESR

H = voltage divider attenuation

V_M=amplitude of the internal sawtooth ramp (V_M=1)

V_{IN}= Input voltage to the power supply

Step 3: Determine the gain boost needed at the crossover frequency (fc)

Typically, 50° of phase margin can be used for most applications. This is a good tradeoff between an overdamped system (slower response to transients) and an underdamped system (overshoot or unstable response to transients). It also allows some margin for component tolerances and variations due to ambient temperature changes. The phase margin at the crossover frequency (fc) can be determined by plotting the $G_{VD}(s)$ phase on a bode plot or can be estimated with the following formula:

$$\varphi_M = \tan^{-1}\left[\frac{\frac{fc}{Q \times fo}}{1-\left(\frac{fc}{fo}\right)^2}\right] + \tan^{-1}\left[\frac{fc}{fz}\right]$$

The additional phase boost required from the error amplifier is:

$$\varphi_{Boost} = 52° - \varphi_M$$

Step 4: Determine the frequencies fz2 and fp1

The frequencies for the zero and pole (fz2 and fp1) are calculated for the desired amount of phase boost at the crossover frequency (fc):

$$fz2 = fc \times \sqrt{\frac{1-\sin[\varphi_{Boost}]}{1+\sin[\varphi_{Boost}]}}$$

$$fp1 = fc \times \sqrt{\frac{1+\sin[\varphi_{Boost}]}{1-\sin[\varphi_{Boost}]}}$$

Step 5: Determine the frequency for fz1

The low-frequency zero, fz1, is initially set to one-fifth of the LC resonant frequency. If it is set too low, it will force the low frequency gain to be low and impact transient response. If set too high, it will not add enough phase boost at the LC resonant frequency. This could cause conditional stability, which when the phase drops below -180° before the gain crosses 0dB. If the DC gain should drop in this situation, this may lead to an unstable system.

$$fz2 = \frac{fo}{5}$$

Step 6: Determine the frequency for fp2

This is the high frequency pole, which is useful in additional attenuation of the switching frequency. It should initially be set at half of the switching frequency. If it is set too low, it will lower the phase margin at the crossover frequency, making it difficult to achieve the proper phase margin. If set too high, it will not provide attenuation of the switching frequency, which could lead to jitter of the switching waveform or instability under certain conditions.

$$fp2 = \frac{fs}{2}$$

Calculating Error Amplifier Component Values

Once the pole and zero frequencies have been fixed, the error amplifier's resistor and capacitor values are calculated.

R1: This value is chosen first. All other component values are calculated from R1. A value of 10K is suggested. If R1 is chosen too high, R2 may be very large and the high impedances could be sensitive to noise. If the remote sense amplifier is used, R1 must be large enough so than not more than 500µA of current is drawn from the amplifier.

R2: The value of R2 is determined from the mid-band gain of the error amplifier. This gain depends on the frequencies of the poles, zeros and LC filter resonant frequency.

Based on the amount of gain necessary at the crossover frequency the mid-band gain and R2 value is calculated using the following formula:

$$G_{CO} = \frac{Vm}{H \times Vin} \times \left(\frac{fo}{fc}\right)^2 \times \left(\frac{fc}{fz}\right) \times \sqrt{\frac{fz2}{fp1}}$$

$$R2 = R1 \times G_{CO}$$

The other component values are calculated as follows:

$$C2 = \frac{1}{2 \times \pi \times fz1 \times R2}$$

$$C3 = \frac{1}{2 \times \pi \times fz2 \times R1}$$

$$C3 = \frac{C2}{2 \times \pi \times (fp1 \times C2 \times R2 - 1)}$$

$$R3 = \frac{1}{2 \times \pi \times fp2 \times C3}$$

Compensation of the Current Sharing Loop

The control circuitry for Channel 2 forces the channel's output current to match the current in Channel 1. The Channel 2 error amplifier compares the inductor currents in the two channels and adjusts the duty cycle of Channel 2 to control its output current. A block diagram is shown in Figure 27.

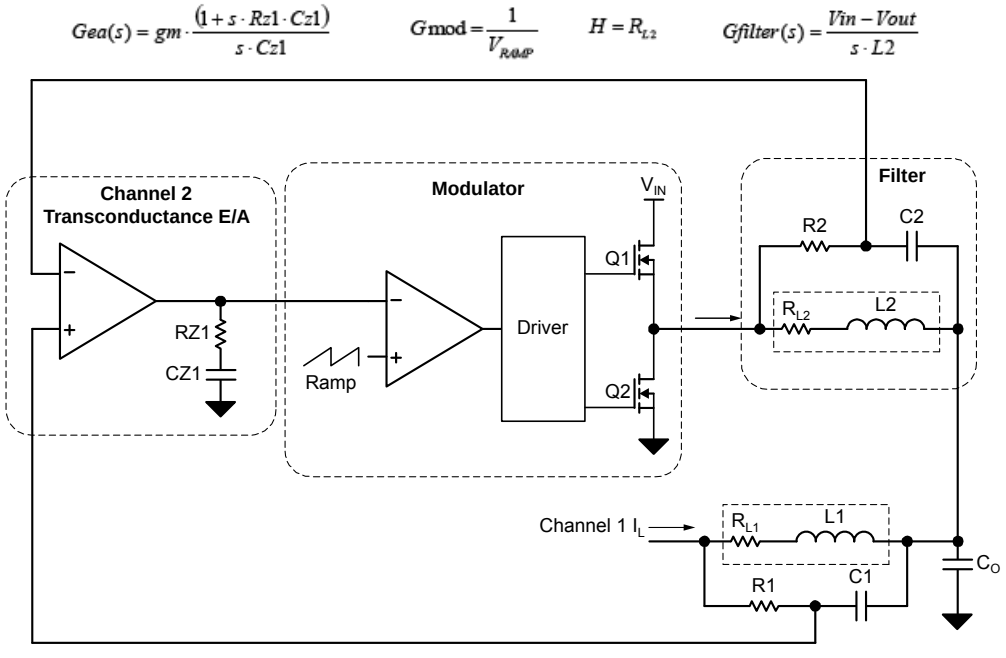


Figure 27. Current Sharing Loop and Transfer Functions

Unlike the voltage output amplifier used for Channel 1 compensation, a transconductance amplifier is used for the Channel 2 compensation since only a pole/zero combination is required for compensation. The transconductance amplifier transfer function is:

$$Gea(s) = gm \times \frac{1 + s \times Rz1 \times Cz1}{s \times Cz1}$$

Where:

Rz1 and Cz1 are the external components connected to the COMP2 pin

gm is the transconductance of the internal amplifier.

The pole and zero frequencies are:

$$f_{POLE} = \frac{gm}{2 \times \pi \times Cz1}$$

$$f_{ZERO} = \frac{1}{2 \times \pi \times Rz1 \times Cz1}$$

The gain of the modulator is:

$$g_{MOD} = \frac{1}{V_M}$$

Where:

V_M is the peak-to-peak amplitude of the internal sawtooth.

The gain of the feedback circuit is output current divide by V_{EA}

$$H = R_{L2}$$

The filter transfer function is the output current over the applied voltage:

$$G_{FILTER(s)} = \frac{V_{IN} - V_{OUT}}{s \times L2}$$

The open loop transfer function is:

$$G_{OL2(s)} = G_{EA(s)} \times G_{MOD} \times H \times G_{FILTER(s)} = \frac{gm \times (1 + s \times Rz1 \times Cz1) \times R_{L2} \times (V_{IN} - V_{OUT})}{(s \times Cz1) \times Vm \times (s \times L2)}$$

The loop is inherently stable because the phase shift is only 90 degrees. The error amplifier pole and zero is selected to achieve a desired crossover frequency. In this example, the desired crossover frequency is 50kHz. The transfer function of the filter, modulator and feedback is plotted in Figure 28.

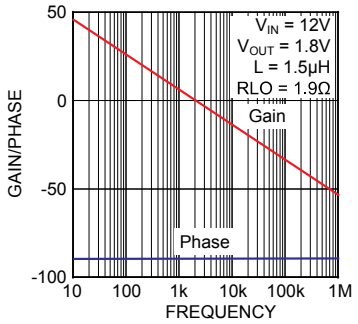


Figure 28. Current Sharing Loop Gain/Phase

The gain boost required at 50kHz is 28dB which is a gain of 25. The gain for frequencies above the zero is:

$$G_{MID} = Rz1 \times gm$$

For a typical gm = 1.25mS, solving for Rz1:

$$Rz1 = \frac{G_{MID}}{gm} = \frac{25}{1.25mS} = 20k\Omega$$

Set the zero frequency to be 1/5 of the crossover frequency:

$$Cz1 = \frac{1}{2 \times \pi \times Rz1 \times fz1}$$

$$Cz1 = \frac{1}{2 \times \pi \times 20k \times 10k} = 800pF$$

The compensated open loop gain/phase plot is shown in Figure 29.

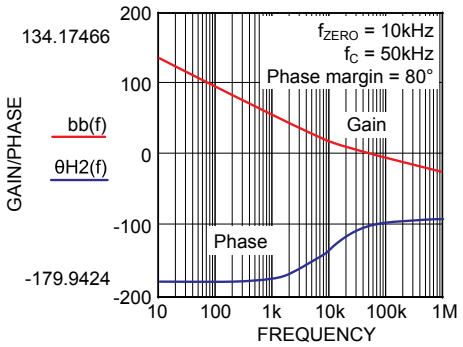


Figure 29. Compensated Current Sharing Loop Gain/Phase

General Layout and Component Placement

There are three basic types of currents in a switching power supply – high di/dt, moderate di/dt and DC. Examples of each are shown in Figure 30.

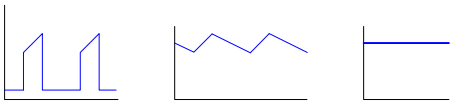


Figure 30. Current Diagram

In a buck converter, high di/dt currents in the 0.5A/ns range are generated by MOSFETs switching on and off. These fast switching currents flow in the high and low-side MOSFETs, external freewheeling schottky diode and the input capacitor. Fast switching currents also flow in the gate drive and return etch between the controller and the power FETs. At that switching speed at 10nH piece of etch generates 5V across itself. Therefore, attention to proper layout techniques is essential. Traces that have high di/dt currents must be kept short and wide. Additionally a power ground plane should be used on an adjacent layer to help minimize etch inductance. Figure 31 shows a layout example that minimizes inductance.

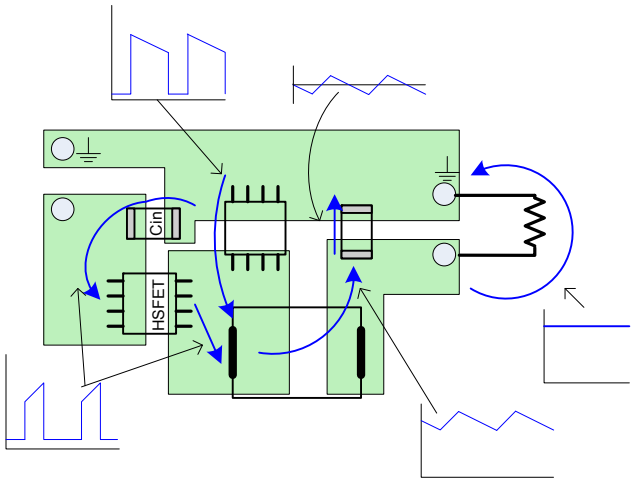


Figure 31. Layout

Moderate di/dt currents flow in the inductor and output capacitor. Although layout is not as critical, it is still important to minimize inductance by using short, wide traces and a ground plane. Figure 31 shows the etch connecting the inductor to the output is shaped to force current to flow past the output capacitor before reaching the output terminal (or output load). This minimizes the series inductance between the inductor and the capacitor, which improves the ability of the capacitor to filter ripple. Additionally, the inductor current has a large DC component and requires a wide trace to minimize voltage drop and power dissipation.

DC currents in a high-current buck converter require wide etch paths to minimize voltage drop and power dissipation. The input and output current are mainly DC. At or near maximum output power, the inductor current is also predominately DC and requires ample etch to reduce copper loss, reduce temperature rise and improve efficiency. Minimizing voltage drops in the output and ground path helps improve output voltage regulation for configurations without remote voltage sensing.

The gate drive connections to both the high-side and low-side MOSFETs must each have their own return current path. The high-side MOSFET's source is connected to the switch node and returns back to the controller's SW1 or SW2 pin. The high-side gate drive and return (switch node) traces should be routed on top of each other on adjacent layers to minimize inductance. These traces swing between V_{IN} and ground and should be routed away from low-voltage and noise-sensitive analog etch or components. The low-side MOSFET return path is power ground. High di/dt currents flow in the low-side gate drive and return paths. These must be kept away from noise sensitive signal traces and signal ground planes.

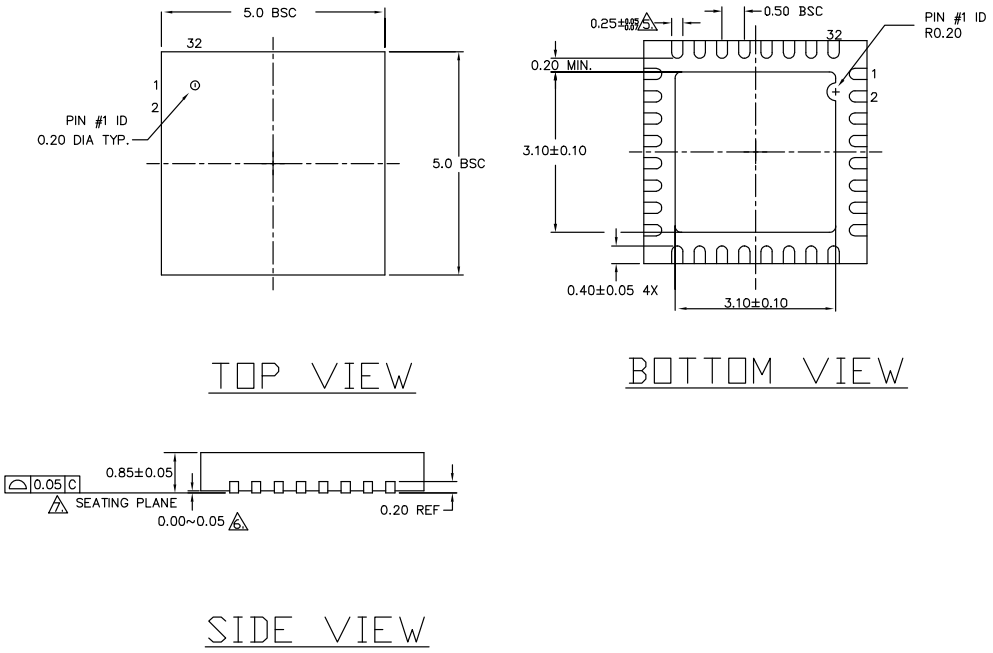
High di/dt Moderate di/dt DC

Ceramic capacitors are recommended for most decoupling and filtering applications because of their low impedance and small size. Depending on the application, most dielectrics (X5R, X7R, NPO) are acceptable, however, Z5U type ceramic capacitor dielectrics are not recommended due to their large change in capacitance over temperature and voltage.

Design and Layout Checklist

- Ceramic capacitor placed between the HS FET drain and the LSFET source.
- MOSFET gate drive traces must be low inductance and routed away from noise sensitive analog signals, components and ground planes.
- The signal and power ground planes must be separated to prevent high current and fast switching signals from interfering with the low level, noise sensitive analog signals. These planes should be connected at only 1 point, next to the MIC2155/6 controller.
- The following signals and their components should be decoupled or referenced to the power ground plane: VIN1, VIN2, VDD, PGND1, PGND2
- These analog signals should be referenced or decoupled to the analog ground plane: AVDD, SYNC, EN, SS, PGOOD, COMP1, COMP2, FB2, EA2, VOUT, FB1, AGND
- Place the current sharing RC components (that connect across the inductor) and any related filtering components close to the FB2, EA2+ and VOUT pins (18, 17, 20). The traces connecting the inductors and these components should be routed close together to minimize pickup or EMI radiation.
- Place the overcurrent sense resistor close to the CS1 pin (pin 4). The trace coming from the switch node to this resistor has high dv/dt and should be routed away from other noise sensitive components and traces.
- The remote sense traces must be routed close together or on adjacent layers to minimize noise pickup. The traces should be routed away from the switch node, inductors, MOSFETs and other high dv/dt or di/dt sources.

Package Information



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