# ISL9241

## Buck-Boost Configurable Battery Charger with SMBus Interface and USB Power Delivery

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The ISL9241 is a digitally configurable buck-boost battery charger that can support both Narrow Voltage Direct Charging (NVDC) and Hybrid Power Buck Boost (HPBB/Bypass) charging and switch between the modes using firmware control. Bypass mode is also supported using the firmware of the controller, which allows the adapter to provide power directly to the system. The ISL9241 provides charging functionality, system bus regulation, and protection features using only NFETs for tablet, Ultrabook, and notebook platforms. The advanced Renesas R3™ technology provides a high, light-load efficient Charging mode. The ISL9241 takes input power from a wide range of DC power sources (such as conventional AC/DC charger adapters, USB Type-C Power ports, and travel adapters) and safely charges battery packs with up to 4-series cell Li-ion batteries.

The system power can be provided from the adapter, battery, or a combination of both. The reconfigurable internal registers of the charger allow the use of a smaller inductor for the HPBB mode to achieve higher efficiencies across multiple power levels. The ISL9241 can operate with only a battery, only an adapter, or both connected. For Intel IMVP compliant systems, the ISL9241 includes System Power monitor (PSYS) functionality, which provides an analog signal representing total platform power. The PSYS output connects to a wide range of IMVP core regulators to provide an IMVP compliant power domain function. The ISL9241 supports reverse buck, boost, or buck-boost operation to the adapter port (OTG mode) from 2- to 4-cell batteries. This allows configurations to support USB-C Power Delivery (PD) output for Programmable Power Supply (PPS) ports. The ISL9241 serial communication uses SMBus/$I^2C$, which allows programming of many key parameters to deliver a customized solution.

## Features

- Buck-boost NVDC or hybrid power (turbo boost) charger for 2-, 3-, or 4-cell Li-ion batteries using all NFET transistors
- Input voltage range: 3.9V to 23.4V (no dead zone)
- System/battery output voltage: 3.9V to 18.304V
- Bypass mode supported to connect system to adapter
- Autonomous charging option (automatic end of charging)
- Adapter current and battery current monitor (AMON/BMON)
- PROCHOT# open-drain output, IMVP compliant
- System power monitor PSYS output, IMVP8/9 compliant
- Internal 8-bit ADC for monitoring key parameters
- USB-C PD Fast Role Swap support and PPS support
- Independent compensation pins for forward and reverse operation (OTG) modes
- Supports supplemental power (Intel $V_{MIN}$ active protection)
- Battery Ship mode: IC ultra-low power state
- Supports JEITA compliance using an NTC
- 4x4 32 Ld TQFN package

## Applications

- 2- to 4-cell tablets, notebooks, power banks, and any USB-C interface portable device requiring batteries

## Related Literature

For a full list of related documents visit our website:

- ISL9241 device page

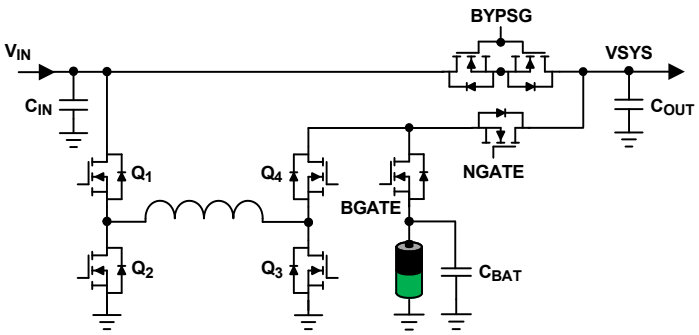



**Figure 1. Typical Application**

# Contents


**1. Overview . . . . . 4**
1.1 Simplified Application Circuits . . . . . 4
1.2 Block Diagram . . . . . 6
1.3 Ordering Information . . . . . 7
1.4 Pin Configuration . . . . . 7
1.5 Pin Descriptions . . . . . 8

**2. Specifications . . . . . 10**
2.1 Absolute Maximum Ratings . . . . . 10
2.2 Thermal Information . . . . . 10
2.3 Recommended Operating Conditions . . . . . 11
2.4 Electrical Specifications . . . . . 11
2.5 SMBus Timing Specification . . . . . 18

**3. Typical Performance . . . . . 19**

**4. General SMBus Architecture . . . . . 23**
4.1 Data Validity . . . . . 23
4.2 START and STOP Conditions . . . . . 23
4.3 Acknowledge . . . . . 24
4.4 SMBus Transactions . . . . . 24
4.5 Byte Format . . . . . 24
4.6 SMBus and $I^2C$ Compatibility . . . . . 24
4.7 ISL9241 SMBus Commands . . . . . 25

**5. ISL9241 Registers . . . . . 26**
5.1 Register Summary . . . . . 26
5.2 DAC Register Summary . . . . . 28
5.3 Control Registers . . . . . 29
5.4 Interrupt Functionality . . . . . 35
5.5 Information Registers . . . . . 36
5.6 ADC Registers . . . . . 38

**6. Application Information . . . . . 39**
6.1 Start-Up and ACOK . . . . . 39
6.2 Programming Resistor . . . . . 40
6.3 Charger Control Register Operations . . . . . 41
6.4 Reverse Modes . . . . . 46
6.5 Monitoring . . . . . 49
6.6 Protection . . . . . 52
6.7 Additional Features . . . . . 53

**7. Modulator Information . . . . . 55**
7.1 ISL9241 Buck-Boost Charger Modes of Operation . . . . . 55
7.2 Modulator Control Loops . . . . . 56
7.3 Buck Boost Configurable Charger . . . . . 59
7.4 R3 Modulator . . . . . 63

**8. Design Guide . . . . . 65**
8.1 Selecting the Sense Resistors . . . . . 65
8.2 Selecting the LC Output Filter . . . . . 65
8.3 Adapter Input Filter . . . . . 66
8.4 Selecting the Input Capacitor . . . . . 67
8.5 Selecting the Switching Power MOSFET . . . . . 68
8.6 Selecting the Bootstrap Capacitor . . . . . 69
8.7 DCIN Filter . . . . . 69

**9. Layout . . . . . 70**

**10. Revision History . . . . . 72**

**11. Package Outline Drawing . . . . . 73**

# 1. Overview

## 1.1 Simplified Application Circuits

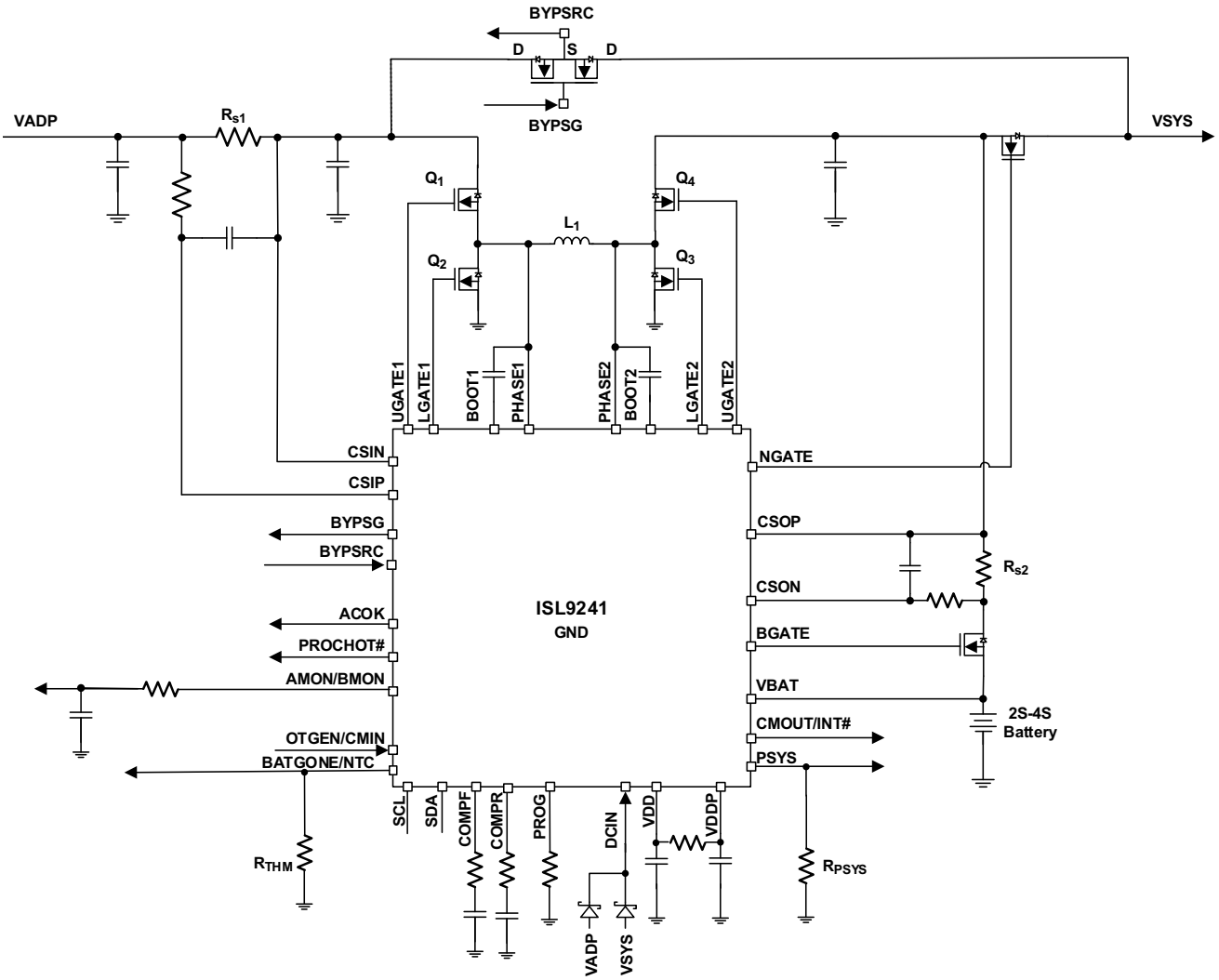



**Figure 2. NVDC Plus HPBB Simplified Application Diagram**

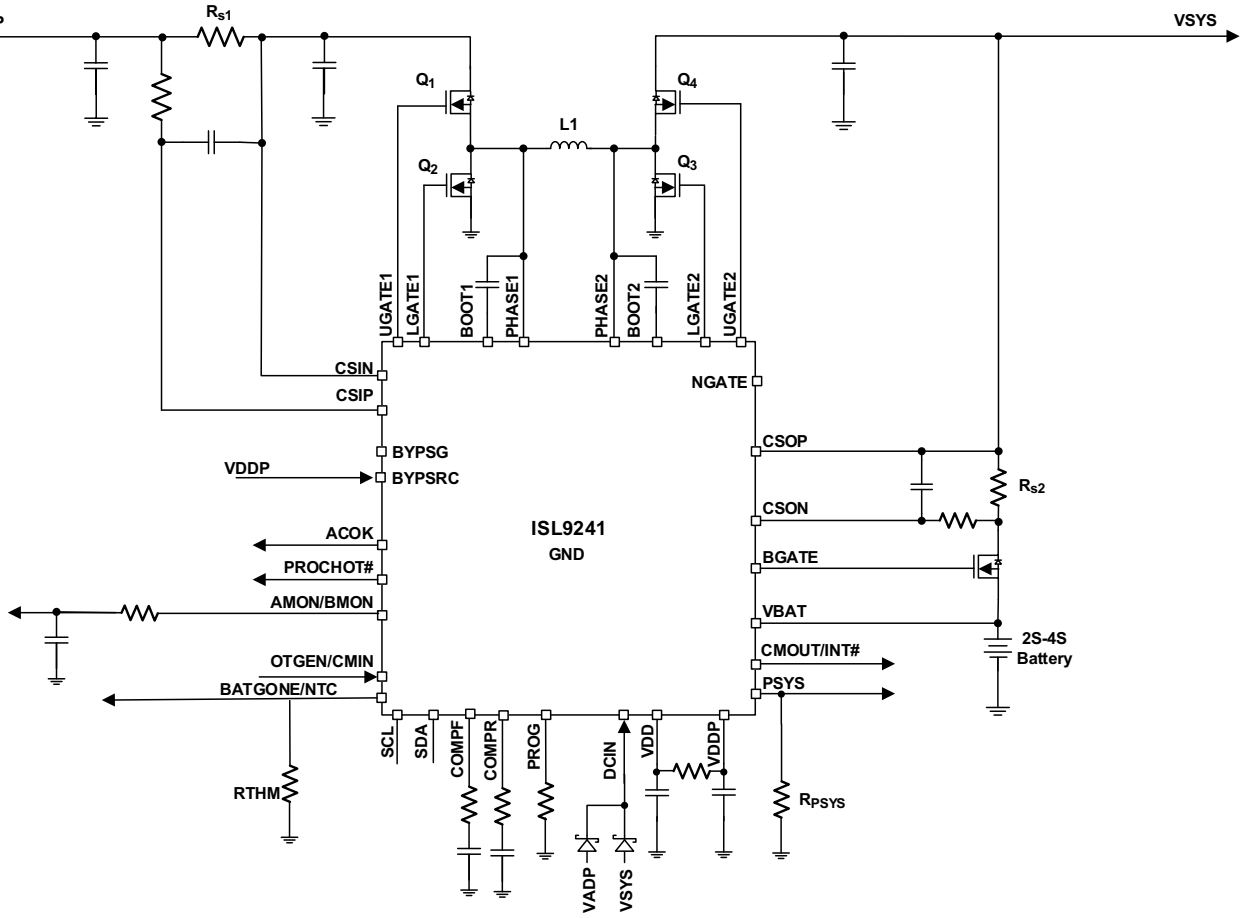



**Figure 3. NVDC Only Simplified Application Diagram**

## 1.2 Block Diagram

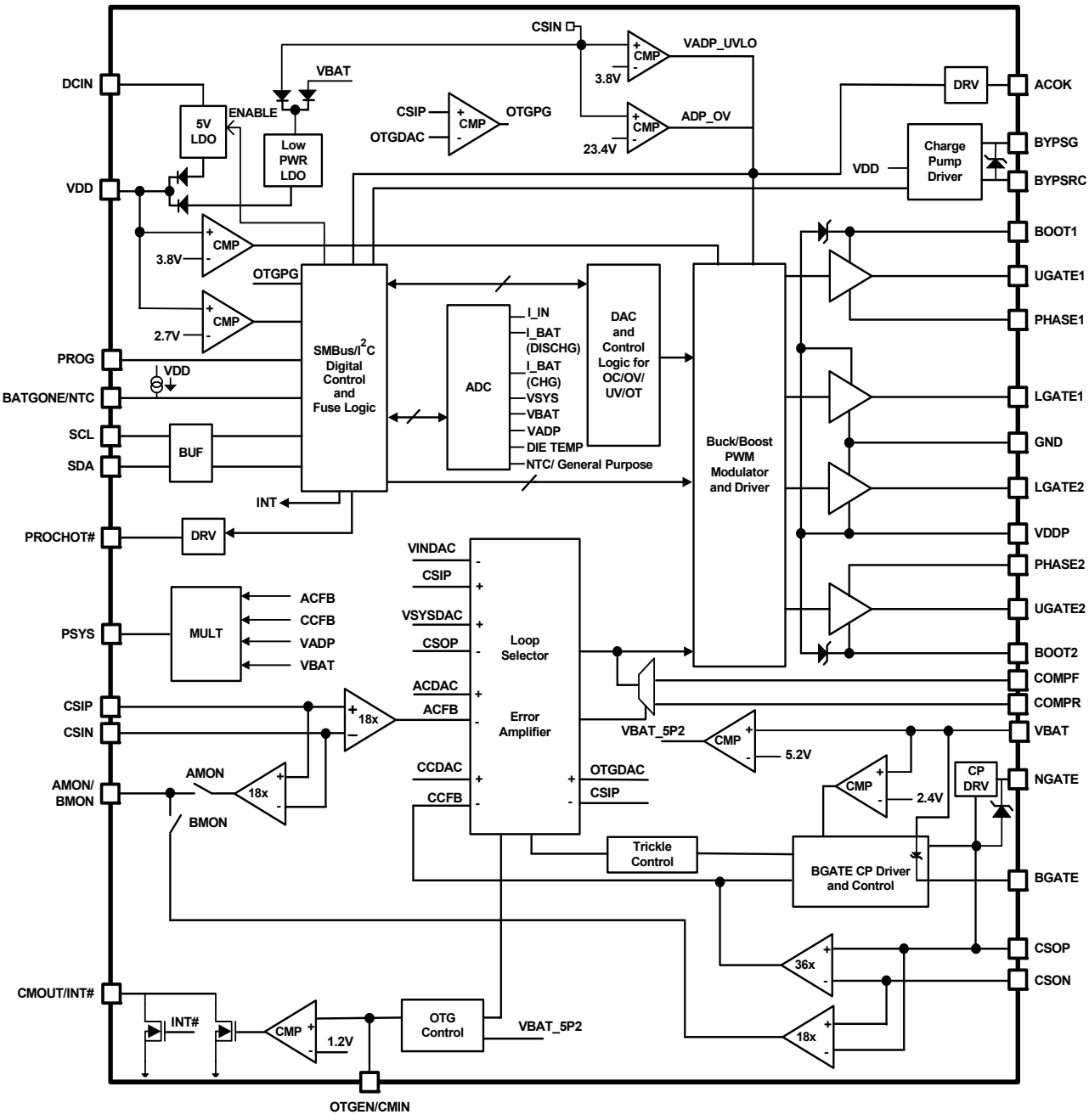



**Figure 4. Block Diagram**

## 1.3 Ordering Information

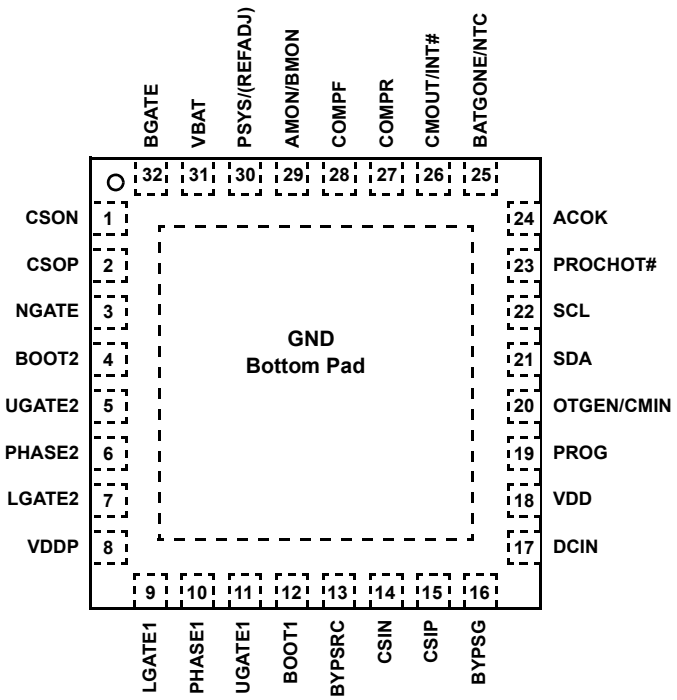
| Part Number (Notes 2, 3) | Part Marking | Temp. Range (°C) | Tape and Reel (Units) (Note 1) | Package (RoHS Compliant) | Pkg. Dwg. # |
|---|---|---|---|---|---|
| ISL9241HRTZ | 9241H | -10 to +100 | - | 32 Ld 4x4 TQFN | L32.4x4D |
| ISL9241HRTZ-T | 9241H | -10 to +100 | 6k | 32 Ld 4x4 TQFN | L32.4x4D |
| ISL9241HRTZ-TK | 9241H | -10 to +100 | 1k | 32 Ld 4x4 TQFN | L32.4x4D |
| ISL9241HRTZ-T7A | 9241H | -10 to +100 | 250 | 32 Ld 4x4 TQFN | L32.4x4D |
| ISL9241IRTZ | 9241I | -40 to +100 | - | 32 Ld 4x4 TQFN | L32.4x4D |
| ISL9241IRTZ-T | 9241I | -40 to +100 | 6k | 32 Ld 4x4 TQFN | L32.4x4D |
| ISL9241IRTZ-TK | 9241I | -40 to +100 | 1k | 32 Ld 4x4 TQFN | L32.4x4D |
| ISL9241EVAL1Z | Evaluation Board | | | | |

**Notes:**

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL9241 device page. For more information about MSL, see TB363.

## 1.4 Pin Configuration

32 Ld 4x4 TQFN
Top View



## 1.5 Pin Descriptions

| Pin Number | Pin Name | Description |
|---|---|---|
| Bottom Pad | GND | Signal common to the IC. Unless otherwise stated, signals are referenced to the GND pin. Use the bottom pad as the thermal pad for heat dissipation. |
| 1 | CSON | Battery current sense “–” input. Connect to the battery current resistor negative input. Place a ceramic capacitor between CSOP to CSON to provide Differential mode filtering. |
| 2 | CSOP | Battery current sense “+” input. Connect to the battery current resistor positive input. Place a ceramic capacitor between CSOP to CSON to provide Differential mode filtering. Reference input for NGATE. Sense node for VSYS voltage. Use a Kelvin line between the VSYS sense point and the CSOP pin. |
| 3 | NGATE | Gate drive output of the N-channel MOSFET. When NGATE is turned on, it is pumped 5V above CSOP. If the NGATE FET is not populated, leave this pin floating. |
| 4 | BOOT2 | High-side MOSFET $Q_4$ gate driver supply. Connect a 0.47µF (25V) MLCC capacitor across the BOOT2 and PHASE2 pins. This boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT2 pins when the PHASE2 pin drops below VDDP minus the voltage drop across the internal boot diode. The bootstrap capacitor must have an effective capacitance higher than 0.25µF at 5V and x50 effective high-side MOSFET gate capacitance. |
| 5 | UGATE2 | High-side MOSFET $Q_4$ gate drive. |
| 6 | PHASE2 | Current return path for the high-side MOSFET $Q_4$ gate drive. Connect this pin to the node consisting of the high-side MOSFET $Q_4$ source, the low-side MOSFET $Q_3$ drain, and one terminal of the inductor. |
| 7 | LGATE2 | Low-side MOSFET $Q_3$ gate drive. |
| 8 | VDDP | Power supply for the gate drivers. Connect to the VDD pin through a resistor and a 4.7µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the Boot pin at 5V. |
| 9 | LGATE1 | Low-side MOSFET $Q_2$ gate drive. |
| 10 | PHASE1 | Current return path for the high-side MOSFET Q1 gate drive. Connect this pin to the node consisting of the high-side MOSFET Q1 source, the low-side MOSFET Q2 drain, and the input terminal of the inductor. |
| 11 | UGATE1 | High-side MOSFET Q1 gate drive. |
| 12 | BOOT1 | High-side MOSFET Q1 gate driver supply. Connect a 0.47µF (25V) MLCC capacitor across the BOOT1 and PHASE1 pins. The boot capacitor is charged through an internal boot diode connected from the VDDP to BOOT1 pins when the PHASE1 pin drops below VDDP minus the voltage drop across the internal boot diode. The bootstrap capacitor must have an effective capacitance higher than 0.25µF at 5V and x50 effective high side MOSFET gate capacitance. |
| 13 | BYPSRC | N-channel MOSFET source input reference for bypass FETs. If not populating bypass FETs, this pin must be tied to VDDP. |
| 14 | CSIN | Connect to the input current sense resistor negative input. Input for sensing input voltage and phase comparator. Also used for sensing $Q_1$ drain for the modulator and VIN in forward-modes and VOUT for the modulator in reverse-modes. Use a Kelvin line between the voltage sense point and the CSIN pin. |
| 15 | CSIP | Connect to the input current sense resistor positive input through a resistor. Place a ceramic capacitor between CSIP and CSIN to provide differential-mode filtering. |
| 16 | BYPSG | Gate drive output of the N-channel MOSFET bypass FETs, pumped 5V above BYPSRC. If bypass FETs are not populated, this pin can be left floating. |
| 17 | DCIN | Input of an internal LDO providing power to the IC. Connect a diode OR from the adapter and system outputs. Bypass this pin with an MLCC capacitor and a resistor for filtering. Connect a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connect a 4.7µF DCIN capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 20V. |
| 18 | VDD | Output of the internal LDO; provides the bias power for the internal analog and digital circuit. Connect a 4.7µF (10V) MLCC capacitor to GND. The capacitor must have an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the Boot pin at 5V.<br>If $V_{DD}$ is pulled below 2.5V, the ISL9241 resets all the SMBus register values to the default. |

| Pin Number | Pin Name | Description |
|---|---|---|
| 19 | PROG | A resistor from the PROG pin to GND sets the following configurations:<br>• Default number of battery cells in series<br>• Default switching frequency<br>• Default adapter current limit value<br>• PSYS or REFADJ functionality<br>See Table 13 on page 40 for programming options. |
| 20 | OTGEN/ CMIN | Input pin. OTG function enable pin or stand-alone comparator input pin.<br>Pull high to enable the OTG function. The OTG function is enabled when the control register is written to select OTG mode and when the battery voltage is above 5.2V.<br>When the OTG function is not selected, this pin is the general purpose stand-alone comparator input.<br>When configured properly, it is also used for fast role swap or supplemental mode control. |
| 21 | SDA | SMBus data I/O. Connect to the data line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification. |
| 22 | SCL | SMBus clock I/O. Connect to the clock line from the host controller or smart battery. Connect a 10k pull-up resistor according to the SMBus specification. |
| 23 | PROCHOT# | Open-drain output. Pulled low when ACHOT, DCHOT, or Low_VSYS are detected. IMVP compliant. Use SMBus commands to pull low with OTGHOT, BATGONE, ACOK, and the general purpose comparator (see Table 6 on page 32). |
| 24 | ACOK | Open-drain output. Adapter presence indicator output to indicate the adapter is ready with a fixed undervoltage threshold and a register for a programmable threshold. |
| 25 | BATGONE/ NTC | Input pin to the IC. Logic high on this pin indicates the battery has been removed. Logic low on this pin indicates the battery is present. BATGONE pin logic high (pull up to VDD) forces the BGATE FET to turn off in any circumstances.<br>A current source on this pin pulls it high if open, but if a battery is present with an NTC to GND (10kΩ at +25°C thermistor), the NTC resistor pulls down on the pin, indicating a battery is present. The pull-up current source is then used to generate a voltage on the NTC that is measured by the part to determine temperature.<br>If NTC and BATGONE are disabled, this pin can be used as a general ADC input.<br>For any pin that is hot-plugged, such as BATGONE/NTC, a 10kΩ resistor is required to reduce any negative voltage on the pin. |
| 26 | CMOUT/ INT# | Open-drain output. The interrupt function is an active-low output and the stand-alone comparator selectable output.<br>When configured, it is the general purpose comparator output.<br>When configured to disable the CMOUT function, it is used as an interrupt for other functions and goes low when an interrupt function is detected.<br>The interrupt status register must be read to clear the latch. |
| 27 | COMPR | Error amplifier output for Reverse/OTG mode. Connect a compensation network externally from COMPR to GND. |
| 28 | COMPF | Error amplifier output for forward/charging mode. Connect a compensation network externally from COMPF to GND. |
| 29 | AMON/ BMON | Adapter current, OTG output current, battery charging current, or battery discharging current monitor output.<br>$V_{AMON}$ = 18x ($V_{CSIP}$ - $V_{CSIN}$) for adapter current monitor<br>$V_{OTGCMON}$ = 18x ($V_{CSIN}$ - $V_{CSIP}$) for OTG output current monitor<br>$V_{BMON_DISCHARGING}$ = 18x ($V_{CSON}$ - $V_{CSOP}$) for battery discharging current monitor<br>$V_{BMON_CHARGING}$ = 36x ($V_{CSOP}$ - $V_{CSON}$) for battery charging current monitor<br>Add an RC filter from the AMON pin to ground. Filter value (4.5kΩ resistor and 220nF capacitor). |
| 30 | PSYS/ (REFADJ) | Current source output that indicates the whole platform power consumption.<br>(REFADJ - Separate pin functionality determined by the PROG pin. This pin is used as the feedback pin for current input to modify OTG output voltage by pushing/pulling current to support QC3.0 and other protocol controllers). |
| 31 | VBAT | Battery voltage sensing. Used for trickle charging detection, Ideal Diode mode control, and charge pump reference for BGATE. Connect a ceramic capacitor from VBAT to GND. |
| 32 | BGATE | Battery Gate drive output to the N-channel MOSFET connecting the system and the battery.<br>When BGATE turns on, it is pumped 5V above the VBAT input pin voltage. |

# 2. Specifications

## 2.1 Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| VDD, VDDP | -0.3 | +6.5 | V |
| COMPF, COMPR, OTGEN/CMIN, BATGONE, PROG | | | |
| ACOK, AMON/BMON, PSYS | | | |
| SCL, SDA, PROCHOT#, CMOUT/INT# | | | |
| (BYPSG - BYPSRC), (NGATE - CSOP), (BGATE - VBAT) | | | |
| (BOOT1 - PHASE1), (BOOT2 - PHASE2) | | | |
| BOOT1 | -0.3 | +33 | V |
| BOOT2, CSIP, CSIN, DCIN, BYPSRC | -0.3 | +30 | V |
| (BOOT1 - VDDP), (BOOT2 - VDDP) | -0.9 | +27 | V |
| (BOOT1 - UGATE1), (BOOT2 - UGATE2) | -0.3, -2 (<20ns) | +6.5 | V |
| LGATE1, LGATE2 | | | |
| (VDDP - LGATE1), (VDDP - LGATE2) | | | |
| (UGATE1 - PHASE1), (UGATE2 - PHASE2) | | | |
| PHASE1 | -0.3, -2 (<20ns) | +30 | V |
| PHASE2 | -0.3, -2 (<20ns) | +24 | V |
| VBAT, CSOP, CSON | -0.3 | +24 | V |
| (CSIP - CSIN), (CSOP - CSON) | -0.3 | +0.3 | V |
| **ESD Ratings** | **Value** | | **Unit** |
| Human Body Model (Tested per JS-001-2017) | 2 | | kV |
| Machine Model (Tested per JESD22-A115C) | 200 | | V |
| Charged Device Model (Tested per JS-002-2014) | 750 | | V |
| Latch-Up (Tested per JESD78E; Class 2, Level A) | 100 | | mA |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

## 2.2 Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 32 Ld TQFN Package (Notes 4, 5) | 37 | 1.5 |

**Notes:**

4. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
5. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Junction Temperature Range ($T_J$) | -40 | +125 | °C |
| Storage Temperature Range ($T_S$) | -65 | +150 | °C |
| Pb-Free Reflow Profile | see TB493 | | |

## 2.3 Recommended Operating Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| **Ambient Temperature** | | | |
| HRTZ | -10 | +100 | °C |
| IRTZ | -40 | +100 | °C |
| **Junction Temperature** | | | |
| HRTZ | -10 | +125 | °C |
| IRTZ | -40 | +125 | °C |
| Adapter Voltage | +5 | +23 | V |

## 2.4 Electrical Specifications

Operating conditions: CSIP = CSIN = 5V and 20V, $V_{SYS}$ = $V_{BAT}$ = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified.**

| Parameter | Symbol | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| **UVLO/ACOK** | | | | | | |
| $V_{ADP}$ (CSIN) ACOK threshold (Note 7) | VADP_ACOK_r | CSIN = ADP | **3.51** | 3.6 | **3.69** | V |
| $V_{ADP}$ (CSIN) ACOK hysteresis (Note 7) | VADP_ACOK_h | | **60** | 120 | **180** | mV |
| $V_{BAT}$ 5P2V Rising | VBAT_5P2_r | | **4.95** | 5.20 | **5.65** | V |
| $V_{BAT}$ 5P2V Hysteresis | VBAT_5P2_h | | | 490 | | mV |
| $V_{DD}$ 2P7 POR Falling Threshold | VDD_2P7_f | SMBus and BGATE/BMON Active | **2.50** | 2.70 | **2.9** | V |
| $V_{DD}$ 2P7 POR Hysteresis | VDD_2P7_h | | | 150 | | mV |
| $V_{DD}$ 3P8 POR Rising | VDD_3P8_r | Modulator and Gate Driver Active | **3.6** | 3.8 | **4** | V |
| $V_{DD}$ 3P8 POR Hysteresis | VDD_3P8_h | | | 150 | | mV |
| ACOK Input Leakage Current | | | | | **1** | µA |
| ACOK, Output Sink Current | | $V_{ACOK}$ = 0.4V | **4** | | | mA |
| **Linear Regulator** | | | | | | |
| $V_{DD}$ Output Voltage | $V_{DD}$ | 6V < $V_{DCIN}$ < 23V, no load | **4.5** | 5.0 | **5.5** | V |
| $V_{DD}$ Dropout Voltage | VDD_dp | 30mA, $V_{DCIN}$ = 4V | | 85 | | mV |
| $V_{DD}$ Overcurrent Threshold | VDD_OC | HRTZ | **80** | 115 | **165** | mA |
| | | IRTZ | **80** | 115 | **170** | mA |

Operating conditions: CSIP = CSIN = 5V and 20V, $V_{SYS}$ = $V_{BAT}$ = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

| Parameter | Symbol | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| Battery Current | $I_{BAT1}$ | Battery only, BGATE off, NGATE off, GPCOMP off, PSYS OFF, BMON OFF, $V_{BAT}$ = 8.4V, DCIN current comes from battery, $I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN}$ | **5** | 20 | **30** | µA |
| | $I_{BAT2}$ | Battery only, BGATE normal, NGATE on, GPCOMP on, PSYS OFF, BMON OFF, $V_{BAT}$ = 16.8V, DCIN current comes from battery, $I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN}$ | **15** | 30 | **55** | µA |
| | $I_{BAT3}$ | Battery only, BGATE normal, NGATE on, GPCOMP on, PSYS ON, BMON ON, ADC on $V_{BAT}$ = 16.8V, DCIN current comes from battery, $I_{BAT} = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN}$ | **700** | 1100 | **1200** | µA |
| | $I_{Q1}$ | VSYS state, no switching $V_{BAT}$ = 12.6V,$V_{ADP}$ = 20V $I_Q = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{PH1} + I_{PH2} + I_{CSIP} + I_{CSIN} + I_{BYPSRC}$ | **2** | 2.2 | **2.35** | mA |
| | $I_{Q2}$ | OTG State, no switching $V_{BAT}$ = 8.4V, $V_{OTG}$ = 5V $I_Q = I_{VBAT} + I_{CSOP} + I_{CSON} + I_{DCIN} + I_{PH1} + I_{PH2} + I_{CSIP} + I_{CSIN} + I_{BYPSRC}$ | **1.5** | 1.7 | **1.85** | mA |
| **Adapter Current Regulation, $R_{s1}$ = 20mΩ** | | | | | | |
| Adapter Current Accuracy | | $V_{CSIP} - V_{CSIN}$ = 80mV (4A) | **-2.25** | | **2.25** | % |
| | | $V_{CSIP} - V_{CSIN}$ = 40mV (2A) | **-2.5** | | **2.5** | % |
| | | $V_{CSIP} - V_{CSIN}$ = 10mV (0.5A) | **-10** | | **10** | % |
| Adapter Current PROCHOT# Threshold $R_{s1}$ = 20mΩ | $I_{ADP_HOT_TH10}$ | ACProchot = 0x1580H (5504mA) | **-1.5** | | **1.5** | % |
| | | ACProchot = 0x0A80H (2688mA) | **-3.0** | | **3.0** | % |
| | | ACProchot = 0x0400H (1024mA) | **-6.0** | | **6.0** | % |
| **System Voltage Regulation** | | | | | | |
| Maximum System Voltage Accuracy | | MaxSystemVoltage for 2-cell ($V_{CSOP}$ = 8.4V) (HRTZ) | **-0.6** | | **0.6** | % |
| | | MaxSystemVoltage for 3-cell and 4-cell ($V_{CSOP}$ = 12.6V and 16.8V) (HRTZ) | **-0.5** | | **0.5** | % |
| | | MaxSystemVoltage for 2-cell ($V_{CSOP}$ = 8.4V) (IRTZ) | **-0.7** | | **0.7** | % |
| | | MaxSystemVoltage for 3-cell and 4-cell ($V_{CSOP}$ = 12.6V and 16.8V) (IRTZ) | **-0.5** | | **0.5** | % |
| Minimum System Voltage Accuracy | | | **-3** | | **3** | % |
| Input Voltage Regulation Accuracy | | $V_{CSIN}$ = 4.096V | **3.98** | | **4.22** | V |
| **Charge Current Regulation, $R_{s2}$ = 10mΩ (Limits apply across temperature range of 0°C to +60°C)** | | | | | | |
| Charge Current Accuracy | | $V_{CSOP} - V_{CSON}$ = 60mV (6A) | -2 | | 2 | % |
| | | $V_{CSOP} - V_{CSON}$ = 20mV (2A) | -4 | | 4 | % |
| | | $V_{CSOP} - V_{CSON}$ = 10mV (1A) | -6 | | 6 | % |
| | | $V_{CSOP} - V_{CSON}$ = 5mV (0.5A) | -12 | | 12 | % |

Operating conditions: CSIP = CSIN = 5V and 20V, $V_{SYS}$ = $V_{BAT}$ = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

| Parameter | Symbol | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| **Trickle Charging Current Regulation, $R_{s2}$ = 10mΩ (Limits apply across temperature range of 0°C to +60°C)** | | | | | | |
| Trickle Charge Current Accuracy | | Control2 register Bit<15:13> = 001 | 20 | 64 | 100 | mA |
| | | Control2 register Bit<15:13> = 010 | 55 | 96 | 135 | mA |
| | | Control2 register Bit<15:13> = 011 | 80 | 128 | 170 | mA |
| | | Control2 register Bit<15:13> = 100 | 112 | 160 | 208 | mA |
| | | Control2 register Bit<15:13> = 101 | 134 | 192 | 250 | mA |
| | | Control2 register Bit<15:13> = 110 | 157 | 224 | 291 | mA |
| | | Control2 register Bit<15:13> = 111 | 180 | 256 | 333 | mA |
| End of Charge Current Accuracy when Using Autonomous Charging | EOC | Control7 register Bit<9:8> = 00 | 40 | 105 | 170 | mA |
| | | Control7 register Bit<9:8> = 01 | 5 | 55 | 120 | mA |
| | | Control7 register Bit<9:8> = 10 | 120 | 190 | 270 | mA |
| | | Control7 register Bit<9:8> = 11 | 75 | 145 | 230 | mA |
| Auto Recharge Threshold Relative to Maximum system voltage | ART | Two cell battery | | 430 | | mV |
| | | Three cell battery | | 600 | | mV |
| | | Four cell battery | | 700 | | mV |
| **Ideal Diode Mode** | | | | | | |
| Entering Ideal Diode Mode VSYS Voltage Threshold | | BGATE off, VSYS falling $V_{VBAT}$ - $V_{VSYS}$ | **110** | 180 | **255** | mV |
| Exiting Ideal Diode Mode Battery Discharging Current Threshold | | $R_{s2}$ = 10mΩ | **25** | 125 | **230** | mA |
| Exiting Ideal Diode Mode Battery Charging Current Threshold | | $R_{s2}$ = 10mΩ | **60** | 160 | **255** | mA |
| **AMON/BMON** | | | | | | |
| **Input Current Sense Amplifier, $R_{s1}$ = 20mΩ** | | | | | | |
| CSIP/CSIN Input Voltage Range | $V_{CSIP/N}$ | | **4** | | **23** | V |
| AMON Gain | | | | 17.97 | | V/V |
| AMON Accuracy $V_{AMON}$ = AMON gain x (CSIP - CSIN) | | $V_{CSIP}$ - $V_{CSIN}$ = 100mV (5A), CSIP = 5V to 20V | **-2.5** | | **2.5** | % |
| | | $V_{CSIP}$ - $V_{CSIN}$ = 20mV (1A), CSIP = 5V to 20V | **-5.5** | | **5.5** | % |
| | | $V_{CSIP}$ - $V_{CSIN}$ = 10mV (0.5A), CSIP = 5V to 20V | **-12** | | **12** | % |
| | | $V_{CSIP}$ - $V_{CSIN}$ = 2mV (0.1A), CSIP = 5V to 20V | **-55** | | **55** | % |
| Reverse AMON Gain | | | | 17.9 | | V/V |
| AMON Accuracy $V_{AMON}$ = AMON gain x (CSIN - CSIP) | | $V_{CSIN}$ - $V_{CSIP}$ = 80mV (4A), CSIP = 4V to 22V | **-3.5** | | **3.5** | % |
| | | $V_{CSIN}$ - $V_{CSIP}$ = 20mV (1A), CSIP = 4V to 22V | **-6.5** | | **6.5** | % |
| | | $V_{CSIN}$ - $V_{CSIP}$ = 10mV (0.5A), CSIP = 4V to 22V | **-12** | | **12** | % |
| | | $V_{CSIN}$ - $V_{CSIP}$ = 5.12mV (0.256A), CSIP = 4V to 22V | **-25** | | **25** | % |
| AMON Minimum Output Voltage | | $V_{CSIP}$ - $V_{CSIN}$ = 0V | | | **30** | mV |

Operating conditions: CSIP = CSIN = 5V and 20V, $V_{SYS}$ = $V_{BAT}$ = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

| Parameter | Symbol | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| **Discharge Current Sense Amplifier, $R_{s2}$ = 10mΩ** | | | | | | |
| BMON Gain (Battery Discharging) | | | | 17.97 | | V/V |
| BMON Accuracy $V_{BMON}$ = BMON Gain x ($V_{CSON}$ - $V_{CSOP}$) | | $V_{CSON}$ - $V_{CSOP}$ = 100mV (10A), $V_{CSON}$ = 8V | **-2** | | **2** | % |
| | | $V_{CSON}$ - $V_{CSOP}$ = 20mV (2A), $V_{CSON}$ = 8V | **-6** | | **6** | % |
| | | $V_{CSON}$ - $V_{CSOP}$ = 10mV (1A), $V_{CSON}$ = 8V | **-10** | | **10** | % |
| | | $V_{CSON}$ - $V_{CSOP}$ = 6mV (0.6A), $V_{CSON}$ = 8V | **-20** | | **20** | % |
| **BMON Charging Accuracy, $R_{s2}$ = 10mΩ (Limits apply across temperature range of 0°C to +60°C)** | | | | | | |
| BMON Gain (Battery Charging) | | | | 35.78 | | V/V |
| BMON Accuracy $V_{BMON}$ = BMON Gain x ($V_{CSON}$ - $V_{CSOP}$) | | $V_{CSOP}$ - $V_{CSON}$ = 60mV (6A), $V_{CSON}$ = 8V | -3 | | 3 | % |
| | | $V_{CSOP}$ - $V_{CSON}$ = 40mV (4A), $V_{CSON}$ = 8V | -4 | | 4 | % |
| | | $V_{CSOP}$ - $V_{CSON}$ = 10mV (1A), $V_{CSON}$ = 8V | -10 | | 10 | % |
| | | $V_{CSOP}$ - $V_{CSON}$ = 5mV (0.5A), $V_{CSON}$ = 8V | -25 | | 25 | % |
| BMON Minimum Output Voltage | | $V_{CSOP}$ - $V_{CSON}$ = 0V | | | 30 | mV |
| Discharging Current PROCHOT# Threshold | $I_{DIS_HOT_TH}$ | $R_{s2}$ = 10mΩ, DCProchot = 2.048A | 1.77 | 2.08 | 2.39 | A |
| Discharging Current PROCHOT# Threshold, Battery Only | $I_{DIS_HOT_TH}$ | $R_{s2}$ = 10mΩ, DCProchot = 12A | 9.4 | 13 | 17 | A |
| | | $R_{s2}$ = 10mΩ, DCProchot = 6A | 4.5 | 6 | 8 | A |
| AMON/BMON Source Resistance | | (Note 7) | | | 5 | Ω |
| AMON/BMON Sink Resistance | | (Note 7) | | | 5 | Ω |
| **BATGONE and OTGEN** | | | | | | |
| OTGEN High-Level Input Voltage | | | **0.9** | | | V |
| OTGEN Low-Level Input Voltage | | | | | **0.4** | V |
| BATGONE High-Level Input Voltage | | | **$V_{DD}$ - 0.6** | | | V |
| BATGONE Low-Level Input Voltage | | | | | **$V_{DD}$ - 1.2** | V |
| Pull-Up Current | | $V_{BATGONE}$ = 3.3V, 5V; $V_{OTGEN}$ = 3.3V, 5V | | 1 | | µA |
| NTC Step1 Pull-Up Current | | | **62** | 65 | **68** | µA |
| NTC Step2 Pull-Up Current | | | **126** | 130 | **134** | µA |
| NTC Step3 Pull-Up Current | | | **250** | 260 | **270** | µA |
| **PROCHOT#** | | | | | | |
| PROCHOT# Debounce Time (Note 7) | | PROCHOT# Debounce register Bit<1:0> = 11 | **0.85** | 1 | **1.15** | ms |
| | | PROCHOT# Debounce register Bit<1:0> = 10 | **425** | 500 | **575** | µs |
| PROCHOT# Duration Time (Note 7) | | PROCHOT# Duration register Bit<2:0> = 011 | **8.5** | 10 | **11.5** | ms |
| | | PROCHOT# Duration register Bit<2:0> = 001 | **17** | 20 | **23** | ms |

Operating conditions: CSIP = CSIN = 5V and 20V, $V_{SYS}$ = $V_{BAT}$ = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

| Parameter | Symbol | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| Low VSYS PROCHOT# Trip Falling Threshold | $V_{LOW_VSYS_HOT}$ | Control1 register Bit<2:0> = 000 | **5.3** | 5.5 | **5.7** | V |
| | | Control1 register Bit<2:0> = 001 | **5.5** | 5.7 | **5.9** | V |
| | | Control1 register Bit<2:0> = 010 | **5.7** | 5.9 | **6.1** | V |
| | | Control1 register Bit<2:0> = 011 | **5.9** | 6.1 | **6.3** | V |
| | | Control1 register Bit<2:0> = 100 | **6.1** | 6.3 | **6.5** | V |
| | | Control1 register Bit<2:0> = 101 | **6.3** | 6.5 | **6.7** | V |
| | | Control1 register Bit<2:0> = 110 | **6.5** | 6.7 | **6.9** | V |
| | | Control1 register Bit<2:0> = 111 | **6.7** | 6.9 | **7.1** | V |
| PROCHOT# Input Leakage Current | | | | | **1** | µA |
| PROCHOT#, Output Sink Current | | $V_{PROCHOT}$ = 0.4V | **4** | | | mA |
| **PSYS** | | | | | | |
| PSYS Output Current (Note 7)<br>$R_{s1}$ = 20mΩ<br>$R_{s2}$ = 10mΩ<br>Control3 Bit<9:8> = 11<br>Control4 Bit<11> = 0<br><br>$I_{PSYS}$ = 0.646 x Power + 0.959 | $I_{PSYS}$ | $V_{CSIP}$ = 12V, $V_{CSIP - CSIN}$ = 80mV,<br>$V_{BAT}$ = 12V, $V_{CSOP - CSON}$ = 0mV | **-5** | | **5** | % |
| | | $V_{CSIP}$ = 20V, $V_{CSIP - CSIN}$ = 0mV,<br>$V_{BAT}$ = 8.4V, $V_{CSOP - CSON}$ = 50mV | **-5** | | **5** | % |
| | | $V_{CSIP}$ = 20V, $V_{CSIP - CSIN}$ = 80mV,<br>$V_{BAT}$ = 12V, $V_{CSOP - CSON}$ = 20mV | **-5** | | **5** | % |
| Maximum PSYS Output Voltage | $V_{PSYS_MAX}$ | | **4** | | | V |
| PSYS Gain<br>$R_{s1}$ = 20mΩ<br>$R_{s2}$ = 10mΩ<br>Control4 Bit<11> = 0 (2:1) | $V_{PSYS_G}$ | Control3 Bit<9:8> = 11 (default)<br>0 < $I_{PSYS}$ < 80µA, Offset = 0.959µA | | 0.646 | | µA/W |
| | | Control3 Bit<9:8> = 10<br>0 < $I_{PSYS}$ < 90µA, Offset = 0.626µA | | 0.431 | | µA/W |
| | | Control3 Bit<9:8> = 01<br>0 < $I_{PSYS}$ < 100µA, Offset = 2.047µA | | 1.315 | | µA/W |
| | | Control3 Bit<9:8> = 00<br>0 < $I_{PSYS}$ < 110µA, Offset = 1.352µA | | 0.896 | | µA/W |
| PSYS Gain<br>$R_{s1}$ = 10mΩ<br>$R_{s2}$ = 10mΩ<br>Control4 Bit<11> = 1 (1:1) | $V_{PSYS_G}$ | Control3 Bit<9:8> = 11 (default)<br>0 < $I_{PSYS}$ < 80µA, Offset =1.265µA | | 0.653 | | µA/W |
| | | Control3 Bit<9:8> = 10<br>0 < $I_{PSYS}$ < 90µA, Offset = 0.831µA | | 0.434 | | µA/W |
| | | Control3 Bit<9:8> = 01<br>0 < $I_{PSYS}$ < 100µA, Offset = 2.654µA | | 1.337 | | µA/W |
| | | Control3 Bit<9:8> = 00<br>0 < $I_{PSYS}$ < 110µA, Offset = 1.773µA | | 0.907 | | µA/W |
| **OTG** | | | | | | |
| OTG Voltage | | OTG voltage register,<br>DAC = Default = 0x0D08h | **4.93** | 5.0 | **5.25** | V |
| OTG Current (5V to 12V) | | $R_{s1}$ = 20mΩ<br>OTG current register = 512mA | **450** | 512 | **585** | mA |
| | | $R_{s1}$ = 20mΩ<br>OTG current register = 1024mA | **960** | 1024 | **1100** | mA |
| | | $R_{s1}$ = 20mΩ<br>OTG current register = 4096mA | **3975** | 4096 | **4240** | mA |

Operating conditions: CSIP = CSIN = 5V and 20V, $V_{SYS}$ = $V_{BAT}$ = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

| Parameter | Symbol | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| Fast Role Swap Digital Filter | | When configured OTG_EN 0 ≥ 1 (Note 7) | | | 1 | µs |
| Analog Support of OTG Output | | When configured OTG_EN = 1 (Note 7) | | | **150** | µs |
| **General Purpose Comparator** | | | | | | |
| General Purpose Comparator Rising Threshold | | Reference = 1.2V | **1.15** | 1.2 | **1.25** | V |
| | | Reference = 2V (not available in Battery mode) | **1.95** | 2 | **2.05** | V |
| General Purpose Comparator Hysteresis | | Reference = 1.2V | **25** | 40 | **50** | mV |
| | | Reference = 2V (not available in Battery mode) | 25 | 40 | **50** | mV |
| CMOUT/INT# Input Leakage Current | | | | | **1** | µA |
| CMOUT/INT#, Output Sink Current | | $V_{CMOUT}$ = 0.4V | **4** | | | mA |
| **Protection** | | | | | | |
| VSYS Overvoltage Rising Threshold | | MaxSystemVoltage register value = 8.4V | **8.9** | 9.15 | **9.35** | V |
| VSYS Overvoltage Hysteresis | | | **250** | 400 | **550** | mV |
| VSYS OK Threshold | | | **0.45** | 0.6 | **0.75** | V |
| VSYS OK Source Current | | | | 10 | | mA |
| Adapter Way Overcurrent Rising Threshold | | $R_{s1}$ = 20mΩ | **7.5** | 12 | **25** | A |
| Battery Discharge Way Overcurrent Rising Threshold | | $R_{s2}$ = 10mΩ | **9** | 20 | **38** | A |
| Over-Temperature Threshold (Note 7) | | | **140** | 150 | **160** | °C |
| Adapter Overvoltage Rising Threshold | | CSIN = ADP | **22.5** | 23.4 | **24** | V |
| Adapter Overvoltage Hysteresis | | | **300** | 400 | **500** | mV |
| OTG Undervoltage Falling Threshold | | OTG voltage setting = 5.004V Register 0x49 = 0xD08h | **3.45** | 3.80 | **4.25** | V |
| OTG Overvoltage Rising Threshold | | OTG voltage setting = 5.004V Register 0x49 = 0xD08h | **5.8** | 6.2 | **6.6** | V |
| **Oscillator** | | | | | | |
| Oscillator Frequency, Digital Core Only | | | **0.85** | 1 | **1.15** | MHz |
| Digital Debounce Time Accuracy (Note 7) | | | **-15** | | **15** | % |
| **Miscellaneous** | | | | | | |
| Switching Frequency Accuracy | | $V_{COMP}$ > 1.7V and not in period stretching | **-15** | | **15** | % |
| Battery Learn Mode Auto-Exit Threshold | | MinSystemVoltage = 5.376V Control1 register Bit<13> = 1 | **5.05** | 5.35 | **5.7** | V |
| Battery Learn Mode Auto-Exit Hysteresis (Note 7) | | | **180** | 330 | **480** | mV |

Operating conditions: CSIP = CSIN = 5V and 20V, $V_{SYS}$ = $V_{BAT}$ = CSOP = CSON = 8V, unless otherwise noted. **Boldface limits apply across the junction temperature range, -10°C to +125°C unless otherwise specified. (Continued)**

| Parameter | Symbol | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| **Gate Driver** | | | | | | |
| UGATE1 Pull-Up Resistance | $UG1_{RPU}$ | 100mA source current | | 800 | **1200** | mΩ |
| UGATE1 Source Current | $UG1_{SRC}$ | $V_{UGATE1}$ - $V_{PHASE1}$ = 2.5V | **1.3** | 2 | | A |
| UGATE1 Pull-Down Resistance | $UG1_{RPD}$ | 100mA sink current | | 350 | **475** | mΩ |
| UGATE1 Sink Current | $UG1_{SNK}$ | $V_{UGATE1}$ - $V_{PHASE1}$ = 2.5V | **1.9** | 2.8 | | A |
| LGATE1 Pull-Up Resistance | $LG1_{RPU}$ | 100mA source current | | 800 | **1200** | mΩ |
| LGATE1 Source Current | $LG1_{SRC}$ | $V_{LGATE1}$ - GND = 2.5V | **1.3** | 2 | | A |
| LGATE1 Pull-Down Resistance | $LG1_{RPD}$ | 100mA sink current | | 300 | **450** | mΩ |
| LGATE1 Sink Current | $LG1_{SNK}$ | $V_{LGATE1}$ - GND = 2.5V | **2.3** | 3.5 | | A |
| LGATE2 Pull-Up Resistance | $LG2_{RPU}$ | 100mA source current | | 800 | **1200** | mΩ |
| LGATE2 Source Current | $LG2_{SRC}$ | $V_{LGATE2}$ - GND = 2.5V | **1.3** | 2 | | A |
| LGATE2 Pull-Down Resistance | $LG2_{RPD}$ | 100mA sink current | | 300 | **450** | mΩ |
| LGATE2 Sink Current | $LG2_{SNK}$ | $V_{LGATE2}$ - GND = 2.5V | **2.3** | 3.5 | | A |
| UGATE2 Pull-Up Resistance | $UG2_{RPU}$ | 100mA source current | | 800 | **1200** | mΩ |
| UGATE2 Source Current | $UG2_{SRC}$ | $V_{UGATE2}$ - $V_{PHASE2}$ = 2.5V | **1.3** | 2 | | A |
| UGATE2 Pull-Down Resistance | $UG2_{RPD}$ | 100mA sink current | | 300 | **450** | mΩ |
| UGATE2 Sink Current | $UG2_{SNK}$ | $V_{UGATE2}$ - $V_{PHASE2}$ = 2.5V | **2.3** | 3.5 | | A |
| UGATE1 to LGATE1 Dead Time | $t_{UG1LG1DEAD}$ | | **10** | 20 | **40** | ns |
| LGATE1 to UGATE1 Dead Time | $t_{LG1UG1DEAD}$ | | **10** | 20 | **40** | ns |
| LGATE2 to UGATE2 Dead Time | $t_{LG2UG2DEAD}$ | | **10** | 20 | **40** | ns |
| UGATE2 to LGATE2 Dead Time | $t_{UG2LG2DEAD}$ | | **10** | 20 | **40** | ns |
| **Charge Pump Gate Drivers** | | | | | | |
| BYPSG Gate Drive Current | | BYPSG Off<br>BYPSG = $V_{BYPSRC}$ + 2V | **165** | 190 | **215** | µA |
| NGATE Gate Drive Current | | NGATE Off<br>NGATE = $V_{CSOP}$ + 2V | **165** | 190 | **215** | µA |
| BGATE Gate Drive Current | | BGATE Off<br>BGATE = $V_{VBAT}$ + 2V | **165** | 190 | **215** | µA |
| BYPSG Gate Drive Current | | BYPSG On<br>$V_{BYPSG}$ = $V_{BYPSRC}$ + 2V, $V_{BYPSRC}$ > 3.9V | **15** | 40 | **70** | µA |
| NGATE Gate Drive Current | | NGATE On<br>$V_{NGATE}$ = $V_{CSOP}$ + 2V, $V_{CSOP}$ > 3.9V | **15** | 40 | **70** | µA |
| BGATE Gate Drive Current | | BGATE On<br>$V_{BGATE}$ = $V_{VBAT}$ + 2V, $V_{VBAT}$ > 2.7V | **15** | 40 | **70** | µA |
| **SMBus** | | | | | | |
| SDA/SCL Input Low Voltage | | | | | **0.7** | V |
| SDA/SCL Input High Voltage | | | **1.5** | | | V |
| SDA/SCL Input Bias Current | | | | | **1** | µA |
| SDA, Output Sink Current | | $V_{SDA}$ = 0.4V, On | **4** | | | mA |

## 2.5 SMBus Timing Specification

| Parameters | Symbol | Test Conditions | Min (Note 6) | Typ | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| SMBus Frequency | $f_{SMB}$ | Supports Standard mode and Fast mode | **10** | | **400** | kHz |
| Bus Free Time | $t_{BUF}$ | | **4.7** | | | µs |
| Start Condition Hold Time from SCL | $t_{HD:STA}$ | | **4** | | | µs |
| Start Condition Set-Up Time from SCL | $t_{SU:STA}$ | | **4.7** | | | µs |
| Stop Condition Set-Up Time from SCL | $t_{SU:STO}$ | | **4** | | | µs |
| SDA Hold Time from SCL | $t_{HD:DAT}$ | | **300** | | | ns |
| SDA Set-Up Time from SCL | $t_{SU:DAT}$ | | **250** | | | ns |
| SCL Low Period | $t_{LOW}$ | For SMBus Standard mode | **4.7** | | | µs |
| SCL High Period | $t_{HIGH}$ | For SMBus Standard mode | **4** | | | µs |
| SMBus Inactivity Timeout | | Maximum charging period without a SMBus Write to MaxSystemVoltage or ChargeCurrent register when enabled | | 175 | | s |

**Notes:**

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Limits established by characterization and are not production tested.

# 3. Typical Performance

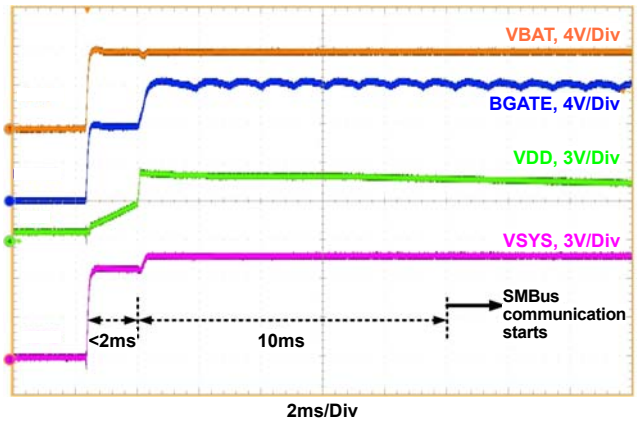



Figure 5. Start-Up Time with Battery for Communication

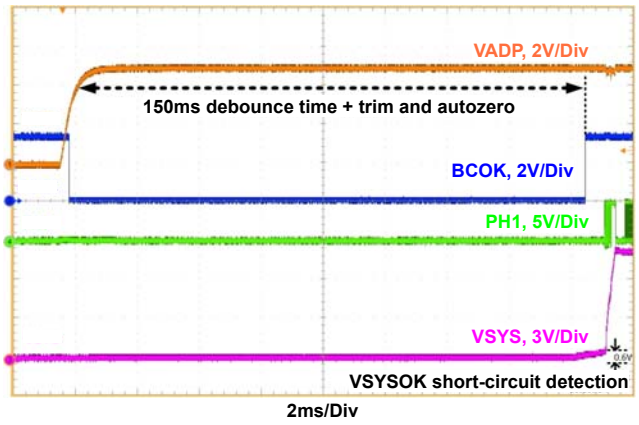



Figure 6. Start Up with 5V Adapter and ACOK Timing

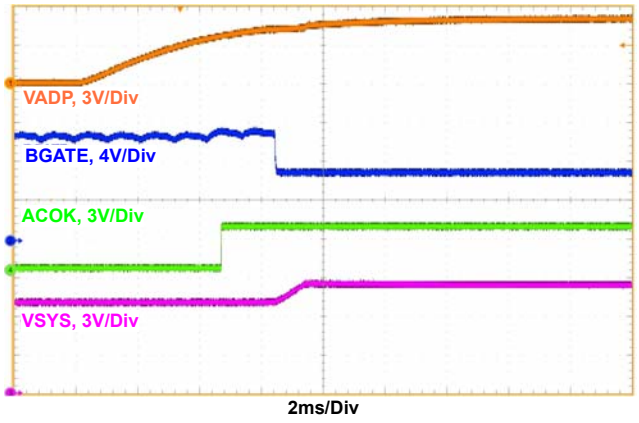



Figure 7. Start Up with Adapter and Battery. $V_{ADP}$ = 5V, MaxSystemVoltage = 8.384V, $V_{BAT}$ = 7V, Charge Current Limit = 0A

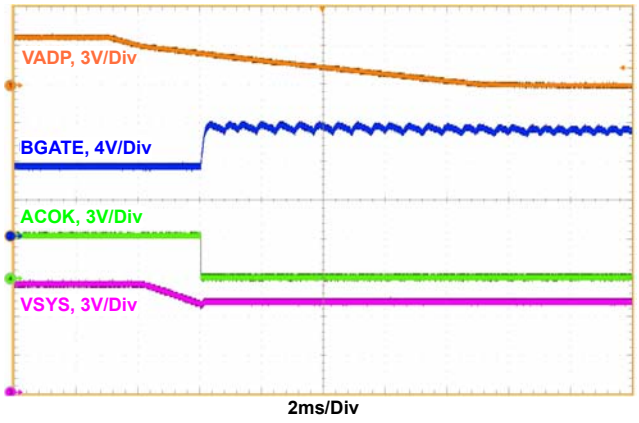



Figure 8. Adapter Removal. $V_{ADP}$ = 5V, MaxSystemVoltage = 8.384V, $V_{BAT}$ = 7V, Charge Current Limit = 0A, System Load = 20mA

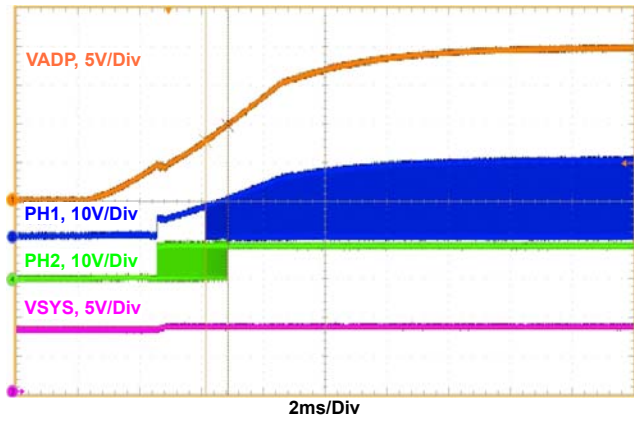



Figure 9. Adapter Voltage Ramp Up, Boost --> Buck_Boost -->Buck Operation Mode Transition

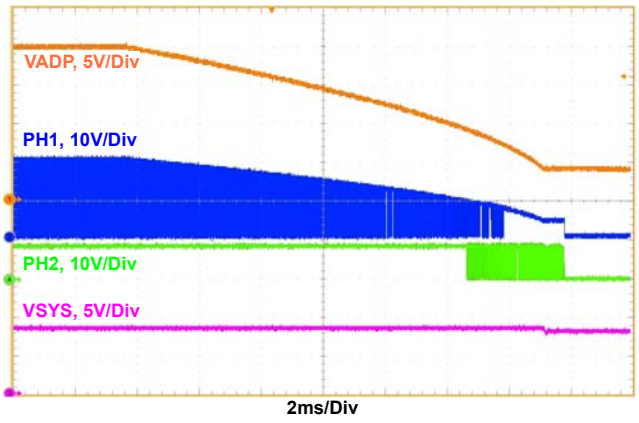



Figure 10. Adapter Voltage Ramp Down, Buck --> Buck_Boost --> Boost Operation Mode Transition

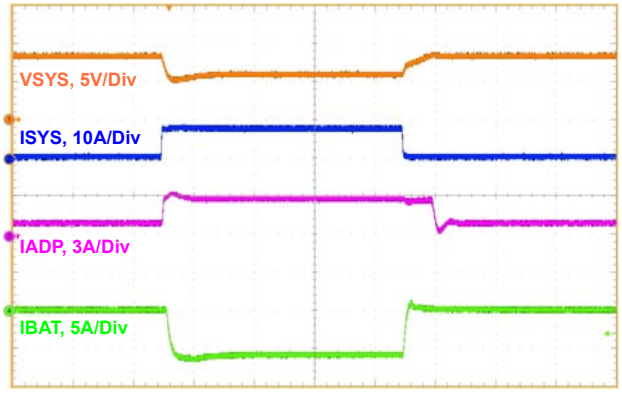



**Figure 11. Boost Mode, Output Voltage Loop to Adapter Current Loop Transition, $V_{ADP}$ = 5V, $V_{BAT}$ = 7V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 0A, System_load = 0.5A to 8A**

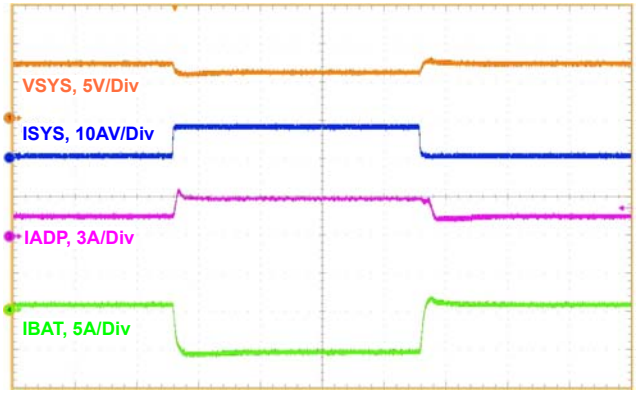



**Figure 12. Boost Mode, Charge Current Loop to Adapter Current Loop Transition, $V_{ADP}$ = 5V, $V_{BAT}$ = 7V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 0.5A, System_load = 0.5A to 8A**

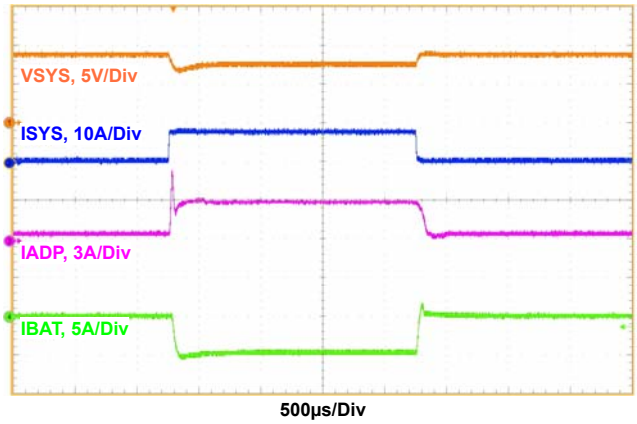



**Figure 13. Buck_Boost Mode, Output Voltage Loop to Adapter Current Loop Transition, $V_{ADP}$ = 9V, $V_{BAT}$ = 8.4V, MaxSystemVoltage = 8.8V, Adapter_current_limit = 3A, Charge_current = 0A, System_load = 0.5A to 8A**

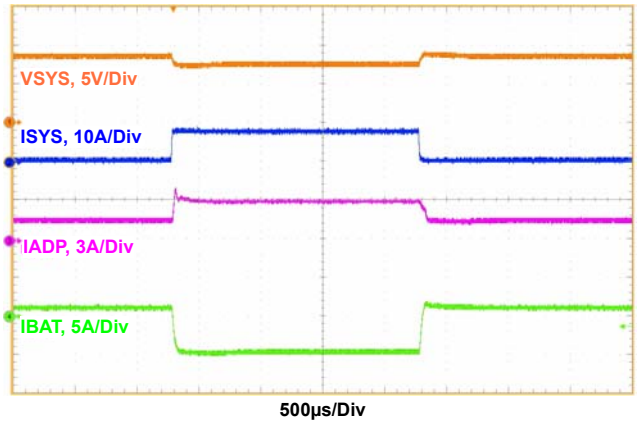



**Figure 14. Buck_Boost Mode, Charge Current Loop to Adapter Current Loop Transition, $V_{ADP}$ = 9V, $V_{BAT}$ = 8.4V, MaxSystemVoltage = 8.8V, Adapter_current_limit = 3A, Charge_current = 1A, System_load = 0.5A to 8A**

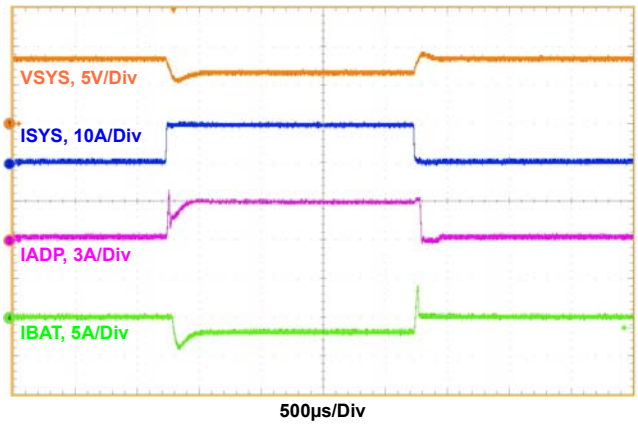



**Figure 15. Buck Mode, Output Voltage Loop to Adapter Current Loop Transition, $V_{ADP}$ = 20V, $V_{BAT}$ = 7V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 0A, System_load = 0.5A to 10A**

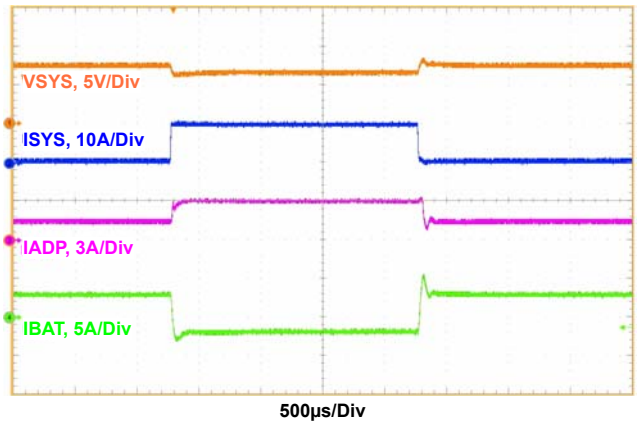



**Figure 16. Buck Mode, Charge Current Loop to Adapter Current Loop Transition, $V_{ADP}$ = 20V, $V_{BAT}$ = 7V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 3A, System_load = 0.5A to 10A**

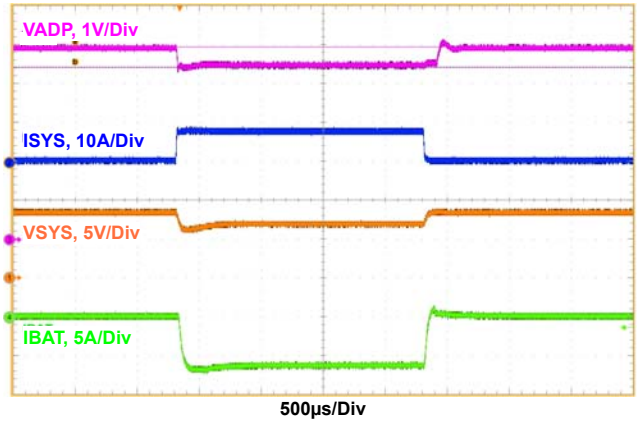



**Figure 17. Boost Mode, Output Voltage Loop to Input Voltage Loop Transition, $V_{ADP}$ = 5V, $V_{BAT}$ = 8V, MaxSystemVoltage = 8.384V, Charge_current = 0A, System_load = 0.5A to 8A, Input_voltage_dac = 4.437V**

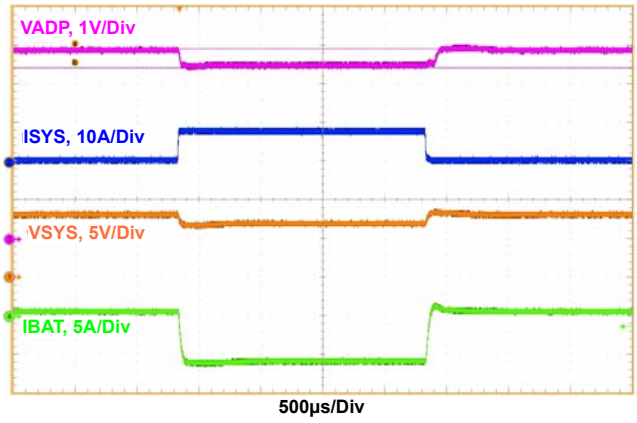



**Figure 18. Boost Mode, Charge Current Loop to Input Voltage Loop Transition, $V_{ADP}$ = 5V, $V_{BAT}$ = 8V, MaxSystemVoltage = 8.384V, Charge_current = 0.5A, System_load = 0.5A to 8A, Input_voltage_dac = 4.437V**

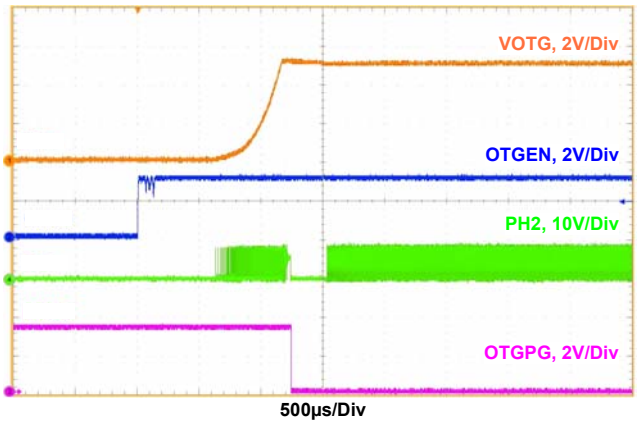



**Figure 19. OTG Mode Enable Using OTGEN Pin. $V_{BAT}$ = 8V, $V_{OTG}$ = 5V, General Purpose Comparator Disabled, OTGEN Control Bit Enabled**

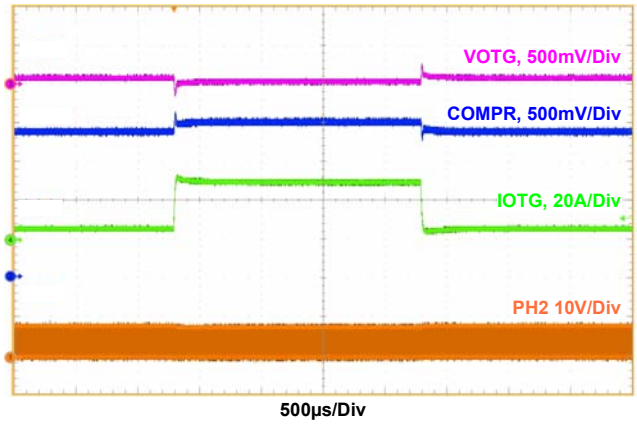



**Figure 20. OTG Mode Transient. $V_{BAT}$ = 8V, $V_{OTG}$ = 5V, OTG Current = 3.2A, Load = 0.5A to 3A**

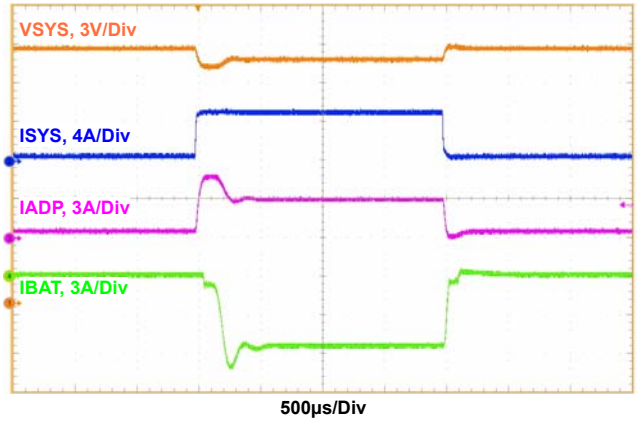



**Figure 21. Bypass (HPBB) Mode, Reverse Turbo Boost Enabled. Output Voltage Loop to Adapter Current Limit Loop Transition. $V_{ADP}$ = 20V, $V_{BAT}$ = 8V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 0A, System_load = 0.5A to 5A**

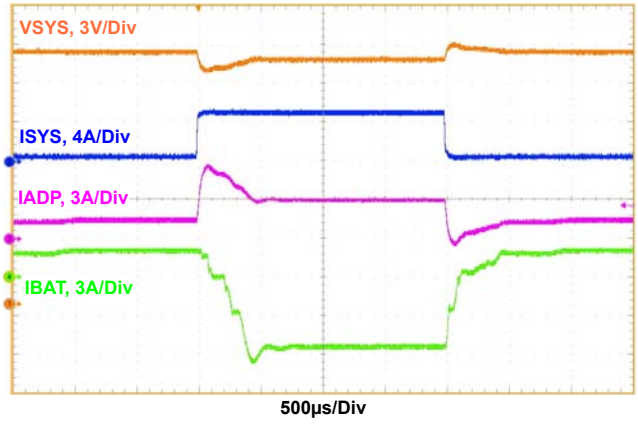



**Figure 22. Bypass (HPBB) Mode, Reverse Turbo Boost Enabled. Charge Current Loop to Adapter Current Limit Loop Transition. $V_{ADP}$ = 20V, $V_{BAT}$ = 8V, MaxSystemVoltage = 8.384V, Adapter_current_limit = 3A, Charge_current = 2A, System_load = 0.5A to 5A**

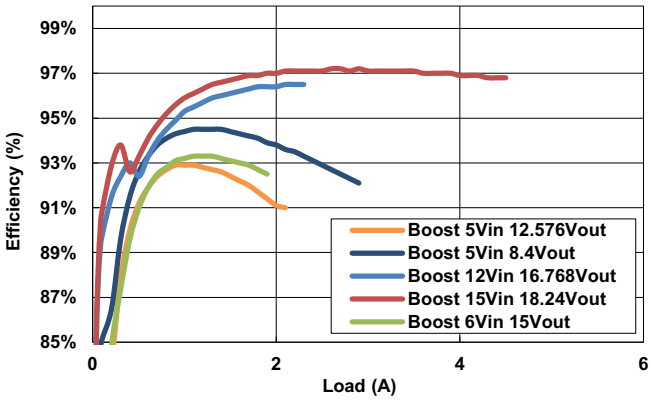



**Figure 23. Boost Mode Efficiency**

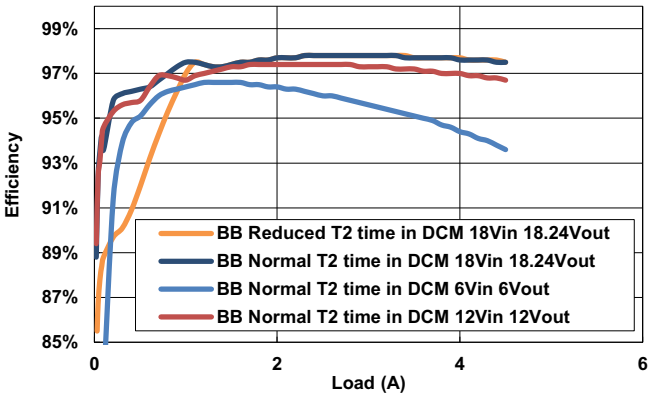



**Figure 24. Buck-Boost Mode Efficiency**

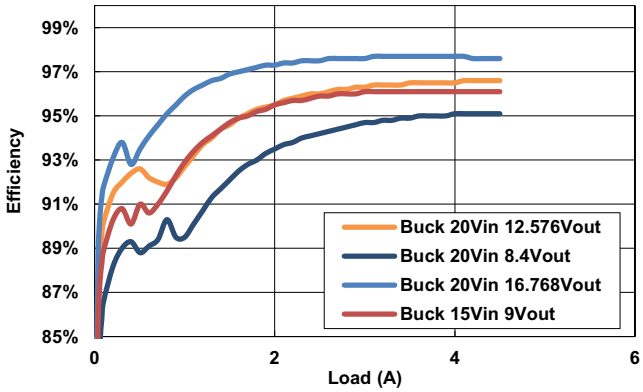



**Figure 25. Buck Mode Efficiency**

# 4. General SMBus Architecture

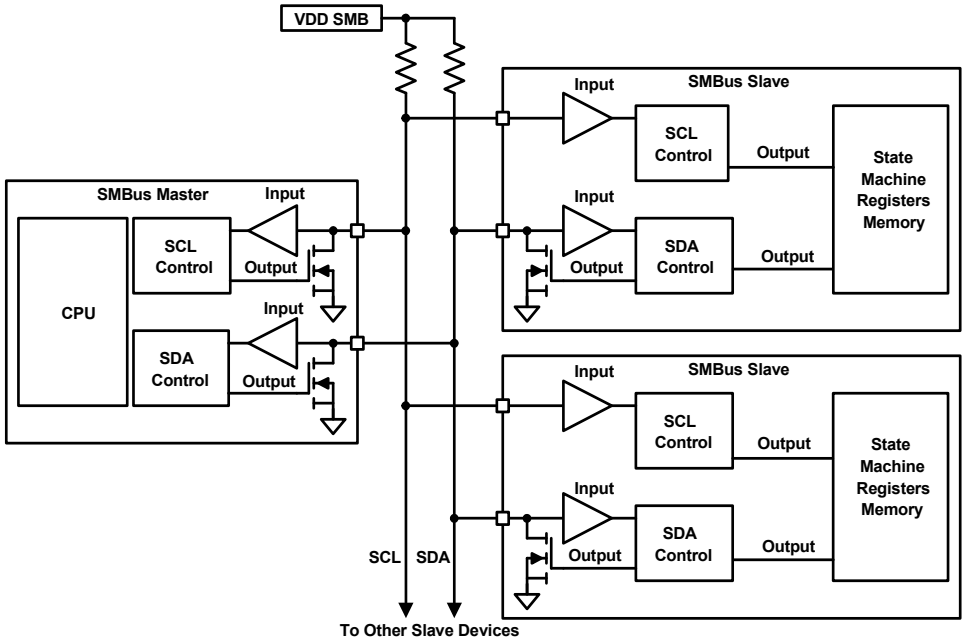



**Figure 26. General SMBus Architecture**

## 4.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. See Figure 27.

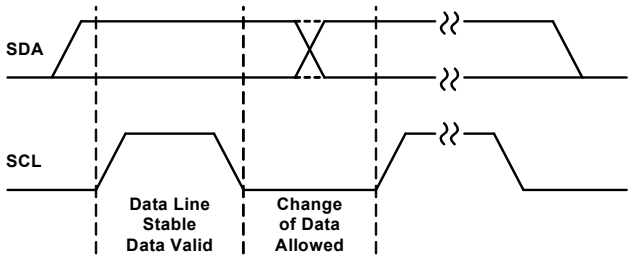



**Figure 27. Data Validity**

## 4.2 START and STOP Conditions

Figure 28 shows that the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH.

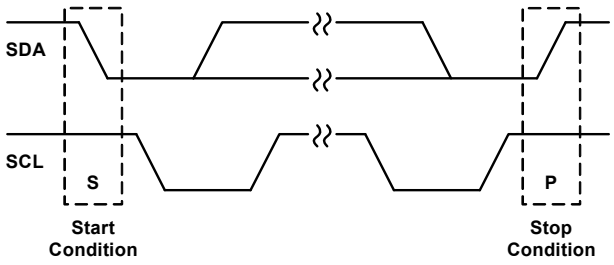



**Figure 28. Start and Stop Waveforms**

## 4.3 Acknowledge

Each address and data transmission uses nine clock pulses. The ninth pulse is the Acknowledge bit (ACK). After the start condition, the master sends seven slave address bits and a R/$\overline{W}$ bit during the next eight clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge (see Figure 29). Both the master and the slave use the ACK bit to acknowledge receipt of register addresses and data.

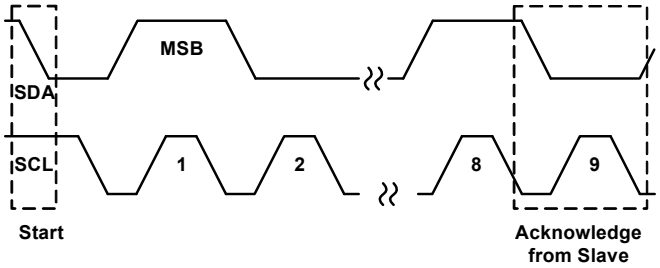



**Figure 29. Acknowledge on the SMBus**

## 4.4 SMBus Transactions

All transactions start with a control byte sent from the SMBus master device. The control byte begins with a Start condition followed by seven bits of slave address (0001001) and the R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a WRITE or 1 for a READ. If any slave device on the SMBus bus recognizes its address, it acknowledges by pulling the Serial Data (SDA) line low for the last clock cycle in the control byte. If no slave exists at that address or it is not ready to communicate, the data line is 1, indicating a not acknowledge condition.

After the control byte is sent and the ISL9241 acknowledges it, the second byte sent by the master must be a register address byte such as 0x14 for the ChargeCurrent register. The register address byte tells the ISL9241 which register the master writes or reads. See Table 1 for details about the registers. When the ISL9241 receives a register address byte, it responds with an acknowledge.

## 4.5 Byte Format

Every byte put on the SDA line must be eight bits long and must be followed by an ACK bit. Data is transferred with the Most Significant Bit (MSB) first and the Least Significant Bit (LSB) last. The LO Byte data is transferred before the HI Byte data. For example, when writing 0x41A0, 0xA0 is written first and 0x41 is written second.

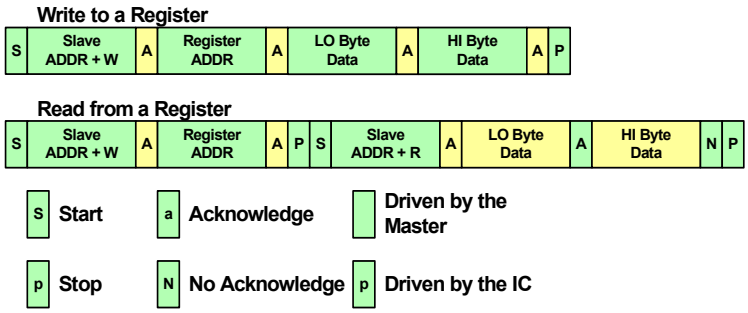



**Figure 30. SMBus Read and Write Protocol**

## 4.6 SMBus and I²C Compatibility

The ISL9241 SMBus minimum input logic high voltage is 1.5V, so it is compatible with an I²C with a pull-up power supply higher than 1.5V.

The ISL9241 SMBus registers are 16 bits, so it is compatible with a 16-bit I²C or an 8-bit I²C with auto-increment capability.

## 4.7 ISL9241 SMBus Commands

The ISL9241 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from www.smbus.org. The ISL9241 uses the SMBus Read-word and Write-word protocols (see Figure 30) to communicate with the host system and a smart battery. The ISL9241 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001x (ISL9241) as follows:

The Read and Write address for the ISL9241 is:

- Read address = 0b00010011 (0x13h)
- Write address = 0b00010010 (0x12h)

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pull-up resistors for SDA and SCL to achieve rise times according to the SMBus specifications.

Register DAC values in this datasheet are based on current-sensing resistors $R_{s1}$ = 20mΩ and $R_{s2}$ = 10mΩ unless otherwise specified.

Other addresses are available on request and require unique part numbers (alternative write addresses are 0x92h, 0x94h, and 0x96h).

# 5. ISL9241 Registers

## 5.1 Register Summary

**Table 1. Detailed Summary of Registers**

| Register Names | Register Address | Read/ Write | # of Bits | Description | Default |
|---|---|---|---|---|---|
| ChargeCurrentLimit (Table 15) | 0x14 | R/W | 11 | [12:2] 11-bit (0x0000h = disables fast charging, trickle charging is allowed) | 0x0000h (0A) |
| MaxSystemVoltage (Table 14) | 0x15 | R/W | 12 | [14:3] 12-bit, (0x0000h = disables switching) | Set by PROG |
| | | | | | 8.384V for 2-cell 0x20C0h |
| | | | | | 12.576V for 3-cell 0x3120h |
| | | | | | 16.768V for 4-cell 0x4180h |
| Control7 (Table 8) | 0x38 | R/W | 16 | Configures two-level adapter current limit duration, sets peak inductor current during supplemental mode, Buck-boost period stretch | 0x0000h |
| Control0 (Table 3) | 0x39 | R/W | 16 | Configures various charger options | 0x0000h |
| Information1 (Table 10) | 0x3A | R | 16 | Indicates various charger status | 0x0000h |
| AdapterCurrentLimit2 | 0x3B | R/W | 11 | [12:2] 11-bit | 0x05DCh (1500mA) |
| Control1 (Table 4) | 0x3C | R/W | 16 | Configures various charger options | 0x0103h (Includes value set by PROG pin) |
| Control2 (Table 5) | 0x3D | R/W | 16 | Configures various charger options | 0x6000h |
| MinSystemVoltage (Table 2) | 0x3E | R/W | 8 | [13:6] 8-bit (0x0000h = disables all battery charging) | 0x0000h (0V) |
| AdapterCurrentLimit1 | 0x3F | R/W | 11 | [12:2] 11-bit | Set by PROG pin |
| ACOK Reference | 0x40 | R/W | 8 | [13:6] x 8-Bit, (0x0000h = disables functionality) | Disabled (0x0000h) |
| Control6 (Table 9) | 0x43 | R/W | 13 | Interrupt trigger level direction<br>0 = Event went High to Low<br>1 = Event went Low to High | 0x1FFFh |
| ACProchot# | 0x47 | R/W | 6 | [12:7] Adapter current PROCHOT# threshold | 0x0C00h (3.072A) |
| DCProchot# | 0x48 | R/W | 6 | [13:8] Battery discharging current PROCHOT# threshold | 0x1000h (4.096A) |
| OTG Voltage (Table 2) | 0x49 | R/W | 12 | [14:3] 12-bit OTG mode voltage reference | 0x0D08h (5.004V) |
| OTG Current (Table 2) | 0x4A | R/W | 8 | [12:5] 8-bit, OTG mode maximum current limit | 0x0200h (0.512A) |
| $V_{IN}$ Voltage (Table 2) | 0x4B | R/W | 6 | [13:6] 8-bit, $V_{IN}$ loop voltage reference | 0x0C00h (4.096V) |
| Control3 (Table 6) | 0x4C | R/W | 16 | Configures various charger options | 0x0300h |
| Information2 (Table 11) | 0x4D | R | 16 | Indicates various charger status | 0x0000h |
| Control4 (Table 7) | 0x4E | R/W | 16 | Configures various charger options | 0x0000h |

**Table 1. Detailed Summary of Registers (Continued)**

| Register Names | Register Address | Read/ Write | # of Bits | Description | Default |
|---|---|---|---|---|---|
| Control5 (Table 9) | 0x4F | R/W | 13 | Interrupt mask control enable<br>0 = Not enabled/masked<br>1 = Enabled/unmasked | 0x0000h |
| NTC ADC Results | 0x80 | R | 10 | ADC result for NTC/GP measurements | Table 12 |
| VBAT ADC Results | 0x81 | R | 8 | ADC result for VBAT measurements, LSB = 64mV | Table 12 |
| TJ ADC Results | 0x82 | R | 8 | ADC result for internal $T_J$ measurements, LSB = 8mV | Table 12 |
| IADP ADC Results | 0x83 | R | 8 | ADC result for adapter current measurements, LSB = 22.2mA | Table 12 |
| DC ADC Results | 0x84 | R | 8 | ADC result for battery discharge current measurements, LSB = 44.4mA | Table 12 |
| CC ADC Results | 0x85 | R | 8 | ADC result for battery charge current measurements, LSB = 22.2mA | Table 12 |
| VSYS ADC Results | 0x86 | R | 8 | ADC result for CSOP (VSYS) measurements, LSB = 96mV | Table 12 |
| VIN ADC Results | 0x87 | R | 8 | ADC result for CSIN (VIN) measurements, LSB = 96mV | Table 12 |
| Information3 (Table 9) | 0x90 | R/W | 13 | Interrupt status - multiple events possible | 0x0000h |
| Information4 (Table 9) | 0x91 | R/W | 13 | Interrupt real-time status | 0x0000h |
| Manufacturer ID | 0xFE | R | 8 | Manufacturer ID register – 0x49. Read only | 0x0049h |
| Device ID | 0xFF | R | 8 | Device ID register. Read only | 0x000Eh |

**Note:** All values in this table are computed with $R_{S1}$ = 20mΩ and $R_{S2}$ = 10mΩ.

## 5.2 DAC Register Summary

**Table 2. DAC Summary Table**

| | Charge Current Limit ($R_{S2}$ = 10mΩ) | Max System Voltage | Min System Voltage | Adapter Current Limit1 ($R_{S1}$ = 20mΩ) | Adapter Current Limit2 ($R_{S1}$ = 20mΩ) | $V_{IN}$ Voltage (ADP Min Voltage) | ACOK Reference for $V_{IN}$ Comparison | ACProchot# (ACHOT) ($R_{S1}$ = 20mΩ) | DCProchot# (DCHOT) ($R_{S2}$ = 10mΩ) | OTG Voltage | OTG Current ($R_{S1}$ = 20mΩ) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **ADDR** | **0x14** | **0x15** | **0x3E** | **0x3F** | **0x3B** | **0x4B** | **0x40** | **0x47** | **0x48** | **0x49** | **0x4A** |
| <0> | - | - | - | - | - | - | - | - | - | | - |
| <1> | - | - | - | - | - | - | - | - | - | | - |
| <2> | 4mA | - | - | 4mA | 4mA | - | - | - | - | | - |
| <3> | 8mA | 8mV | - | 8mA | 8mA | - | - | - | - | 12mV | - |
| <4> | 16mA | 16mV | - | 16mA | 16mA | - | - | - | - | 24mV | - |
| <5> | 32mA | 32mV | - | 32mA | 32mA | - | - | - | - | 48mV | 32mA |
| <6> | 64mA | 64mV | 64mV | 64mA | 64mA | 85mV | 96mV | - | - | 96mV | 64mA |
| <7> | 128mA | 128mV | 128mV | 128mA | 128mA | 171mV | 192mV | 128mA | - | 192mV | 128mA |
| <8> | 256mA | 256mV | 256mV | 256mA | 256mA | 341mV | 384mV | 256mA | 256mA | 384mV | 256mA |
| <9> | 512mA | 512mV | 512mV | 512mA | 512mA | 683mV | 768mV | 512mA | 512mA | 768mV | 512mA |
| <10> | 1024mA | 1024mV | 1024mV | 1024mA | 1024mA | 1365mV | 1536mV | 1024mA | 1024mA | 1536mV | 1024mA |
| <11> | 2048mA | 2048mV | 2048mV | 2048mA | 2048mA | 2731mV | 3072mV | 2048mA | 2048mA | 3072mV | 2048mA |
| <12> | 4096mA | 4096mV | 4096mV | 4096mA | 4096mA | 5461mV | 6144mV | 4096mA | 4096mA | 6144mV | 4096mA |
| <13> | - | 8192mV | 8192mV | - | - | 10923mV | 12288mV | - | 8192mA | 12288mV | - |
| <14> | - | 16384mV | - | - | - | - | - | - | - | 24576mV | - |
| <15> | - | - | - | - | - | - | - | - | - | - | - |
| Max | 6140mA | 18.304V | 16.32V | 6140mA | 6140mA | 16.384V | 24.48V | 6.4A | 12.8A | 23.4V (Note 8) | 6112mA |

**Note:**

8. This maximum for OTG voltage is limited by the internal overvoltage shutdown threshold. The register accepts the higher settings.

## 5.3 Control Registers

The Control0, Control1, Control2, Control3, Control4, and Control7 registers configure the operation of the ISL9241. To change certain functions or options after POR, write a 16-bit control command to any control register address. See the Write-word protocol shown in Figure 30 and the data format shown in Tables 3, 4, 5, and 6.

**Table 3. Control0 Register 0x39H**

| Bit | Bit Name | Description |
|---|---|---|
| <15> | CSIN Sink/Discharge | Enables or turns on the discharge FET to pull down the CSIN.<br>0 = Disable, 10mA sink turned off (default)<br>1 = Enable, 10mA sink turned on |
| <14> | CSIN Auto Sink/Discharge | Enables or disables the discharge path for CSIN for 50ms when entering the ready state.<br>0 = Disable (default)<br>1 = Enable |
| <13> | CSOP Sink | Enables or turns on the discharge FET to pull down the CSOP.<br>0 = Disable, 10mA sink turned off (default)<br>1 = Enable, 10mA sink turned on |
| <12> | NGATE Off | 0 = NGATE on (NGATE = CSOP + 5V); (default)<br>1 = NGATE off (NGATE = CSOP) |
| <11> | BYPASS On | 0 = BYPSG off (BYPSG = BYPSRC) (default)<br>1 = BYPSG on (BYPSG = BYPSRC + 5V) |
| <10> | BGATE Force On | 0 = BGATE normal operation (default)<br>1 = BGATE forced ON (BGATE = VBAT + 5V) |
| <9:8> | Dither Enable | 00 = Disable dither (default)<br>01 = Dither1x<br>10 = Dither2x<br>11 = Dither3x |
| <7> | SMBus Timeout | Default time is 175s (see Control3<12:11> and "SMBus Timeout" on page 43).<br>0 = Enable the SMBus timeout function (default)<br>1 = Disable the SMBus timeout function |
| <6> | Enable Charge Pumps to 100% Duty Cycle | Enables the charge pumps for BGATE and NGATE for 100% of the time.<br>0 = Normal operation (reduced supply current) (default)<br>1 = Enable charge pumps 100% of the time to ensure the charge pump good bit does not toggle due to gate leakage (see Table 10 on page 36) |
| <5> | BYP $V_{IN}$ < $V_{OUT}$ Comparator to turn off BYPSG | Enables or disables the bypass comparator and turns off the BYPSG when $V_{IN}$ < $V_{OUT}$.<br>0 = Disable (default)<br>1 = Enable |
| <4:3> | DCProchot# Threshold in Battery Only Mode (Low Power Mode) | Configures the battery discharging current DCProchot# threshold in battery only Low Power mode indicated by the Information1 register 0x3A Bit<15>. If PSYS is enabled, the battery discharge current DCProchot# threshold is set by the DCProchot# register 0x48 setting. |
| <2> | Input Voltage Regulation | Enables or disables the input voltage regulation loop.<br>0 = Enable (default)<br>1 = Disable |
| <1> | VSYS Regulation Offset Voltage Adder | Adds offset above the VSYSMAX register setting when not charging.<br>0 = 0mV (default)<br>1 = 384mV<br>(384mV is always added to MinsysVoltage in Trickle Charge mode - irrespective of this bit) |

| Bit<4:3> | $R_{s2}$ = 10mΩ (A) | $R_{s2}$ = 20mΩ (A) | $R_{s2}$ = 5mΩ (A) |
|---|---|---|---|
| 00 | 12 (default) | 6 (default) | 24 (default) |
| 01 | 10 | 5 | 20 |
| 10 | 8 | 4 | 16 |
| 11 | 6 | 3 | 12 |

**Table 3. Control0 Register 0x39H (Continued)**

| Bit | Bit Name | Description |
|---|---|---|
| <0> | Reverse Turbo Boost | Reverse Turbo Boost when in hybrid/bypass configuration. If adapter current drawn exceeds the current limit, the modulator operates in reverse mode and takes energy from the battery to hold up the input.<br>**Note:** This bit should not be enabled in NVDC mode. Not allowed while using Autonomous Charging mode or if battery capacity is low.<br>0 = Disable (default)<br>1 = Enable |

**Table 4. Control1 Register 0x3CH**

| Bit | Bit Name | Description |
|---|---|---|
| <15:14> | General Purpose Comparator Debounce Time | Configures the general purpose comparator assertion debounce time.<br>00 = 2µs (default)<br>01 = 12µs<br>10 = 2ms<br>11 = 720µs |
| <13> | Exit Learn Mode | Provides the option to Exit Learn mode when the battery voltage is lower than MinSystemVoltage register setting.<br>0 = Stay in Learn mode even if $V_{BAT}$ < MinSystemVoltage register setting (default)<br>1 = Exit Learn mode if $V_{BAT}$ < MinSystemVoltage register setting |
| <12> | Learn Mode | Enables or disables the Battery Learn mode used in NVDC mode only.<br>(see "Battery Learn Mode" on page 45)<br>0 = Disable (default)<br>1 = Enable<br>To enter Learn mode, the BATGONE pin needs to be low and a battery must be present. |
| <11> | OTG Function | Enables or disables the OTG function.<br>0 = Disable OTG (default)<br>1 = Enable OTG (adapter output power supply) |
| <10> | Supplemental Support Mode | Enables or disables Supplemental functionality.<br>(see "Supplemental Power Support Mode" on page 47)<br>0 = Disable supplemental support (Intel Vmin Active Protection (VAP)) - (default)<br>1 = Enable supplemental support (Intel VAP support) |
| <9:7> | Switching Frequency | Configures the switching frequency and overrides the default switching frequency set by the PROG pin.<br>000 = 1420kHz<br>001 = 1180kHz<br>010 = 1020kHz<br>011 = 890kHz<br>100 = 808kHz<br>101 = 724kHz<br>110 = 656kHz<br>111 = 600kHz<br>To keep the switching frequency set by the PROG pin resistor, leave Bit<9:7> as it is read. |
| <6> | BGATE Force Off | Disables BGATE. This forces the BGATE FET to turn off and overwrite Turbo mode. See Table 17 on page 60.<br>0 = Normal operation (default)<br>1 = Force BGATE Off (BGATE = VBAT) (also disables Turbo mode/Ideal Diode mode) |
| <5> | IMON Function in Battery Only Mode | Enables or disables the current monitor function AMON and BMON.<br>0 = Enable IMON (default)<br>1 = Disable IMON<br>Bit<5> is valid only in Battery Only mode. When an adapter is present, IMON is automatically enabled and Bit<5> becomes invalid. |
| <4> | IMON Selection | Selects AMON or BMON as the output of the AMON/BMON pin (see Control3<3> for direction).<br>0 = AMON (default)<br>1 = BMON |

**Table 4. Control1 Register 0x3CH (Continued)**

| Bit | Bit Name | Description |
|---|---|---|
| <3> | PSYS | Enables or disables the system power monitor PSYS function.<br>0 = Disable (default)<br>1 = Enable |
| <2:0> | Low_VSYS_Prochot# Reference | VSYSLO reference for PROCHOT# and Supplemental mode activation.<br>000: 5.4V<br>001: 5.6V<br>010: 5.8V<br>011: 6.0V (default)<br>100: 6.2V<br>101: 6.4V<br>110: 6.6V<br>111: 6.8V |

**Table 5. Control2 Register 0x3DH**

| Bit | Bit Name | Description |
|---|---|---|
| <15:13> | Trickle Charging Current | Configures the charging current in Trickle Charging mode.<br><000> 32mA (do not use)<br><001> 64mA<br><010> 96mA<br><011> 128mA (default)<br><100> 160mA<br><101> 192mA<br><110> 224mA<br><111> 256mA |
| <12> | Two-Level Adapter Current Limit | Enables or disables the two-level adapter current limit function.<br>(see "Adapter Current Loop and Current Limit 1 and 2 and Two Level Current Limit" on page 57)<br>0 = Disable (default)<br>1 = Enable |
| <11> | Fault Timer Debounce Time for OT and WCOP | Configures the debounce fault time for die Over Temperature (OT) or Way Overcurrent (WOC).<br>0 = 1.3s (default)<br>1 = 150ms |
| <10:9> | PROCHOT# Debounce | Configures the PROCHOT# debounce time before its assertion for ACProchot# and DCProchot#.<br>00: 7µs (default)<br>01: 100µs<br>10: 500µs<br>11: 1ms<br>The Low_VSYS_Prochot# has a fixed 7µs debounce time. |
| <8:6> | PROCHOT# Duration | Configures the minimum duration of the PROCHOT# signal when asserted.<br>000 = 10ms (default)<br>001 = 20ms<br>010 = 15ms<br>011 = 5ms<br>100 = 1ms<br>101 = 500µs<br>110 = 100µs<br>111 = 0s |
| <5> | JEITA Control Bit<1> | JEITA Control Bit<1>. See Table 7 on page 33, Control4<14> for JEITA Control Bit<0><br>JEITA Bit<1:0> truth table.<br>00 - General purpose ADC input, NTC current source OFF (default)<br>01 - Original JEITA profiles, NTC current source ON<br>10 - Profile 1, NTC current source ON<br>11 - Profile 2, NTC current source ON |
| <4> | CMIN Reference | Configures the general purpose comparator reference voltage.<br>0 = 1.2V (default)<br>1 = 2V (this option is not available in Battery only mode) |

**Table 5. Control2 Register 0x3DH (Continued)**

| Bit | Bit Name | Description |
|---|---|---|
| <3> | General Purpose Comparator | Enables or disables the general purpose comparator.<br>0 = Enable (default)<br>1 = Disable (Interrupt Enabled - allows interrupt functionality on pin) |
| <2> | CMOUT Polarity | Configures the general purpose comparator output polarity when asserted. The comparator reference voltage is connected at the inverting input node.<br>0 = Not inverted, CMOUT is High when CMIN is higher than the reference (default)<br>1 = Inverted, CMOUT is Low when CMIN is higher than the reference |
| <1> | Internal Resistor Compensation for COMPR RCOMP | Changes the internal compensation resistor to speed up or slow down the loop response for reverse modulator operations (OTG).<br>0 = Faster (default)<br>1 = Slower |
| <0> | Internal Resistor Compensation for COMPF RCOMP | Changes the internal compensation resistor to speed up or slow down the loop response for forward modulator operations and Reverse Turbo Boost mode.<br>0 = Faster (default)<br>1 = Slower |

**Table 6. Control3 Register 0x4CH**

| Bit | Bit Name | Description |
|---|---|---|
| <15> | Digital OV Control and OTG UV Control | 0 = Normal digital overvoltage, shuts down switching after debounce time (default)<br>1 = PPS operations; disables the undervoltage for OTG and overvoltage digital for OTG and VSYS (see Control7<7> in Table 8 on page 34) |
| <14> | ACLIM Reload | Reloads the AdapterCurrentLimit1 register with the value set by the last read of the PROG pin resistor on the falling edge of ACOK to prepare for a new adapter attaching.<br>0 = Reload AdapterCurrentLimit1 register (default)<br>1 = Do not reload |
| <13> | Autonomous Charging Termination Time | Configures the autonomous charging termination time.<br>0 = 20ms (default)<br>1 = 200ms |
| <12:11> | SMBus Charger Timeout | Configures the SMBus Timeout time (see "SMBus Timeout" on page 43).<br>00 = 175s (default)<br>01 = 87.5s<br>10 = 43.75s<br>11 = 4.95s |
| <10> | DCM/CCM Hysteresis | 0 = Disabled (default)<br>1 = Enables hysteresis for the DCM to CCM boundary |
| <9:8> | PSYS Gain | Configures the system power monitor PSYS output gain. (Default = 11)<br>See PSYS GAIN values in the "Electrical Specifications" on page 11. |
| <7> | Charge Control | Enables Autonomous Charging mode<br>(see "Autonomous Charging Mode" on page 43).<br>0 = SMBus Control, Battery charging current control through SMBus only (default)<br>1 = Enable Autonomous Charging mode (resets if 12-hour timer expires or a Fault occurs, PROCHOT# configured for autonomous charging mode indicator, End of Charge enabled) |
| <6> | AC and CC Current Feedback Gain | Configures AC and CC feedback gain for high current applications.<br>0 = x1.0 (default)<br>1 = x0.5 |
| <5> | Input Current Limit Loop | Disables the input current limit loop.<br>0 = Enable input current limit loop (default)<br>1 = Disable input current limit loop |
| <4> | Input Current Limit Loop when BATGONE = 1 | Disables the input current limit loop when BATGONE = 1.<br>0 = Enable ACLIM when BATGONE = 1 (default)<br>1 = Disable ACLIM when BATGONE = 1 |

**Table 6. Control3 Register 0x4CH (Continued)**

| Bit | Bit Name | Description |
|---|---|---|
| <3> | IMON Direction | Configures the AMON/BMON direction (see Control1<4> for AMON/BMON selection).<br>0 = Adapter current monitor/battery charging current monitor (default)<br>1 = OTG output current monitor/battery discharging current monitor |
| <2> | Digital Reset | Resets all SMBus register values to the POR default value, including re-reading PROG settings.<br>0 = Idle (default)<br>1 = Reset |
| <1> | T2DCM | Buck-Boost T2 time in DCM (T2DCM), reduces input ripple.<br>0 = Reduced T2 time (increases switching frequency in DCM) (default)<br>1 = Normal T2 time |
| <0> | Enable ADC | 0 = ADC is active only when adapter is plugged in and charging (default)<br>1 = Enables ADC for all modes |

**Table 7. Control4 Register 0x4EH**

| Bit | Bit Name | Description |
|---|---|---|
| <15> | BATGONE Disable | 0 = Normal BATGONE input (default)<br>1 = Ignore BATGONE input |
| <14> | JEITA Control Bit<0> | JEITA Control Bit<0> (see Table 5 on page 31, Control2<5> for JEITA Control Bit<1>)<br>JEITA Bit<1:0> truth table.<br>00 = GPADC, NTC current source OFF (default)<br>01 = Original JEITA profiles, NTC current source ON<br>10 = Profile 1, NTC current source ON<br>11 = Profile 2, NTC current source ON |
| <13> | Slew Rate Control | 0 = Slew Rate Control Disabled (default)<br>1 = Slew Rate enabled to ramp DAC voltage; OTG 12mV/µs and VSYS 8mV/µs;<br>Not recommended in OTG mode until after establishing 5V to prevent OV issues. |
| <12> | Disable GP Comparator | 0 = Enabled for all modes (default)<br>1 = Disabled for Battery Only mode (REF = 1.2V in Battery Only mode) |
| <11> | PSYS Rsense Ratio | $R_{SENSE}$ ($R_{s1}$:$R_{s2}$) ratio for PSYS.<br>0 = 2:1 (default)<br>1 = 1:1 |
| <10> | Force Buck Mode | 0 = Normal modulator operations (default)<br>1 = Forward Force Buck/Reverse Force Boost |
| <9> | WOCP Function | 0 = Enable way overcurrent detection (default)<br>1 = Disable |
| <8> | VSYS Short Check | Enables or disables VSYS short detection before enabling the modulator.<br>0 = Enable (default)<br>1 = Disable |
| <7> | OTGCURRENT PROCHOT# | Enables or disables trigger PROCHOT# with OTGCURRENT.<br>0 = Disable (default)<br>1 = Enable |
| <6> | BATGONE PROCHOT# | Enables or disables trigger PROCHOT# with BATGONE.<br>0 = Disable (default)<br>1 = Enable |
| <5> | ACOK PROCHOT# | Enables or disables trigger PROCHOT# with ACOK.<br>0 = Disable (default)<br>1 = Enable |
| <4> | GP Comparator PROCHOT# | Enables or disables trigger PROCHOT# with general purpose comparator rising.<br>0 = Disable (default)<br>1 = Enable |

**Table 7. Control4 Register 0x4EH (Continued)**

| Bit | Bit Name | Description |
|---|---|---|
| <3:2> | ACOK falling or BATGONE Rising Debounce | Configures the debounce time from ACOK falling or BATGONE rising to PROCHOT# trip.<br>00 = 2µs (default)<br>01 = 25µs<br>10 = 125µs<br>11 = 250µs |
| <1> | PROCHOT# Clear | Clears PROCHOT#.<br>0 = Idle (default)<br>1 = Clear PROCHOT# |
| <0> | PROCHOT# Latch | Manually resets PROCHOT#.<br>0 = PROCHOT# signal auto-clear (default)<br>1 = Hold PROCHOT# low when tripped, must be clear using Bit<1> above |

**Table 8. Control7 Register 0x38H**

| Bit | Bit Name | Description |
|---|---|---|
| <15:13> | t2 - Time corresponding to Adapter Current Limit 2 (Two level ACLIM enabled) | 000 = 10µs (default)<br>001 = 100µs<br>010 = 500µs<br>011 = 1ms<br>100 = 300µs<br>101 = 750µs<br>110 = 2ms<br>111 = 10ms |
| <12:10> | t1 - Time Corresponding to Adapter Current Limit 1 (Two level ACLIM enabled) | 000 = 10ms (default)<br>001 = 20ms<br>010 = 15ms<br>011 = 5ms<br>100 = 1ms<br>101 = 0.5ms<br>110 = 0.1ms<br>111 = 0ms |
| <9:8> | End of Charge (EOC) Settings | End of charge settings when using Autonomous Charging mode. Also see Control3<7> in Table 6.<br>00 = 105mA (default)<br>01 = 55mA<br>10 = 190mA<br>11 = 145mA |
| <7> | Analog OV Control | Analog overvoltage disable (also see Control3<15> in Table 6).<br>0 = Normal, OV pulls down on comp and disables switching (default)<br>1 = Disable |
| <6> | GM_SUPN | Set Supplemental mode loop gain (GM_SUPN).<br>0 = 1x (default)<br>1 = 2x |
| <5> | T_SUP Multiplier (T_SUPM) | Set Supplemental mode period (T_SUPM) multiplier.<br>0 = 1x (default)<br>1 = 0.5x |
| <4:2> | T_SUP | Set Supplemental Buck mode period (T_SUP).<br>000 = Standard T_SUP (default)<br>001 = 7/6 * Standard T_SUP<br>010 = 8/6 * Standard T_SUP<br>011 = 9/6 * Standard T_SUP<br>100 = 10/6 * Standard T_SUP<br>101 = 11/6 * Standard T_SUP<br>110 = 12/6 * Standard T_SUP<br>111 = 13/6* Standard T_SUP |

**Table 8. Control7 Register 0x38H**

| Bit | Bit Name | Description |
|---|---|---|
| <1:0> | Buck-Boost Stretch CCM Period | Buck-boost stretch CCM period (T2 TIME).<br>00 = 2x (default)<br>01 = 3x<br>10 = 1x<br>11 = 0.6x |

## 5.4 Interrupt Functionality

The INT# pin is shared with the CMOUT pins, so it must be enabled by setting Control2 Bit<3> = 1 (see Table 5). Setting the bit to 1 disables the comparator output function. After the INT# pin is enabled, configure the faults or flags to be masked or unmasked and have the INT# trigger. If the flag is a fault, it must be read to clear the INT#. Thirteen possible functions are supported by the interrupt control registers. INT# is an active low, open-drain output that is shared with the GP comparator. It pulls low to signal an interrupt event and requires a pull-up source to toggle.

Information4 provides the event real-time status and always shows the event flag, even if the interrupt is not enabled. This could be as small as a one clock pulse, and may not be useful without being latched, such as for “Changed NTC Temperature Boundary”.

If Control5 bit is set to 1, an interrupt is enabled to trigger. A 0 masks it and the event is ignored for triggering an interrupt.

Setting Control6 to a 1 means a 1 level triggers the interrupt. This interrupt function is not an edge trigger event.

If Control6 is set to a 1, an interrupt flag is set if the signal becomes a 1. If Control6 is set to 0, an interrupt flag is set when the signal becomes a 0. If Control6 is changed from a 1 to a 0 when the event is 0, this also triggers an interrupt on completion of the SMBus command.

The Information3 register shows results only for unmasked/enabled events. Interrupt flags are cleared by reading the status bit in the Information3 register but only if the fault condition has been removed or the level is changed. To catch the opposite edge, such as when leaving an event, toggle the appropriate bit in Control6.

The Information4 register shows the real-time status of the event. It is not affected by the mask/unmask bit and is not latched.

**Table 9. Interrupt Control and Status Registers**

| | Control Inputs | | | Flag Outputs | | | |
|---|---|---|---|---|---|---|---|
| | Control5 Interrupt Mask | | Control6 Interrupt Trigger Level | Information3 Interrupt Status | | Information4 Interrupt Real-Time Status | |
| | Address:0x4F | | Address:0x43 | Address:0x90 | | Address:0x91 | |
| | 0 = Not Enabled<br>1 = Enabled | | 0 = Event triggers when low<br>1 = Event is triggers when high | 0 = No event<br>1 = Event Set interrupt flag | | 0 = Not in state<br>1 = In this state | |
| Bit# | R/W | Default | Default | R/W | Default | Default | Description |
| 12 | R/W | 0 | 1 | R | 0 | 0 | SMBus timeout timer expired |
| 11 | R/W | 0 | 1 | R | 0 | 0 | 12-hour charge timer expired for Autonomous Charging mode only |
| 10 | R/W | 0 | 1 | R | 0 | 0 | SYS OV (CSOP OV) |
| 9 | R/W | 0 | 1 | R | 0 | 0 | ADP OV (CSIN OV) |
| 8 | R/W | 0 | 1 | R | 0 | 0 | ADP VMIN (selector info) |
| 7 | R/W | 0 | 1 | R | 0 | 0 | ADP current (selector info) |
| 6 | R/W | 0 | 1 | R | 0 | 0 | Thermal warning ($T_J$) |

**Table 9. Interrupt Control and Status Registers (Continued)**

| | Control Inputs | | | Flag Outputs | | | |
|---|---|---|---|---|---|---|---|
| | Control5 Interrupt Mask | | Control6 Interrupt Trigger Level | Information3 Interrupt Status | | Information4 Interrupt Real-Time Status | |
| | Address:0x4F | | Address:0x43 | Address:0x90 | | Address:0x91 | |
| | 0 = Not Enabled<br>1 = Enabled | | 0 = Event triggers when low<br>1 = Event is triggers when high | 0 = No event<br>1 = Event Set interrupt flag | | 0 = Not in state<br>1 = In this state | |
| Bit# | R/W | Default | Default | R/W | Default | Default | Description |
| 5 | R/W | 0 | 1 | R | 0 | 0 | OTGPG, OTG output voltage not UV or OV |
| 4 | R/W | 0 | 1 | R | 0 | 0 | Battery charging terminated for Autonomous Charging mode only |
| 3 | R/W | 0 | 1 | R | 0 | 0 | Battery charging CC to CV |
| 2 | R/W | 0 | 1 | R | 0 | 0 | FET fault state |
| 1 | R/W | 0 | 1 | R | 0 | 0 | Enter READY |
| 0 | R/W | 0 | 1 | R | 0 | 0 | Changed NTC temperature boundary |

## 5.5 Information Registers

The information registers contain SMBus readable information about manufacturing and operating modes. Tables 10 and 11 identify the bit locations of the information available.

**Table 10. Information1 Register 0x3AH**

| Bit | Bit Name | Description |
|---|---|---|
| <0> | Diode Mode Status | 0 = Diode mode is not active<br>1 = Diode mode is active |
| <1> | Reverse Turbo Mode Status | 0 = Reverse turbo mode is not active<br>1 = Reverse turbo mode is active |
| <2> | Bypass Gate Power Good Status | 0 = BYPSG charge pump is not good<br>1 = BYPSG charge pump is good (Note 9) |
| <3> | NGATE Power Good Status | 0 = NGATE charge pump is not good<br>1 = NGATE charge pump is good (Note 9) |
| <4> | Trickle Charging Mode Status | 0 = Trickle Charging mode is not active<br>1 = Trickle Charging mode is active |
| <5> | CSIN_CSOP Comparator Status | CSIN to CSOP comparator<br>0 = CSIN < CSOP<br>1 = CSIN > CSOP |
| <6> | BGATE Power Good Status | 0 = BGATE charge pump is not good<br>1 = BGATE charge pump is good (Note 9) |
| <9:7> | | Not used |
| <10> | Low_Vsys_PROCHOT# Status | Indicates if the Low_VSYS_Prochot# is tripped.<br>0 = Low_VSYS PROCHOT# is not tripped<br>1 = Low_VSYS PROCHOT# is tripped |
| <11> | DC PROCHOT# Status | Indicates if DCProchot# is tripped.<br>0 = DCProchot# is not tripped<br>1 = DCProchot# is tripped |
| <12> | AC PROCHOT# Status | Indicates if ACProchot#/OTGCURRENTProchot# is tripped.<br>0 = ACProchot#/OTGCURRENTProchot# is not tripped<br>1 = ACProchot#/OTGCURRENTProchot# is tripped |

**Table 10. Information1 Register 0x3AH (Continued)**

| Bit | Bit Name | Description |
|---|---|---|
| <14:13> | Active Control Loop | Indicates the active control loop.<br>00 = MaxSystemVoltage control loop is active<br>01 = Charging current loop is active<br>10 = Input adapter current limit loop is active<br>11 = Input voltage loop is active |
| <15> | Internal Reference Status | Indicates if the internal reference circuit is active.<br>0 = Reference is not active<br>1 = Reference is active |

**Note:**

9. Depending on leakage on the pin, the bit may toggle unless set to 100% charge pump mode using Control3<6> (see Table 3 on page 29).

**Table 11. Information2 Register 0x4DH**

| Bit | Bit Name | Description |
|---|---|---|
| <4:0> | PROG Resistor Read Out | Program Resistor read out (Table 13)<br>Number of battery cells<br>Switching frequency<br>Adapter current limit<br>PSYS/REFADJ Selection |
| <7:5> | Power Stage Operation Mode | Indicates the ISL9241 operation mode.<br>001 = Forward Boost mode<br>010 = Forward Buck mode<br>011 = Forward Buck-Boost mode<br>101 = OTG Boost mode<br>110 = OTG Buck mode<br>111 = OTG Buck-Boost mode |
| <11:8> | State Machine | Indicates the ISL9241 state machine status.<br>0000 = RESET<br><br>0001,0011,0101,1000,1011 = STARTUP: The IC wakes up internal circuits biases, reads trim, and autozeros comparators; wait state for $V_{DD}$ > 3.8V<br><br>0010 = ACHRG. Charge state. The system is charging the battery through the Autocharge setting<br><br>0100 = BAT. Battery only mode with PSYS, ADC, and OTG disabled (ACOK is low)<br><br>0110 = CHRG. Charge state. Charging is enabled and the system is charging the battery through SMBus charging<br><br>0111 = FAULT. OTP or WOCP is triggered<br><br>1001 = OTG. Charger is operating in Reverse/OTG mode or Supplemental mode is enabled<br><br>1010 = READY. The charger is not switching but the circuits are biased and ready (for example, with the MaxsysV register set to 0).<br>May also be reached by enabling PSYS or ADC in Battery Only mode (from BAT state)<br><br>1100 = VSYS. The charger is in the forward mode and switching, the system voltage or adapter current (or input voltage) can be regulated in this state. |
| <12> | BATGONE Pin Status | Indicates the BATGONE pin status.<br>0 = Battery is present<br>1 = No battery |

**Table 11. Information2 Register 0x4DH (Continued)**

| Bit | Bit Name | Description |
|---|---|---|
| <13> | General Purpose Comparator Status | Indicates the general purpose comparator output after debounce time.<br>0 = Comparator output is low<br>1 = Comparator output is high |
| <14> | ACOK Pin Status | Indicates the ACOK pin status.<br>0 = No adapter<br>1 = Adapter is present |
| <15> | | Not used |

## 5.6 ADC Registers

**Table 12. ADC Output Value Bits**

| ADDR | Description | LSB | Sample Window TIme | Polling Time |
|---|---|---|---|---|
| Control3 Reg 0x4C Bit<0>. See Table 6 on page 32. | 0 = Disables the ADC, except when required for charging the state machine<br>1 = Enables the ADC | | | |
| 0x80 | [9:0] NTC voltage<br>If enabled as General Purpose ADC Voltage [9:2] 0 to 2.040V | 2mV (Bit<0>) for NTC<br>8mV (Bit<2>) for GPADC | 80µs | 100ms |
| 0x81 | $V_{BAT}$ voltage [13:6] 0 to 16.32V | 64mV | 80µs | 100ms |
| 0x82 | Internal junction temperature [7:0] $T_J$ voltage 0 to 2.040V | 8mV | 80µs | 100ms |
| 0x83 | Input current ($R_{s1}$ = 20mΩ) [7:0] 0 - 5.68A | 22.2mA | 80µs | 400µs |
| 0x84 | Battery discharge current ($R_{s2}$ = 10mΩ) [7:0] 0 - 11.37A | 44.4mA | 80µs | 400µs |
| 0x85 | Battery charge current ($R_{s2}$ = 10mΩ) [7:0] 0 - 5.68A | 22.2mA | 80µs | 400µs |
| 0x86 | CSOP (VSYS) voltage [13:6] VSYS voltage 0 to 24.48V | 96mV | 80µs | 400µs |
| 0x87 | CSIN ($V_{IN}$) voltage [13:6] $V_{IN}$ voltage 0 to 24.48V | 96mV | 80µs | 400µs |

# 6. Application Information

## 6.1 Start-Up and ACOK

The ISL9241 includes a low power LDO with a nominal 4.7V output and an internal input OR-ed from the VBAT and CSIN inputs. The ISL9241 also includes a high power LDO with a nominal 5V output that has an input from the DCIN pin connected both to the adapter and the system bus through an external OR-ing diode circuit. The low power LDO must be active above 2.7V to enable the high power LDO. Both LDO outputs are tied to the VDD pin to provide the bias power and gate drive power for the ISL9241. The VDDP pin is the ISL9241 gate drive power supply input. Use an RC filter to generate the VDDP pin voltage from the VDD pin voltage.

The ISL9241 monitors the CSIN pin voltage to determine the presence of the adapter. When CSIN is higher than the ACOK threshold and after VDD POR releases, the charger is initialized for 150ms of debounce time. Initialization takes about 4ms, and next the trim settings are read, the internal circuitry is autozeroed, and configuration is completed during the STARTUP state (see Table 11 on page 37). During the first time an adapter is plugged in, while the 150ms debounce time is running, the ISL9241 uses a Renesas technique to check if the VSYS output is shorted (see “System Voltage Rail Short Protection” on page 52).

When $V_{DD}$ > 2.7V, the ISL9241 digital block is activated and the SMBus register is ready to communicate with the master controller.

When the ISL9241 turns on the LDOs, it sources a current out of the PROG pin and reads the pin voltage to determine the PROG resistor value. The PROG resistor programs the ISL9241 configurations. See Table 13 on page 40.

When $V_{DD}$ > 3.8V, the ISL9241 allows the external circuit to pull up the ACOK pin. When ACOK is asserted, the ISL9241 starts switching.

ACOK is an open-drain output pin indicating the presence of the adapter and readiness of the adapter to supply power to the system bus. The ISL9241 actively pulls ACOK low in the absence of the adapter, or for Way Overcurrent (WCOP) or for Over-Temperature (OTP).

Two thresholds affect ACOK. The higher threshold controls ACOK. One threshold is fixed at 3.6V rising and one programmable threshold using the DAC (see Table 2 on page 28 for the ACOK Ref register). Register 0x40 value sets the threshold. The default register value is set to 0x0000h, which disables the programmable threshold detection. The programmable threshold is helpful for monitoring the input supply when targeting higher voltages with USB Power Delivery communications. The ADC is automatically enabled when the ACOK Ref register is programmed to a non-zero value. To detect an unplugged adapter, the adapter voltage has to fall below the ACOK threshold (the higher of 3.4V falling and the ACOK Ref register value).

For switching to start and continue, the CSIN voltage should be higher than the ACOK threshold and VDD should be higher than 3.8V.

In Battery Only mode, the ISL9241 enters Low Power mode if only the battery is present. $V_{DD}$ is 4.5V from the low power LDO to minimize the power consumption. $V_{DD}$ becomes 5V when it exits Low Power mode, such as when PSYS or ADC are enabled.

## 6.2 Programming Resistor

A 1% resistor from the PROG pin to GND programs the configuration of the ISL9241.

The AdapterCurrentLimit2 register default value is 1.5A.

Table 13 shows the programming options.

**Table 13. PROG Pin Programming Table**

| PROG-GND Resistance (Ω) | | | Cell Count | Default Switching Frequency (kHz) | PSYS or REFADJ Pin Selection | Default ACLimit1 Reg (A) | Information 2 (0x4D) <4:0> Readout |
|---|---|---|---|---|---|---|---|
| Min | Nominal | Max | | | | | |
| 305.91 | 309 | 312.09 | 2 | 724 | REFADJ | 1.5 | 00010 |
| 427.68 | 432 | 436.3 | 2 | 724 | REFADJ | 0.476 | 00011 |
| 556.38 | 562 | 567.6 | 2 | 724 | PSYS | 1.5 | 00100 |
| 674.19 | 681 | 687.8 | 2 | 724 | PSYS | 0.476 | 00101 |
| 797.94 | 806 | 814.06 | 2 | 1050 | PSYS | 0.476 | 00110 |
| 930.069 (Note 10) | 931 (Note 10) | 931.931 (Note 10) | 2 | 1050 | PSYS | 0.2 | 00111 |
| 1089.0 | 1100 | 1111 | 2 | 724 | PSYS | 3.0 | 01000 |
| 1356.3 | 1370 | 1383.7 | 2 | 724 | REFADJ | 0.2 | 01001 |
| 1603.8 | 1620 | 1636.2 | 3 | 724 | REFADJ | 0.2 | 01010 |
| 1851.3 | 1870 | 1888.7 | 3 | 724 | PSYS | 3.0 | 01011 |
| 2187.9 | 2210 | 2232.1 | 3 | 724 | PSYS | 0.2 | 01100 |
| 2712.6 | 2740 | 2767.4 | 3 | 724 | PSYS | 1.5 | 01101 |
| 3207.6 | 3240 | 3272.4 | 3 | 1050 | PSYS | 1.5 | 01110 |
| 3702.6 | 3740 | 3777.4 | 3 | 1050 | PSYS | 0.476 | 01111 |
| 4375.8 | 4420 | 4464.2 | 3 | 724 | REFADJ | 0.476 | 10000 |
| 5435.1 | 5490 | 5544.9 | 3 | 724 | REFADJ | 1.5 | 10001 |
| 6425.1 | 6490 | 6554.9 | 4 | 724 | REFADJ | 0.2 | 10010 |
| 7425.0 | 7500 | 7575.0 | 4 | 724 | REFADJ | 0.476 | 10011 |
| 8365.5 | 8450 | 8534.5 | 4 | 1050 | PSYS | 0.476 | 10100 |
| 9216.9 | 9310 | 9403.1 | 4 | 1050 | PSYS | 0.2 | 10101 |
| 1089 | 11000 | 11110 | 4 | 724 | PSYS | 1.5 | 10110 |
| 12573 | 12700 | 12827 | 4 | 724 | PSYS | 0.476 | 10111 |

**Note:**

10. Tolerance is tighter for this selection, 0.1% required. Other selections are typically 1% tolerance.

An open or short on the PROG pin configures the charger output to a safe value of 4.2V. The ISL9241 uses the default number of cells in series as Table 13 shows and sets the default MaxSystemVoltage register value accordingly, but the default MinSystemVoltage register is 0V to prevent charging.

The switching frequency can be changed through SMBus Control1 register Bit<9:7> after POR. See Table 4 on page 30 for a detailed description.

When VDD is turned on, the ISL9241 typically sources 130µA current out of the PROG pin and reads the PROG pin voltage to determine the resistor value. However, application environmental noise can pollute the PROG pin voltage and cause an incorrect reading. If noise is a concern, Renesas recommends connecting a capacitor from the PROG pin to GND to provide filtering. The resistor and the capacitor R-C time constant should be less than 40µs so the PROG pin voltage can rise to a steady state before the ISL9241 reads it.

By default, whenever the adapter is unplugged and ACOK goes from high to low, the ISL9241 resets the AdapterCurrentLimit1 register to the default setting determined by the PROG pin resistor. This current limit reloading can be disabled using Control3 Bit<14> as shown in Table 6 on page 32.

If PSYS is not enabled in Battery Only mode, the ISL9241 resets the MaxSystemVoltage register to the default value according to the PROG pin cell number setting. If PSYS is enabled, the ISL9241 keeps the value in the register.

The diagrams in this datasheet are based on current-sensing resistors $R_{s1}$ = 20mΩ and $R_{s2}$ = 10mΩ unless specified otherwise.

## 6.3 Charger Control Register Operations

### 6.3.1 System Voltage Regulation and Maximum Charging Voltage Regulation

If the battery is absent, or if a battery is present but BGATE is turned off, the ISL9241 regulates the system bus voltage at the MaxSystemVoltage register setting or optionally to the MaxSystemVoltage setting plus 384mV. The CSOP pin senses the system bus voltage. When a valid adapter voltage is not present and only the battery is present, the ISL9241 enters a low power state. In this state, the BGATE is turned on, and the charge current is not controlled if VSYS is raised above the battery voltage by an external source connected directly to VSYS. To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command to register address 0x15H using the Write-word protocol shown in Figure 30 on page 24 and the data format shown in Table 2 on page 28.

The MaxSystemVoltage register accepts any voltage command, but only the valid register bits are written to the register and the maximum value is clamped. A 0x0000H command in REG 0x15H causes the ISL9241 to stop switching and enter READY state.

When the device is not charging but is in the VSYS state and Control0 register Bit<1> is a 0, the system voltage is regulated to the same setting as the DAC. When Control0 register Bit<1> is a 1 then system voltage is regulated to the DAC plus an offset of 384mV, which is useful to avoid discharging a full battery in VSYS state when there is a system load transient.

The MaxSystemVoltage register sets the battery full charging voltage limit. The MaxSystemVoltage register setting is also the system bus voltage regulation point when the battery is absent or present but not in Charging mode. The MinSystemVoltage register setting is also the system voltage regulation point when it is in Trickle Charging mode. The CSOP pin is the system voltage regulation sense point in Trickle Charging mode. See Table 2 for more information about the Min System Voltage register.

The CSOP pin senses the battery voltage for maximum charging voltage regulation. The CSOP pin is also the system bus voltage regulation sense point and controls the VSYS operating voltage.

### 6.3.2 Normal/Fast Battery Charging and Charging Current Limit

To set the charging current limit, write a 16-bit ChargeCurrentLimit command to register address 0x14H (Table 2) using the Write-word protocol shown in Figure 30 on page 24. Set ChargeCurrentLimit = 0 and MinSystemVoltage = 0 to stop charging. Set ChargeCurrent Limit and MinSystemVoltage to non zero to start trickle or fast/normal charging. It is not recommended to set only one of these registers to 0.

By default, the adapter current-sensing resistor, $R_{s1}$, is 20mΩ and the battery current-sensing resistor, $R_{s2}$, is 10mΩ. Using the $R_{s1}$ = 20mΩ and $R_{s2}$ = 10mΩ option results in a 4mA/LSB correlation in the SMBus current commands.

If the $R_{s1}$ and $R_{s2}$ values are different from the $R_{s1}$ = 20mΩ and $R_{s2}$ = 10mΩ option, scale the SMBus commands accordingly to obtain the correct current. Smaller current sense resistor values reduce the power loss and larger current sense resistor values give better accuracy. For example, if using a 5mΩ $R_{s2}$, multiply each value in the DAC table by 2.

The ISL9241 limits the charging current by limiting the CSOP - CSON voltage, so reducing the current sense resistor value doubles the current being regulated to. By using the recommended current sense resistor values $R_{s1}$ = 20mΩ and $R_{s2}$ = 10mΩ, the LSB of the register (Charge current register <2>) always translates to 4mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register.

If different current-sensing resistors are used, the $R_{s1}$:$R_{s2}$ ratio should be kept as 2:1. If Control4 register Bit<11> is set, a 1:1 ratio is allowed but accuracy decreases. The PSYS output can be scaled accordingly to reflect the total system power correctly.

After POR, the ChargeCurrentLimit register is reset to 0x0000H, which disables fast charging and trickle charging. To enable fast charging the battery, write a non-zero number to the ChargeCurrentLimit register. The ChargeCurrentLimit register should be read back to verify its content.

When charging, system voltage is regulated to VBAT plus some IR drop due to sense resistor and BFET ON-resistance. The system voltage is above the MinSystemVoltage DAC setting and below the MaxSystemVoltage DAC setting plus appropriate offsets.

### 6.3.3 Trickle Charging and Minimum System Voltage Regulation

Writing the MinSystemVoltage register 0x3EH to 0x0000h disables all battery charging.

The ISL9241 supports trickle charging to an overly discharged battery. It can activate the trickle charging function when the battery voltage is lower than the MinSystemVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode. While trickle charging the battery, system regulation voltage is the DAC setting plus 384mV. It can take up to 100ms to transition from trickle-to-fast charge or fast-to-trickle charge.

To set the minimum system voltage, write a 16-bit MinSystemVoltage command to register address 0x3EH using the Write-word protocol shown in Figure 30 on page 24 and the data format shown in Table 2. To enable Trickle Charging, set the MinSystemVoltage and Charge Current register to a non-zero value higher than the battery voltage. To disable trickle charging, set the MinSystemVoltage and Charge Current register to 0. Setting the MinSystemVoltage and Charge Current register to 0x0000h disables all charging, which is the default and must be changed to allow any charging. The MinSystemVoltage register accepts any voltage command, but only the valid register bits are written to the register. The MinSystemVoltage register value should be set lower than the MaxSystemVoltage register value.

See Table 17 on page 60 for trickle charging control logic. When using the standard sense resistor, the trickle charging current can be programmed through SMBus Control2 register Bit<15:13> in Table 5 on page 31.

In Trickle Charging mode, the ISL9241 regulates the system voltage to the MinSystemVoltage DAC setting with voltage sensed at the CSOP pin and regulates the charge current to the trickle charge current to the setting in the Control2 <15:13>.

When the battery voltage is charged above the MinSystemVoltage register value, the ISL9241 enters Fast Charging mode by limiting the charging current at the ChargeCurrentLimit register setting using just the buck-boost switcher. The BFET is fully turned on. There may be a small amount of mode chatter at the trickle/fast charge boundary that stabilizes when trickle or fast charge mode is fully entered. The EOC flag may be set at the trickle-to-fast charge (or fast-to-trickle charge) boundary, so the flag needs to be reset before the actual EOC in autonomous mode.

The MinSystemVoltage register sets the battery voltage threshold to enter and exit Trickle Charging mode and Learn mode. The VBAT pin senses the battery voltage to compare with the MinSystemVoltage register setting. See "Battery Learn Mode" on page 45 for details.

### 6.3.4 Autonomous Charging Mode

The ISL9241 supports Autonomous Charging mode and enables automatic end of charge termination. This mode can be enabled or disabled through SMBus Control3 register Bit<7> (Table 6). When Autonomous Charging mode is enabled, the SMBus timeout timer is disabled and Reverse Turbo Mode must be disabled. Autonomous mode is not disabled by writing SMBus ChargingCurrentLimit or MaxSystemVoltage commands. If Autonomous Charging mode is set for 12 hours and the battery does not terminate charging, the control bit is reset disabling Autonomous Charging. This bit is also reset if a fault occurs. Control7 register Bit<9:8> sets the End of Charging (EOC) current settings (Table 8), and the Control3 register Bit<13> sets the debounce time (Table 6).

The ISL9241 enters Autonomous Charging mode when the BGATE MOSFET is on and the battery voltage is lower than the MaxSystemVoltage by a certain threshold (See Auto Recharge Threshold in the EC table) for 1ms debounce time.

In Autonomous Charging mode, the ISL9241 starts to charge the battery with the programmed value (REG0x14h). The PROCHOT# pin behaves as the Autonomous Charging mode indication pin and is pulled down to GND, and the SMBus timeout timer is disabled. The ISL9241 exits from Autonomous Charging mode when the battery charging current is less than the EOC setting for 20ms and 200ms in the CV loop. The autonomous charging termination time can be set by Control3 register Bit<13>. The ISL9241 enters Autonomous charging mode when the battery voltage falls below the MaxsystemVoltage - Auto Recharge Threshold for 1ms debounce time and the BGATE MOSFET is on. When the ISL9241 stays in Autonomous Charging mode for 12hrs (which means the battery charging current is higher than EOC), the ISL9241 stops charging the battery and exits Autonomous Charging mode, and the control bit is reset.

When not in Autonomous Charging mode, the charger does not terminate charging but instead enters a CV charge state with a small charging current. The termination and start of another recharge cycle is controlled by the SMBus master. If SMBus Timeout is disabled and a fault occurs, the ISL9241 stays in the fault mode until the disable bit is cleared.

Enabling Autonomous Charge disables the SMBus Timeout Timer and sets PROCHOT# to be an Autonomous Charging indicator.

### 6.3.5 SMBus Timeout

The ISL9241 includes a watchdog timer to ensure the SMBus master is active and to prevent overcharging the battery. The ISL9241 terminates charging by turning off the BGATE FET if the charger has not received a SMBus write command to the MaxSystemVoltage or ChargeCurrent register within 175s (default value in Control3 register Bit<12:11> = 00).

SMBus timeout time can be configured through SMBus Control3 register Bit<12:11>.

When the charging is stopped by the SMBus timeout, the ISL9241 transitions from charging to the VSYS regulation state. The ChargeCurrent register retains its value instead of resetting to zero. When a timeout occurs, the MaxSystemVoltage or ChargeCurrent register must be written to re-enable charging.

Enabling Autonomous Charge disables the SMBus Timeout Timer. You can disable the SMBus timeout function through SMBus Control0 register Bit<7> as Table 3 on page 29 shows.

### 6.3.6 BATGONE

The BATGONE pin is a dual-purpose pin that provides both an analog and a digital function. If pulled to VDD, the pin indicates a “battery gone” state, the digital function. In addition, an NTC can be connected from this pin to ground, the analog function.

A 1µA current pulls up on the BATGONE pin when not making an NTC ADC sample. A BATGONE condition is indicated if the pin voltage exceeds VDD minus a threshold (see “Electrical Specifications” on page 11 for value).

BATGONE needs to be low to enable OTG mode. When BATGONE is high the device exits Battery Learn mode.

### 6.3.7 NTC for Supporting JEITA Profiles

In addition to the internal die temperature, a thermistor for an NTC can be used on the BATGONE pin. The NTC is sensed using pulsed current source with three source current levels for reading the thermistor voltage on the pin. Table 14 shows the control truth table.

**Table 14. JEITA Control Bits Truth Table**

| Control2<5> JEITA Bit<1> | Control4<14> JEITA Bit<0> | Description |
|---|---|---|
| 0 | 0 | No JEITA profiles enabled, used for general purpose ADC input, current source on NTC is turned off. |
| 0 | 1 | JEITA profiles for 2-4 cell batteries enabled, NTC current source is turned on for measurements as Figure 31 shows. |
| 1 | 0 | Profile 1 is enabled, NTC current source is turned on for measurements as Figure 32 on page 45 shows. |
| 1 | 1 | Profile 2 is enabled, NTC current source is turned on for measurements as Figure 33 on page 45 shows. |

The ISL9241 charging profile follows one of the three JEITA profiles as shown in <Hyperlink>Figures 31, 32, and 33 if a thermistor with a 10k at +25°C (typically B = 3435) is used on the NTC pin. The temperature ranges for battery charging is followed if the JEITA charging profile is enabled. There are three automatic profiles for 2-4 cell batteries (cell count is determined by the PROG pin). Different temperature ranges can be selected by modifying the resistor network on the NTC pin; however, the steps in the graphs remain the same but at different temperatures.

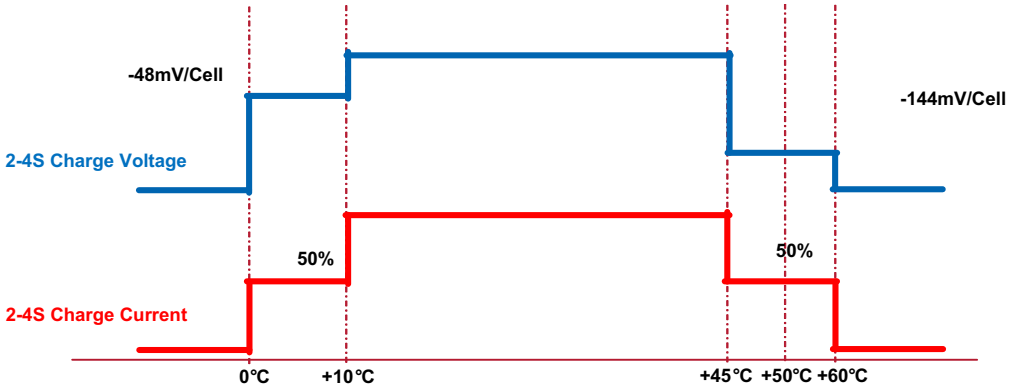



**Figure 31. JEITA Profile for 2-4 Cell Battery**

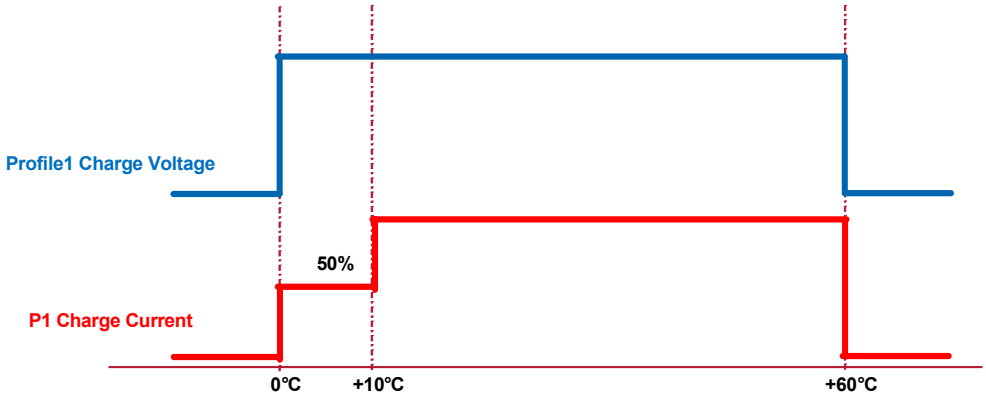



Figure 32. JEITA Profile 1

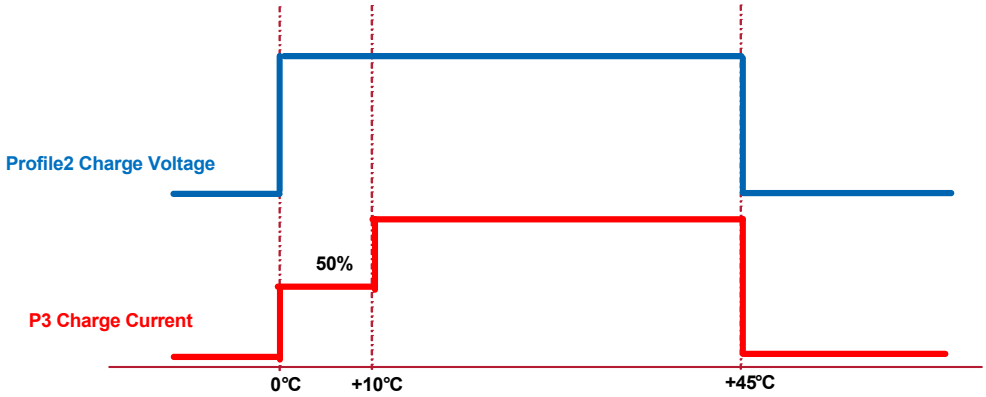



Figure 33. JEITA Profile 2

### 6.3.8 Battery Learn Mode

The ISL9241 supports Battery Learn mode when in NVDC mode only. The ISL9241 enters Battery Learn mode when it receives the SMBus Control command.

Use Battery Learn mode to supply the system power from the battery even when the adapter is plugged in, such as calibration of the battery fuel gauge (so the name “Battery Learn mode”).

In Battery Learn mode, the ISL9241 turns on BGATE and turns off the buck-boost switcher regardless of whether the adapter is present.

The three ways of exiting Battery Learn mode are as follows:

• Receive the Battery Learn mode exit command through SMBus (Control1 Bit<12> setting)

• Battery voltage is less than the MinSystemVoltage register setting (Control1 Bit<13> setting)

• BATGONE pin voltage goes from logic LOW to HIGH

In all these cases, the ISL9241 resumes switching immediately to supply power to the system bus from the adapter to prevent system voltage collapse.

### 6.3.9 Battery Only Operation Mode

When the battery voltage $V_{BAT}$ is higher than 2.7V and the adapter voltage $V_{ADP}$ (CSIN) is less than 3.2V, the ISL9241 operates in Battery Only mode. During Battery Only mode, the ISL9241 turns on the BGATE and NGATE to connect the battery to the system. In Battery Only mode, the ISL9241 consumes very low power. The battery discharging current monitor BMON can be turned on during this mode to monitor the battery

discharging current. If the battery voltage $V_{BAT}$ is high enough to maintain VDD above 3.8V, the system power monitor PSYS or ADC functions can be turned on during this mode to monitor system power or other parameters. OTG mode can be enabled only if the battery voltage is above 5.2V.

Turning on additional functionality increases current consumed.

### 6.3.10 Battery Ship Mode

Battery Ship mode sets the lowest power state for the IC. Ship mode can only be entered from Battery Only mode. To achieve the lowest power, the following analog functions must be disabled. Many are disabled by default and do not need to be written, but all are listed for completeness. However, the power level can be customized for the system.

**Control0 0x39h** (Table 3 on page 29)

• Bit<12> = 1 NGATE Off

• Bit<11> = 0 BPYSG Off

• Bit<10> = 0 BGATE Normal Operation

• Bit<6> = 0 Normal Charge Pump Operation

**Control1 0x3Ch** (Table 4 on page 30)

• Bit<10> = 0 Disable Supplemental support

• Bit<6> = 1 Force BGATE Off

• Bit<5> = 1 Disable IMON

• Bit<3> = 0 Disable PSYS

**Control3 0x4Ch** (Table 6 on page 32)

• Bit<0> = 0 ADC active only if adapter is plugged in and charging is enabled

**Control4 0x4Eh** (Table 7 on page 33)

• Bit<12> = 1 Disable GP Comparator for battery only mode

To exit Ship mode, either plug in an adapter or use the SMBus to change these control bits.

## 6.4 Reverse Modes

### 6.4.1 USB On The Go (OTG), USB - Power Delivery (PD)

When the OTG function is enabled with the SMBus command and OTGEN pin and if the battery voltage $V_{BAT}$ is higher than 5.2V, the ISL9241 operates in Reverse Buck, Reverse Boost, or Reverse Buck-Boost mode.

When the ISL9241 receives the command to enable the OTG function, it starts switching after a small delay. When the OTG output voltage reaches to the OTG output voltage set by register 0x49 Bit<14:3>, OTG power-good OTGPG is internally set and can be observed on the INT# if the interrupt is enabled (Table 9 on page 35).

**Note:** The OTGPG on ISL9241 is latched on the INT# pin and needs to be cleared. Information4 indicates the real-time status. In previous generations, the OTGPG pin indicated the real-time OTGPG status.

Before OTG mode starts switching, the CSIN pin voltage needs to drop below the OTG output overvoltage protection threshold (OTGVDAC + 100mV).

The ISL9241 includes the OTG output undervoltage and overvoltage protection functions. The UVP threshold is OTG output voltage -1.2V and the OVP threshold is OTG output voltage +1.2V.

The UVP threshold can be disabled for USB-C Programmable Power Supply (PPS) support using Control3<15>.

When OV is detected, the ISL9241 stops switching and deasserts OTGPG. It resumes switching 100µs after the OTG voltage drops below the OTG OV threshold.

BATGONE needs to be low to enable OTG mode. OTG mode is not available if the battery voltage is below 5.2V.

#### 6.4.1.1 OTG Voltage Register

The OTG voltage register contains SMBus readable and writable OTG mode output regulation voltage references. The default is 5.004V. This register accepts any voltage command. Do not program it higher than 23.4V due to internal overvoltage protection (OVP), although the register accepts the value.

OTG mode is allowed to be enabled only if the battery voltage is above 5.2V.

#### 6.4.1.2 OTG Current Register

The OTG current register contains the SMBus readable and writable OTG current limit. The default is 512mA. This register accepts any current command, but only the valid register bits are written to the register and the maximum value is clamped at 6112mA when the current is sensed across $R_{s1}$ = 20mΩ.

### 6.4.2 Fast Role Swap

The ISL9241 supports USB-C Power Delivery Fast Role Swap (FRS). FRS means quickly going from charging the battery to providing an OTG output voltage to provide power to accessories when another power source is disconnected. If FRS support is needed, enable OTG mode using the external pin, set up the OTG Voltage register for 5.004V, and toggle the external pin for OTGEN/CMIN to enable OTG mode when the FRS command is detected. If the adapter voltage is higher than 5V, the ISL9241 does not switch until CSIN is below the 5.004V DAC target.

### 6.4.3 Supplemental Power Support Mode

Supplemental power mode (also known as Intel VMIN Active mode or VAP) allows the use of the unattached input bias capacitor to store energy and releases it to the system during a high power demand. In this mode, the IC uses OTG mode to fill the input capacitance to store energy. When a large power event drops the VSYS voltage below the Low_VSYS_PROCHOT# level (set by Control1 Bit<1:0>), it quickly uses the stored energy and begins to buck from the input capacitance to hold up the VSYS node voltage. Additionally, the VSYS drop causes a PROCHOT# to let the processor know to throttle the power request. Supplemental mode is designed to temporarily support the VSYS rail because impedance from the battery pack (including battery impedance) to VSYS causes a drop during increased current loads. Set the OTGV voltage register 0x49H (Table 2 on page 28) to the highest tolerable voltage on the input capacitance to store the maximum available energy.

**Note:** Many capacitors reduce their total capacitance with higher applied voltage. Using the recommend maximum input capacitor of 150µF, the stored capacitor energy momentarily supplements the power provided by the battery under this condition.

During the OTG mode switching operation to fill the input capacitance, the battery discharge current should be limited to prevent an undesired PROCHOT warning during the charging of the input capacitor. The current used to refill the input capacitance is the value of the discharge current set by register 0x14H (Table 2 on page 28) minus the system load.

In ISL9241, the Low_Vsys_PROCHOT# during supplemental mode is asserted when one of the following two events happen:

- Supplemental mode runs ($C_{IN}$ capacitor discharges) for around 369µs
- $C_{IN}$ capacitor discharges enough for CSIN voltage to fall below CSOP+400mV voltage.

The 7µs debounce time for Low_Vsys_PROCHOT# assertion does not apply here.

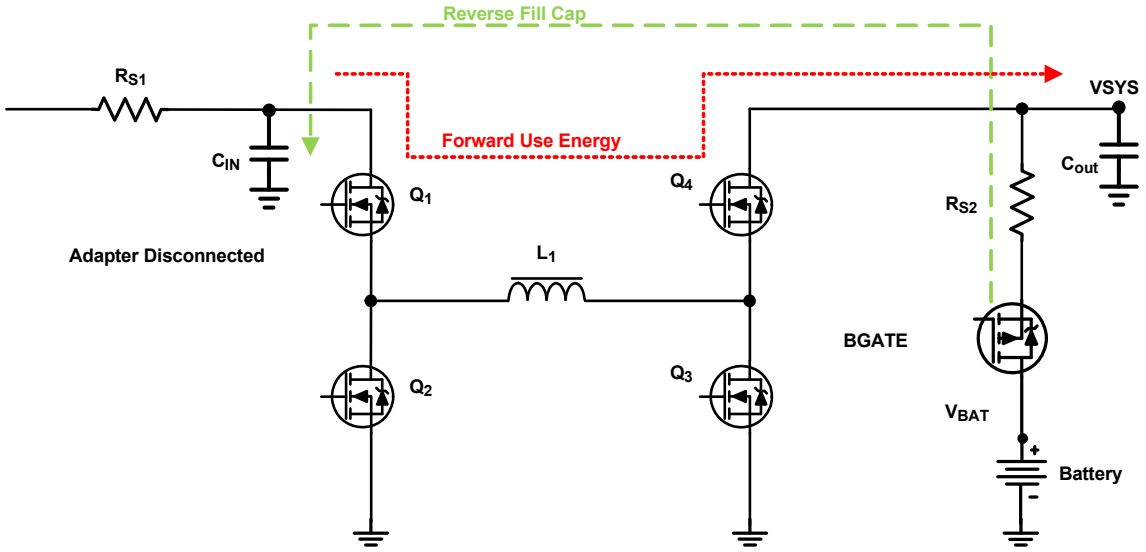



**Figure 34. Supplemental Mode Energy Flow**

Because the GPCOMP is shared with the same pin OTGEN, there is some logic to control whether it is supplemental support or OTG mode.

- If GPCOMP is enabled (Control2<3> = 0), only OTG can be enabled, and what directly follows is that the OTG function register bit (Control1<11>), supplemental mode bit (Control1<10>, and the OTGEN pin become don't care conditions.
- If GPCOMP is disabled (Control2<3> = 1), supplemental mode is disabled (Control1<10> = 0), OTG function register bit is enabled (Control1<11>), and OTGEN pin is enabled (Pin 26), OTG can be enabled.
- If GPCOMP is disabled (Control2<3> = 1), supplemental mode register bit is enabled (Control1<10> = 1), OTGEN register bit is low (Control1<11> = 0), OTGEN pin is high, supplemental mode can be enabled.

The function must be set up and armed. Figure 35 and Table 15 describe the logical function.

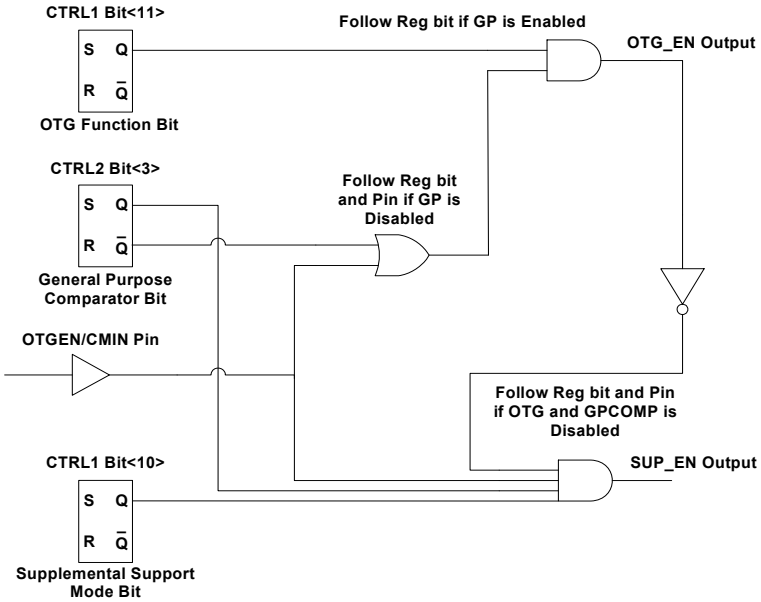



**Figure 35. Simplified Control Logic for OTG and Supplemental Mode**

**Table 15. Control Logic Truth Table for OTG and Supplemental Mode**

| Inputs | | | | Outputs | |
|---|---|---|---|---|---|
| External Pin OTGEN/CMIN | Control1 Bit<10> Supplemental Mode<br>1 - SUP<br>0 - OTG | Control2 Bit<3> GP Comparator<br>1 - Disable<br>0 - Enable | Control1 Bit<11> OTG Function<br>1 -Enable<br>0 - Disable | Logic Control Signal<br>OTG mode (OTG_EN) | Logic Control Signal<br>Supplemental mode (SUP_EN) |
| 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| x | x | 0 | 0 | 0 | 0 |
| x | x | 0 | 1 | 1 | 0 |

### 6.4.4 Reverse Mode Discharge Current Loop

When the charger is in reverse mode of operation (OTG, Supplemental mode), there is a discharge current limit loop that is set by 2xCharge Current limit register (0x14). This discharge current limit loop is in addition to the voltage regulation loop set by the OTG Voltage register and the current limit loop set by the OTG Current register. The discharge current limit loop is disabled when charge current(0x14) is zero. When the charge current is a non-zero value, the charger limits the battery discharge current to be less than the Discharge current, which is set by 2xCharge current limit register setting. This function can be used to limit inrush current from the battery when the OTG Voltage ramps up or down (in addition to the slew rate function).

## 6.5 Monitoring

### 6.5.1 Current Monitor

The ISL9241 provides an adapter current monitor/OTG current monitor or a battery charging current monitor/battery discharging current monitor through the AMON/BMON pin. The AMON output voltage is 18x (CSIP - CSIN) and 18x (CSIN - CSIP) voltage. The BMON output voltage is 18x (CSON - CSOP) and 36x (CSOP - CSON) voltage.

The AMON and BMON functions can be enabled or disabled through SMBus Control1 register Bit<5>, AMON or BMON can be selected through SMBus Control1 register Bit<4>, and AMON/BMON direction can be configured through SMBus Control3 register Bit<3>.

### 6.5.2 PSYS Monitor

The ISL9241 PSYS pin provides a measure of the instantaneous power consumption of the entire platform. The PSYS pin outputs a current source described by Equation 1.

$$I_{PSYS} = K_{PSYS} \times (V_{ADP} \times I_{ADP} + V_{BAT} \times I_{BAT}) + Offset \quad \text{(EQ. 1)}$$

$K_{PSYS}$ is based on current-sensing resistor $R_{s1}$ = 20mΩ and $R_{s2}$ = 10mΩ. $V_{ADP}$ (CSIN) is the adapter voltage in Volts, $I_{ADP}$ is the adapter current in Amperes, $V_{BAT}$ (CSON) is the battery voltage, and $I_{BAT}$ is the battery discharging current. When the battery is discharging, $I_{BAT}$ is a positive value; when the battery is being charged, $I_{BAT}$ is a negative value. The battery voltage $V_{BAT}$ is detected through the CSON pin to maximize the power monitor accuracy in NVDC configuration Trickle Charge mode.

The $R_{s1}$ to $R_{s2}$ ratio must be 2:1 for a valid power calculation to occur. If the PSYS information is not needed, any $R_{s1}$:$R_{s2}$ ratio is acceptable. Optionally, the $R_{s1}$ to $R_{s2}$ ratio can be 1:1 and for valid power calculation to occur, Control4 Bit<11> needs to be changed accordingly.

The overall gain KPSYS is affected by three parameters and is defined as follows:

(EQ. 2) $$K_{PSYS} = G_{PSYS} \times F_{RS2} \times H$$

- GPSYS is the PSYS gain set by Control3<9:8>.
- FRS2 is the value of the battery current sense resistor used (RS2) divided by 10mohm. For example, a 5mΩ $R_{S2}$ results in FRS2 = 5mΩ/10mΩ = 0.5
- H is the current feedback gain bit and is set by Control3<6>. Setting this bit to 0 is the default and results in H = 1. Setting this bit to 1 results in H = 0.5.

The PSYS gain can be configured through SMBus Control3 register Bit<9:8>. The default PSYS gain is set on VDD POR and three other settings for PSYS gain are available (see Table 6 on page 32). This gain scaling selection allows a range of power to be sensed on PSYS. The default setting is good for 60W systems, and the lowest (00) setting is good for 200W systems. You can change this gain based on the operating conditions to achieve the best accuracy.

The PSYS information includes the power loss of the charger circuit and the actual power delivered to the system. Resistor $R_{PSYS}$ connected between the PSYS pin and GND converts the PSYS information from current to voltage.

The PSYS function can be enabled or disabled through SMBus Control1 register Bit<3> as shown in Table 4 on page 30. Enabling the PSYS function increases the ISL9241 IC current consumption.

### 6.5.3 PROCHOT#

PROCHOT# is an open-drain output used to support IMVP protocols. On systems that do not need IMVP this pin can be used as an additional interrupt pin.

In Autonomous Charging mode, the ISL9241 starts to charge the battery with the programmed value (REG0x14h). The PROCHOT# pin behaves as Autonomous Charging mode indication pin and is pulled down to GND while charging.

#### 6.5.3.1 Setting the PROCHOT# Threshold for Adapter Overcurrent Conditions

To set the PROCHOT# assertion threshold for adapter overcurrent conditions, write a 16-bit ACProchot# command to register address 0x47H using the Write-word protocol shown in Table 30 on page 24 and the data format shown in Table 2 on page 28. By using the recommended current sense resistor values, the LSB of the register always translates to 128mA of adapter current. The ACProchot# register accepts any current command; however, only the valid register bits are written to the register, and the maximum value is clamped at 6400mA for $R_{s1}$ = 20mΩ.

After POR, the ACProchot# register is reset to 0x0C00H. The ACProchot# register can be read back to verify its content.

If the adapter current exceeds the ACProchot# register setting, the PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit<10:9> and latches on for a minimum time programmed by Control2 register Bit<8:6>.

#### 6.5.3.2 Setting the PROCHOT# Threshold for Battery Over Discharging Current Conditions

To set the PROCHOT# signal assertion threshold for battery over discharging current conditions, write a 16-bit DCProchot# command to register address 0x48H using the Write-word protocol shown in Figure 30 on page 24. By using the recommended current sense resistor values, the LSB of the register always translates to

256mA of adapter current. The DCProchot# register accepts any current command; however, only the valid register bits are written to the register, and the maximum value is clamped at 12.8A for $R_{s2}$ = 10mΩ.

After POR, the DCProchot# register is reset to 0x1000H. The DCProchot# register can be read back to verify its content.

If the battery discharging current exceeds the DCProchot# register setting, the PROCHOT# signal asserts after the debounce time programmed by the Control2 register Bit<10:9> and latches on for a minimum time programmed by Control2 register Bit<8:6>.

In Battery Only and Low Power mode, the DCProchot# threshold is set by Control0 register Bit<4:3>.

In Battery Only mode, the DCProchot# function using the DAC (0x48H) works only when PSYS or ADC is enabled because the charger is in READY state (not BAT state) when these two functions are enabled. When the charger is in READY state, DCProchot# works using the 0x48H register. When in BAT state, DCProchot# is set by Control 0<4:3>.

#### 6.5.3.3 Low_VSYS PROCHOT#

Low_VSYS is configured using Control1 Bits<2:0> (Table 4 on page 30); there are eight settings available.

#### 6.5.3.4 Supplemental Mode Low_VSYS PROCHOT#

During supplemental mode, the Low_VSYS is configured to activate the forward mode using the energy stored in the input capacitance. See "Supplemental Power Support Mode" on page 47 for more information about how supplemental power affects PROCHOT#.

Low_VSYS is set using Control1 Bits<2:0> (Table 4 on page 30). Eight settings are available.

#### 6.5.3.5 Other PROCHOT# Configuration

Control4 Bits<7:4> (see Table 7 on page 33) can be used to configure the PROCHOT# to be asserted for the following triggers: OTG Current, BATGONE, ACOK, or General Purpose Comparator.

#### 6.5.3.6 Setting PROCHOT# Debounce Time and Duration Time

Control2 register Bit<10:9> (see Table 5 on page 31) configures the PROCHOT# signal debounce time before its assertion for ACProchot# and DCProchot#.

The low system (VSYS_LOW) voltage PROCHOT# has a fixed debounce time of 7µs.

Control2 register Bit<8:6> configures the minimum duration of the PROCHOT# signal when asserted for VSYS_LOW, ACPROCHOT#, and DCPROCHOT#.

For the ACOK and BATGONE, Control4 Bits<3:2> (see Table 7 on page 33) can configure the debounce time before PROCHOT# is asserted.

#### 6.5.3.7 Setting PROCHOT# Clear and Latch Control Bits

Control4 Bit<0> Table 7 on page 33 can be used to configure the PROCHOT# to latch and hold its state. This configuration is helpful as an interrupt flag to allow the system to determine what happened. If this bit is set, the Control4 Bit<1> Table 7 on page 33 must be used to clear the asserted PROCHOT#.

### 6.5.4 ADC Operation

The Analog to Digital Converter (ADC) is a successive-approximation 8-bit converter. Table 12 on page 38 identifies the bit locations of the control and information available. The ADC monitors and loops though measuring, battery voltage, current, temperature through NTC, input current, and internal die temperature. The ADC is always disabled if $V_{DD}$ falls below 3.8V. Data is always valid to be read as a raw number from the last completed sample, and it updates once per polling time. Equation 3 shows the ADC measurement for the junction temperature ($T_J$ in °C). The measured code has a maximum value of 255.

$$\text{Reg0x82(decimal)} = 251.7 - 0.6154 \times T_J \quad \text{(EQ. 3)}$$

Example timing windows are shown in Figure 36.

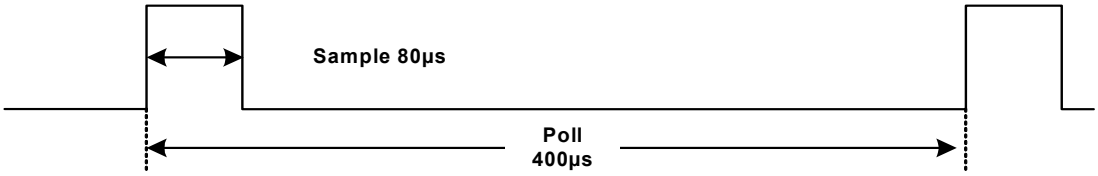



**Figure 36. ADC Sample and Polling Time**

## 6.6 Protection

### 6.6.1 Adapter Overvoltage Protection

If the adapter voltage sensed on the CSIN pin voltage exceeds 23.4V for more than 2µs, an adapter overvoltage condition occurs. The device stops switching to isolate the adapter from the system and BGATE turns on for the battery to support the system load. When the CSIN voltage drops below 23.05V for more than 2µs, it starts switching again. ACOK does not change states during this fault state.

### 6.6.2 Battery Protection

The battery is monitored by the ADC by reading register 0x81h and controlled using a NMOS FET (BFET). The gate (BGATE) of the BFET operates in trickle mode to protect the battery from excessive voltages. The ISL9241 controls the charging current using register 0x14h. An NTC input provides thermal protection to protect the battery from charging when outside of the normal operating region. For excessive voltage during constant current phase, the system overvoltage protection prevents excessive voltage on the battery.

When no valid adapter voltage is present (on CSIN) and only the battery is present, the ISL9241 enters a low power state. In this state the BGATE is turned on, but charge current is not controlled if VSYS is raised above the battery by an external source connected directly on VSYS (CSOP).

### 6.6.3 System Voltage Rail Short Protection

The ISL9241 has a system rail short protection to prevent powering on the system rail into a short-circuit before start of switching. When the VSYS voltage is below 0.6V, the ISL9241 sources 10mA current from VDDP to charge VSYS before the switching can start. When the VSYS pin is charged above 0.6V, an internal timer starts to count. After 10µs debounce time of the VSYS voltage being above 0.6V, the ISL9241 stops sourcing 10mA current and allows the ISL9241 to start switching. Any time a transition occurs from the READY state (disable switching with MaxSystemVoltage = 0V) back to the VSYS state (switching enabled by setting MaxSystemVoltage > 0V), the 10mA turns on again and CSOP voltage has to be charged above 0.6V to allow switching again.

### 6.6.4 System Voltage Overvoltage Protection

If the system voltage VSYS is 800mV higher than the MaxSystemVoltage register set value, the ISL9241 declares the system overvoltage and stops switching. It resumes switching without debounce when VSYS drops 400mV below the system overvoltage threshold.

### 6.6.5 Way Overcurrent Protection (WOCP)

If the system bus is shorted (either a MOSFET short or an inductor short) the input current could be high. The ISL9241 includes input overcurrent protection to turn off the BYPSG and stop switching.

The ISL9241 provides adapter current and battery discharging current Way Overcurrent Protection (WOCP) function against MOSFET shorts, system bus shorts, and inductor shorts. The ISL9241 monitors the CSIP - CSIN voltage and CSON - CSOP voltage, and compares them with the WOCP threshold (12A for adapter current and 20A for battery discharge current).

When the WOC comparator is tripped, the ISL9241 increments a timer every 10µs. Whenever the timer reaches 7 counts, the charger deasserts ACOK, and stops switching immediately. The timer is reset every 50ms. After the 1.3s or 150ms debounce time set by Control2 register Bit<11>, it goes through the start-up sequence to retry.

The WOCP function can be disabled through Control4 register Bit<9>.

### 6.6.6 Over-Temperature Protection

The ISL9241 stops switching for self protection when the junction temperature exceeds +140°C.

When the temperature falls below +120°C for 100µs and after the 1.3s or 150ms delay, the ISL9241 resumes switching.

Internal die temperature can be monitored using the ADC, and firmware can update parameters to avoid thermal shutdown.

In addition to the internal die temperature, you can use a thermistor for an NTC on the BATGONE pin to control charging in accordance to the JEITA profiles. See "BATGONE" on page 43 for more details.

## 6.7 Additional Features

### 6.7.1 Stand-Alone Comparator

The ISL9241 includes a general purpose stand-alone comparator. The OTGEN/CMIN pin is the comparator input. The internal comparator reference is connected to the inverting input of the comparator and is configured by Control2 register Bit<4> as 1.2V or 2V (Table 5 on page 31). The comparator output is the CMOUT/INT# pin, and the output polarity when the comparator is tripped can be configured through the SMBus register bit.

When Control2 register Bit<2> = 0 for normal comparator output polarity and if CMIN > Reference, CMOUT = High; if CMIN < Reference, CMOUT = Low.

When Control2 register Bit<2> = 1 for inversed comparator output polarity and if CMIN > Reference, CMOUT = Low; if CMIN < Reference, CMOUT = High.

By default in Battery Only mode, the stand-alone comparator is enabled. This comparator can be enabled/disabled in Battery Only mode using Control4 register Bit<12> (Table 7 on page 33); however, the reference is set to 1.2V. Control2 <3> should also be enabled to enable the General purpose comparator in Battery only mode.

The general purpose comparator and INT# share the same pin, so either of them can pull the pin low if interrupts and GPCOMP are enabled. If all interrupts are disabled, the CMOUT/INT# pin shows the output of the GPCOMP. If GPCOMP is disabled, the pin indicates interrupt status only.

Figure 37 shows the Interrupt and the stand-alone comparator implementation.

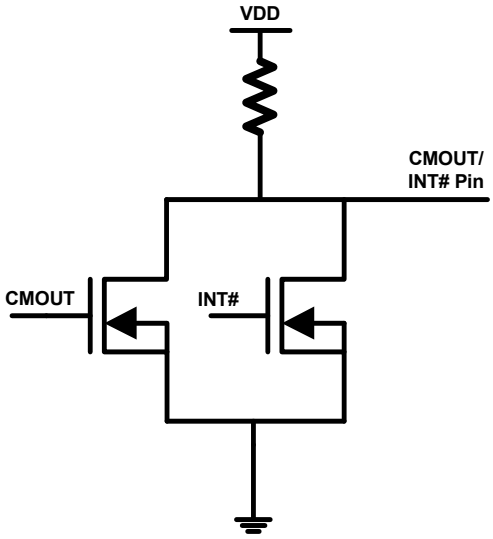



**Figure 37. INT# and CMOUT Implementation**

### 6.7.2 REFADJ Feedback Mode

The ISL9241 can support an external feedback resistor on the REFADJ pin. REFADJ mode allows the OTG output voltage to be controlled with an external feedback resistor. This mode is determined by the PROG resistor on power up (see Table 13) and is mutually exclusive to PSYS pin functionality.

One design method can be used to support Qualcomm quick charge feedback devices. These devices decode the D+/D- inputs and send a current into the resistor divider to make an adjustment in the OTG output voltage.

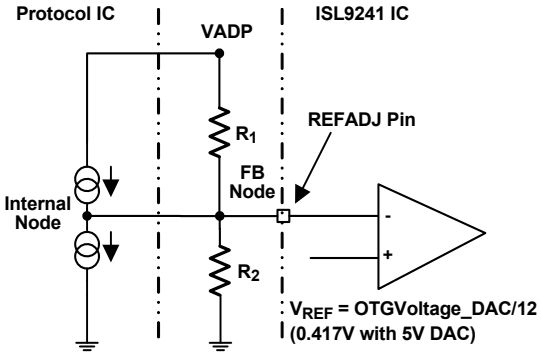



**Figure 38. Simplified REFADJ Application**

The schematic shown in Figure 38 on page 54 shows how the REFADJ pin is tied to the feedback (FB node) resistor divider node off the VADP node for a quick charge protocol IC. This schematic sets up the FB node to use the reference voltage of 0.417V from ISL9241, but the output on the VADP node can be set up to any voltage over the standard operating range using the $R_1/R_2$ ratio.

# 7. Modulator Information

## 7.1 ISL9241 Buck-Boost Charger Modes of Operation

The ISL9241 buck-boost charger drives an external N-channel MOSFET bridge made up of two transistor pairs as shown in Figure 39. The first pair, $Q_1$ and $Q_2$, is a buck arrangement with the transistor center tap connected to an inductor "input", as is the case with a buck converter. The second transistor pair, $Q_3$ and $Q_4$, is a boost arrangement with the transistor center tap connected to the same output of the inductor, as is the case with a boost converter. This arrangement supports bucking from a voltage input higher than the battery and also boosting from a voltage input lower than the battery.

**Note:** In OTG mode the output sensing point is the CSIN pin.

**Table 16. Operation Mode**

| Mode | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
|---|---|---|---|---|
| Buck | Control FET | Sync. FET | OFF | ON |
| Boost | ON | OFF | Control FET | Sync. FET |
| Buck-Boost | Control FET | Sync. FET | Control FET | Sync. FET |
| OTG Buck | ON | OFF | Sync. FET | Control FET |
| OTG Boost | Sync. FET | Control FET | OFF | ON |
| OTG Buck-Boost | Sync. FET | Control FET | Sync. FET | Control FET |

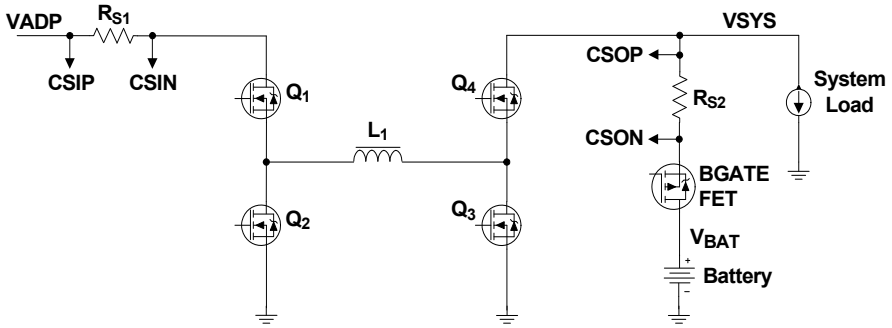



**Figure 39. Buck-Boost Charger Topology**

The ISL9241 optimizes the Operation mode transition algorithm by considering the input and output voltage ratio and the load condition. When the adapter voltage $V_{ADP}$ is rising and is higher than 94% of the system bus voltage VSYS, the ISL9241 transitions from Boost mode to Buck-Boost mode; if $V_{ADP}$ is higher than 112% of VSYS, the ISL9241 is forced to transition from Buck-Boost mode to Buck mode regardless of other conditions. At heavier load, the mode transition point changes accordingly to accommodate the duty cycle change due to the power loss on the charger circuit.

When the adapter voltage $V_{ADP}$ is falling and is lower than 106% of the system bus voltage VSYS, the ISL9241 transitions from Buck mode to Buck-Boost mode; if $V_{ADP}$ is lower than 92% of VSYS, the ISL9241 transitions from Buck-Boost mode to Boost mode.

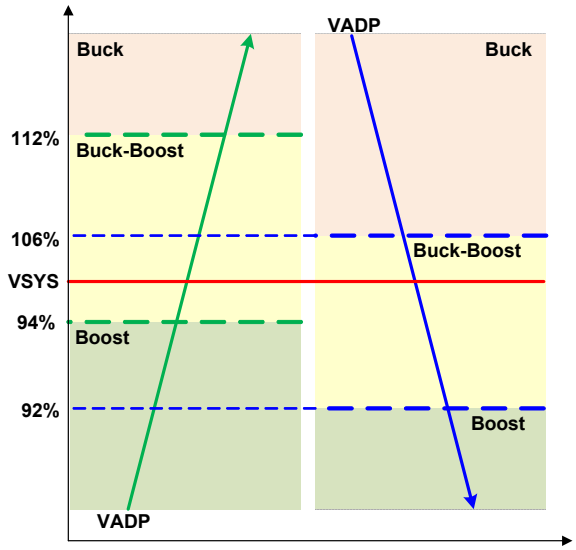



**Figure 40. Operation Mode**

When the OTG function is enabled with the SMBus command and OTGEN pin and if the battery voltage $V_{BAT}$ is higher than 5.2V, the ISL9241 operates in OTG mode. Fast role swap is similar to OTG but uses shorter filters to allow a very quick response to hold up the input when the adapter is detected as unplugged.

## 7.2 Modulator Control Loops

The four main control loops for the modulator are shown in Figure 41. Each loop has a DAC register to provide settings as needed for each system.

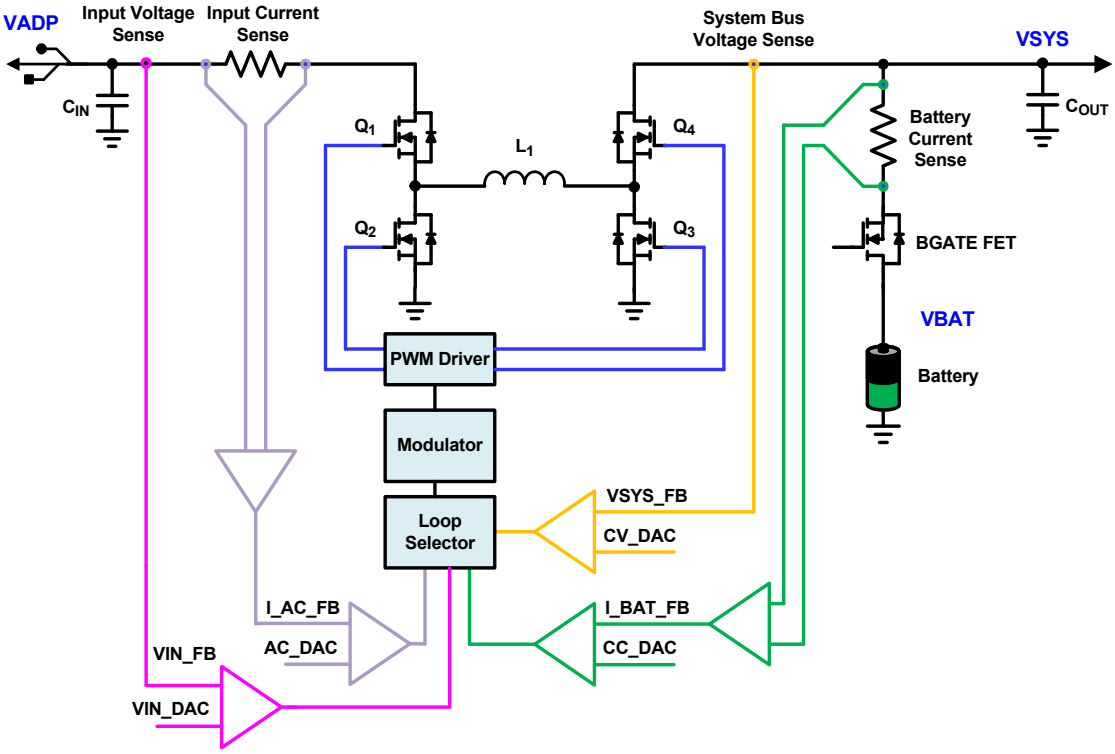



**Figure 41. Charger Control Loops**

### 7.2.1 Adapter Current Loop and Current Limit 1 and 2 and Two Level Current Limit

To set the adapter current limit, write a 16-bit AdapterCurrentLimit1 command to register address 0x3FH and/or AdapterCurrentLimit2 command to register address 0x3BH using the Write-word protocol shown in Figure 30 on page 24 for a 20mΩ $R_{s1}$. For the DAC summary of values, see Table 2 on page 28.

The ISL9241 limits the adapter current by limiting the CSIP - CSIN voltage. By using the recommended current sense resistor values, the LSB of the register always translates to 4mA of adapter current. Any adapter current limit command is accepted; however, only the valid register bits are written to the AdapterCurrentLimit1 and AdapterCurrentLimit2 registers, and the maximum value is clamped.

After adapter POR, the AdapterCurrentLimit1 register is reset to the value programmed through the PROG pin resistor. The AdapterCurrentLimit2 register is set to its default value of 1.5A or keeps the value that is written to it previously if the battery is present first. The AdapterCurrentLimit1 and AdapterCurrentLimit2 registers can be read back to verify their content. By default, the two level adapter current limit is disabled.

The AdapterCurrentLimit2 register has the same specification as the AdapterCurrentLimit1 register.

The two-level adapter current limit function can be enabled and disabled through SMBus Control2 register Bit<12>, and the t1, t2 settings are configured by Control7 register (Table 8 on page 34). When the two-level adapter current limit function is disabled, only the AdapterCurrentLimit1 value is used as the adapter current limit and AdapterCurrentLimit2 value is ignored

In a real system, a Turbo event usually does not last very long. It is often no longer than milliseconds, a time during which the adapter can supply current higher than its DC rating. The ISL9241 employs a two-level adapter current limit to fully take advantage of the surge capability of the adapter and minimize the power drawn from the battery.

Figure 42 shows the two SMBus programmable adapter current limit levels, AdapterCurrentLimit1 and AdapterCurrentLimit2, as well as the durations t1 and t2. The two-level adapter current limit function is initiated when the adapter current is less than 100mA lower than the AdapterCurrentLimit1 register setting. The adapter starts at AdapterCurrentLimit2 for t2 duration and then changes to AdapterCurrentLimit1 for t1 duration before repeating the pattern. These parameters can set the adapter current limit with an envelope that allows the adapter to temporarily output surge current without requiring the charger to enter Turbo mode. This operation maximizes battery life.

The AdapterCurrentLimit1 register value can be higher or lower than AdapterCurrentLimit2 value.

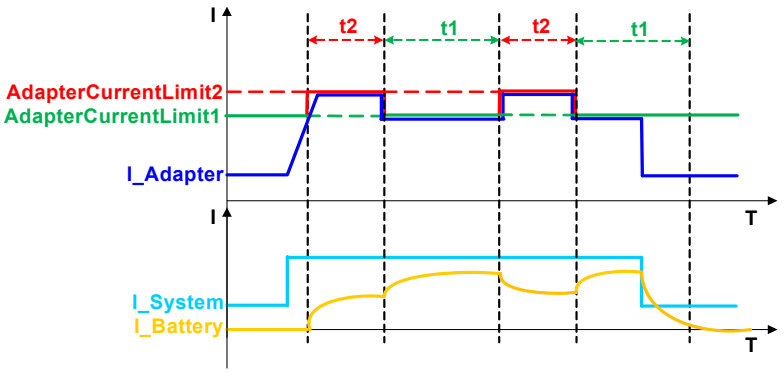



**Figure 42. Two-Level Adapter Current Limit**

#### 7.2.1.1 USB-PD On-the-Go Output Current

The OTG output current regulation register DAC (Table 2 on page 28) contains the SMBus readable and writable current that the current sense loop tries to regulate. This loop reuses the input current sense amplifier. If USB-PD Programmable Power Supply is needed, this is the current limit loop. **Note:** The OTG_UV needs to be disabled (see Control3 Bit<15> in Table 6 on page 32).

This register accepts any current command, but only the valid register bits are written to the register. The maximum value is clamped.

### 7.2.2 Input Voltage Regulation Loop

#### 7.2.2.1 Adapter Support Voltage

The input voltage regulation register DAC (Table 2 on page 28) contains the SMBus readable and writable input voltage limit at which the input voltage loop tries to regulate when the input voltage is dropping. When the ADP is browning out or weak, the input voltage can droop and the input voltage loop tries to regulate to this setting by reducing battery charging current and then system power to try to hold up the input voltage. The system voltage may start to drop if the input power is not high enough to support the system.

This register accepts any current command but only the valid register bits are written to the register The maximum value is clamped.

#### 7.2.2.2 USB-PD On-the-Go Output Voltage

The OTG output voltage regulation register DAC (Table 2 on page 28) contains the SMBus readable and writable voltage that the voltage loop tries to regulate. This loop reuses the input voltage sense amp.

This register accepts any current command, but only the valid register bits are written to the register the maximum value is clamped.

### 7.2.3 System Voltage Regulation Loop

This loop works for two different voltage settings: MaxSystemVoltage and MinSystemVoltage.

If the battery is absent, or is present but BGATE is turned off or not charging and if Control0 register Bit<1> is a 0, the system voltage is regulated to the same setting as the DAC. When Control0 register Bit<1> is a 1, the system voltage is regulated to the DAC plus an offset of 384mV (Table 3 on page 29). This additional offset is useful to avoid discharging a full battery in the VSYS state when there is a system load transient.

To set the maximum charging voltage or the system regulating voltage, write a 16-bit MaxSystemVoltage command to register address 0x15H using the Write-word protocol shown in Figure 30 on page 24 and the data format shown in Table 14 on page 44. A 0V command causes the ISL9241 to stop switching and enter the READY state.

The ISL9241 supports trickle charging to an overly discharged battery. It can activate the trickle charging function when the battery voltage is lower than the MinSystemVoltage setting. The VBAT pin is the battery voltage sense point for Trickle Charge mode. While trickle charging the battery, the system regulation voltage is the DAC setting plus 384mV.

To enable Trickle Charging, set the MinSystemVoltage and Charge Current register to a non-zero value higher than the battery voltage. To disable trickle charging, set the MinSystemVoltage and Charge Current register to 0. See Table 17 on page 60 for trickle charging control logic.

The CSOP pin senses the system voltage for MaxSystemVoltage and MinSystemVoltage during trickle charging and controls the VSYS operating voltage.

### 7.2.4 Charging Current Loop

The charging current loop uses the charge current DAC (see Table 15 on page 49) to set the fast charging current limit. In Trickle Charging mode, the ISL9241 regulates the trickle charging current through the buck-boost switcher. Another independent control loop controls the BGATE FET so the system voltage is maintained at the voltage set in the MinSystemVoltage register.

To set it, write a 16-bit ChargeCurrentLimit command to register address 0x14H (Table 2) using the Write-word protocol shown in Figure 30 on page 24.

The ISL9241 limits the charging current by limiting the CSOP - CSON voltage, so reducing the current sense resistor value doubles the current being regulated to. By using the recommended current sense resistor values $R_{s1}$ = 20mΩ and $R_{s2}$ = 10mΩ, the LSB of the register always translates to 4mA of charging current. The ChargeCurrentLimit register accepts any charging current command, but only the valid register bits are written to the register.

## 7.3 Buck Boost Configurable Charger

The ISL9241 is a Buck-Boost battery charger that can support both Narrow Voltage DC (NVDC) charging or Hybrid Power Buck Boost (HPBB) charging. NVDC is the initial start up state for the ISL9241, and firmware from a controller using the $I^2C$ interface is used to change the configuration to HPBB.

The ISL9241 allows the system to be optimized for both types of configurations. For lower power systems, the NVDC mode may be appropriate and reduces system complexity. For higher power systems, the hybrid mode may be the best choice to allow a smaller inductor but support higher system power with improved efficiency.

Because the system power does not pass through the inductor, hybrid power mode allows high power systems to size the inductor for just the maximum charging current or the turbo boost current. Because main power goes directly from the adapter to the system, the system efficiency improves and the inductor is smaller, which saves board area. For NVDC mode configuration, the inductor has to support the full system power and needs to be a larger size because it supports both charging and system power.

This mode allows the whole switch circuit to be bypassed only when the ADP is greater than the battery voltage. It connects the ADP to the VSYS through two NFETs using an internal charge pump for the gate drive. This mode is primarily controlled by firmware to ensure flexibility and has only fault protections for safety. Ensure that ADP > VBAT either by ensuring that ADP > VBAT or by enabling the VIN > VOUT bypass comparator (Control0 Bit<5> (Table 3 on page 29) to automatically turn off the BYPSG gate.

After exiting Bypass mode, wait to turn NGATE on until discharge current or VSYS ≈ VBAT.

OTG and Fast role swap must not be allowed while in Bypass mode, and firmware must prevent the toggling of the OTGEN pin. Bypass mode must be enabled to allow reverse turbo boost operation.

See the ISL9241 device page for firmware documentation.

### 7.3.1 NVDC Charger

In NVDC mode, the inductor supports the full system power and the power for charging the battery; therefore, the inductor typically needs to be a larger size because it supports both charging and system power.

The ISL9241 automatically selects the adapter and/or the battery as the source for system power. The BGATE pin drives an N-channel MOSFET (NFET) gate that connects or disconnects the battery from the system and the switcher.

#### 7.3.1.1 Normal Charging

In NVDC mode, the charging current is selected for the charge rate into the battery. However, the input current limit should be set for the total system plus battery charging current.

If VDD is higher than 3.8V, the ISL9241 enters Forward Buck, Forward Boost, or Forward Buck-Boost mode depending on the adapter and system voltage VSYS duty cycle ratio. The system bus voltage is regulated at the

voltage set on the MaxSystemVoltage register. If the charge current register is programmed (non-zero), the ISL9241 charges the battery either in Trickle Charging mode or Fast Charging mode as long as BATGONE is low.

#### 7.3.1.2 Turbo Support

In NVDC charger configuration and Turbo mode (also known as Ideal Diode Mode, IDM), the ISL9241 turns on the BGATE FET to limit the adapter current at the adapter current limit set point while the battery supplies the rest of the power required by the system. To turn on BGATE in Turbo mode, the CSON pin voltage needs to be 175mV lower than the VBAT pin voltage. If the ISL9241 detects 150mA charging current or if the battery discharging current is less than 140mA for 40ms, it turns off BGATE to exit Turbo mode. See Table 17 for BGATE operation.

In most systems, a Turbo event usually does not last very long. It is often no longer than milliseconds, a time during which the adapter can supply current higher than its DC rating. The ISL9241 employs a two-level adapter current limit to fully take advantage of the surge capability of the adapter and minimize the power drawn from the battery.

**Table 17. NVDC Charger Behavior Truth Table**

| Turbo - BGATE Force Off Control Bit | Charging Enabled CC ≠ 0; VSYSMIN ≠ 0 | BGATE On/Off | |
|---|---|---|---|
| 0 = Enable 1 = Disable | 0 = Disabled Charging 1 = Enabled Charging | System Load Not In Turbo Mode Range | System Load In Turbo Mode Range |
| 0 | 0 | Off | On |
| 0 | 1 | ON for fast charge; trickle charge enabled | On |
| 1 | 0 | Off | Off |
| 1 | 1 | ON for fast charge; trickle charge enabled | On |

### 7.3.2 Bypass Mode/Hybrid Power Buck-Boost (HPBB)

The ISL9241 can operate in HPBB configuration when the adapter voltage is higher than the battery voltage. The adapter voltage should be higher than the battery voltage at all times, under heavy DC and transient load conditions- so I*R drops and tolerances should be taken into consideration. To allow margin for the $V_{IN} < V_{OUT}$ comparator, the adapter voltage should be at least 1-2V higher than the battery after I*R drop and tolerances considered. Set the ACOK reference to a value lower than 1V below the minimum adapter voltage (after tolerances and I*R drop) and higher than the battery full charge voltage (so the charger can detect and let the input ramp down during adapter removal events). Because ACOKREF and $V_{IN} < V_{OUT}$ comparator are critical protections for the charger, it is advised to enable both features and set them at appropriate values as previously described. Four operational modes are supported when using the HPBB configuration. Bypass refers to both passing the adapter power directly to the system and bypassing the inductor and charger. Bypass can be combined with charging when the adapter power is higher than the system plus charging power. If the input power is not enough for the system, Reverse Turbo-Boost mode can take power from the battery and provide it to the system. If the device was charging but the input power droops, the ISL9241 can automatically switch from charging to reverse turbo-boost.

#### 7.3.2.1 Bypass

The BYPSG pin drives a pair of back-to-back common source NFETs to connect or disconnect the adapter from the system and the battery. When the NFETs are turned on, it bypasses the switching FETs and inductor to provide a higher efficiency path from the adapter input to the system output. At the same time, the battery path is isolated by turning off the NGATE NFET. When using the BYPSG, the BYPSRC must be greater than 2.7V, or the BYPSG needs a leakage resistance around 10MΩ placed from gate to source (BYPSG to BYPSRC) to prevent over charging the gate.

Bypass mode can exited only by command or an OVP/OC fault. While in Bypass mode, the buck-boost path can support a Reverse Turbo Boost mode and augment the adapter power from the battery.

An optional $V_{IN} > V_{OUT}$ (CSIN > CSOP) comparator can be used to turn off the Bypass gate when the CSIN falls below CSOP + 400mV. This comparator can be enabled and used with ACOK threshold to detect an adapter unplug event. The comparator turns on the Bypass gate again when CSIN rises above CSOP + 800mV.

When using Bypass mode, Renesas recommends setting the Force Buck mode, Control4 Bit<10> = 1. This configuration prevents chatter and possible exit if the $V_{IN} > V_{OUT}$ comparator trips due to the chatter.

Use of the BYPSG/BYPSRC/NGATE pins is optional.

#### 7.3.2.2 Bypass + Charging

When in Bypass mode, normal battery charging is similar to normal charging.

#### 7.3.2.3 Reverse Turbo-Boost Mode

Turbo mode refers to the system drawing more power than the power rating of the adapter. Turbo mode prompts the need for the switcher to change from Forward mode of operation to Reverse mode of operation to reverse the energy flow from going into the battery from going out of the battery. This mode of operation enables the battery to help the adapter provide the required system power. This operation has been widely used in many systems, such as Sun mode and Eclipse mode for bidirectional battery charger/discharger used on satellites with solar panels as the power source acting as the adapter (reference *A zero voltage switching bidirectional battery charger/discharger for the NASA EOS Satellite*, Dan M. Sable, Fred C. Lee and Bo H. Cho, APEC 1992 Conference Proceedings). To use the HPBB charger configuration, follow the steps from R16AN0001: *ISL9241 Operation Modes*.

The ISL9241 automatically selects the adapter and/or the battery as the source for system power. When the adapter power is not enough for the system as detected by the input current limit loop, the battery needs to supplement the adapter. As a result, the charger operates in the reverse direction and takes energy from the battery to hold up the input voltage.

The Control0 register Bit<0> enables or disables the Reverse Turbo-Boost function. See Table 3 on page 29 for details. Use caution when enabling reverse Turbo because the BFET is held on and there is potential to have excessive current into the battery. Autonomous Charging must be disabled before enabling the Reverse Turbo-Boost function.

In Reverse Turbo-Boost mode, the ISL9241 operates the switcher in reverse mode to pull energy from the battery and give energy to the adapter voltage rail so that the adapter current is limited at the adapter current limit set point, while the battery supplies the additional power required by the system.

#### 7.3.2.4 Reverse Turbo Boost Mode + Charging

When in Bypass mode with Reverse Turbo Enabled, normal battery charging is similar to normal charging, unless the adapter power is not enough for the system as detected by the input current limit loop. If there is not enough adapter power, the battery needs to supplement the adapter. When this occurs, first the charging stops, and if the power demand increases, the ISL9241 operates in the reverse direction and takes energy from the battery to hold up the input voltage.

The ISL9241 automatically enters Reverse Turbo mode when all of the following three criteria are met:

- The adapter current is within 80mA of the AdapterCurrentLimit1 (or AdapterCurrentLimit2 if two-level adapter current limit function is enabled) register setting
- The battery charging current is less than 150mA
- The COMP pin voltage is lower than 1.4V

Meeting all of these criteria means that the ISL9241 enters Reverse Turbo mode only when it is absolutely necessary.

For example, assume the adapter voltage is 20V, the adapter current limit is 4A (80W rating), and the ISL9241 is charging an 8V battery at a 5A rate (40W charging power). If the system load increases from 0W to 79W instantaneously, the adapter current increases from 2A to 5.95A instantaneously and exceeds the 4A current limit level. However, the adapter current loop takes control and decreases the charging current to limit the adapter current at 4A, eventually providing 79W of system power and 1W of battery charging power. In this case, the ISL9241 does not need to enter Turbo mode adapter and can conserve battery energy. In the same example, if the system load increases from 0W to 81W instantaneously, the adapter current increases from 2A to 6.05A instantaneously and exceeds the 4A current limit level. The adapter current loop takes control and decreases the charging current to limit the adapter current at 4A. Therefore, the ISL9241 eventually determines that it needs to enter Turbo mode, so that the adapter provides 80W, and the battery provides 1W to provide 81W to the system.

The interaction of the control loops within the ISL9241, including the adapter current loop, the charging current loop, and the battery full charging voltage loop, determines the timing of the Reverse Turbo mode entry. The timing strongly depends on the control loop compensation design and the interaction among the loops. In the previous example, compared with system power instantaneously increasing from 0W to 81W, system power instantaneously increasing from 0W to 160W causes the ISL9241 to enter Reverse Turbo mode much faster because the loops drive the circuit parameters to meet the three Turbo mode entry criteria much quicker when the adapter is more severely overloaded.

The ISL9241 exits Reverse Turbo mode when one of the following three criteria are met:

- The battery charging current exceeds 150mA ($R_{s2}$ = 10mΩ)
- The adapter current is less than the AdapterCurrentLimit register setting and the COMP voltage is lower than 1.4V
- The battery discharging current is less than 140mA (for $R_{s2}$ = 10mΩ) for 40ms

Table 18 shows the ISL9241 HPBB configuration charge function and Turbo Boost function control truth table.

**Table 18. HPBB Charger Behavior Truth Table**

| Reverse Turbo Boost Mode Control Bit | Enable Charging Control Bit (VSYSMIN ≠ Zero) | Charge Current Register | | |
|---|---|---|---|---|
| 0 = Enable Turbo<br>1 = Disable Turbo | 0 = Disable Charging<br>1 = Enable Charging | 0 = 0h Command<br>1 = Non-Zero Valid Command | Charge? | Boost? |
| 0 | 0 | 0 | No | Yes |
| 0 | 0 | 1 | No | Yes |
| 0 | 1 | 0 | Do not set (Note 11) | Yes |
| 0 | 1 | 1 | Yes<br>(Fast charge and trickle charge enabled) | Yes |
| 1 | 0 | 0 | No | No |
| 1 | 0 | 1 | No | No |
| 1 | 1 | 0 | Do not set (Note 11) | No |
| 1 | 1 | 1 | Yes<br>(Fast charge and trickle charge enabled) | No |

**Note:**

11. Set MinSystemVoltage and Charge current register both to zero or non zero. Setting only one register to zero is not recommended.

## 7.4 R3 Modulator

The ISL9241 uses the Renesas Robust Ripple Regulator (R3) modulation scheme. The R3 modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 43 conceptually shows the R3 modulator circuit and Figure 44 shows the operation principles in steady state.

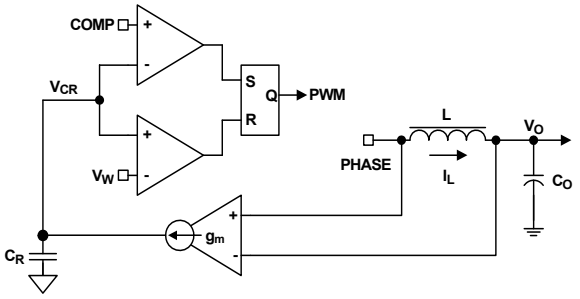



**Figure 43. R3 Modulator**

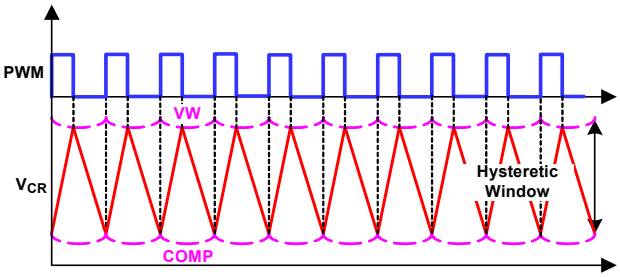



**Figure 44. R3 Modulator Operation Principles in Steady State**

A fixed voltage window (VW window) exists between VW and COMP. The modulator charges the ripple capacitor $C_R$ with a current source equal to $g_m(V_{IN} - V_O)$ during PWM on-time and discharges the ripple capacitor $C_R$ with a current source equal to $g_m V_O$ during PWM off-time where $g_m$ is a gain factor. The $C_R$ voltage $V_{CR}$ therefore emulates the inductor current waveform. The modulator turns off the PWM pulse when $V_{CR}$ reaches VW and turns on the PWM pulse when it reaches COMP.

Because the modulator works with $V_{CR}$, which is a large amplitude and noise free synthesized signal, it achieves lower phase jitter than conventional hysteretic mode modulators.

Figure 45 shows the operation principles during dynamic response. The COMP voltage rises during dynamic response, temporarily turning on PWM pulses earlier and more frequently, which allows for higher control loop bandwidth than conventional fixed frequency PWM modulators at the same steady state switching frequency.

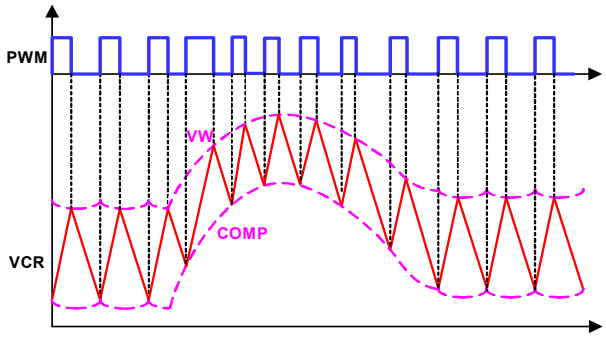



**Figure 45. R3 Modulator Operation Principles in Dynamic Response**

### 7.4.1 DE (Diode Emulation) Operation

In Diode Emulation (DE) mode, the ISL9241 uses a phase comparator to monitor the PHASE node voltage during the low-side switching FET on-time to detect the inductor current zero crossing. The phase comparator needs a minimum on-time of the low-side switching FET for it to recognize inductor current zero crossing. If the low-side switching FET on-time is too short for the phase comparator to successfully recognize the inductor zero crossing, the ISL9241 can lose diode emulation ability. To prevent this scenario, the ISL9241 uses a minimum low-side switching FET on-time. When the intended low-side switching FET on-time is shorter than the minimum value, the ISL9241 stretches the switching period to keep the low-side switching FET on-time at the minimum value, which causes the CCM switching frequency to drop below the set point.

The R3 modulator can operate in DE mode to increase light-load efficiency. In DE mode, the low-side MOSFET emulates a diode by conducting when the current is flowing from source-to-drain and not allowing

reverse current. As Figure 46 shows, when LGATE is on, the low-side MOSFET carries current and creates negative voltage on the phase node due to the voltage drop across the ON-resistance. The IC monitors the current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

If the load current is light enough, as Figure 46 shows, the inductor current reaches and stays at zero before the next phase node pulse, and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current never reaches 0A, and the regulator is in Continuous Conduction Mode (CCM) although the controller is in DE mode.

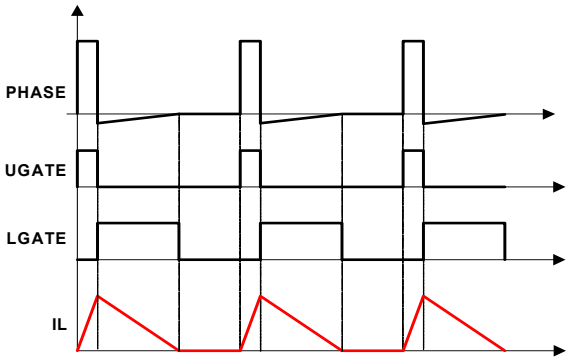



**Figure 46. Diode Emulation**

Figure 47 shows the operation principle of DE mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size and therefore is the same, making the inductor current triangle the same in the three cases. The R3 modulator clamps the ripple capacitor voltage $V_{CR}$ in DE mode to make it mimic the inductor current. The COMP voltage takes longer to reach $V_{CR}$, which naturally stretches the switching period. The inductor current triangles move farther apart from each other so that the inductor current average value is equal to the load current. The reduced switching frequency helps increase light-load efficiency.

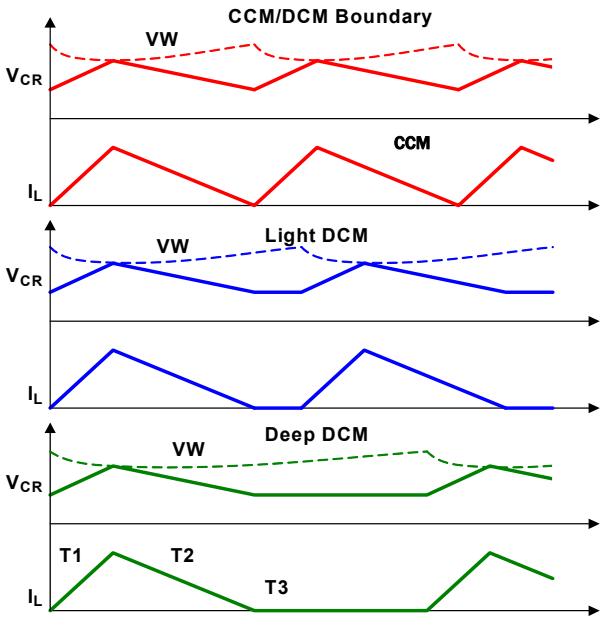



**Figure 47. Period Stretching**

# 8. Design Guide

This design guide provides a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition, complete reference designs are provided that include schematics, bills of materials, and example board layouts.

## 8.1 Selecting the Sense Resistors

Sense resistors are the easiest and most flexible method of monitoring/controlling current in the battery charge, discharge path, or the adapter input/output current. Most of the electrical specifications in this datasheet used $R_{s1}$ = 20mΩ and $R_{s2}$ = 10mΩ. However, any value can be selected because it is the voltage across the CSIN/CSIP and CSON/CSOP pins that are used for the control loops.

A sense resistor can introduce significant voltage drop and power loss to the load. In an application with high current requirements, the sense resistors require the use of low value sense resistor or a parallel combination of multiple sense resistors to support the higher power.

Appropriate scaling of the current values should be based on the voltage across the CSIN/CSIP and CSON/CSOP.

For example, if DAC is set for 2A at R = 20mΩ, $V_{sx}$ = 40mV; with R = 10mΩ, which is half the previous value, the DAC setting ends up being doubled to 4A to preserve $V_{sx}$ = 40mV.

### 8.1.1 Adapter Sense Resistor

The adapter sense resistor ($R_{s1}$) controls the current being pulled from an adapter when in forward mode, and senses the maximum current for ACProchot#. In Reverse mode, the sense resistor regulates the output current for OTG mode.

### 8.1.2 Battery Sense Resistor

The battery sense resistor ($R_{s2}$) controls the battery charging current when in Forward mode. In Reverse mode, the sense resistor senses the battery discharging current for DCProchot#.

## 8.2 Selecting the LC Output Filter

The duty cycle of an ideal buck converter in CCM is a function of the input and the output voltage. The relationship is written by Equation 4:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 4)}$$

The output inductor peak-to-peak ripple current is written by Equation 5:

$$I_{P\text{-}P} = \frac{V_{OUT} \cdot (1 - D)}{f_{SW} \cdot L} \quad \text{(EQ. 5)}$$

A typical step-down DC/DC converter has an $I_{P\text{-}P}$ of 20% to 40% of the maximum DC output load current for a practical design. The value of $I_{P\text{-}P}$ is selected based on several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding.

The DC copper loss of the inductor can be estimated by Equation 6:

$$P_{COPPER} = I_{LOAD}^{2} \cdot DCR \quad \text{(EQ. 6)}$$

where $I_{LOAD}$ is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor can destroy circuit components.

A DC/DC buck regulator must have output capacitance $C_O$ into which ripple current $I_{P-P}$ can flow. Current $I_{P-P}$ develops a corresponding ripple voltage $V_{P-P}$ across $C_O$, which is the sum of the voltage drop across the capacitor ESR and of the voltage change stemming from charge moved in and out of the capacitor. These two voltages are written as Equations 7 and 8:

(EQ. 7) $$\Delta V_{ESR} = I_{P-P} \cdot ESR$$

(EQ. 8) $$\Delta V_C = \frac{I_{P-P}}{8 \cdot C_O \cdot f_{SW}}$$

If the output of the converter has to support a load with high pulsating current, several capacitors need to be paralleled to reduce the total ESR until the required $V_{P-P}$ is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that $I_{P-P}$ is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at $f_{SW}$. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

## 8.3 Adapter Input Filter

The adapter cable parasitic inductance and capacitance can cause some voltage ringing or an overshoot spike at the adapter connector node when the adapter is hot plugged in. This voltage spike can damage the BYPSG MOSFET or the ISL9241 pins connecting to the adapter connector node. One low cost solution is to add an RC snubber circuit at the adapter connector node to clamp the voltage spike as shown in Figure 48. A practical value of the RC snubber is 2.2Ω to 2.2µF while the appropriate values and power rating should be carefully characterized based on the actual design. However, do not add a pure capacitor at the adapter connector node, which can cause an even bigger voltage spike due to the adapter cable or the adapter current path parasitic inductance.

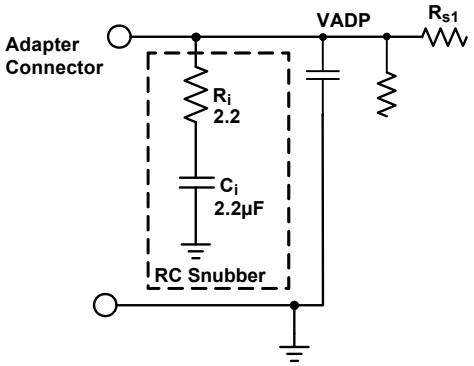



**Figure 48. Adapter Input RC Snubber Circuit**

## 8.4 Selecting the Input Capacitor

The important parameters for the input capacitance are the voltage rating and the RMS current rating. For reliable operation, select capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. Figure 49 is a graph of the input capacitor RMS ripple current normalized relative to output load current as a function of duty cycle and is adjusted for converter efficiency. The normalized RMS ripple current calculation is written as Equation 9.

(EQ. 9)
$$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1 - D) + \frac{D \cdot k^2}{12}}}{I_{MAX}}$$

where:

- $I_{MAX}$ is the maximum continuous $I_{LOAD}$ of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to peak ripple amplitude expressed as a ratio of $I_{MAX}$ (0 to 1)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter, which is written as Equation 10:

(EQ. 10)
$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF}$$

In addition to the capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

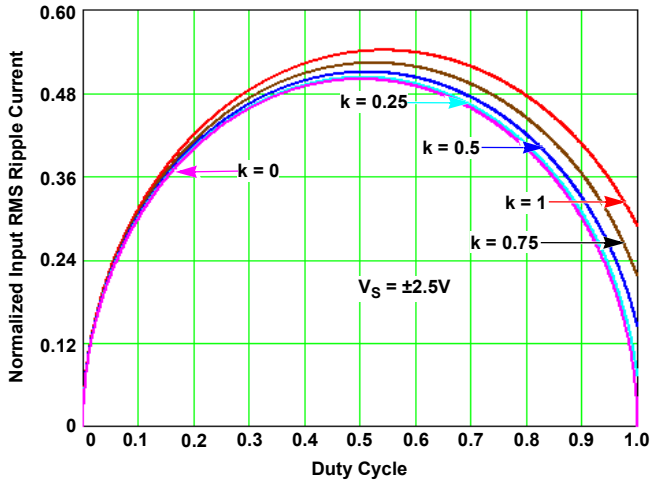



**Figure 49. Normalized RMS Input Current at EFF = 1**

## 8.5 Selecting the Switching Power MOSFET

### 8.5.1 Switching Power MOSFET Gate Capacitance

The ISL9241 includes an internal 5V LDO output at VDD pin, which can provide the switching MOSFET gate driver power through the VDDP pin with an RC filter. The 5V LDO output overcurrent protection threshold is 115mA, nominal. When selecting the switching power MOSFET, carefully consider the MOSFET gate capacitance to avoid overloading the 5V LDO, especially in Buck-Boost mode when four MOSFETs are switching at the same time. For one MOSFET, the gate drive current can be estimated by Equation 11:

(EQ. 11) $$I_{driver} = Q_g \bullet f_{SW}$$

where:

- $Q_g$ is the total gate charge in the MOSFET datasheet
- $f_{SW}$ is switching frequency

### 8.5.2 Switching Power MOSFET Power

Typically, a MOSFET cannot tolerate even brief excursions beyond its maximum drain-to-source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum VDS rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

Several power MOSFETs are readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region and does not exceed the VDDP current rating. Unlike the low-side MOSFET, which has the drain-to-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with a VDS of approximately $V_{IN}$ - $V_{OUT}$ plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. **Note:** This is an optimal configuration of MOSFET selection for low duty cycle applications (D < 50%). For higher output and low input voltage solutions, a more balanced MOSFET selection for high-side and low-side devices may be needed.

For the Low-Side (LS) MOSFET, the power loss can be assumed to be conductive only and is written as Equation 12:

(EQ. 12) $$P_{CON_LS} \approx I_{LOAD}^{2} \cdot r_{DS(ON)_LS} \bullet (1 - D)$$

For the High-Side (HS) MOSFET, the conduction loss is written by Equation 13:

(EQ. 13) $$P_{CON_HS} = I_{LOAD}^{2} \bullet r_{DS(ON)_HS} \bullet D$$

For the High-Side MOSFET, the switching loss is written as Equation 14:

(EQ. 14) $$P_{SW_HS} = \frac{V_{IN} \bullet I_{VALLEY} \bullet t_{SWON} \bullet f_{SW}}{2} + \frac{V_{IN} \bullet I_{PEAK} \bullet t_{SWOFF} \bullet f_{SW}}{2}$$

where:

- $I_{VALLEY}$ is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- $I_{PEAK}$ is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- $t_{SW(ON)}$ is the time required to drive the device into saturation
- $t_{SW(OFF)}$ is the time required to drive the device into cut-off
- Renesas recommends using a 4.7µF (10V) VDD/VDDP capacitor, which has an effective capacitance higher than 0.4µF at 5V and x1.6 effective capacitance at the BOOT pin at 5V.

## 8.6 Selecting the Bootstrap Capacitor

The selection of the bootstrap capacitor is written by Equation 15:

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad \text{(EQ. 15)}$$

where:

- $Q_g$ is the total gate charge required to turn on the high-side MOSFET
- $\Delta V_{BOOT}$ is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on.

As an example, suppose the high-side MOSFET has a total gate charge $Q_g$, of 25nC at $V_{GS}$ = 5V, and a $\Delta V_{BOOT}$ of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double or more the calculated capacitance. Use an X7R or X5R ceramic capacitor.

Renesas recommends using a bootstrap capacitor of 0.47µF (25V), which has an effective capacitance higher than 0.25µF at 5V and x50 effective high side MOSFET gate capacitance.

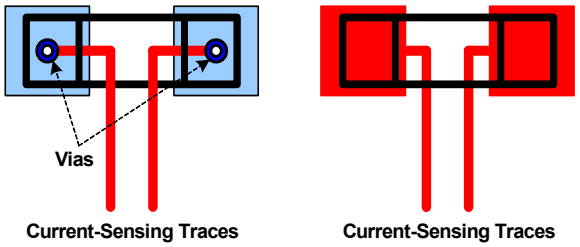
One additional consideration is the gate charge power loss written by Equation 16 and the VDDP current consumption. Keep the Pg below the VDDP overcurrent threshold.

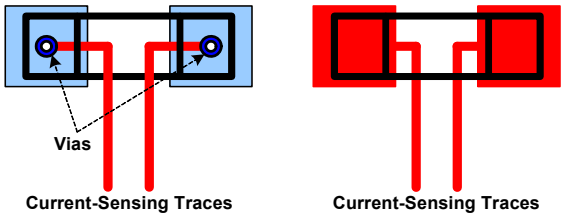
$$Pg = (Q_g(LS)) + (Q_g(HS)) \bullet V_{GS} \bullet SFW \quad \text{(EQ. 16)}$$

## 8.7 DCIN Filter

An RC filter is connected at the DCIN pin. Renesas recommends connecting a 10Ω DCIN resistor between the DCIN pin and the VADP/VSYS diodes, and connecting a 4.7µF DCIN capacitor to GND, which has an effective capacitance higher than 0.4µF at 20V.

# 9. Layout

| Pin # | Pin Name | Layout Guidelines |
|---|---|---|
| Bottom Pad | GND | Connect this ground pad to the ground plane through a low impedance path. Renesas recommends using at least five vias to connect to ground planes in the PCB to ensure sufficient thermal dissipation directly under the IC. |
| 1 | CSON | Run two dedicated traces with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the battery current-sensing resistor to the IC. Place the differential mode and common-mode R-C filter components in the general proximity of the controller.<br>Route the current-sensing traces through vias to connect the center of the pads or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces.<br>  <br> |
| 2 | CSOP | |
| 3 | NGATE | Switching pin. Run the NGATE trace to the NGATE N-type MOSFET Gate node. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. |
| 4 | BOOT2 | Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide trace. Avoid any sensitive analog signal trace from crossing over or getting close. |
| 5 | UGATE2 | Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Renesas recommends routing the PHASE2 trace to the high-side MOSFET source pin instead of general copper.<br>Place the IC close to the switching MOSFETs gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs.<br>Place the output capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use shortest PCB trace connection. Place these capacitors on the same PCB layer as the MOSFETs instead of on different layers and using vias to make the connection.<br>Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB. |
| 6 | PHASE2 | |
| 7 | LGATE2 | Switching pin. Run the LGATE2 trace in parallel with the UGATE2 and PHASE2 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. |
| 8 | VDDP | Place the decoupling capacitor in the general proximity of the controller. Run the trace connecting to the VDD pin with sufficient width. |
| 9 | LGATE1 | Switching pin. Run the LGATE1 trace in parallel with the UGATE1 and PHASE1 traces on the same PCB layer. Use sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. |
| 10 | PHASE1 | Run these two traces in parallel fashion with sufficient width. Avoid any sensitive analog signal trace from crossing over or getting close. Renesas recommends routing the PHASE1 trace to the high-side MOSFET source pin instead of general copper.<br>Place the IC close to the switching MOSFETs gate terminals and keep the gate drive signal traces short for a clean MOSFET drive. The IC can be placed on the opposite side of the switching MOSFETs.<br>Place the input capacitors as close as possible to the switching high-side MOSFET drain and the low-side MOSFET source; and use shortest PCB trace connection. Place these capacitors on the same PCB layer as the MOSFETs instead of on different layers and using vias to make the connection.<br>Place the inductor terminal to the switching high-side MOSFET drain and low-side MOSFET source terminal as close as possible. Minimize this phase node area to lower the electrical and magnetic field radiation but make this phase node area large enough to carry the current. Place the inductor and the switching MOSFETs on the same layer of the PCB. |
| 11 | UGATE1 | |

| Pin # | Pin Name | Layout Guidelines |
|---|---|---|
| 12 | BOOT1 | Switching pin. Place the bootstrap capacitor in the general proximity of the controller. Use sufficiently wide trace. Avoid any sensitive analog signal trace from crossing over or getting close. |
| 13 | BYPSRC | Run this trace with sufficient width to the bypass N-type MOSFET sources/reference node. |
| 14 | CSIN | Run two dedicated trace with sufficient width in parallel (close to each other to minimize the loop area) from the two terminals of the adapter current-sensing resistor to the IC. Place the Differential mode and common-mode R-C filter components in general proximity of the controller. Keep the CSIN node near the $Q_1$ drain.<br>Route the current-sensing traces through vias to connect the center of the pads; or route the traces into the pads from the inside of the current-sensing resistor. The following drawings show the two preferred ways of routing current-sensing traces.<br>  <br> |
| 15 | CSIP | |
| 16 | BYPSG | Run this trace with sufficient width to the bypass N-type MOSFET gates. |
| 17 | DCIN | Place the OR diodes and the R-C filter in the general proximity of the controller. Run the VADP trace and VSYS trace to the OR diodes with sufficient width. |
| 18 | VDD | Place the R-C filter connecting with VDDP pin in the general proximity of the controller. Run the trace connecting to the VDDP pin with sufficient width. |
| 19 | PROG | Signal pin. Place the PROG programming resistor in the general proximity of the controller. |
| 20 | OTGEN/CMIN | Digital pins. No special consideration. |
| 21 | SDA | Digital pins. No special consideration. Run the SDA and SCL traces in parallel. |
| 22 | SCL | |
| 23 | PROCHOT# | Digital pin, open-drain output. No special consideration. |
| 24 | ACOK | |
| 25 | BATGONE/NTC | Digital pin (BATGONE), analog pin (NTC). Place the 10kΩ resistor series in the BATGONE signal trace and the optional decoupling capacitor in the general proximity of the controller. |
| 26 | CMOUT/INT# | Digital pin, open-drain output. No special consideration. |
| 27 | COMPR | Place the compensation components in the general proximity of the controller. Avoid any switching signal from crossing over or getting close. |
| 28 | COMPF | |
| 29 | AMON/BMON | No special consideration. Place the optional R-C filter in the general proximity of the controller. |
| 30 | PSYS(REFADJ) | Signal pin, current source output. No special consideration. REFADJ is an analog signal pin for feedback of the output voltage. Place near the controller and run a dedicated trace for each resistor divider node (TOP, MIDDLE, BOTTOM). Do not inject noise or additional capacitance. |
| 31 | VBAT | Place the optional R-C filter in the general proximity of the controller. Run a dedicated trace from the battery positive connection point to the IC. |
| 32 | BGATE | Use a sufficiently wide trace from the IC to the BGATE N-type MOSFET gate. Place the capacitor from BGATE to ground close to the MOSFET. |

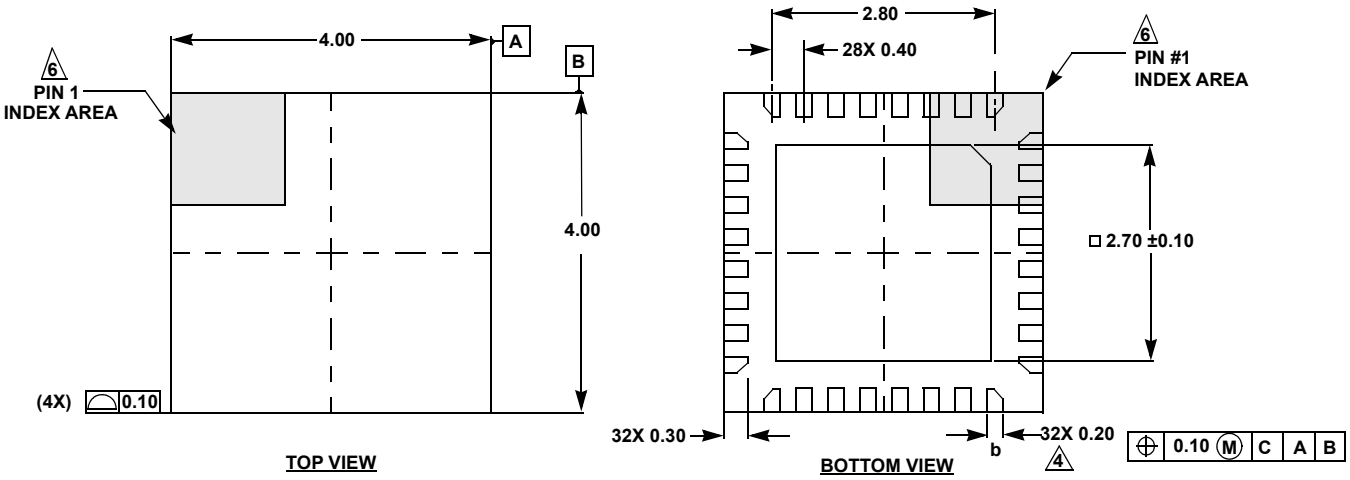
# 10. Revision History

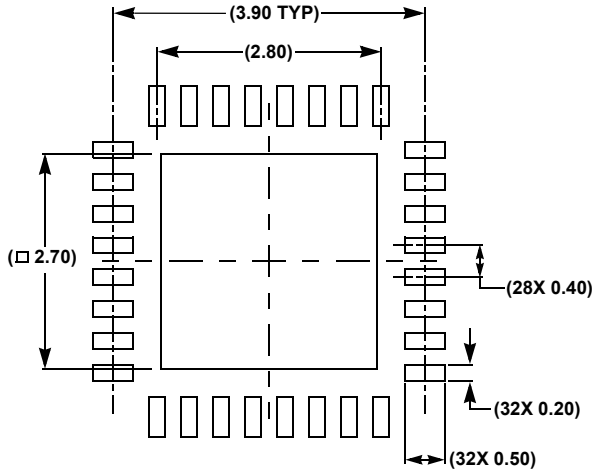
| Rev. | Date | Description |
|---|---|---|
| 4.02 | Jul 23, 2020 | Added section on discharge current loop in reverse modes.<br>Changed PROCHOT# latch and clear control bit in the application section.<br>Changed description of internal reference in the control bits section and application section.<br>Updated filter guidance for AMON.<br>Added guidance on setting ACOKREF for Bypass mode.<br>Updated Auto Recharge Threshold number in the Application section of Autonomous charging. |
| 4.01 | Nov 1, 2019 | Added information about the Low_Vsys_PROCHOT# for supplemental mode in the Supplemental Power Support Mode section on page 49. |
| 4.00 | Sep 27, 2019 | Block Diagram updated.<br>Added decoupling capacitor specification to BOOT2, VDDP, BOOT1, DCIN and VDD pins in the Pin description table.<br>Added decoupling capacitor recommendation to the “Selecting the Switching Power MOSFET” and “Selecting the Bootstrap capacitor” sections.<br>Added a section called “DCIN Filter” to provide recommendation on the R-C filter on DCIN pin.<br>Changed LowVsysPROCHOT# debounce time in the Control2 register and PROCHOT# sections.<br>Changed the logic output in the table “Control Logic Truth Table for OTG and Supplemental Mode”.<br>Changed Control2 bit 1 and 0 description.<br>Change TSUP and TSUP_M descriptions in Control7 register.<br>Updated the ACOK reference value in the DAC summary table.<br>Added note to SMBus timing specification.<br>Added Information register read out column in the PROG table.<br>Added note that adapter voltage should be 1-2V higher than batter voltage after I*R drop and tolerance considerations in the Bypass mode section.<br>Table 3 “Control0 Register 0x39H” - Reverse Turbo boost bit function edited.<br>Changed the Ideal Diode Mode exit timer and Reverse Turbo Boost exit timer from 140ms to 40ms.<br>Clarified Psys offset in the EC table.<br>Updated LSB for NTC ADC register.<br>Added note that ADC is enabled when ACOK Ref register is programmed to non zero value. |
| 3.00 | Mar 11, 2019 | Added ISL9241IRTZ-TK to Ordering Information table on page 7.<br>Modified BATGONE/NTC pin description on page 9.<br>On page 13, updated the MaxSystemVoltage for 3-cell and 4-cell Min value from 0.5% to -0.5%.<br>Updated disclaimer. |
| 2.00 | Dec 10, 2018 | Changed a sentence on page 1, 2nd paragraph<br>Updated the Typical Application diagram on page 1<br>Updated Figure 26 - General SMBus architecture<br>Updated NTC/GPADC LSB and GPADC register bits in Table 12<br>Removed cross reference in Control7 <1:0> |
| 1.00 | Oct 31, 2018 | Updated test condition for $I_{BAT2}$ on page 13.<br>Updated PSYS Monitor section by updating paragraph 3 and adding Equation 2. |
| 0.00 | Oct 22, 2018 | Initial release |

# 11. Package Outline Drawing

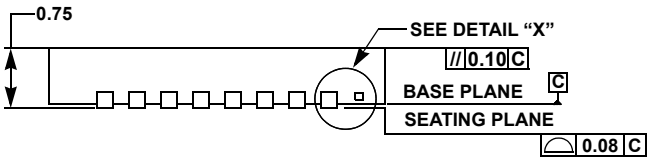
For the most recent package outline drawing, see L32.4x4D.

L32.4x4D 32 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/16

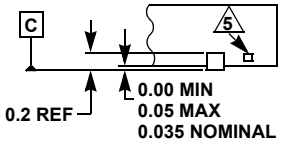



TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

**NOTES:**

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05.
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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### Contact Information

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**Офис по работе с юридическими лицами:**

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9