

BUK9605-30A

N-channel TrenchMOS logic level FET Rev. 03 — 19 April 2011

Product data sheet

Product profile 1.

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

■ AEC Q101 compliant

Low conduction losses due to low on-state resistance

1.3 Applications

Automotive and general purpose power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	30	V
I _D	drain current	T _{mb} = 25 °C	-	-	75	Α
P _{tot}	total power dissipation		-	-	230	W
Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}$	-	4.3	5	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}$	-	3.9	4.6	mΩ
Avalanci	Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \le$ 25 V; R_{GS} = 50 Ω ; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	500	mJ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain[1]	mb	D
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

^[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9605-30A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	30	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-10	10	V
I _D	drain current	T _{mb} = 100 °C	-	75	Α
		T _{mb} = 25 °C	-	75	Α
I _{DM}	peak drain current	T _{mb} = 25 °C; pulsed	-	400	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C	-	230	W
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
V_{GSM}	peak gate-source voltage	pulsed; t _p ≤ 50 μs	-15	15	V
Source-drai	in diode				
Is	source current	T _{mb} = 25 °C	-	75	Α
I _{SM}	peak source current	pulsed; T _{mb} = 25 °C	-	240	Α
Avalanche r	ruggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \le 25$ V; R_{GS} = 50 Ω ; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	500	mJ

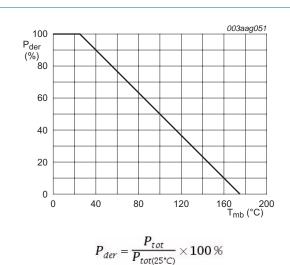


Fig 1. Normalized total power dissipation as a function of mounting base temperature

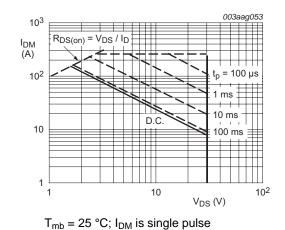
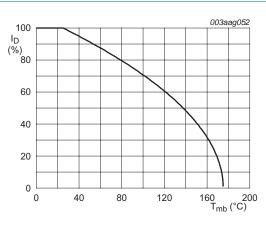


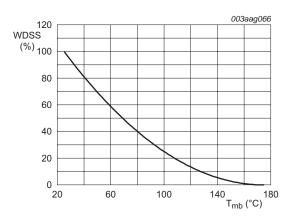
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

V_{GS} ≥ 5 V

Fig 2. Normalized continuous drain current as a function of mounting base temperature



 $I_D = 75 A$

Fig 4. Normalised drain-source non-repetitive avalanche energy as a function of mounting-base temperature

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.65	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint ; FR4 board	-	50	-	K/W

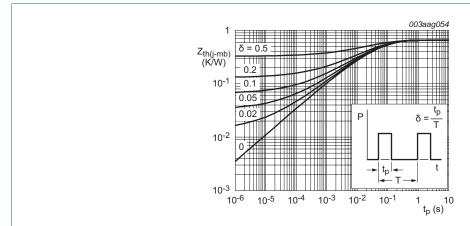


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
$V_{(BR)DSS}$	drain-source breakdown	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	30	-	-	V
	voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	27	-	-	V
V _{GS(th)}	gate-source threshold	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	1	1.5	2	V
	voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C}$	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}$	-	-	2.3	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	0.05	10	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	30	100	nΑ	
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
R _{DSon}	drain-source on-state	$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$	-	4.3	5	mΩ
	resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	3.9	4.6	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C}$		-	5.4	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^{\circ}\text{C}$	-	-	9.3	mΩ
Dynamic	characteristics					
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	6500	8600	pF
C_{oss}	output capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = \text{nk }^{\circ}\text{C}$	-	1500	1800	pF
C _{rss}	reverse transfer capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}$	-	1000	1350	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	45	65	ns
t _r	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 °C$	-	220	330	ns
t _{d(off)}	turn-off delay time		-	435	600	ns
t _f	fall time		-	320	450	ns
L _D	internal drain inductance	measured from upper edge of drain tab to centre of die; $T_j = 25$ °C	-	2.5	-	nΗ
L _S	internal source inductance	from source lead soldering point to source bond pad; $T_j = 25$ °C	-	7.5	-	nΗ
Source-d	rain diode					
V _{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.85	1.2	V
		I _S = 75 A; V _{GS} = 0 V; T _j = 25 °C	-	1.1	-	V
t _{rr}	reverse recovery time	$I_S = 75 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	400	-	ns
Q _r	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	1	-	μC

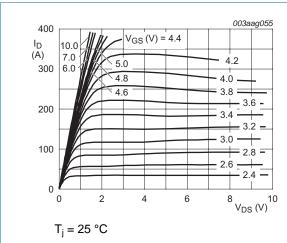


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

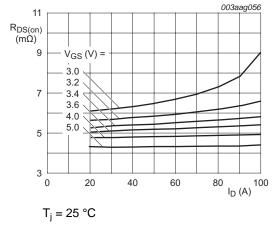


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

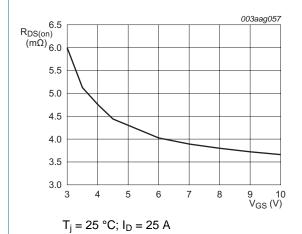


Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

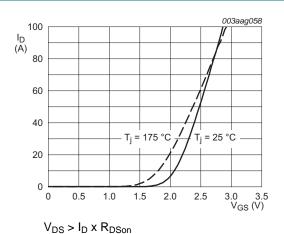


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

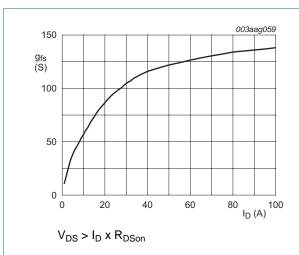
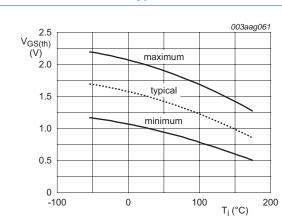
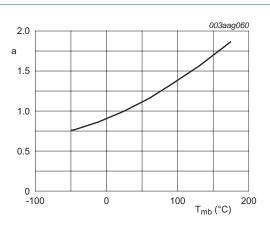


Fig 10. Forward transconductance as a function of drain current; typical values



 $I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

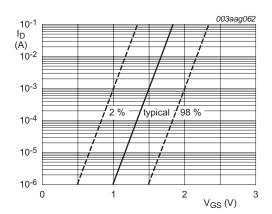
Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

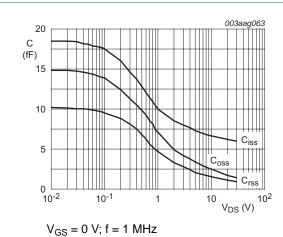
 $I_D = 25 A; V_{GS} = 5 V$

Fig 11. Normalized drain-source on-state resistance factor as a function of junction temperature



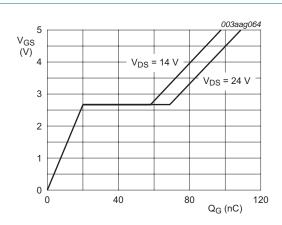
 $T_j = 25 \, ^{\circ}C; \, V_{DS} = V_{GS}$

Fig 13. Sub-threshold drain current as a function of gate-source voltage



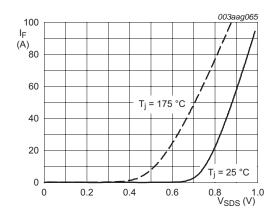
VGS = 0 V, I = 1 WII IZ

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $T_j = 25 \, ^{\circ}C; I_D = 50 \, A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



 $V_{GS} = 0 V$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

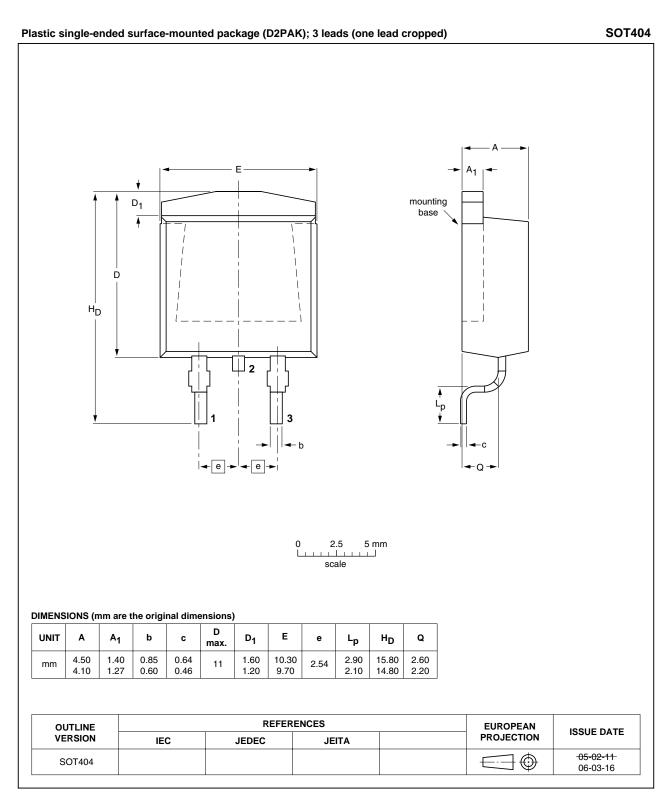


Fig 17. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9605-30A v.3	20110419	Product data sheet	-	BUK9605-30A v.2
Modifications:		nat of this data sheet has been redesigned to comply with the new identity guidel Semiconductors.		the new identity guidelines
	 Legal texts have 	ve been adapted to the new	company name where	appropriate.
BUK9605-30A v.2	19990801	Product specification	-	BUK9605-30A v.1

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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N-channel TrenchMOS logic level FET

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Офис по работе с юридическими лицами:

105318, г. Москва, ул. Щербаковская д. 3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru moschip.ru_6 moschip.ru_4 moschip.ru_9