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May 2016

FCH041N65EFL4

N-Channel SuperFET[®] II FRFET[®] MOSFET 650 V, 76 A, 41 m Ω

Features

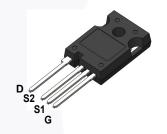
- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)} = 36 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_q = 229 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 631 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

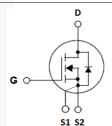
Applications

- LCD / LED / PDP TV Telecom / Server Power Supplies
- · Solar Inverter
- AC DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET® MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.





S1: Kelvin Source S2: Power Source

Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCH041N65EFL4	Unit
V_{DSS}	Drain to Source Voltage			650	V
V	Cata to Course Voltage	- DC		±20	V
V_{GSS}	Gate to Source Voltage	- AC	(f > 1 Hz)	±30	7 V
	Drain Current	- Continuous (T _C = 25°C)		76	^
ID	Drain Current	- Continuous (T _C = 100°C)	- Continuous (T _C = 100°C)		A
I _{DM}	Drain Current	- Pulsed	(Note 1)	228	Α
E _{AS}	Single Pulsed Avalanche Energ	ЭУ	(Note 2)	2025	mJ
I _{AR}	Avalanche Current		(Note 1)	15	Α
E _{AR}	Repetitive Avalanche Energy		(Note 1)	5.95	mJ
dv/dt	MOSFET dv/dt		100	V/ns	
αν/αι	Peak Diode Recovery dv/dt		(Note 3)	50	V/IIS
D	Payer Dissipation	(T _C = 25°C)	-	595	W
P_D	Power Dissipation	- Derate Above 25°C		4.76	W/°C
T _J , T _{STG}	Operating and Storage Temper	ature Range		-55 to +150	°C
T _L	Maximum Lead Temperature for 1/8" from Case for 5 Seconds	or Soldering,		300	°C

Thermal Characteristics

Symbol	Parameter	FCH041N65EFL4	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.21	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH041N65EFL4	FCH041N65EF	TO-247 4L	Tube	N/A	N/A	30 units

Test Conditions

Min.

Тур.

Max.

Unit

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted. Parameter

Off Chara	acteristics					
D) /	Drain to Course Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	650	-	-	W
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	700	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.72	-	V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	-	-	10	
DSS	Zero Gate Voltage Drain Current	$V_{DS} = 520 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	145	-	μΑ
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

Symbol

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 7.6$ mA	3	-	5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 38 A	-	36	41	mΩ
9 _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 38 A	-	71.7	1	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V = 400 V V = 0 V	-	9446	12560	pF
C _{oss}	Output Capacitance	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1 MHz	-	366	490	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1011 12	-	35	-	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	-	197	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	-	631	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 38 A,	-	229	298	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	50	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	90	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.6	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time		-	55	120	ns
t _r	Turn-On Rise Time	$V_{DD} = 380 \text{ V}, I_{D} = 38 \text{ A},$	- /	25	60	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_g = 4.7 \Omega$	-	169	348	ns
t _f	Turn-Off Fall Time	(Note 4)	_/	18	46	ns

Drain-Source Diode Characteristics

Is	Maximum Continuous Drain to Source Diode	Maximum Continuous Drain to Source Diode Forward Current			76	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current			-	228	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 38 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 38 A,	-	207	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	1.5	-	μС

- 1. Repetitive rating: pulse width limited by maximum junction temperature.
- 2. I_{AS} = 15 A, R_{G} = 25 Ω , starting T_{J} = 25°C.
- 3. I $_{SD} \leq$ 38 A, di/dt \leq 200 A/µs, V $_{DD} \leq$ 380 V, starting T $_{J}$ = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

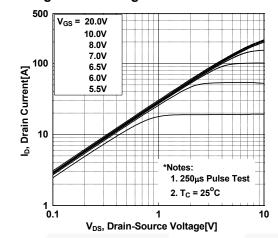


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

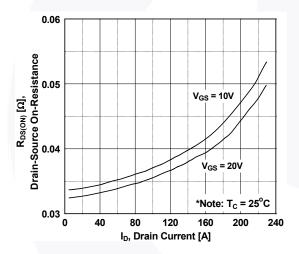


Figure 5. Capacitance Characteristics

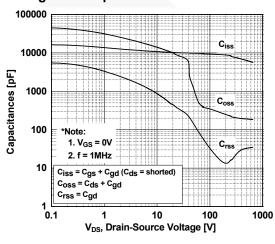


Figure 2. Transfer Characteristics

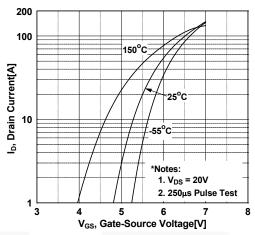


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

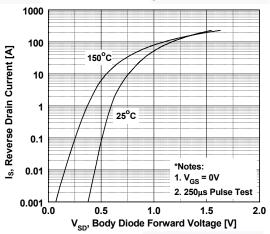
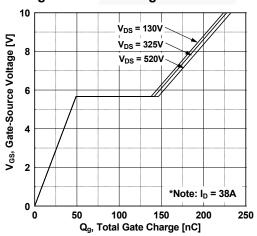


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

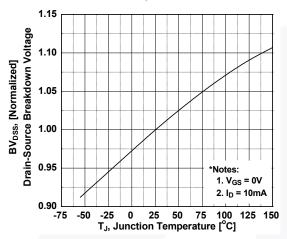


Figure 9. Maximum Safe Operating Area

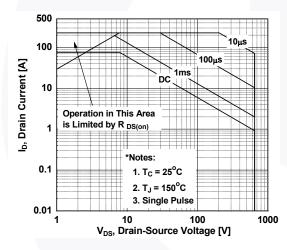


Figure 11. Eoss vs. Drain to Source Voltage

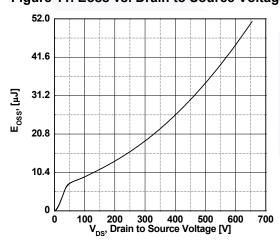


Figure 8. On-Resistance Variation vs. Temperature

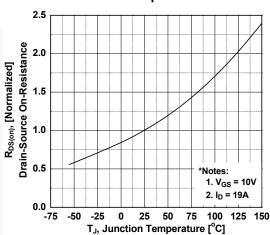
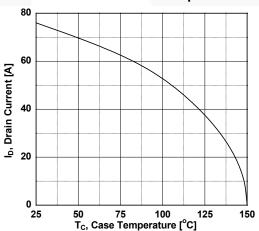
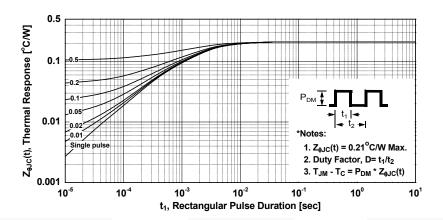


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



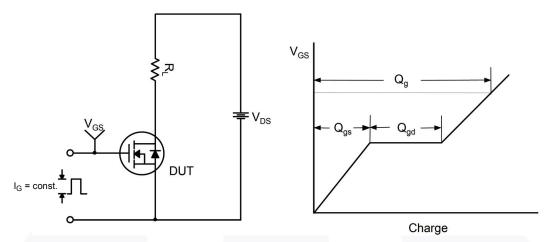


Figure 15. Gate Charge Test Circuit & Waveform

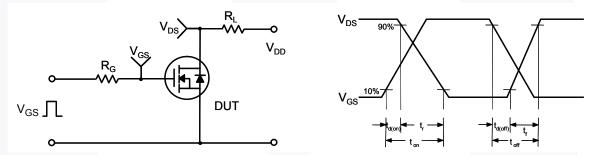


Figure 16. Resistive Switching Test Circuit & Waveforms

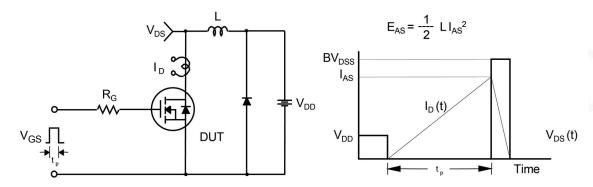


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

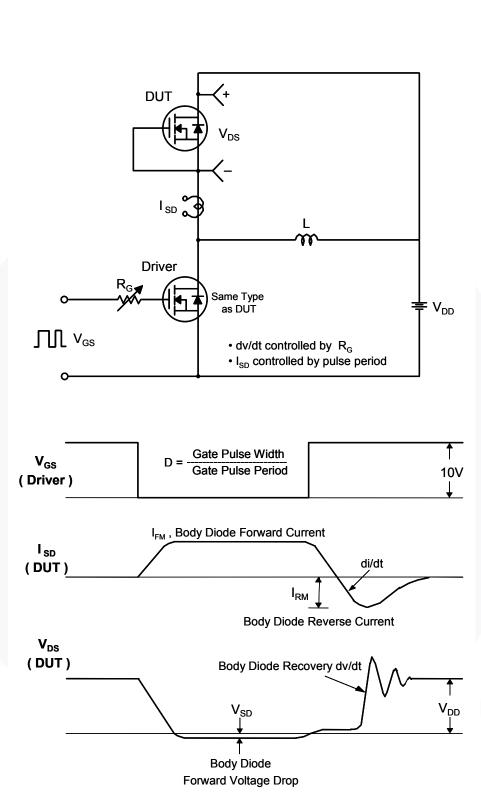
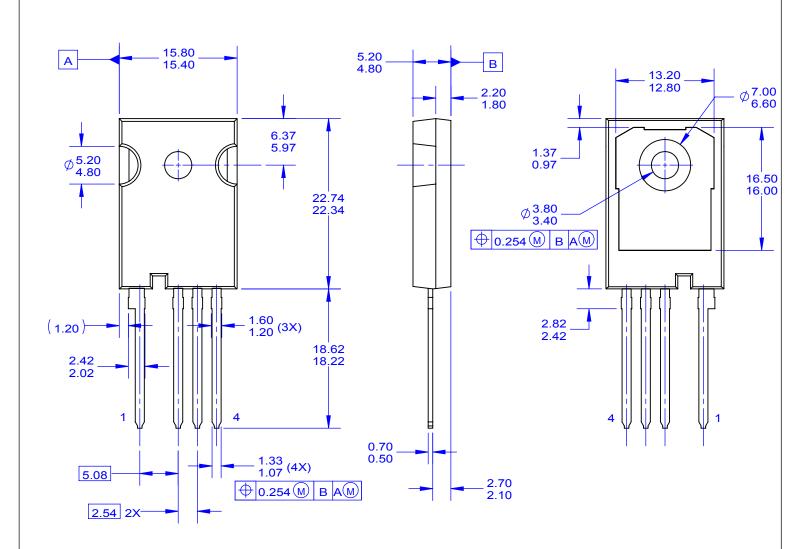


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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