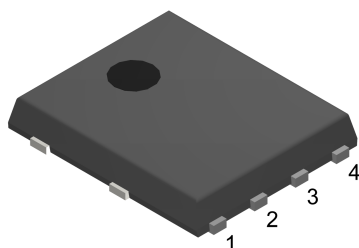
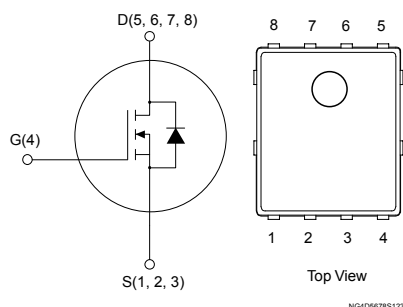


N-channel 30 V, 1.1 mΩ typ., 260 A, STripFET™ H6 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT™ 5x6



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	Package
STL260N3LLH6	30 V	1.3 mΩ	260 A	PowerFLAT™ 5x6

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.



Product status link

[STL260N3LLH6](#)

Product summary

Order code	STL260N3LLH6
Marking	260N3LH6
Package	PowerFLAT™ 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	260	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	190	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	1040	A
$I_D^{(3)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	45	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	32	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	180	A
$P_{TOT}^{(1)}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	166	W
$P_{TOT}^{(3)}$	Total power dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
$E_{AS}^{(4)}$	Single pulse avalanche energy	900	mJ
T_{stg} T_J	Storage temperature range Operating junction temperature range	-55 to 175	$^\circ\text{C}$

1. The value is rated according to R_{thj-c} .
2. Pulse width limited by safe operating area.
3. The value is rated according to $R_{thj-pcb}$.
4. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 35\text{ A}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.9	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

1. When mounted on an 1-inch² FR-4, 2 Oz copper board, $t < 10\text{ s}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 30\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 30\text{ V}$, $T_{\text{C}} = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			10	μA
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 20\text{ V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	1			V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 22.5\text{ A}$		1.1	1.3	m Ω
		$V_{\text{GS}} = 4.5\text{ V}$, $I_{\text{D}} = 22.5\text{ A}$		1.6	2.0	

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	6375	-	pF
C_{oss}	Output capacitance		-	1230	-	
C_{rss}	Reverse transfer capacitance		-	675	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 15\text{ V}$, $I_{\text{D}} = 45\text{ A}$, $V_{\text{GS}} = 0\text{ to }4.5\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	61.5	-	nC
Q_{gs}	Gate-source charge		-	20	-	
Q_{gd}	Gate-drain charge		-	24	-	
R_{g}	Gate input resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	1.4	-	Ω

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 15\text{ V}$, $I_{\text{D}} = 22.5\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$	-	22.5	-	ns
t_{r}	Rise time		-	32	-	
$t_{\text{d(off)}}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	107.5	-	
t_{f}	Fall time		-	54	-	

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		45	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		180	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 45\text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 45\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	37.2		ns
Q_{rr}	Reverse recovery charge		-	36		nC
I_{RRM}	Reverse recovery current		-	1.9		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

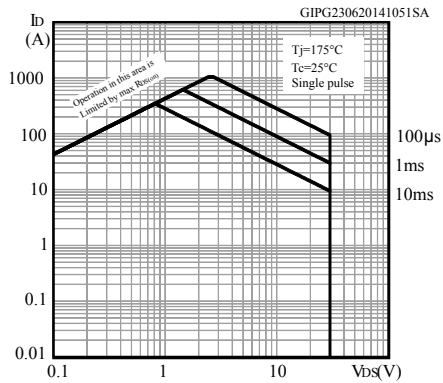
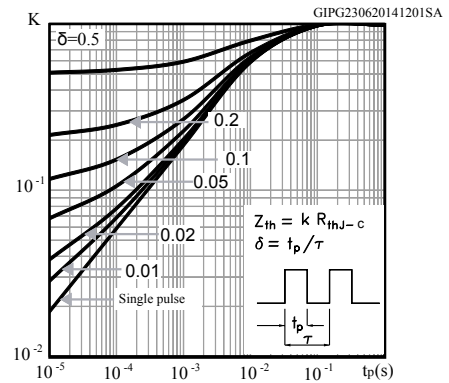
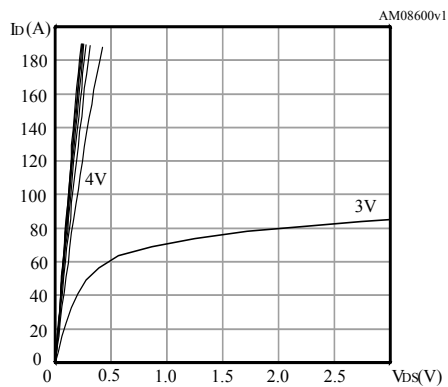
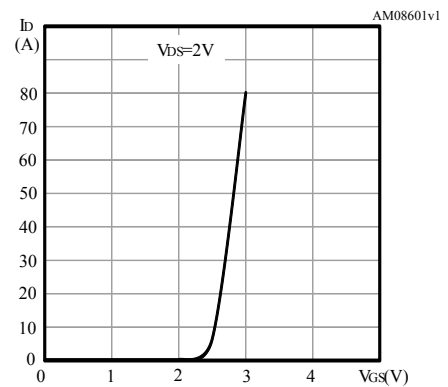
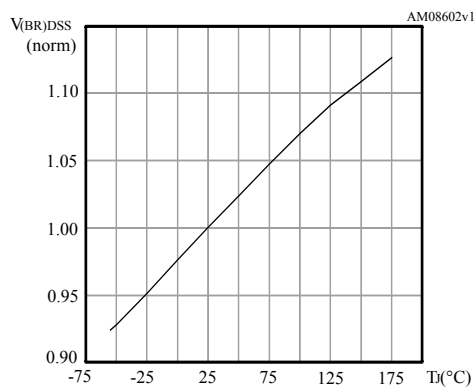
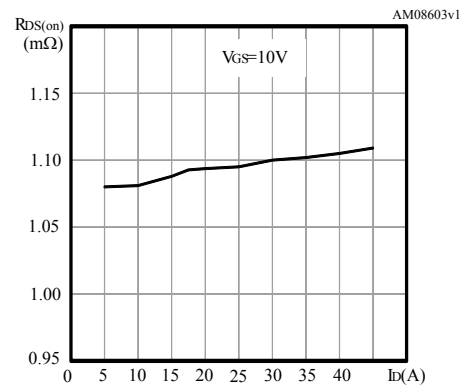
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

Figure 6. Static drain-source on-resistance


Figure 7. Gate charge vs gate-source voltage

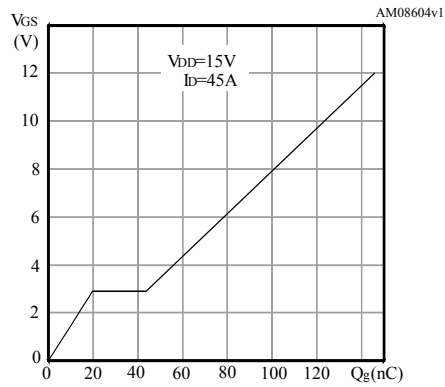


Figure 8. Capacitance variations

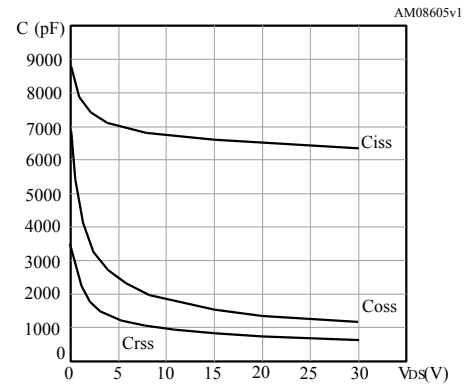


Figure 9. Normalized gate threshold voltage vs temperature

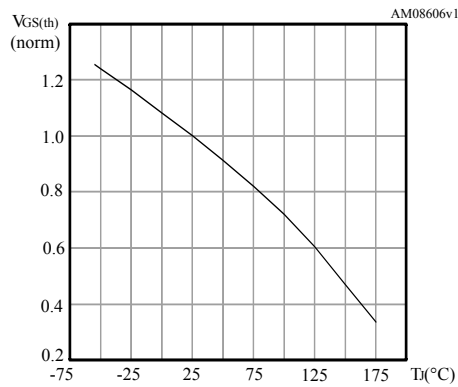


Figure 10. Normalized on-resistance vs temperature

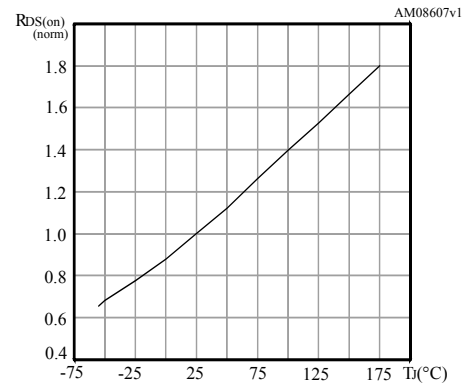
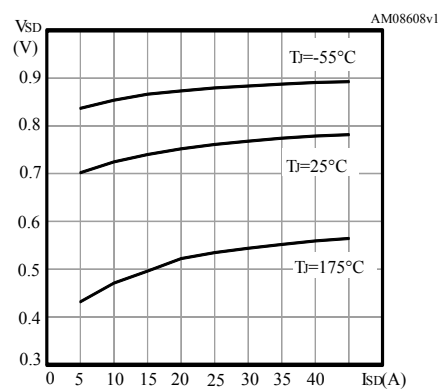
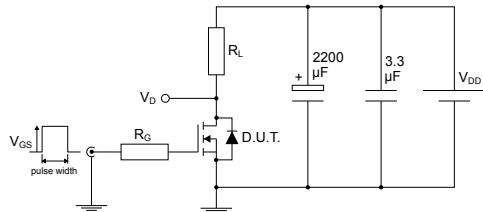


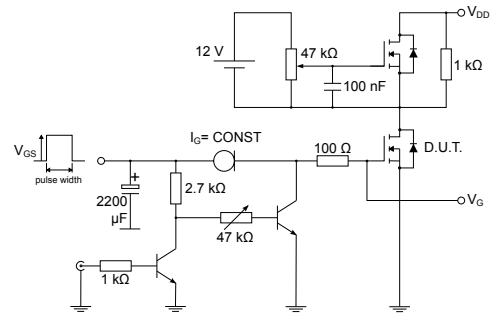
Figure 11. Source-drain diode forward characteristics



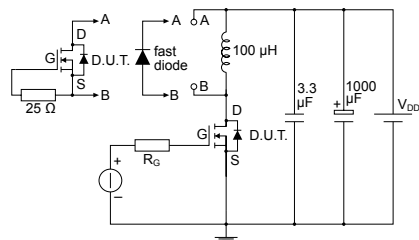
3 Test circuits

Figure 12. Test circuit for resistive load switching times


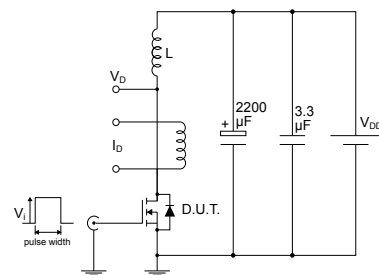
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Figure 13. Test circuit for gate charge behavior


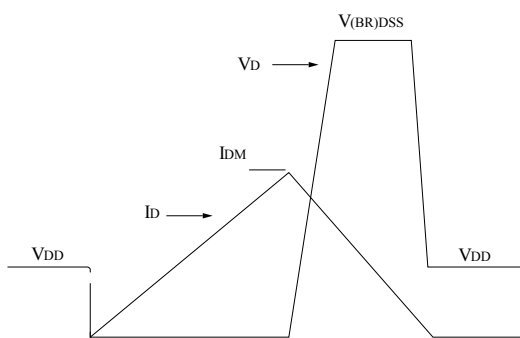
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Figure 14. Test circuit for inductive load switching and diode recovery times


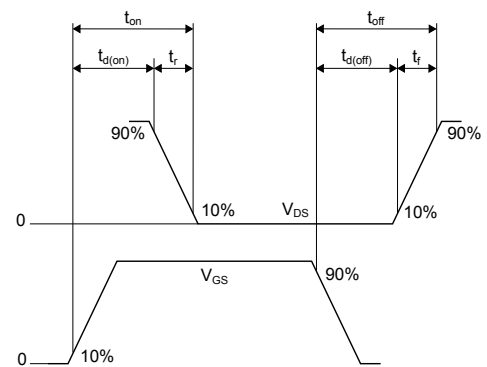
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Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


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Figure 17. Switching time waveform


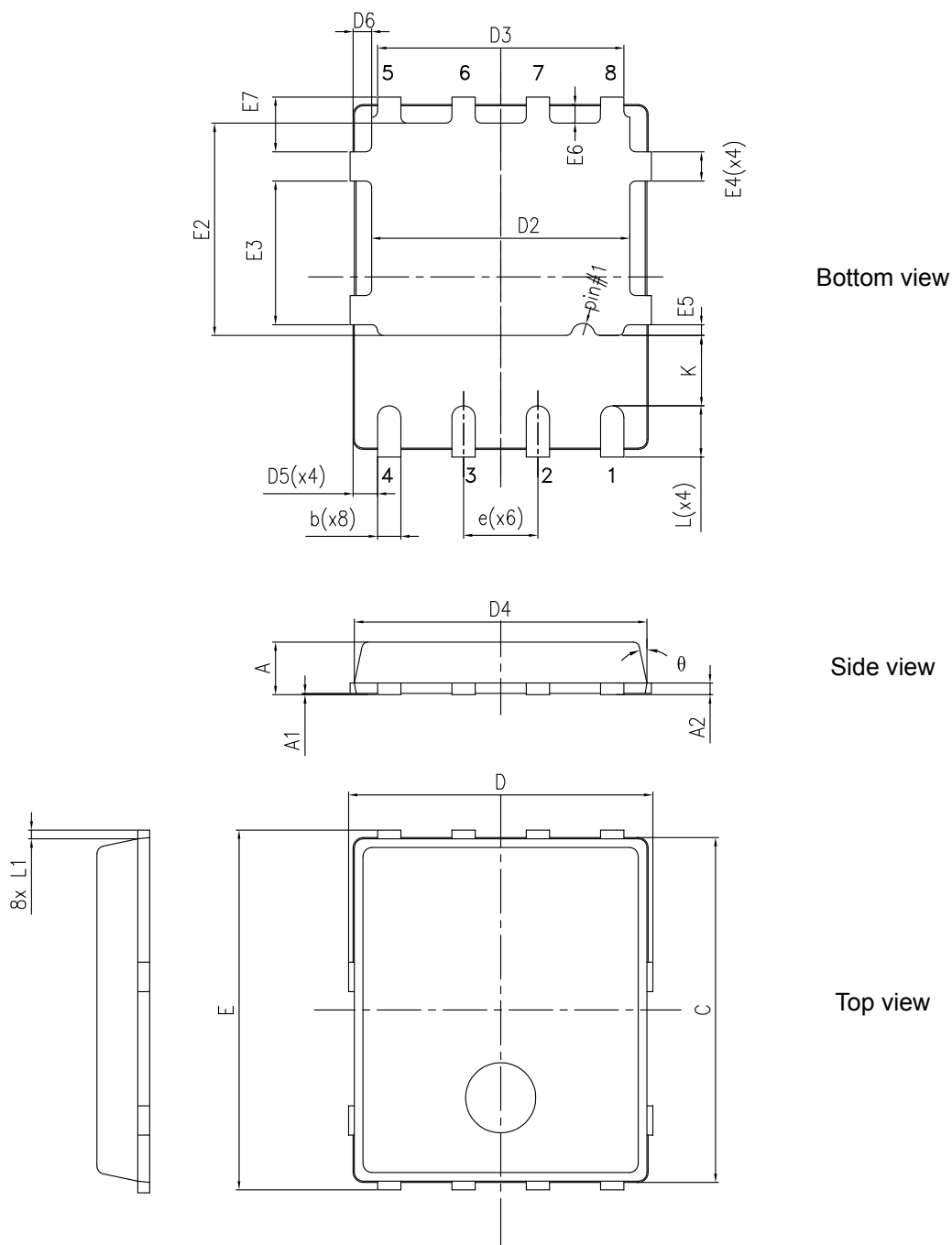
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package information

Figure 18. PowerFLAT™ 5x6 type C package outline

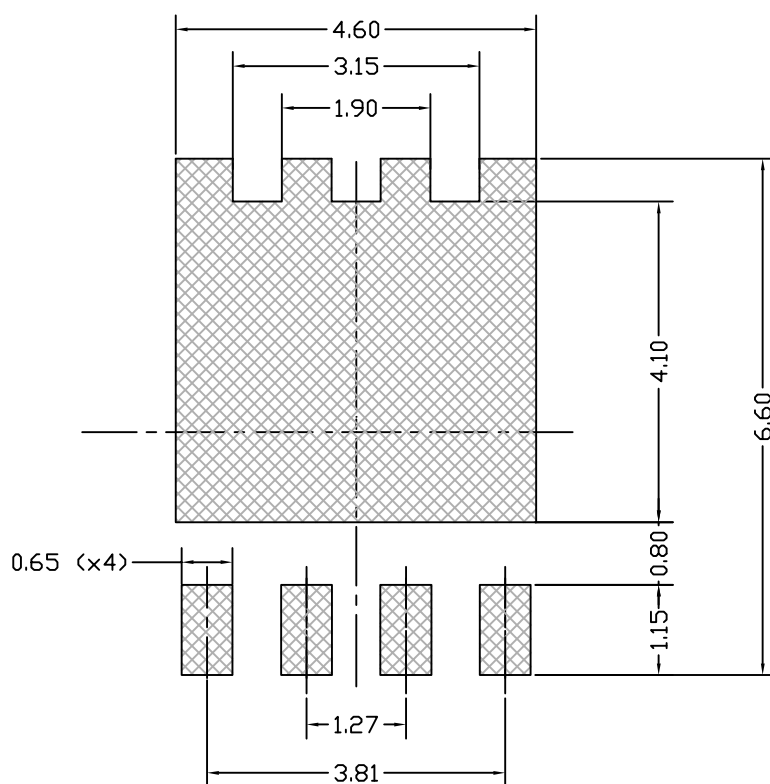


8231817_typeC_Rev18

Table 7. PowerFLAT™ 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

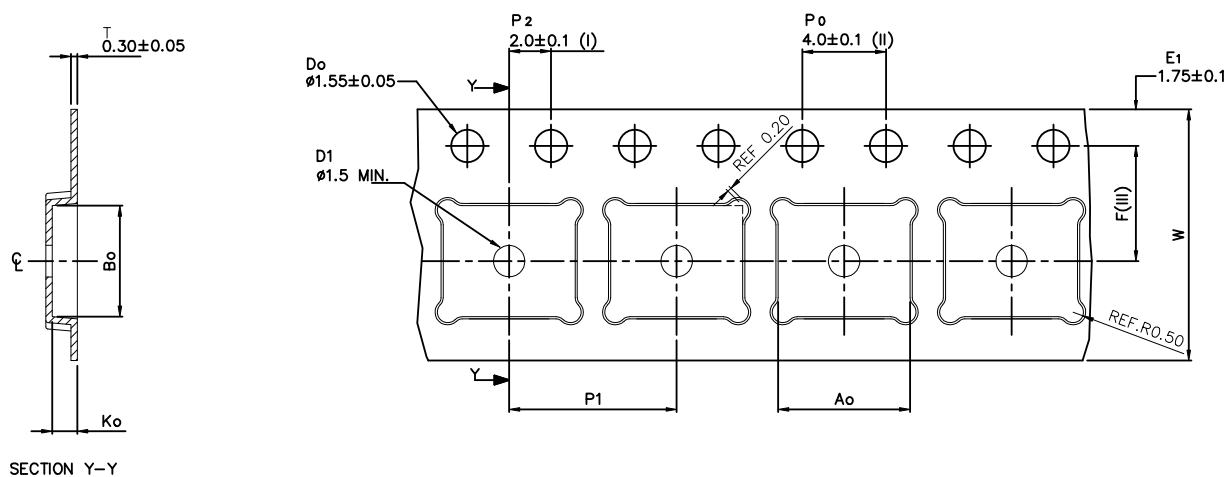
Figure 19. PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



8231817_FOOTPRINT_simp_Rev_18

4.2 PowerFLAT™ 5x6 packing information

Figure 20. PowerFLAT™ 5x6 tape (dimensions are in mm)



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 21. PowerFLAT™ 5x6 package orientation in carrier tape

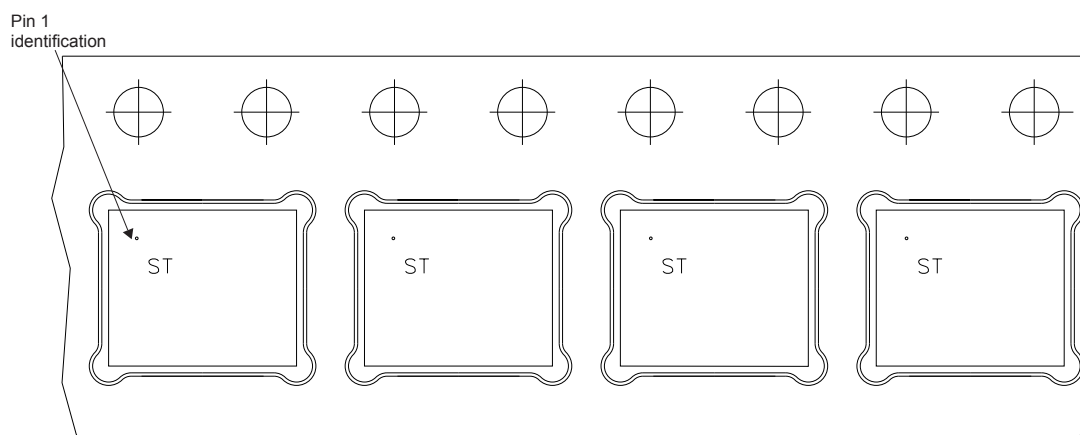
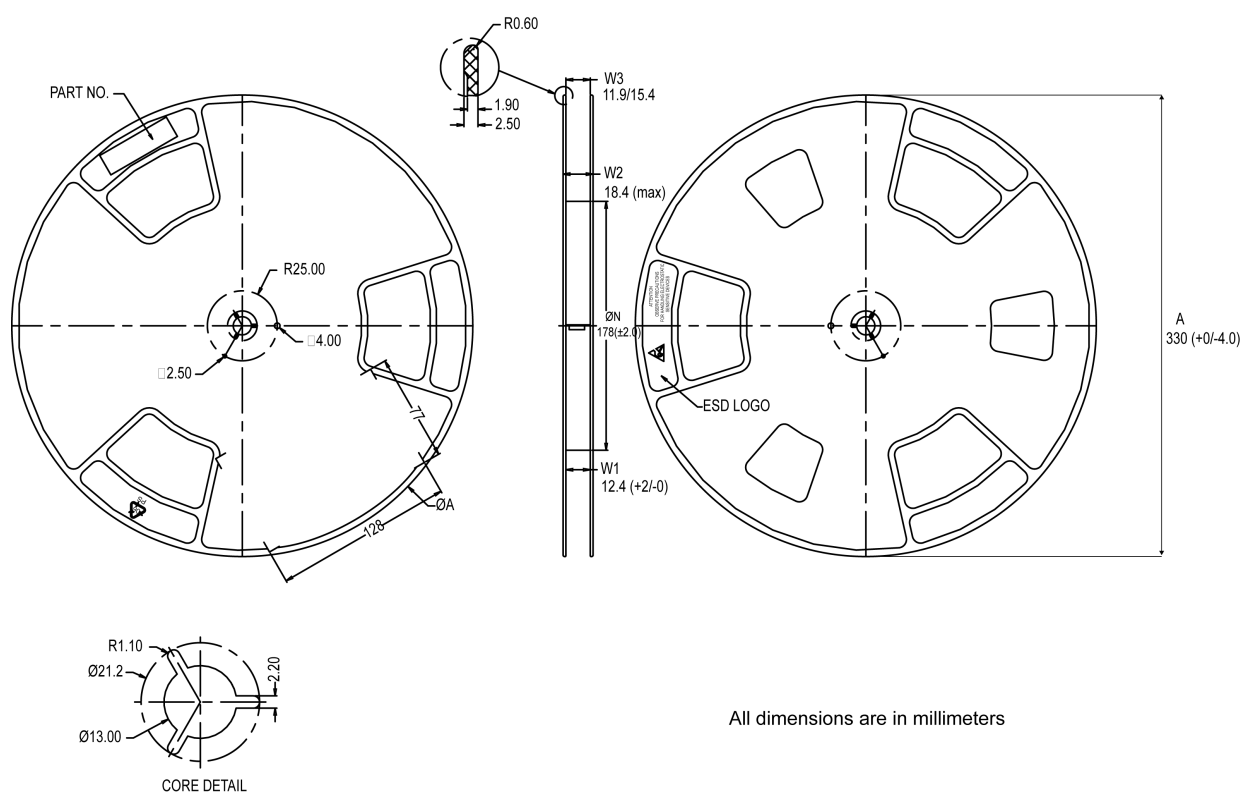


Figure 22. PowerFLAT™ 5x6 reel



8234350_Reel_rev_C

Revision history

Table 8. Document revision history

Date	Version	Changes
03-Aug-2014	1	First release.
03-Nov-2014	2	Updated value Table 2: Electrical characteristics Minor text changes
06-Feb-2019	3	Removed maturity status indication from cover page. The document status is production data. Updated marking information in Product summary table in cover page. Updated Section 4 Package information . Minor text changes.

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