10 MHz, 14.5 nV/√Hz, Rail-to-Rail I/O, Zero Input Crossover Distortion Amplifier

Data Sheet **ADA4500-2**

FEATURES

Power supply rejection ratio (PSRR): 98 dB minimum
Common-mode rejection ratio (CMRR): 95 dB minimum
Offset voltage: 120 µV maximum
Single-supply operation: 2.7 V to 5.5 V
Dual-supply operation: ±1.35 V to ±2.75 V
Wide bandwidth: 10 MHz
Rail-to-rail input and output
Low noise
- **2 µV p-p from 0.1 Hz to 10 Hz**
- **14.5 nV/√Hz at 1 kHz**

Very low input bias current: 2 pA maximum

APPLICATIONS

Pressure and position sensors
Remote security
Medical monitors
Process controls
Hazard detectors
Photodiode applications

PIN CONFIGURATION

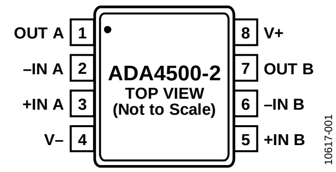

Figure 1. 8-Lead MSOP Pin Configuration

For more information on the pin connections, see the Pin Configurations and Function Descriptions section

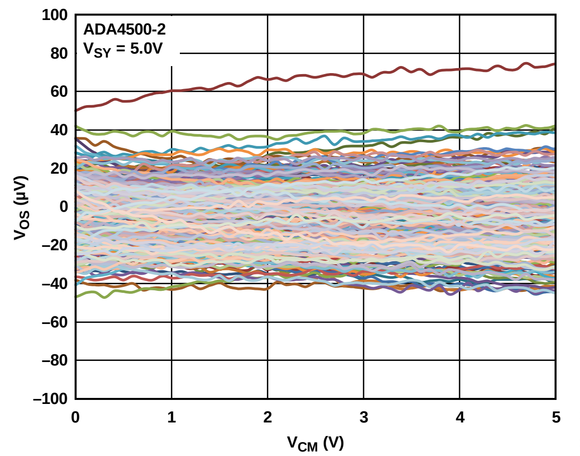

Figure 2. The ADA4500-2 Eliminates Crossover Distortion Across its Full Supply Range

GENERAL DESCRIPTION

The ADA4500-2 is a dual 10 MHz, 14.5 nV/√Hz, low power amplifier featuring rail-to-rail input and output swings while operating from a 2.7 V to 5.5 V single power supply. Compatible with industry-standard nominal voltages of +3.0 V, +3.3 V, +5.0 V, and ±2.5 V.

Employing a novel zero-crossover distortion circuit topology, this amplifier offers high linearity over the full, rail-to-rail input common-mode range, with excellent power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR) performance without the crossover distortion seen with the traditional complementary rail-to-rail input stage. The resulting op amp also has excellent precision, wide bandwidth, and very low bias current.

This combination of features makes the ADA4500-2 an ideal choice for precision sensor applications because it minimizes errors due to power supply variation and maintains high CMRR over the full input voltage range. The ADA4500-2 is also an excellent amplifier for driving analog-to-digital converters (ADCs) because the output does not distort with the common-mode voltage, which enables the ADC to use its full input voltage range, maximizing the dynamic range of the conversion subsystem.

Many applications such as sensors, handheld instrumentation, precision signal conditioning, and patient monitors can benefit from the features of the ADA4500-2.

The ADA4500-2 is specified for the extended industrial temperature range (−40°C to +125°C) and available in the standard 8-lead MSOP and 8-lead LFCSP packages.

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SPECIFICATIONS

V_{SY} = 2.7 V ELECTRICAL CHARACTERISTICS

V_{SY} = 2.7 V, V_{CM} = V_{SY}/2, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				120	µV
		−40°C < T_A < +125°C			700	µV
Offset Voltage Drift	TCV_{OS}	−40°C < T_A < +125°C		0.8	5.5	µV/°C
Input Bias Current	I_B			0.3	1	pA
		−40°C < T_A < +125°C			170	pA
Input Offset Current	I_{OS}			0.3	1	pA
		−40°C < T_A < +125°C			20	pA
Input Voltage Range	IVR	−40°C < T_A < +125°C	V−		V+	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V− to V+	95	110		dB
		−40°C < T_A < +125°C	90			dB
		V_{CM} = [(V−) − 0.2 V] to [(V+) + 0.2 V]	90	110		dB
		−40°C < T_A < +125°C	80			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, [(V−) + 0.05 V] < V_{OUT} < [(V+) − 0.05 V]	100	110		dB
		−40°C < T_A < +125°C	100			dB
		R_L = 10 kΩ, [(V−) + 0.05 V] < V_{OUT} < [(V+) − 0.05 V]	105	120		dB
		−40°C < T_A < +125°C	105			dB
Input Capacitance						
Common Mode	C_{INCM}			5		pF
Differential	C_{INDM}			1.7		pF
Input Resistance	R_{IN}	Common mode and differential mode		400		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V−	2.685	2.695		V
		−40°C < T_A < +125°C	2.68			V
		R_L = 2 kΩ to V−	2.65	2.68		V
		−40°C < T_A < +125°C	2.65			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V+		3	5	mV
		−40°C < T_A < +125°C			10	mV
		R_L = 2 kΩ to V+		13	20	mV
		−40°C < T_A < +125°C			25	mV
Short Circuit Limit	I_{SC}	Sourcing, V_{OUT} shorted to V−		26		mA
		Sinking, V_{OUT} shorted to V+		−48		mA
Closed-Loop Impedance	Z_{OUT}	f = 10 MHz, A_V = 1		70		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 5.5 V	98	119		dB
		−40°C to +125°C	94			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		1.5	1.65	mA
		−40°C < T_A < +125°C			1.7	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 30 pF, A_V = +1, V_{IN} = V_{SY}		5.5		V/µs
		R_L = 10 kΩ, C_L = 30 pF, A_V = −1, V_{IN} = V_{SY}		8.7		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = +100		10.1		MHz
Unity Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = +1		10.3		MHz
−3 dB Bandwidth	−3 dB	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = −1		18.4		MHz
Phase Margin	ΦM	V_{IN} = 5 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		52		Degrees
Settling Time to 0.1%	t_s	V_{IN} = 2 V p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = −1		1		µs

Parameter	Symbol	Test Conditions/Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	G = 1, f = 10 Hz to 20 kHz, V_{IN} = 0.7 V rms at 1 kHz				
Bandwidth = 80 kHz				0.0006		%
Bandwidth = 500 kHz				0.001		%
Peak-to-Peak Noise	$e_{n\ p\text{-}p}$	f = 0.1 Hz to 10 Hz		3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		14.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<0.5		fA/√Hz

V_{SY} = 5.0 V ELECTRICAL CHARACTERISTICS

V_{SY} = 5.0 V, $V_{CM} = V_{SY}/2$, T_A = 25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				120	µV
		−40°C < T_A < +125°C			700	µV
Offset Voltage Drift	TCV_{OS}	−40°C < T_A < +125°C		0.9	5.5	µV/°C
Input Bias Current	I_B			0.7	2	pA
		−40°C < T_A < +125°C			190	pA
Input Offset Current	I_{OS}			0.3	3	pA
		−40°C < T_A < +125°C			20	pA
Input Voltage Range	IVR	−40°C < T_A < +125°C	V−		V+	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V− to V+	95	115		dB
		−40°C < T_A < +125°C	95			dB
		V_{CM} = [(V−) − 0.2 V] to [(V+) + 0.2 V]	95	115		dB
		−40°C < T_A < +125°C	84			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, [(V−) + 0.05 V] < V_{OUT} < [(V+) − 0.05 V]	105	110		dB
		−40°C < T_A < +125°C	80			dB
		R_L = 10 kΩ, [(V−) + 0.05 V] < V_{OUT} < [(V+) − 0.05 V]	110	120		dB
		−40°C < T_A < +125°C	110			dB
Input Capacitance						
Common Mode	C_{INCM}			5		pF
Differential	C_{INDM}			1.7		pF
Input Resistance	R_{IN}	Common mode and differential mode		400		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ to V−	4.975	4.99		V
		−40°C < T_A < +125°C	4.97			V
		R_L = 2 kΩ to V−	4.95	4.97		V
		−40°C < T_A < +125°C	4.95			V
Output Voltage Low	V_{OL}	R_L = 10 kΩ to V+		7	15	mV
		−40°C < T_A < +125°C			20	mV
		R_L = 2 kΩ to V+		24	40	mV
		−40°C < T_A < +125°C			50	mV
Short Circuit Limit	I_{SC}	Sourcing, V_{OUT} shorted to V−		75		mA
		Sinking, V_{OUT} shorted to V+		−75		mA
Closed-Loop Impedance	Z_{OUT}	f = 10 MHz, A_V = +1		60		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_{SY} = 2.7 V to 5.5 V	98	119		dB
		−40°C to +125°C	94			dB
Supply Current per Amplifier	I_{SY}	I_O = 0 mA		1.55	1.75	mA
		−40°C < T_A < +125°C			1.8	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, C_L = 30 pF, A_V = +1, $V_{IN} = V_{SY}$		5.5		V/µs
		R_L = 10 kΩ, C_L = 30 pF, A_V = −1, $V_{IN} = V_{SY}$		8.7		V/µs
Gain Bandwidth Product	GBP	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = +100		10		MHz
Unity Gain Crossover	UGC	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = +1		10.5		MHz
−3 dB Bandwidth	−3 dB	V_{IN} = 5 mV p-p, R_L = 10 kΩ, A_V = −1		19.2		MHz
Phase Margin	ΦM	V_{IN} = 5 mV p-p, R_L = 10 kΩ, C_L = 20 pF, A_V = +1		57		Degrees
Settling Time to 0.1%	t_s	V_{IN} = 4 V p-p, R_L = 10 kΩ, C_L = 10 pF, A_V = −1		1		µs

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	G = 1, f = 20 Hz to 20 kHz, V_{IN} = 1.4 V rms at 1 kHz				
Bandwidth = 80 kHz				0.0004		%
Bandwidth = 500 kHz				0.0008		%
Peak-to-Peak Noise	$e_{n\ p\text{-}p}$	f = 0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		14.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		<0.5		fA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	(V–) – 0.2 V to (V+) + 0.2 V
Differential Input Voltage[1]	(V–) – 0.2 V to (V+) + 0.2 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Differential input voltage is limited to 5.6 V or the supply voltage + 0.6 V, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

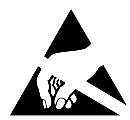
θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP (RM-8)[1]	142	45	°C/W
8-Lead LFCSP (CP-8-12)[2, 3]	85	2	°C/W

[1] Thermal numbers were simulated on a 4-layer JEDEC printed circuit board (PCB).
[2] Thermals numbers were simulated on a 4 layer JEDEC PCB with the exposed pad soldered to the PCB.
[3] θ_{JC} was simulated at the exposed pad on the bottom of the package.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

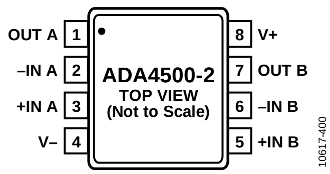


Figure 3. 8-Lead MSOP Pin Configuration

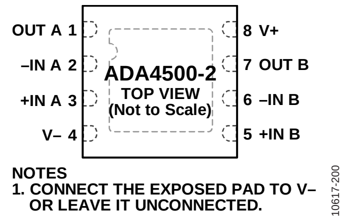


Figure 4. 8-Lead LFCSP Pin Configuration

Table 5. 8-Lead MSOP and 8-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	−IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V−	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	−IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.
	EPAD	For the LFCSP package only, connect the exposed pad to V− or leave it unconnected.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

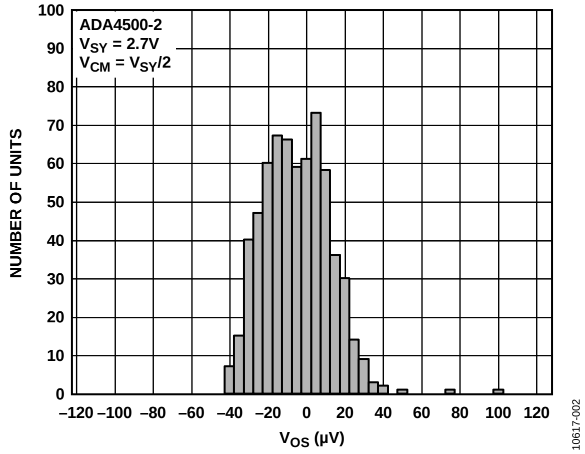


Figure 5. Input Offset Voltage Distribution, V_{SY} = 2.7 V

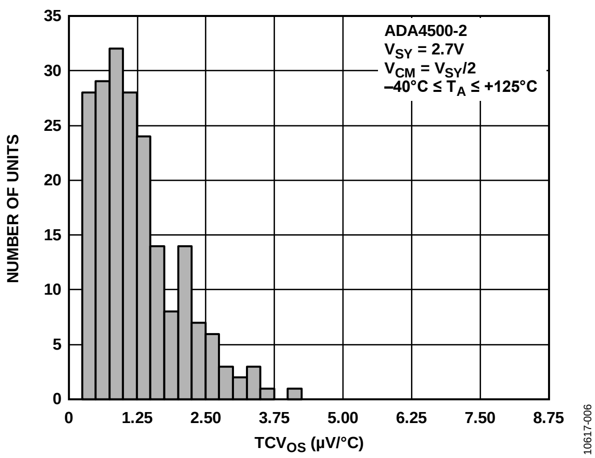


Figure 6. Input Offset Voltage Drift Distribution, V_{SY} = 2.7 V

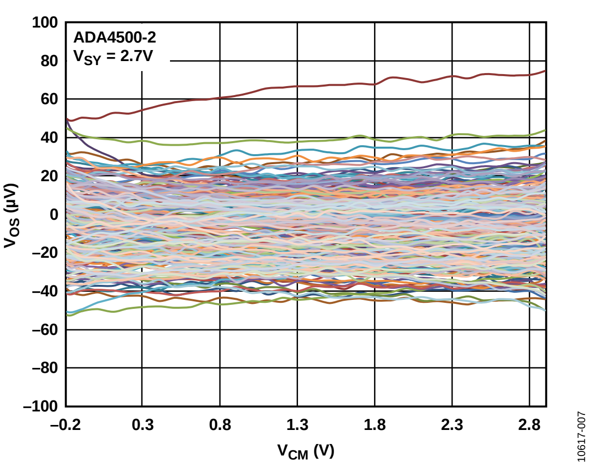


Figure 7. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 2.7 V

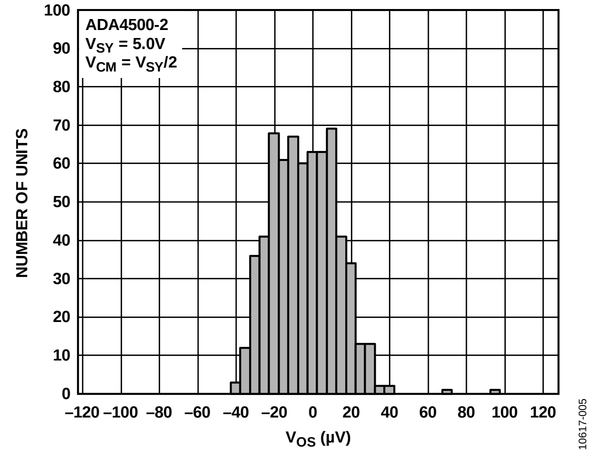


Figure 8. Input Offset Voltage Distribution, V_{SY} = 5.0 V

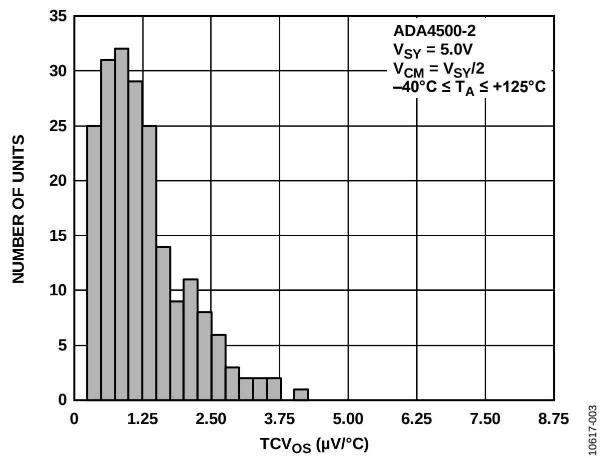


Figure 9. Input Offset Voltage Drift Distribution, V_{SY} = 5.0 V

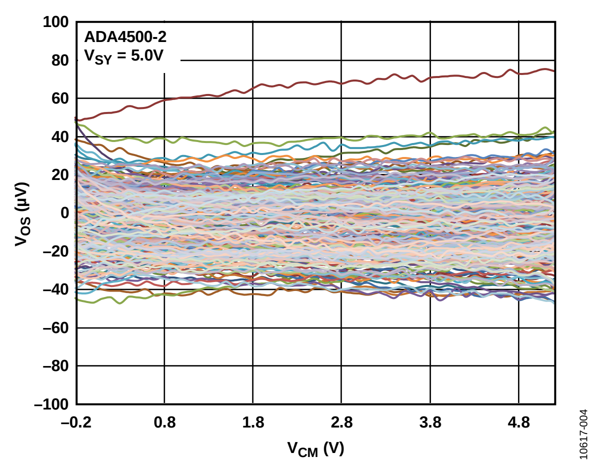


Figure 10. Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 5.0 V

T_A = 25°C, unless otherwise noted.

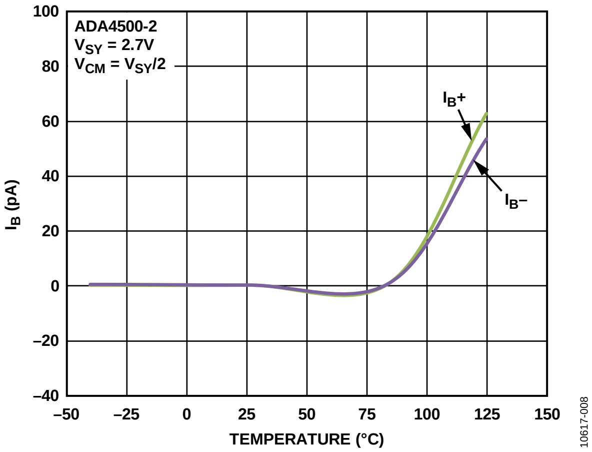


Figure 11. Input Bias Current (I_B) vs. Temperature, V_{SY} = 2.7 V

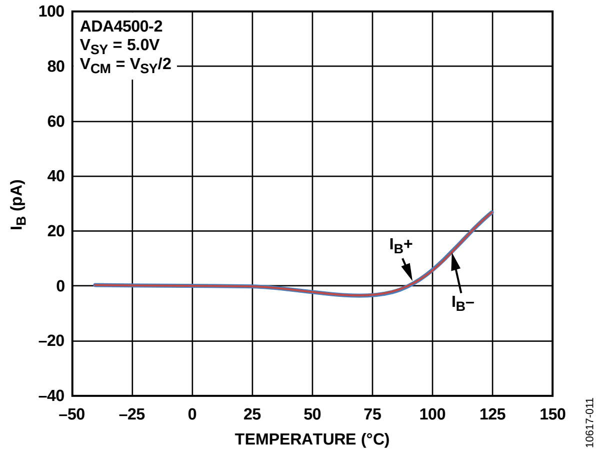


Figure 14. Input Bias Current (I_B) vs. Temperature, V_{SY} = 5.0 V

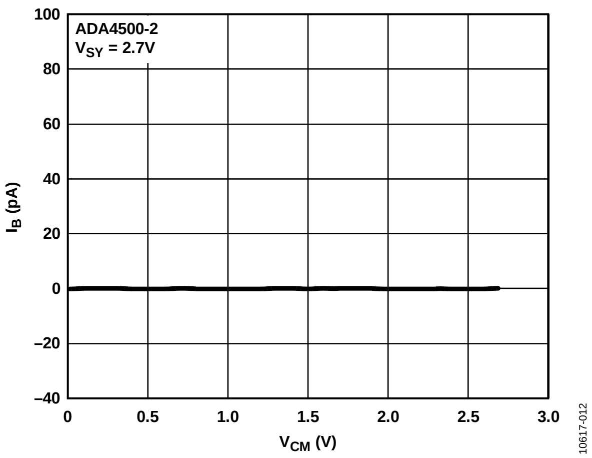


Figure 12. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 2.7 V

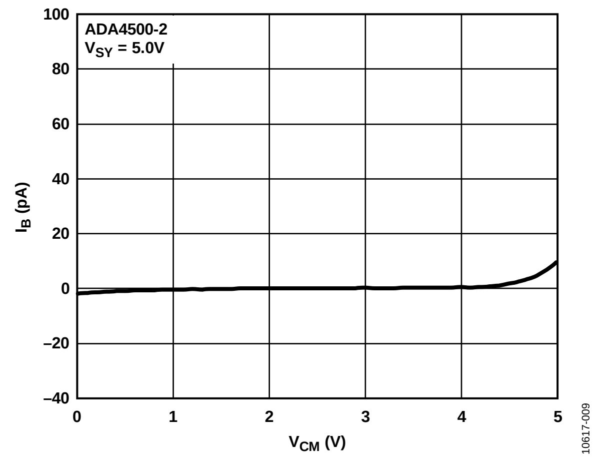


Figure 15. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM}), V_{SY} = 5.0 V

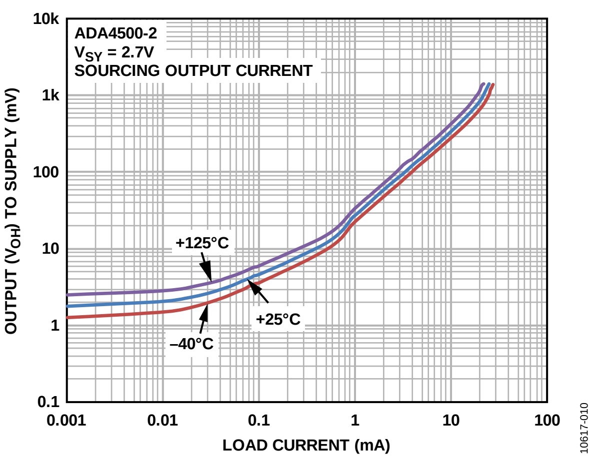


Figure 13. Output Voltage (V_{OH}) to Supply Rail vs. Load Current, V_{SY} = 2.7 V

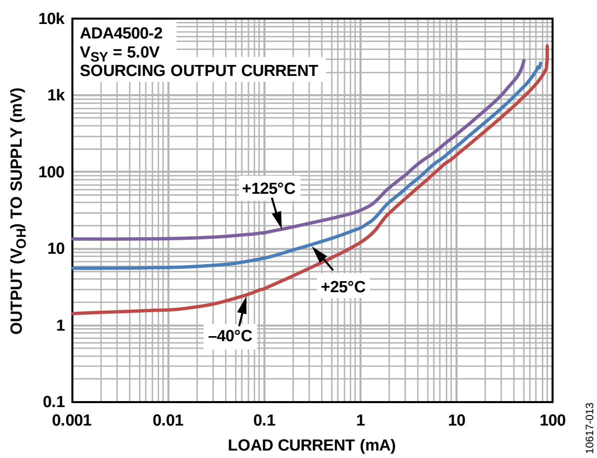


Figure 16. Output Voltage (V_{OH}) to Supply Rail vs. Load Current, V_{SY} = 5.0 V

T_A = 25°C, unless otherwise noted.

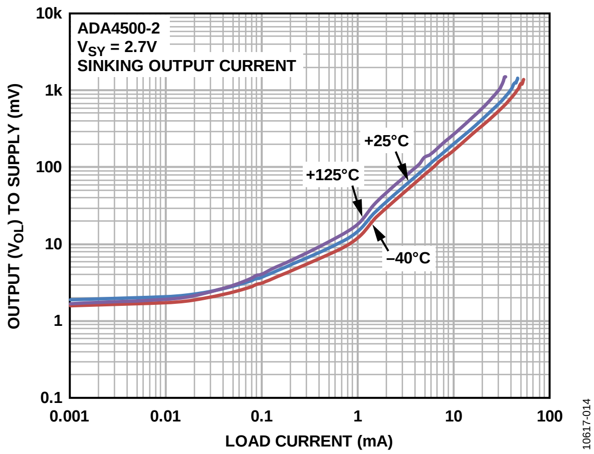


Figure 17. Output Voltage (V_{OL}) to Supply Rail vs. Temperature, V_{SY} = 2.7 V

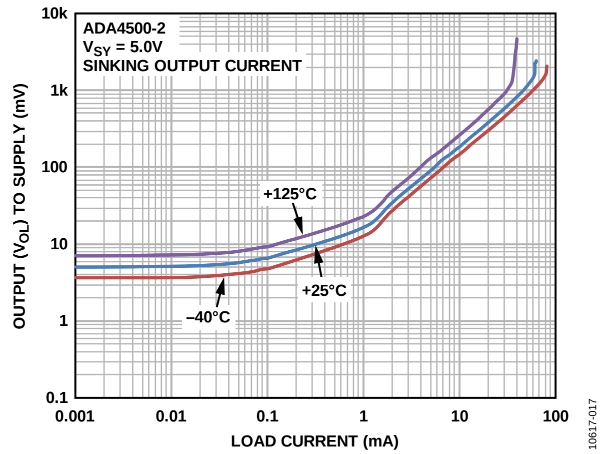


Figure 20. Output Voltage (V_{OL}) to Supply Rail vs. Load Current, V_{SY} = 5.0 V

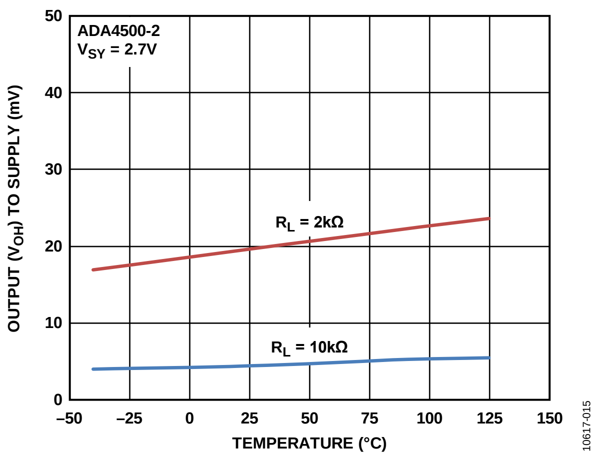


Figure 18. Output Voltage (V_{OH}) to Supply Rail vs. Temperature, V_{SY} = 2.7 V

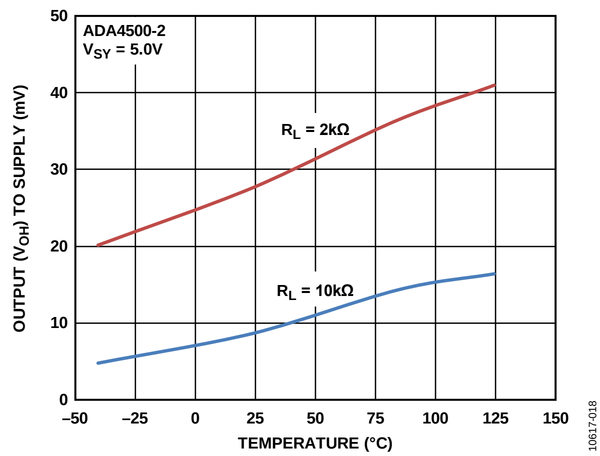


Figure 21. Output Voltage (V_{OH}) to Supply Rail vs. Temperature, V_{SY} = 5.0 V

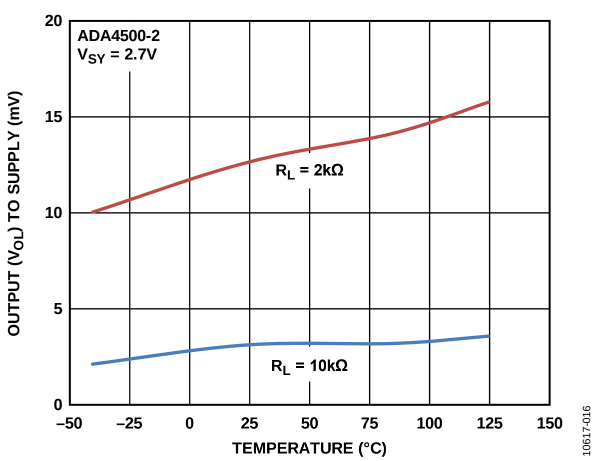


Figure 19. Output Voltage (V_{OL}) to Supply Rail vs. Temperature, V_{SY} = 2.7 V

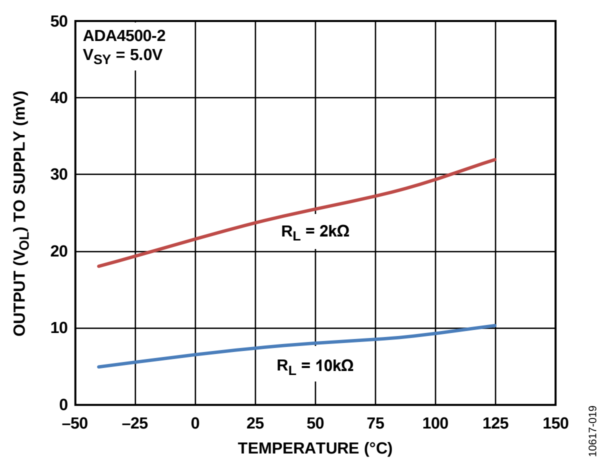


Figure 22. Output Voltage (V_{OL}) to Supply Rail vs. Temperature, V_{SY} = 5.0 V

T_A = 25°C, unless otherwise noted.

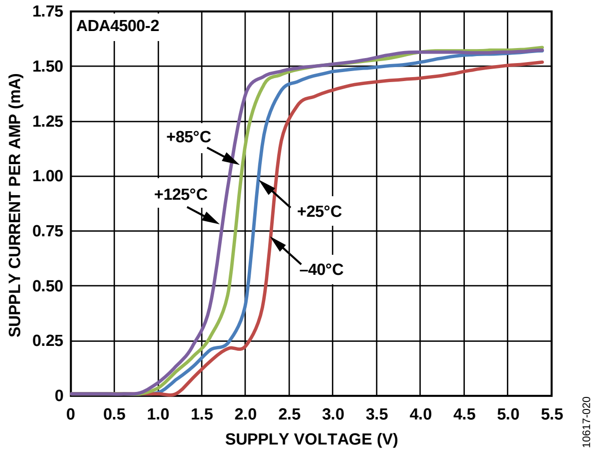


Figure 23. Supply Current per Amp vs. Supply Voltage

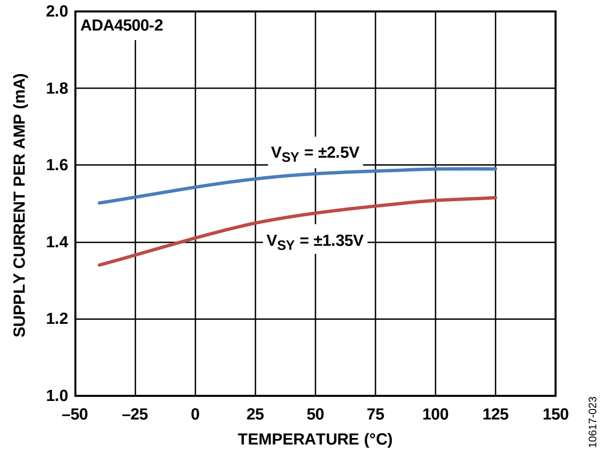


Figure 26. Supply Current per Amp vs. Temperature

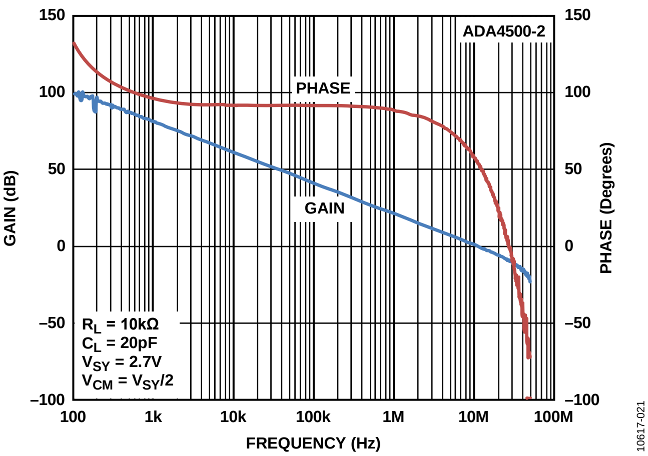


Figure 24. Open-Loop Gain and Phase vs. Frequency, V_{SY} = 2.7 V

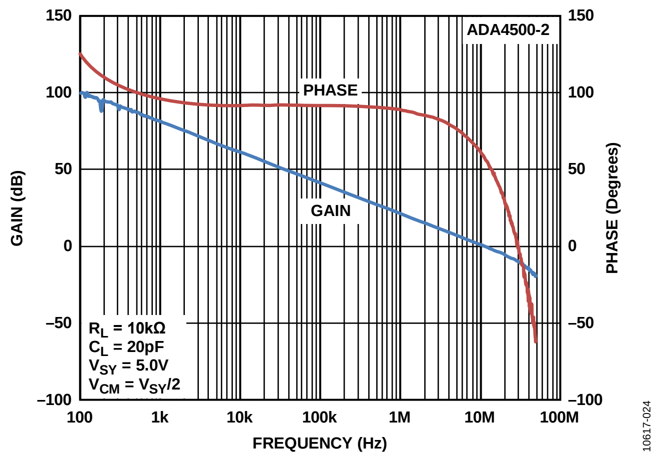


Figure 27. Open-Loop Gain and Phase vs. Frequency, V_{SY} = 5.0 V

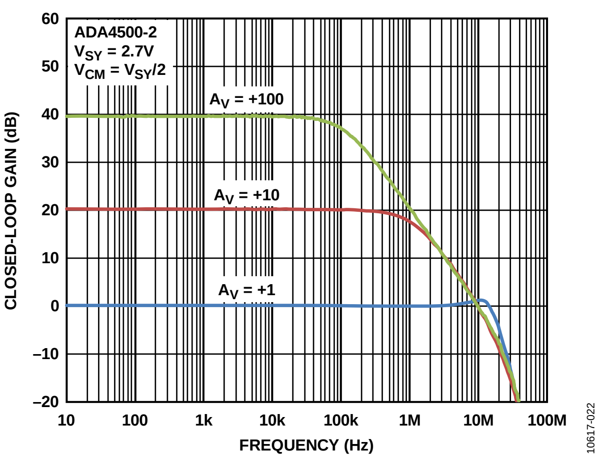


Figure 25. Closed Loop Gain vs. Frequency, V_{SY} = 2.7 V

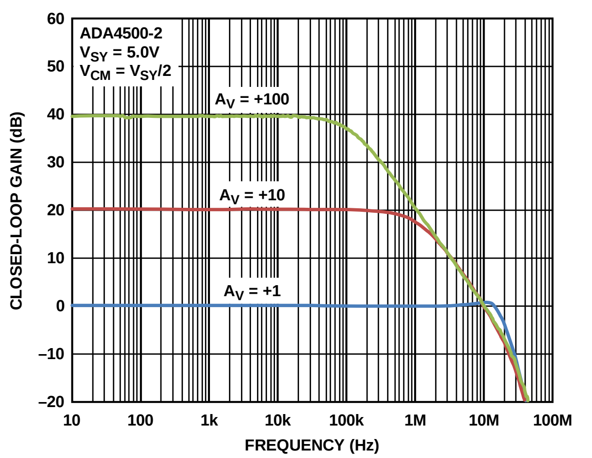


Figure 28. Closed-Loop Gain vs. Frequency, V_{SY} = 5.0 V

T_A = 25°C, unless otherwise noted.

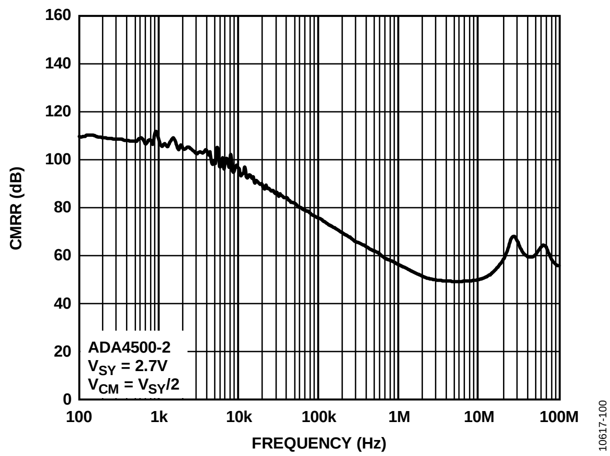


Figure 29. CMRR vs. Frequency, V_{SY} = 2.7 V

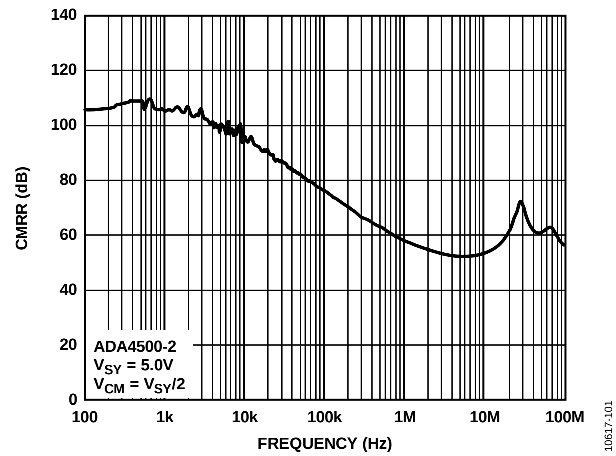


Figure 32. CMRR vs. Frequency, V_{SY} = 5.0 V

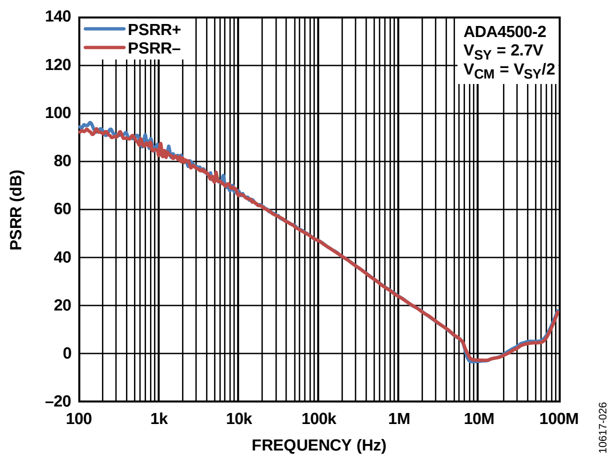


Figure 30. PSRR vs. Frequency, V_{SY} = 2.7 V

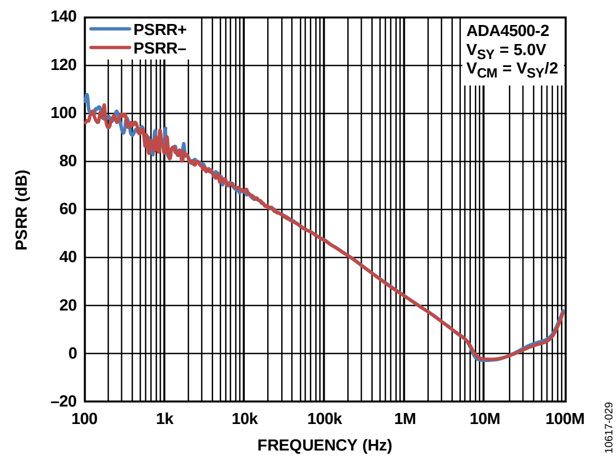


Figure 33. PSRR vs. Frequency, V_{SY} = 5.0 V

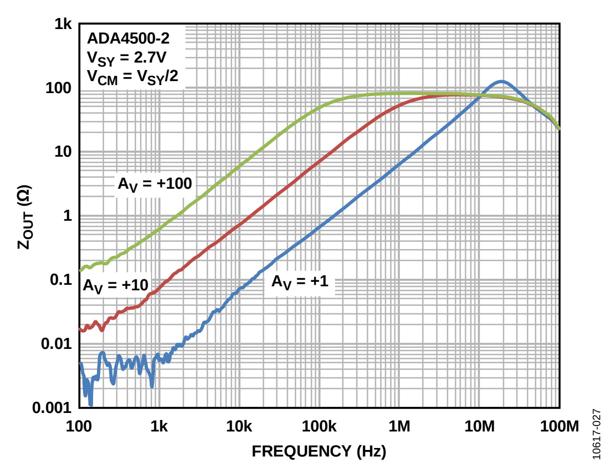


Figure 31. Closed Loop Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = 2.7 V

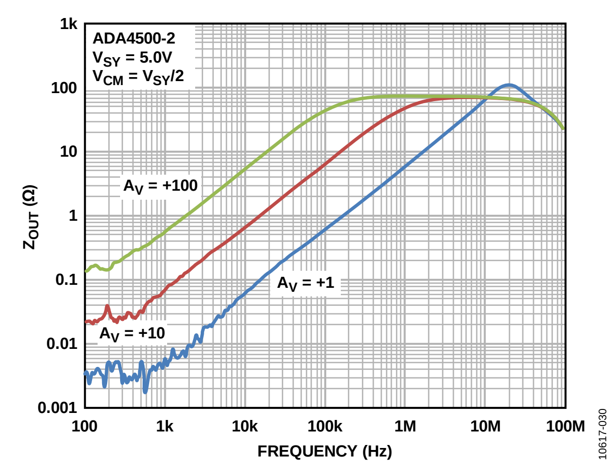


Figure 34. Closed Loop Output Impedance (Z_{OUT}) vs. Frequency, V_{SY} = 5.0 V

T_A = 25°C, unless otherwise noted.

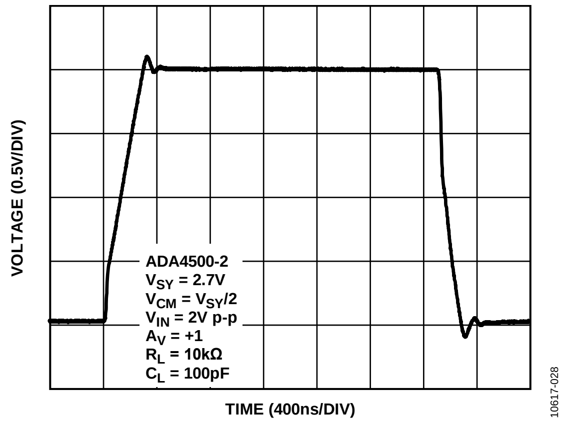


Figure 35. Large Signal Transient Response, V_{SY} = 2.7 V

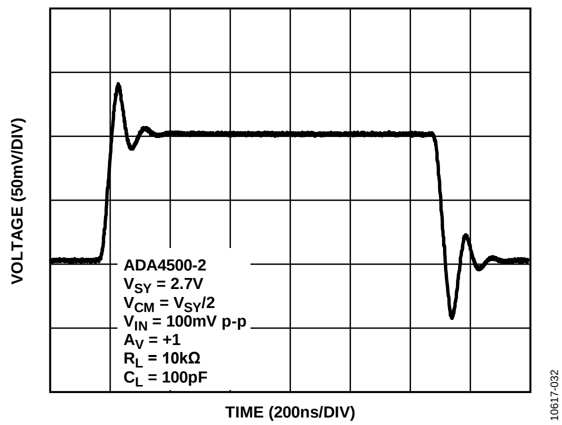


Figure 36. Small Signal Transient Response, V_{SY} = 2.7 V

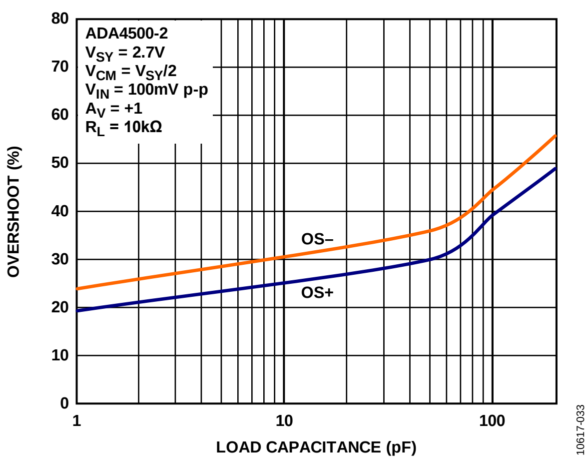


Figure 37. Small Signal Overshoot vs. Load Capacitance, V_{SY} = 2.7 V

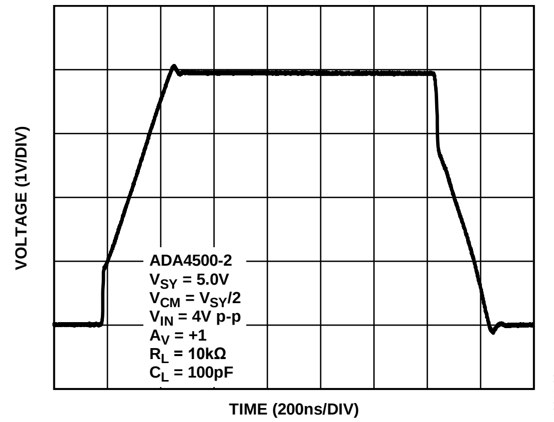


Figure 38. Large Signal Transient Response, V_{SY} = 5.0 V

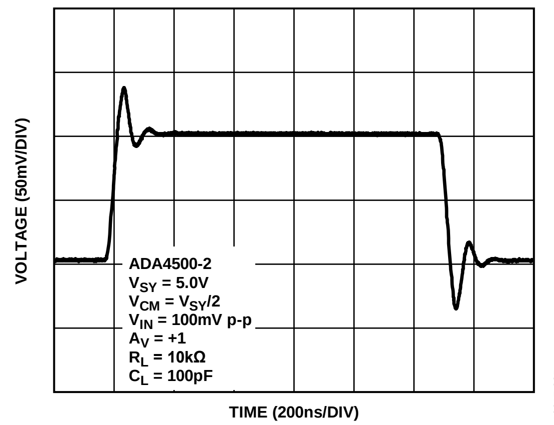


Figure 39. Small Signal Transient Response, V_{SY} = 5.0 V

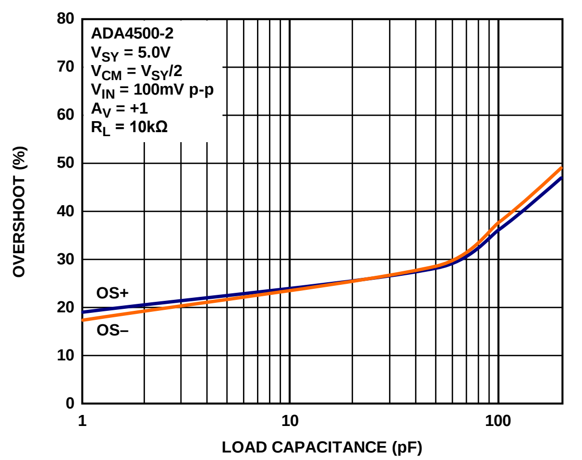


Figure 40. Small Signal Overshoot vs. Load Capacitance, V_{SY} = 5.0 V

T_A = 25°C, unless otherwise noted.

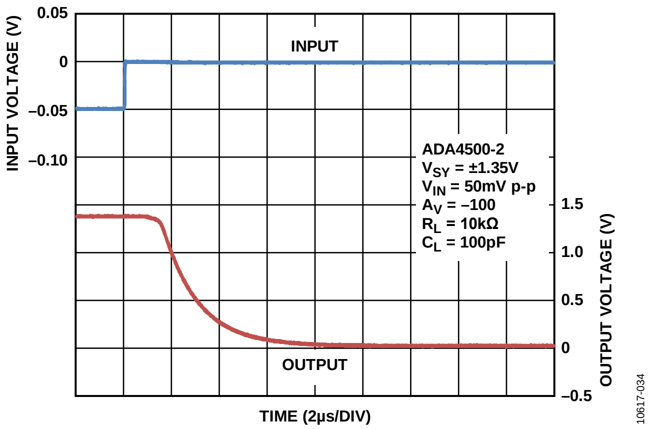


Figure 41. Positive Overload Recovery, V_{SY} = ±1.35 V

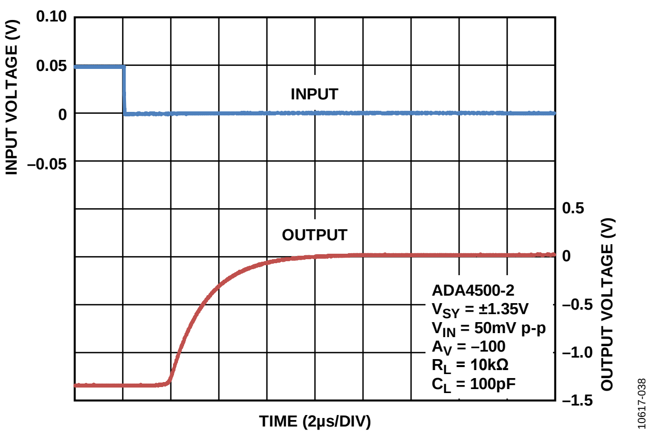


Figure 42. Negative Overload Recovery, V_{SY} = ±1.35 V

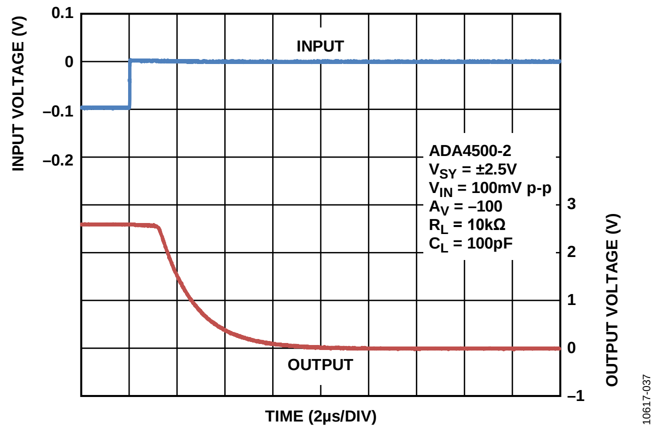


Figure 43. Positive Overload Recovery, V_{SY} = ±2.5 V

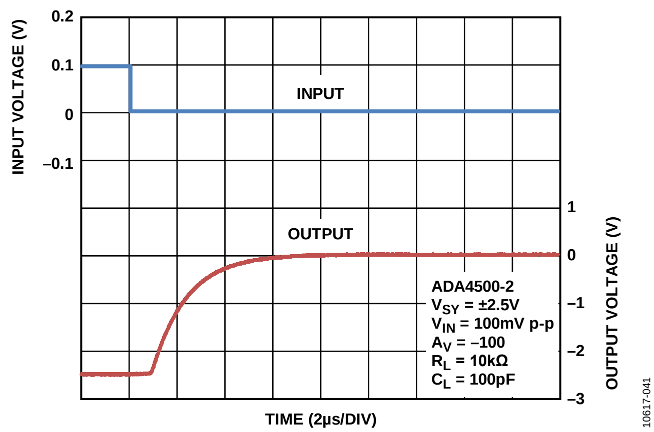


Figure 44. Negative Overload Recovery, V_{SY} = ±2.5 V

T_A = 25°C, unless otherwise noted.

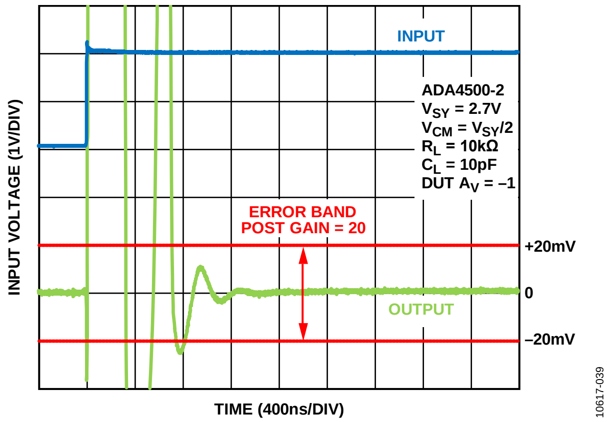


Figure 45. Positive Settling Time to 0.1%, V_{SY} = 2.7 V

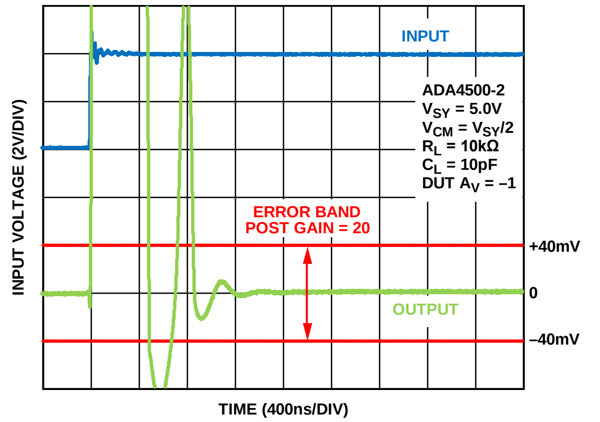


Figure 47. Positive Settling Time to 0.1%, V_{SY} = 5.0 V

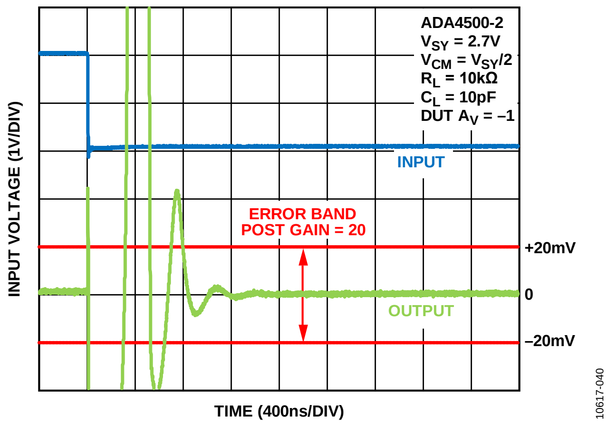


Figure 46. Negative Settling Time to 0.1%, V_{SY} = 2.7 V

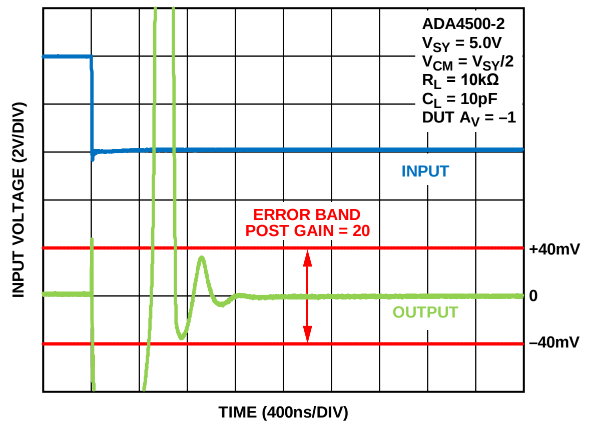


Figure 48. Negative Settling Time to 0.1%, V_{SY} = 5.0 V

T_A = 25°C, unless otherwise noted.

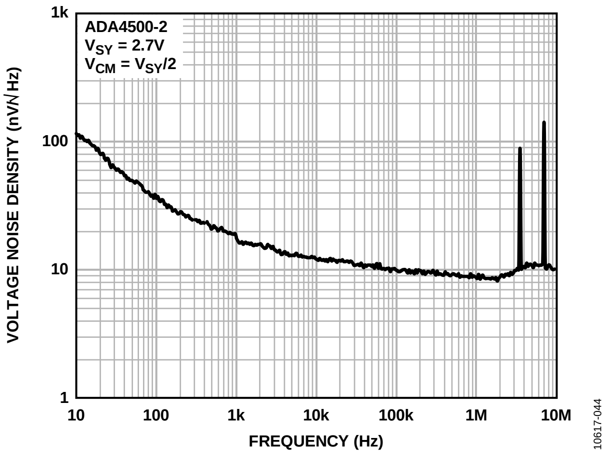


Figure 49. Voltage Noise Density vs. Frequency, V_{SY} = 2.7 V (10 Hz to 10 MHz)

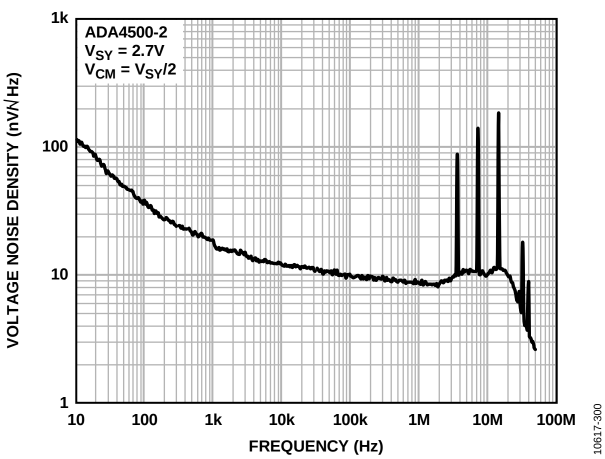


Figure 50. Voltage Noise Density vs. Frequency, V_{SY} = 2.7 V (10 Hz to 100 MHz)

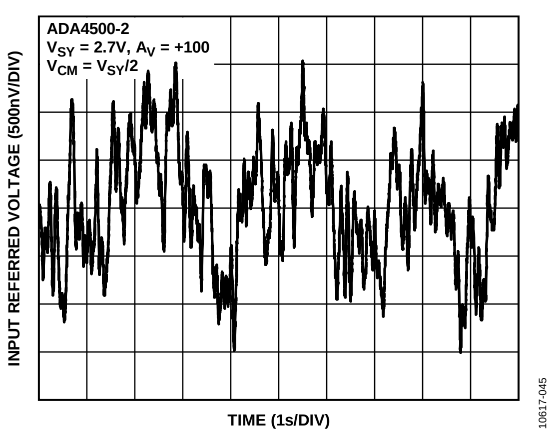


Figure 51. 0.1 to 10 Hz Noise, V_{SY} = 2.7 V

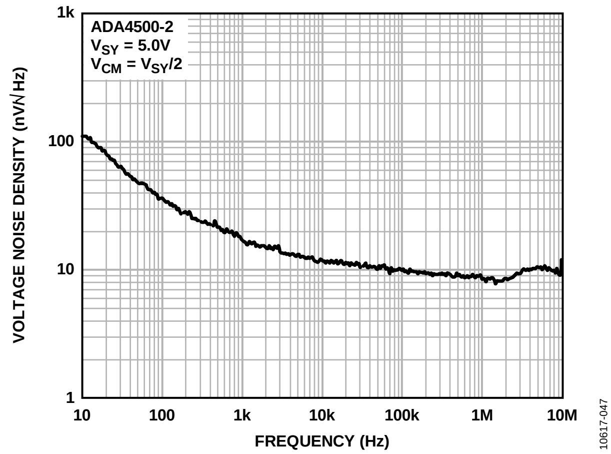


Figure 52. Voltage Noise Density vs. Frequency, V_{SY} = 5.0 V (10 Hz to 10 MHz)

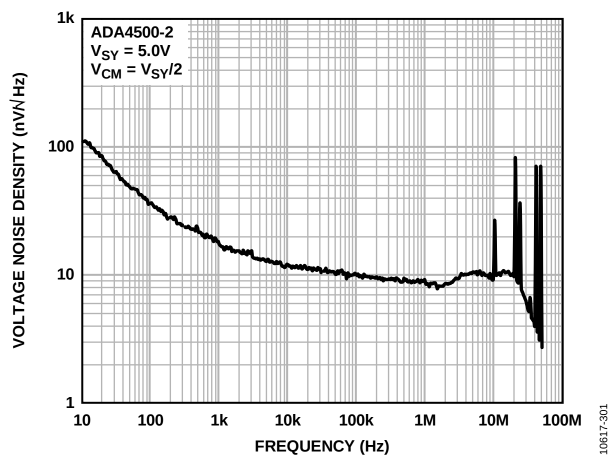


Figure 53. Voltage Noise Density vs. Frequency, V_{SY} = 5.0 V (10 Hz to 100 MHz)

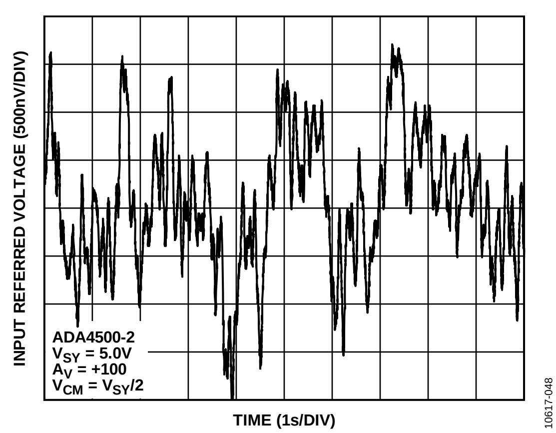


Figure 54. 0.1 to 10 Hz Noise, V_{SY} = 5.0 V

T_A = 25°C, unless otherwise noted.

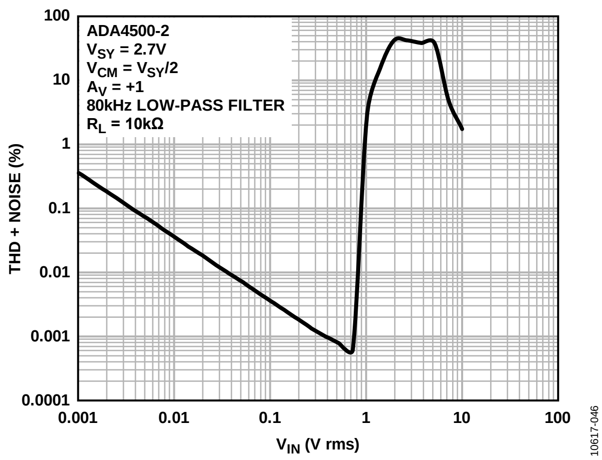


Figure 55. THD + Noise vs. Amplitude, V_{SY} = 2.7 V

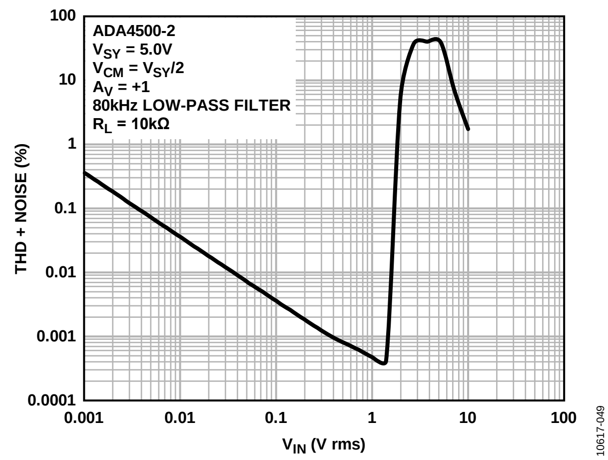


Figure 57. THD + Noise vs. Amplitude, V_{SY} = 5.0 V

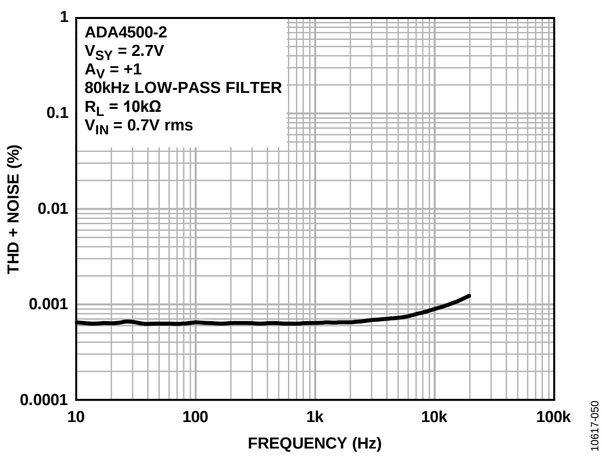


Figure 56. THD + Noise vs. Frequency, V_{SY} = 2.7 V

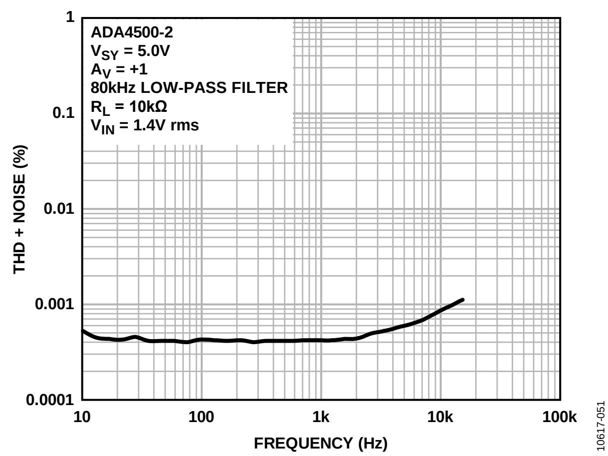


Figure 58. THD + Noise vs. Frequency, V_{SY} = 5.0 V

THEORY OF OPERATION

RAIL-TO-RAIL OUTPUT

When processing a signal through an op amp to a load, it is often desirable to have the output of the op amp swing as close to the voltage supply rails as possible. For example, when an op amp is driving an ADC and both the op amp and ADC are using the same supply rail voltages, the op amp must drive as close to the V+ and V− rails as possible so that all codes in the ADC are usable. A non-rail-to-rail output can require as much as 1.5 V or more between the output and the rails, thus limiting the input dynamic range to the ADC, resulting in less precision (number of codes) in the converted signal.

The ADA4500-2 can drive its output to within a few millivolts of the supply rails (see the output voltage high and output voltage low specifications in Table 1 and Table 2). The rail-to-rail output maximizes the dynamic range of the output, increasing the range and precision, and often saving the cost, board space, and added error of the additional gain stages.

RAIL-TO-RAIL INPUT (RRI)

Using a CMOS nonrail-to-rail input stage (that is, a single differential pair) limits the input voltage to approximately one gate-source voltage (V_{GS}) away from one of the supply lines. Because V_{GS} for normal operation is commonly more than 1 V, a single differential pair, input stage op amp greatly restricts the allowable input voltage. This can be quite limiting with low supply voltages supplies. To solve this problem, RRI stages are designed to allow the input signal to range to the supply voltages (see the input voltage range specifications in Table 1 and Table 2). In the case of the ADA4500-2, the inputs continue to operate 200 mV beyond the supply rails (see Figure 7 and Figure 10).

ZERO CROSS-OVER DISTORTION

A typical rail-to-rail input stage uses two differential pairs (see Figure 59). One differential pair amplifies the input signal when the common-mode voltage is on the high end, and the other pair amplifies the input signal when the common-mode voltage is on the low end. This classic dual-differential pair topology does have a potential drawback. If the signal level moves through the range where one input stage turns off and the other input stage turns on, noticeable distortion occurs. Figure 60 shows the distortion in a typical plot of V_{OS} (voltage difference between the inverting and the noninverting input) vs. V_{CM} (input voltage).

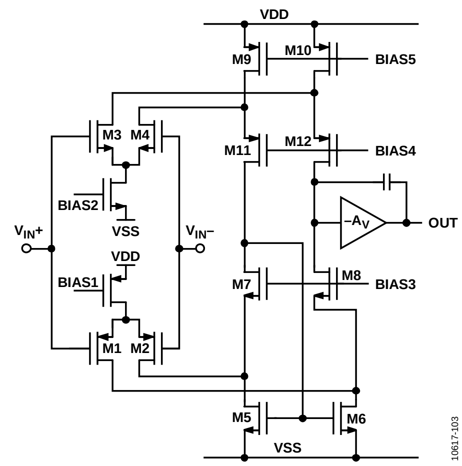


Figure 59. Typical PMOS-NMOS Rail-to-Rail Input Structure

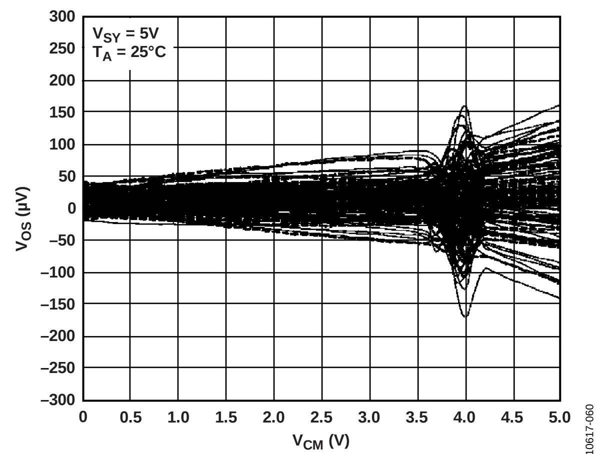


Figure 60. Typical Input Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}) Response in a Dual Differential Pair Input Stage Op Amp (Powered by a 5 V Supply; Results of Approximately 100 Units per Graph Are Displayed)

This distortion in the offset error forces the designer to live with the bump in the common-mode error or devise impractical ways to avoid the crossover distortion areas, thereby narrowing the common-mode dynamic range of the op amp.

The ADA4500-2 solves the crossover distortion problem by using an on-chip charge pump in its input structure to power the input differential pair (see Figure 61). The charge pump creates a supply voltage higher than the voltage of the supply, allowing the input stage to handle a wide range of input signal voltages without using a second differential pair. With this solution, the input voltage can vary from one supply voltage to the other with no distortion, thereby restoring the full common-mode dynamic range of the op amp.

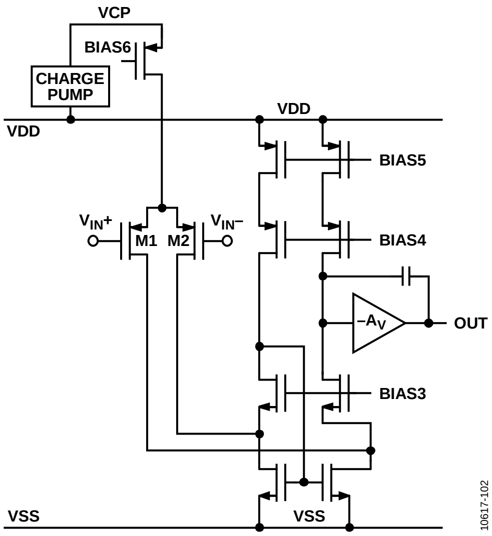


Figure 61. ADA4500-2 Input Structure

Some charge pumps are designed to run in an open-loop configuration. Disadvantages of this design include: a large ripple voltage on the output, no output regulation, slow start-up, and a large power-supply current ripple. The charge pump in this op amp uses a feedback network that includes a controllable clock driver and a differential amplifier. This topology results in a low ripple voltage; a regulated output that is robust to line, load, and process variations; a fast power-on startup; and lower ripple on the power supply current.[1] The charge pump ripple does not show up on an oscilloscope; however, it can be seen at a high frequency on a spectrum analyzer. The charge pump clock speed adjusts between 3.5 MHz (when the supply voltage is 2.7 V) to 5 MHz (at V_{SY} = 5 V). The noise and distortion are limited only by the input signal and the thermal or flicker noise.

Figure 62 shows the elimination of the crossover distortion in the ADA4500-2. This solution improves the CMRR performance tremendously. For example, if the input varies from rail to rail on a 5 V supply rail, using a part with a CMRR of 70 dB minimum, an input-referred error of 1581 µV is introduced. The ADA4500-2, with its high CMRR of 90 dB minimum (over its full operating temperature) reduces distortion to a maximum error of 158 µV with a 5 V supply. The ADA4500-2 eliminates crossover distortion without unnecessary circuitry complexity and increased cost.

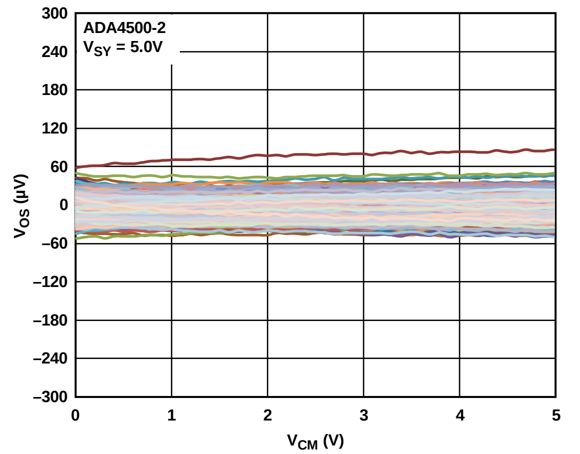


Figure 62. Charge Pump Design Eliminates Crossover Distortion

OVERLOAD RECOVERY

When the output is driven to one of the supply rails, the ADA4500-2 is in an overload condition. The ADA4500-2 recovers quickly from the overload condition. Typical op amp recovery times can be in the tens of microseconds. The ADA4500-2 typically recovers from an overload condition in 1 µs from the time the overload condition is removed until the output is active again. This is important in, for example, a feedback control system. The fast overload recovery of the ADA4500-2 greatly reduces loop delay and increases the response time of the control loop (see Figure 41 to Figure 44).

[1] Oto, D.H.; Dham, V.K.; Gudger, K.H.; Reitsma, M.J.; Gongwer, G.S.; Hu, Y.W.; Olund, J.F.; Jones, H.S.; Nieh, S.T.K.; "*High-Voltage Regulation and Process Considerations for High-Density 5 V-Only E^{2}PROM's*," *IEEE Journal of Solid-State Circuits*, Vol. SC-18, No.5, pp.532-538, October 1983.

POWER-ON CURRENT PROFILE

The ADA4500-2 powers up with a smooth current profile, with no supply current overshoot (see Figure 63). When powering up a system, spikes in the power-up current are undesirable (see Figure 64). The overshoot requires a designer to source a large enough power supply (such as a voltage regulator) to supply the peak current, even though a heavier supply is not necessary once the system is powered up. If multiple amplifiers are pulling a spike in current, the system can go into a current limit state and not power up. This is all avoided with the smooth power up of the ADA4500-2.

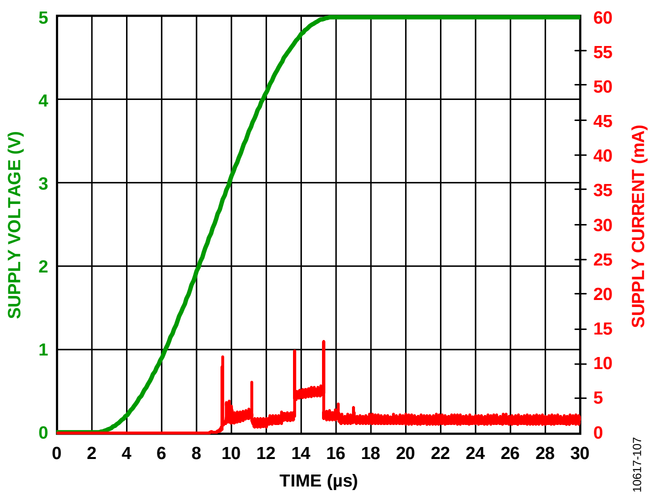


Figure 63. I_{SY} and V_{SY} vs. Time for ADA4500-2 with No Spike

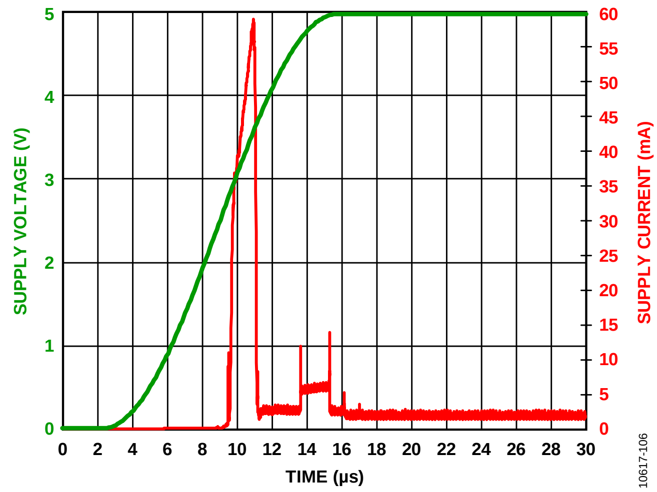


Figure 64. I_{SY} and V_{SY} vs. Time with a Power-Up Spike

For systems that are frequently switching off and on, the power-up overshoot results in excess power use. As the amplifier switches off and on, the power consumed by the large spike is repeated on each power-up, increasing the total power consumption by magnitudes. As an example, if a battery-powered sensor system periodically powers up the sensor and signal path, takes a reading, and shuts down until the next reading, the ADA4500-2 enables much longer battery life because there is no excess charge being consumed at each power-up.

APPLICATIONS INFORMATION

RESISTANCE AND CAPACITANCE SENSOR CIRCUIT

The application shown in Figure 65 generates a square-wave output in which the period is proportional to the value of R_X and C_X by Equation 1. By fixing the C_X and measuring the period of the output signal, R_X can be determined. Fixing R_X allows for the measurement of C_X.

$$Period = 4.80 \times R_X \times C_X \quad (1)$$

U1A takes advantage of the high input impedance and large rail-to-rail input dynamic range of the ADA4500-2 to measure a wide range of resistances (R_X).

U1B is used as a comparator; with the noninverting input swinging between $(1/12) \times V_{POS}$ and $(11/12) \times V_{POS}$, and the output swinging from rail to rail. Because the accuracy of the circuit depends on the propagation time through the amplifers, the fast recovery of U1B from the output overload conditions makes it ideal for this application.

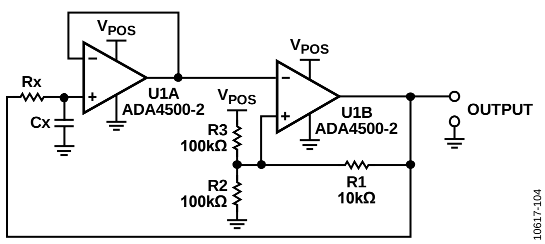


Figure 65. A Resistance/Capacitance Sensor

ADAPTIVE SINGLE-ENDED-TO-DIFFERENTIAL SIGNAL CONVERTER

The Challenge

When designing a signal path in systems that have a single voltage supply, the biggest challenge is how to represent the full range of an input signal that may have positive, zero, and negative values. By including zero in the output, the output signal must go completely to ground, which single-supply amplifiers cannot do. Converting the single-ended input signal to a differential signal (through a single-ended-to-differential signal converter circuit) allows zero to be represented as the positive and negative outputs being equal, requiring neither amplifier to go to ground.

There are other benefits of the single-ended-to-differential signal conversion, such as doubling the amplitude of the signal for better signal-to-noise ratio, rejecting common-mode noise, and driving the input of a high precision differential ADC.

In addition to converting to a differential signal, the circuit must set the common-mode dc level of its output to a level that gives the ac signal maximum swing at the load (like the input to an ADC).

Three key challenges are encountered often when designing a single-ended-to-differential signal converter circuit with a single supply:

- When the supply is limited to a single voltage, the input signal level to the circuit is generally limited to operate from ground to the supply voltage (V_{SY}). This limitation on the input dynamic range can require attenuation and/or level-shifting of the source signal before it even gets to the single-ended-to-differential signal converter. This results in reduced signal-to-noise ratio (SNR) and additional error.
- The dc part of the input signal, on which the ac signal rides, is generally not known during system operation. For example, if multiple input signals from varying sources are multiplexed into the single-ended-to-differential signal converter circuit, each one could have a different dc level. Accommodating multiple dc input levels means that the system design must compromise the maximum allowed peak voltage of the ac part of the input so that it does not clip against the rails.
- The system processor does not know what the dc level is of the original signal so it cannot make adjustments accordingly.

The Solution

These challenges are solved with the adaptive single-ended to differential converter shown in Figure 66. This circuit operates off a single supply from 2.7 V to 5.5 V, it automatically adjusts the dc common mode of the output to a desired level, and it provides the ability to measure the dc component of the input signal. This circuit uses two voltage sources: a positive supply rail (V_{SY}) and a reference voltage (V_{REF}). U1A buffers the input signal, while U1B integrates that signal and feeds the integrated (dc) voltage back to U1A to center the output signal on V_{REF}. Resistors R10 and R11 are set to equal the impedance of the resistors R8 and R9 for a matched ac response and for balancing the effects of the bias current.

The input frequency can range from 10 Hz to 1 MHz. Peak-to-peak amplitude of the input signal can be as large as V_{SY} − 100 mV. The dc common mode (V_{CM}) of the input signal can be as high as $+1.5 \times V_{SY}$ and $-0.5 \times V_{SY}$; therefore, a system with a +5 V supply voltage can take a common mode from as high as +7.5 V and as low as −2.5 V with a signal amplitude of 5 V p-p. The wide range of V_{CM} above and below ground, along with a signal amplitude as large as the supply, eliminates the need to reduce the amplitude of the input signal and sacrifice SNR. When measuring both the ac and the dc parts of the signal, a capacitor cannot be in the signal path. Figure 66 shows examples of the voltage ranges of the single-ended-to-differential signal converter circuit.

Besides converting the ac signal from single-ended to differential, this circuit separates the ac and dc part of the input signal and automatically adjusts the common-mode dc level of the output signal to the same voltage as V_{REF}. The output signal is then a differential version of the input signal with its common-mode voltage set to an optimal value (such as, ½ the full-scale input range to the ADC). The noninverted ac part of the signal is output at OUTP, and the inverted ac signal is output at OUTN. The differential output signal (OUTP to OUTN) is centered on the voltage applied to REF. In this design, R3 and R4 set REF to ½V_{POS} for maximum signal peak-to-peak swing; however, these resistors can be eliminated, and the REF input can be driven from an external source, such as a reference or the output of a digital-to-analog converter (DAC).

The dc common-mode part of the input signal (V_{DC}) was measured using the voltage applied at REF and the voltage measured at the feedback (FB) output using Equation 2. With V_{CM} of the input signal known to the system, it can respond appropriately to, for example, a situation when the common mode is getting too close to the rails.

$$V_{DC} = (2 \times FB) - (REF) \quad (2)$$

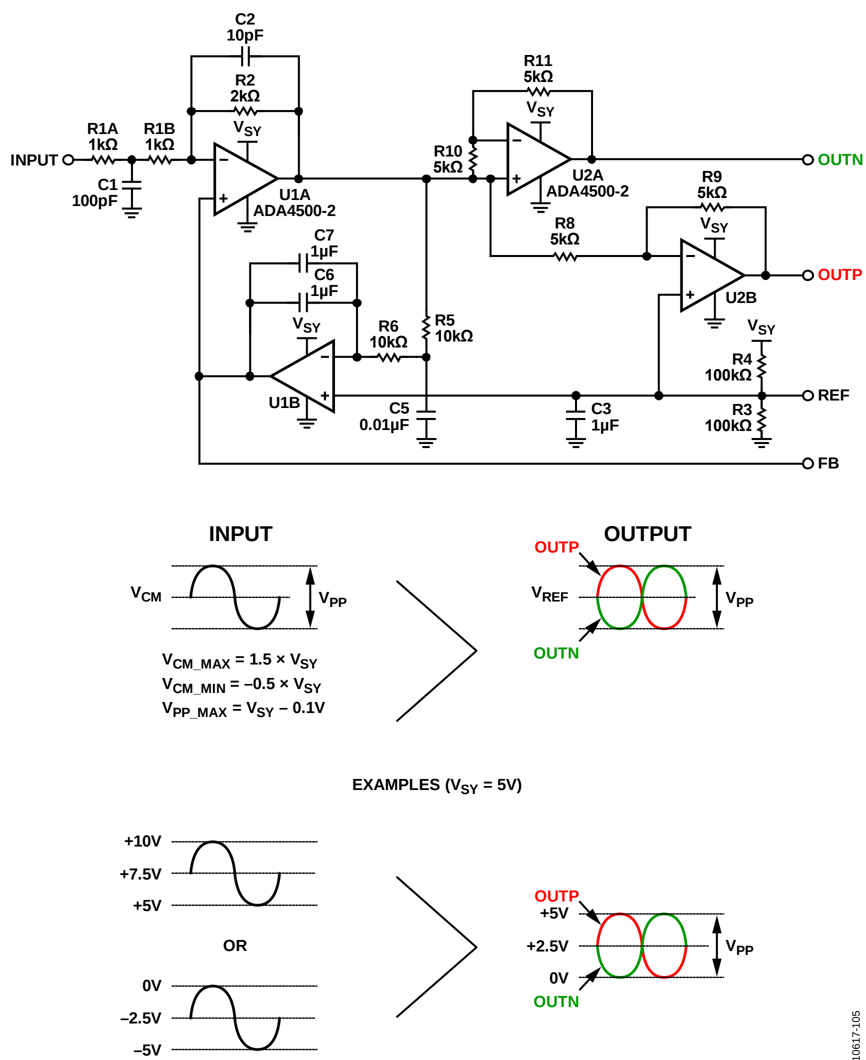


Figure 66. Single-Ended-to-Differential Conversion Circuit Separates the AC and DC Part of the Signal

OUTLINE DIMENSIONS

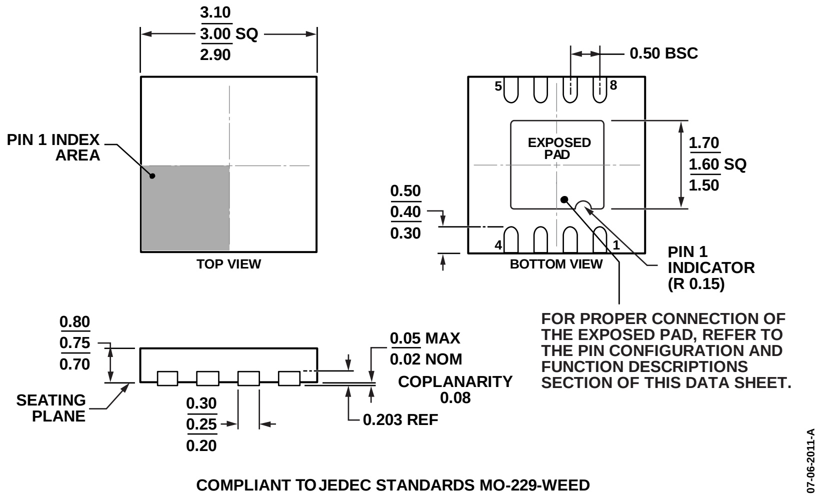


Figure 67. 8-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very, Very Thin, Dual Lead
(CP-8-12)
Dimensions shown in millimeters

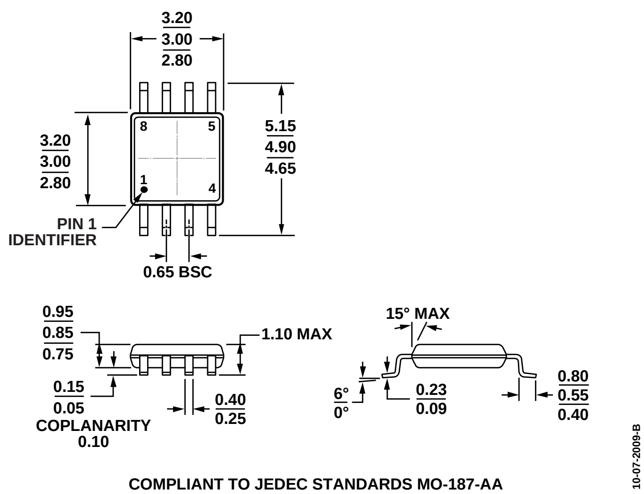


Figure 68. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature	Package Description	Package Option	Branding
ADA4500-2ACPZ-R7	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-12	A2Z
ADA4500-2ACPZ-RL	−40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-12	A2Z
ADA4500-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Z
ADA4500-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Z
ADA4500-2ARMZ-RL	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2Z

[1] Z = RoHS Compliant Part.

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