



16-Bit, 135ksps, Single-Supply ADCs with Bipolar Analog Input Range

General Description

The MAX1179/MAX1187/MAX1189 16-bit, low-power, successive-approximation analog-to-digital converters (ADCs) feature automatic power-down, a factory-trimmed internal clock, and a 16-bit wide parallel interface. The devices operate from a single +4.75V to +5.25V analog supply and feature a separate digital supply input for direct interface with +2.7V to +5.25V digital logic.

The MAX1179 accepts a bipolar input voltage range of $\pm 5V$. The MAX1187 accepts an analog input voltage range from 0 to +10V, while the MAX1189 accepts a bipolar analog input voltage range of $\pm 10V$. All devices consume only 23mW at a sampling rate of 135ksps when using an external reference and 29mW when using the internal +4.096V reference. AutoShutdown™ reduces supply current to 0.4mA at 10ksps. The MAX1179/MAX1187/MAX1189 are ideal for high-performance, battery-powered data-acquisition applications. Excellent AC performance (THD = -100dB) and DC accuracy (± 2 LSB INL) make the MAX1179/MAX1187/MAX1189 ideal for industrial process control, instrumentation, and medical applications.

The MAX1179/MAX1187/MAX1189 are available in a 28-pin TSSOP package and are fully specified over the -40°C to +85°C extended temperature range and the 0°C to +70°C commercial temperature range.

Applications

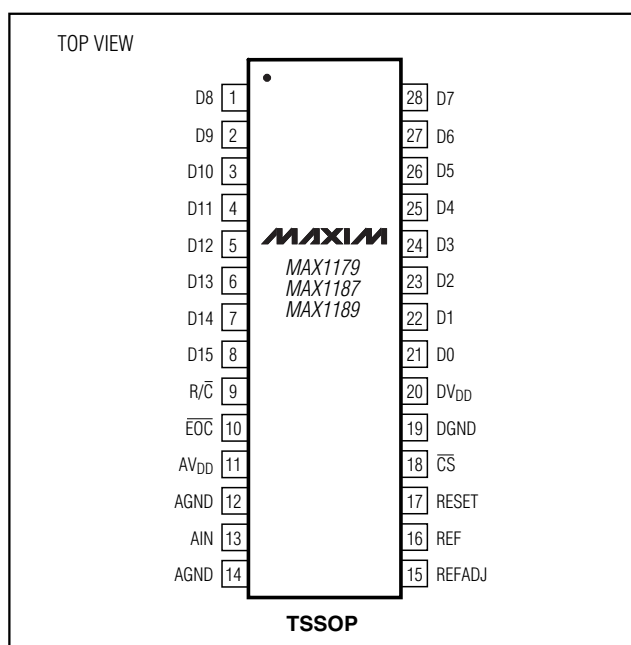
Temperature Sensing and Monitoring
Industrial Process Control
I/O Modules
Data-Acquisition Systems
Precision Instrumentation

AutoShutdown is a trademark of Maxim Integrated Products, Inc.

Features

- ◆ Analog Input Voltage Range: $\pm 10V$, $\pm 5V$, or 0 to 10V
- ◆ 16-Bit Wide Parallel Interface
- ◆ Single +4.75V to +5.25V Analog Supply Voltage
- ◆ Interfaces with +2.7V to +5.25V Digital Logic
- ◆ ± 2 LSB INL (max)
- ◆ ± 1 LSB DNL (max)
- ◆ Low Supply Current (MAX1189)
5.3mA (External Reference)
6.2mA (Internal Reference)
5 μ A AutoShutdown Mode
- ◆ Small Footprint
28-Pin TSSOP Package

Pin Configuration



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	INPUT VOLTAGE RANGE	INL (LSB)
MAX1179ACUI	0°C to +70°C	28 TSSOP	$\pm 5V$	± 2
MAX1179BCUI	0°C to +70°C	28 TSSOP	$\pm 5V$	± 2

Ordering Information continued at end of data sheet.



Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX1179/MAX1187/MAX1189

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ABSOLUTE MAXIMUM RATINGS

AVDD to AGND-0.3V to +6V
 DVDD to DGND-0.3V to +6V
 AGND to DGND-0.3V to +0.3V
 AIN to AGND-16.5V to +16.5V
 REF, REFADJ to AGND-0.3V to (AVDD + 0.3V)
 CS, R/C, RESET to DGND-0.3V to +6V
 D-, EOC to DGND-0.3V to (DVDD + 0.3V)
 Maximum Continuous Current Into Any Pin 50mA

Continuous Power Dissipation (TA = +70°C)
 28-Pin TSSOP (derate 12.8mW/°C above +70°C) 1026mW
 Operating Temperature Range
 MAX11__CUI 0°C to +70°C
 MAX11__EUI-40°C to +85°C
 Storage Temperature Range-65°C to +150°C
 Junction Temperature+150°C
 Lead Temperature (soldering, 10s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AVDD = DVDD = +5V ±5%, external reference = +4.096V, CREF = 10μF, CREFADJ = 0.1μF, VREFADJ = AVDD, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution	RES			16			Bits
Differential Nonlinearity	DNL	No missing codes over temperature	MAX11_ _A	-1	+1		LSB
			MAX11_ _B	-1.0	+1.5		
			MAX11_ _C	-1	+2		
Integral Nonlinearity	INL	MAX11_ _A		-2	+2		LSB
		MAX11_ _B		-2	+2		
		MAX11_ _C		-4	+4		
Transition Noise		RMS noise, external reference		0.6			LSBRMS
		Internal reference		0.75			
Offset Error				-10	0	+10	mV
Gain Error					0	±0.2	%FSR
Offset Drift					16		μV/°C
Gain Drift					±1		ppm/°C
AC ACCURACY (fIN = 1kHz, VAIN = full range, 135ksps)							
Signal-to-Noise Plus Distortion	SINAD			86	90		dB
Signal-to-Noise Ratio	SNR			87	91		dB
Total Harmonic Distortion	THD				-100	-92	dB
Spurious-Free Dynamic Range	SFDR			92	103		dB
ANALOG INPUT							
Input Range	VAIN	MAX1179		-5	+5		V
		MAX1187		0	+10		
		MAX1189		-10	+10		
Input Resistance	RAIN	MAX1179/MAX1187	Normal operation	5.3	6.9	9.2	kΩ
		MAX1179	Shutdown mode	3			
		MAX1177	Shutdown mode	5.3			
		MAX1189	Normal operation	7.8	10	13.0	
			Shutdown mode	6			

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MAX1179/MAX1187/MAX1189

ELECTRICAL CHARACTERISTICS (continued)

(AVDD = DVDD = +5V ±5%, external reference = +4.096V, CREF = 10μF, CREFADJ = 0.1μF, VREFADJ = AVDD, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	IAIN	MAX1179, Normal operation	-1.8		+0.4	mA
		-5V ≤ VAIN ≤ +5V Shutdown mode	-1.8		+1.8	
		MAX1187, Normal/shutdown mode	-0.1		+2.0	
		0 ≤ VAIN ≤ +10V				
		MAX1189, Normal operation	-1.8		+1.2	
		-10V ≤ VAIN ≤ +10V Shutdown mode	-1.8		+1.8	
Input Current Step at Power-Up	IPU	MAX1179, VAIN = +5V, shutdown mode to operating mode		1	1.4	mA
		MAX1189, VAIN = +10V, shutdown mode to operating mode		0.5	0.7	
Input Capacitance	CIN			10		pF
INTERNAL REFERENCE						
REF Output Voltage	VREF		4.056	4.096	4.136	V
REF Output Tempco				±35		ppm/°C
REF Short-Circuit Current	IREF(SC)			±10		mA
EXTERNAL REFERENCE						
REF and REFADJ Input Voltage Range			3.8		4.2	V
REFADJ Buffer Disable Threshold			AVDD - 0.4		AVDD - 0.1	V
REF Input Current	IREF	Normal mode, fSAMPLE = 135ksps		60	100	μA
		Shutdown mode (Note 1)		±0.1	±10	
REFADJ Input Current	IREFADJ	REFADJ = AVDD		16		μA
DIGITAL INPUTS/OUTPUTS						
Output High Voltage	VOH	ISOURCE = 0.5mA, DVDD = +2.7V to +5.25V, AVDD = +5.25V	DVDD - 0.4			V
Output Low Voltage	VOL	ISINK = 1.6mA, DVDD = +2.7V to +5.25V, AVDD = +5.25V			0.4	V
Input High Voltage	VIH		0.7 × DVDD			V
Input Low Voltage	VIL				0.3 × DVDD	V
Input Leakage Current		Digital input = DVDD or 0V	-1		+1	μA
Input Hysteresis	VHYST			0.2		V
Input Capacitance	CIN			15		pF
Three-State Output Leakage	IOZ				±10	μA
Three-State Output Capacitance	COZ			15		pF

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ELECTRICAL CHARACTERISTICS (continued)

(AVDD = DVDD = +5V ±5%, external reference = +4.096V, CREF = 10μF, CREFADJ = 0.1μF, VREFADJ = AVDD, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Analog Supply Voltage	AVDD		4.75		5.25	V
Digital Supply Voltage	DVDD		2.70		5.25	V
Analog Supply Current	IAVDD	External reference, 135ksps	MAX1187		2.9	mA
			MAX1179/MAX1189		4.0	
		Internal reference, 135ksps	MAX1187		3.8	
			MAX1179/MAX1189		5.2	
Shutdown Supply Current	ISHDN	Shutdown mode, IAVDD + IDVDD (Note 1), digital input = DVDD or 0V		0.5	5	μA
		Standby mode		3.7		mA
Digital Supply Current	IDVDD				0.75	mA
Power-Supply Rejection		AVDD = DVDD = +4.75V to +5.25V		3.5		LSB

TIMING CHARACTERISTICS (Figures 1 and 2)

(AVDD = +5V ±5V, DVDD = +2.7V to AVDD, external reference = +4.096V, CREF = 10μF, CREFADJ = 0.1μF, VREFADJ = AVDD, CLOAD = 20pF, TA = TMIN to TMAX.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Sampling Rate	fSAMPLE(MAX)				135	ksps
Acquisition Time	tACQ		2			μs
Conversion Time	tCONV				4.7	μs
CS Pulse Width High	tCSH	(Note 2)	40			ns
CS Pulse Width Low	tCSL	(Note 2)	DVDD = +4.75V to +5.25V	40		ns
			DVDD = +2.7V to +5.25V	60		
R/C to CS Fall Setup Time	tDS		0			ns
R/C to CS Fall Hold Time	tDH	DVDD = +4.75V to +5.25V	40			ns
		DVDD = +2.7V to +5.25V	60			
CS to Output Data Valid	tDO	DVDD = +4.75V to +5.25V			40	ns
		DVDD = +2.7V to +5.25V			80	
EOC Fall to CS Fall	tDV		0			ns
CS Rise to EOC Rise	tEOC	DVDD = +4.75V to +5.25V			40	ns
		DVDD = +2.7V to +5.25V			80	
Bus Relinquish Time	tBR	DVDD = +4.75V to +5.25V			40	ns
		DVDD = +2.7V to +5.25V			80	

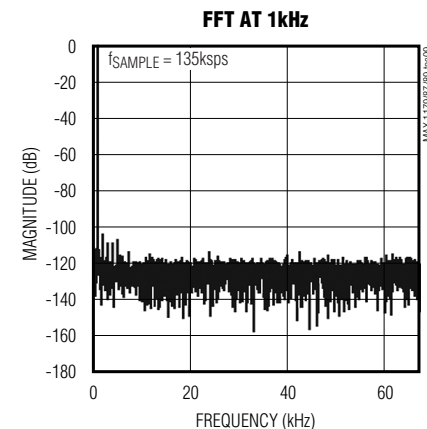
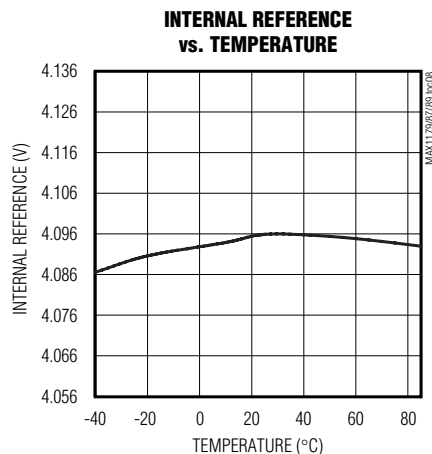
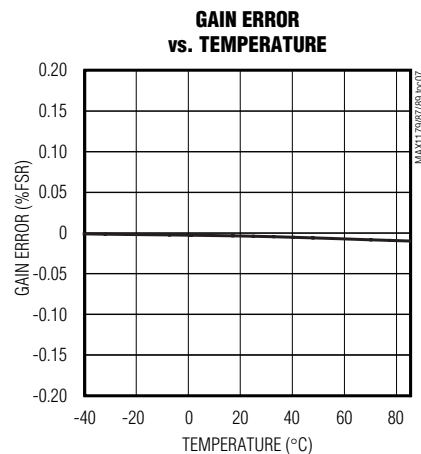
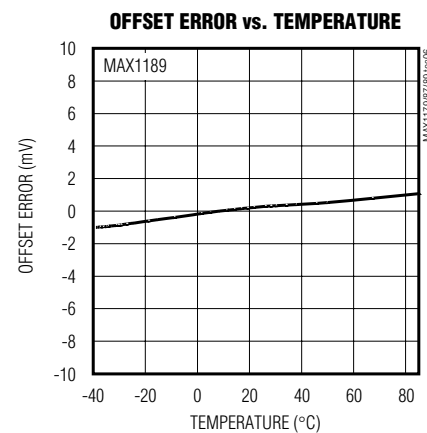
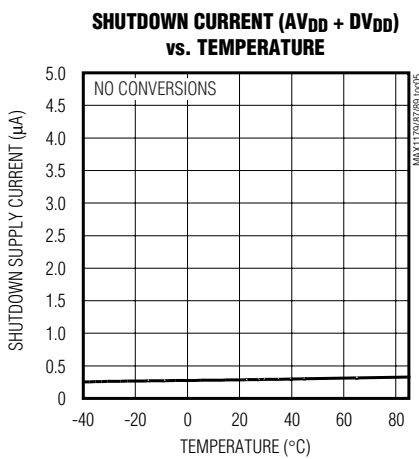
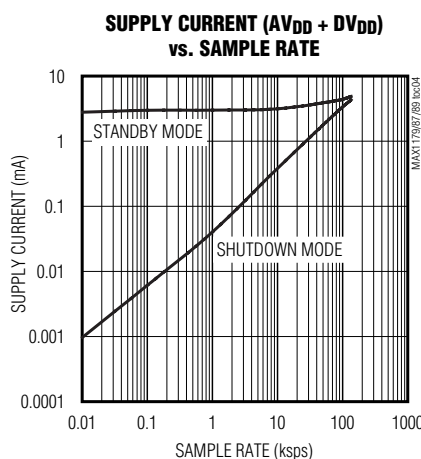
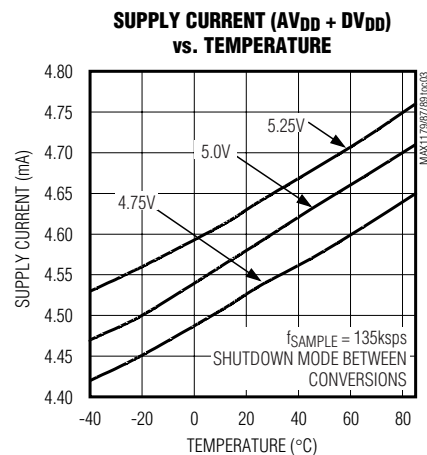
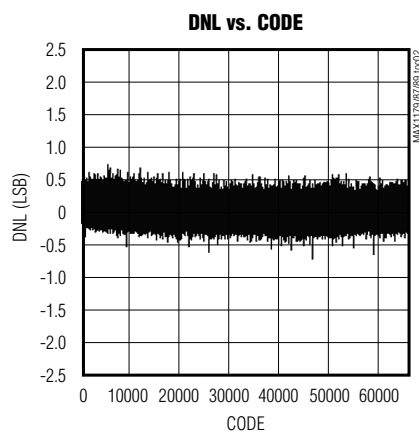
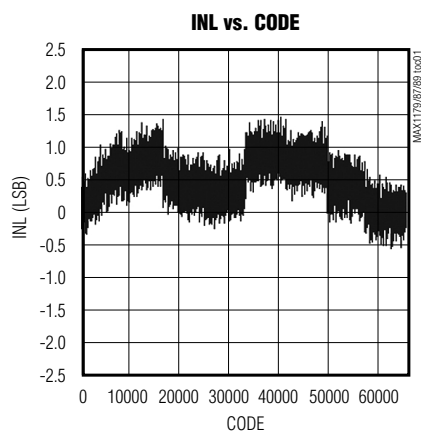
Note 1: Maximum specification is limited by automated test equipment.

Note 2: To ensure best performance, finish reading the data and wait tBR before starting a new acquisition.

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Typical Operating Characteristics

($AV_{DD} = DV_{DD} = +5V$, external reference = $+4.096V$, $C_{REF} = 10\mu F$, $C_{REFADJ} = 0.1\mu F$, $V_{REFADJ} = AV_{DD}$, $C_{LOAD} = 20pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Typical Application Circuit)

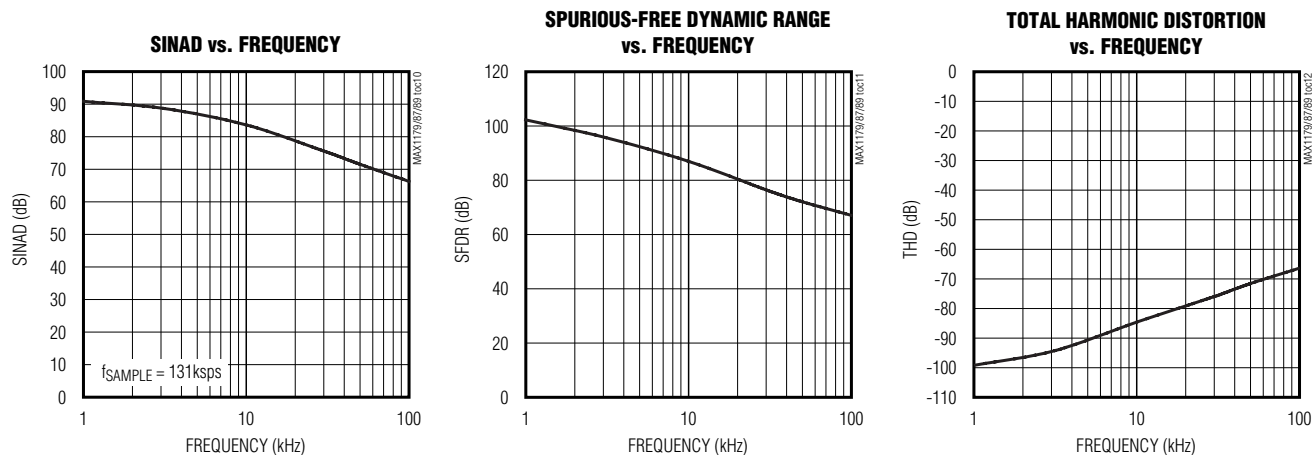


MAX1179/MAX1187/MAX1189

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Typical Operating Characteristics (continued)

($AV_{DD} = DV_{DD} = +5V$, external reference = +4.096V, $C_{REF} = 10\mu F$, $C_{REFADJ} = 0.1\mu F$, $V_{REFADJ} = AV_{DD}$, $C_{LOAD} = 20pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Typical Application Circuit)



Pin Description

PIN	NAME	FUNCTION
1	D8	Three-State Digital Data Output
2	D9	Three-State Digital Data Output
3	D10	Three-State Digital Data Output
4	D11	Three-State Digital Data Output
5	D12	Three-State Digital Data Output
6	D13	Three-State Digital Data Output
7	D14	Three-State Digital Data Output
8	D15	Three-State Digital Data Output (MSB)
9	$R/\overline{C}$	Read/ $\overline{C}$ onvert Input. Power up and place the MAX1179/MAX1187/MAX1189 in acquisition mode by holding $R/\overline{C}$ low during the first falling edge of $\overline{CS}$. During the second falling edge of $\overline{CS}$, the level on $R/\overline{C}$ determines whether the reference and reference buffer power down or remain on after conversion. Set $R/\overline{C}$ high during the second falling edge of $\overline{CS}$ to power down the reference and buffer, or set $R/\overline{C}$ low to leave the reference and buffer powered up. Set $R/\overline{C}$ high during the third falling edge of $\overline{CS}$ to put valid data on the bus.
10	$\overline{EOC}$	End of Conversion. $\overline{EOC}$ drives low when conversion is complete.
11	AV_{DD}	Analog Supply Input. Bypass with a $0.1\mu F$ capacitor to AGND.
12	AGND	Analog Ground. Primary analog ground (star ground).
13	AIN	Analog Input
14	AGND	Analog Ground. Connect pin 14 to pin 12.

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Pin Description (continued)

PIN	NAME	FUNCTION
15	REFADJ	Reference Buffer Output. Bypass REFADJ with a 0.1 μ F capacitor to AGND for internal reference mode. Connect REFADJ to AVDD to select external reference mode.
16	REF	Reference Input/Output. Bypass REF with a 10 μ F capacitor to AGND. REF is the external reference input when in external reference mode.
17	RESET	Reset Input. Logic high resets the device.
18	$\overline{CS}$	Convert Start. The first falling edge of $\overline{CS}$ powers up the device and enables acquisition when R/ $\overline{C}$ is low. The second falling edge of $\overline{CS}$ starts conversion. The third falling edge of $\overline{CS}$ loads the result onto the bus when R/ $\overline{C}$ is high.
19	DGND	Digital Ground
20	DVDD	Digital Supply Voltage. Bypass with a 0.1 μ F capacitor to DGND.
21	D0	Three-State Digital Data Output (LSB)
22	D1	Three-State Digital Data Output
23	D2	Three-State Digital Data Output
24	D3	Three-State Digital Data Output
25	D4	Three-State Digital Data Output
26	D5	Three-State Digital Data Output
27	D6	Three-State Digital Data Output
28	D7	Three-State Digital Data Output

MAX1179/MAX1187/MAX1189

Detailed Description

Converter Operation

The MAX1179/MAX1187/MAX1189 use a successive-approximation (SAR) conversion technique with an inherent track-and-hold (T/H) stage to convert an analog input into a 16-bit digital output. Parallel outputs provide a high-speed interface to microprocessors (μ Ps). The *Functional Diagram* at the end of the data sheet shows a simplified internal architecture of the MAX1179/MAX1187/MAX1189. Figure 3 shows a typical application circuit for the MAX1179/MAX1187/MAX1189.

Analog Input

Input Scaler

The MAX1179/MAX1187/MAX1189 have an input scaler which allows conversion of true bipolar input voltages and input voltages greater than the power supply, while operating from a single +5V analog supply. The input scaler attenuates and shifts the analog input to match the input range of the internal DAC. The MAX1179 input voltage range is $\pm 5V$, while the MAX1189 input voltage

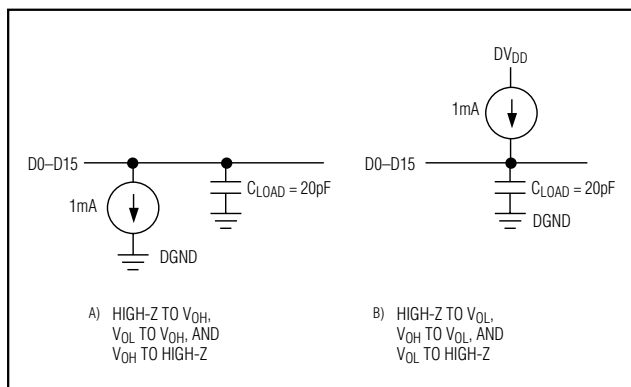


Figure 1. Load Circuits

range is $\pm 10V$. The MAX1187 has a unipolar input voltage range of 0 to +10V. Figure 4 shows the equivalent input circuit of the MAX1179/MAX1187/MAX1189. This circuit limits the current going into or out of AIN to less than 1.8mA.

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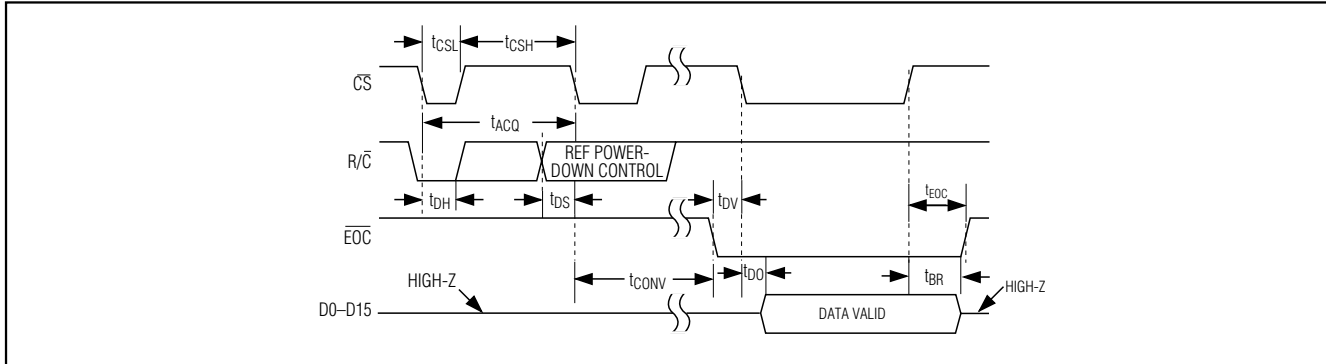


Figure 2. MAX1179/MAX1187/MAX1189 Timing Diagram

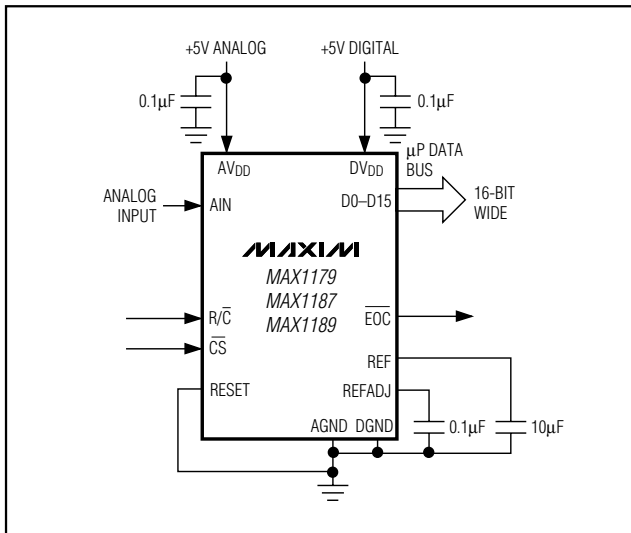


Figure 3. Typical Application Circuit for the MAX1179/MAX1187/MAX1189

Track and Hold (T/H)

In track mode, the internal hold capacitor acquires the analog signal (see Figure 4). In hold mode, the T/H switches open and the capacitive DAC samples the analog input. During the acquisition, the analog input (AIN) charges capacitor C_{HOLD} . The acquisition ends on the second falling edge of $\overline{CS}$. At this instant, the T/H switches open. The retained charge on C_{HOLD} represents a sample of the input. In hold mode, the capacitive DAC adjusts during the remainder of the conversion time to restore node T/H OUT to zero within the limits of a 16-bit resolution. Force $\overline{CS}$ low to put valid data on the bus after conversion is complete.

Power-Down Modes

Select standby mode or shutdown mode with $\overline{R/C}$ during the second falling edge of $\overline{CS}$ (see *Selecting Standby or Shutdown Mode* section). The MAX1179/MAX1187/MAX1189 automatically enter either standby mode (reference and buffer on) or shutdown (reference and buffer off) after each conversion depending on the status of $\overline{R/C}$ during the second falling edge of $\overline{CS}$.

Internal Clock

The MAX1179/MAX1187/MAX1189 generate an internal conversion clock to free the microprocessor from the burden of running the SAR conversion clock. Total conversion time after entering hold mode (second falling edge of $\overline{CS}$) to end-of-conversion (EOC) falling is 4.7µs (max).

Applications Information

Starting a Conversion

$\overline{CS}$ and $\overline{R/C}$ control acquisition and conversion in the MAX1179/MAX1187/MAX1189 (see Figure 2). The first falling edge of $\overline{CS}$ powers up the device and puts it in acquire mode if $\overline{R/C}$ is low. The convert start ($\overline{CS}$) is ignored if $\overline{R/C}$ is high. The MAX1179/MAX1187/MAX1189 need at least 12ms ($C_{REFADJ} = 0.1\mu\text{F}$, $C_{REF} = 10\mu\text{F}$) for the internal reference to wake up and settle before starting the conversion, if powering up from shutdown. Reset the MAX1179/MAX1187/MAX1189 by toggling RESET with $\overline{CS}$ high. The next falling edge of $\overline{CS}$ begins acquisition.

Selecting Standby or Shutdown Mode

The MAX1179/MAX1187/MAX1189 have a selectable standby or low-power shutdown mode. In standby mode, the ADC's internal reference and reference buffer do not power down between conversions, eliminating the need to wait for the reference to power up before performing the next conversion. Shutdown mode powers down the reference and reference buffer after

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MAX1179/MAX1187/MAX1189

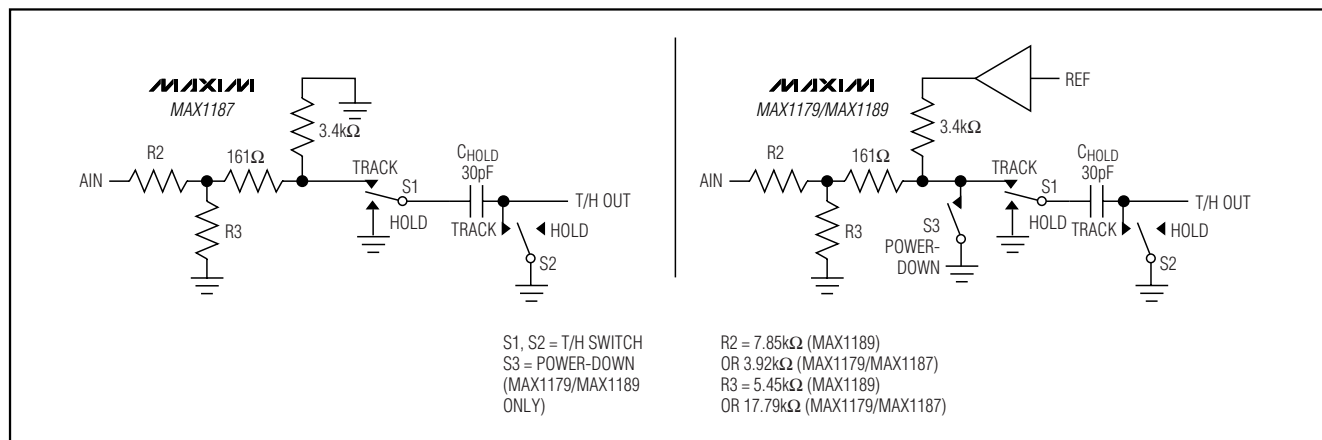


Figure 4. Equivalent Input Circuit

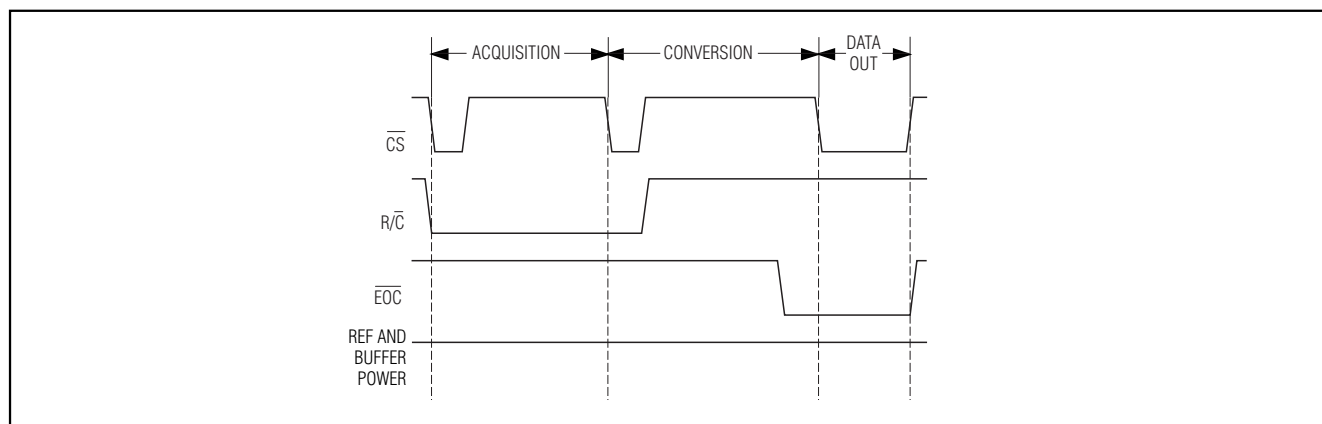


Figure 5. Selecting Standby Mode

completing a conversion. The reference and reference buffer require a minimum of 12ms ($C_{REFADJ} = 0.1\mu\text{F}$, $C_{REF} = 10\mu\text{F}$) to power up and settle from shutdown.

The state of $R/\overline{C}$ during the second falling edge of $\overline{CS}$ selects which power-down mode the MAX1179/MAX1187/MAX1189 enters upon conversion completion. Holding $R/\overline{C}$ low causes the MAX1179/MAX1187/MAX1189 to enter standby mode. The reference and buffer are left on after the conversion completes. $R/\overline{C}$ high causes the MAX1179/MAX1187/MAX1189 to enter shutdown mode and power down the reference and

buffer after conversion (see Figures 5 and 6). Set the voltage at REF high during the second falling edge of $\overline{CS}$ to realize the lowest current operation.

Standby Mode

While in standby mode, the supply current is less than 3.7mA (typ). The next falling edge of $\overline{CS}$ with $R/\overline{C}$ low causes the MAX1179/MAX1187/MAX1189 to exit standby mode and begin acquisition. The reference and reference buffer remain active to allow quick turn-on time.

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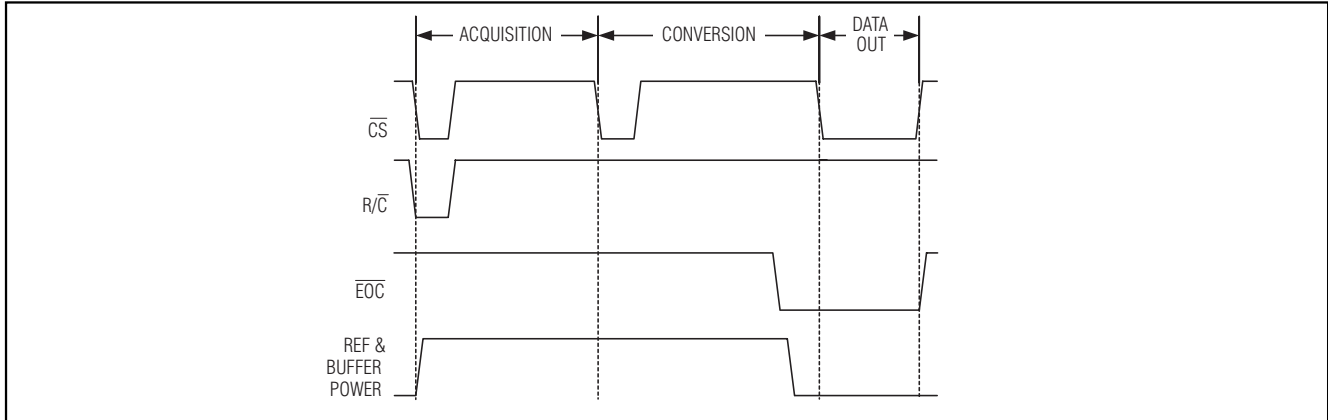


Figure 6. Selecting Shutdown Mode

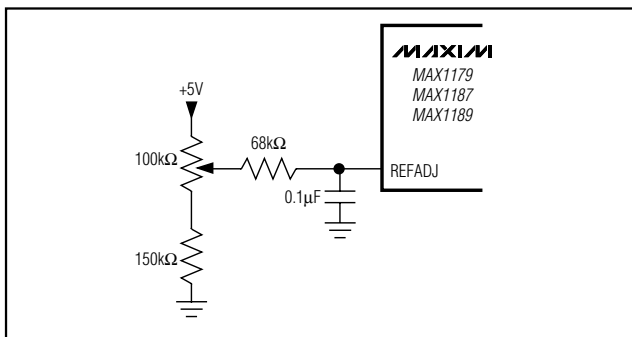


Figure 7. MAX1179/MAX1187/MAX1189 Reference Adjust Circuit

Shutdown Mode

In shutdown mode, the reference and reference buffer shut down between conversions. Shutdown mode reduces supply current to 0.5μA (typ) immediately after the conversion. The next falling edge of $\overline{CS}$ with $R/\overline{C}$ low causes the reference and buffer to wake up and enter acquisition mode. To achieve 16-bit accuracy, allow 12ms ($C_{REFADJ} = 0.1\mu\text{F}$, $C_{REF} = 10\mu\text{F}$) for the internal reference to wake up.

Internal and External Reference

Internal Reference

The internal reference of the MAX1179/MAX1187/MAX1189 is internally buffered to provide +4.096V output at REF. Bypass REF to AGND and REFADJ to AGND with 10μF and 0.1μF, respectively.

Sink or source current at REFADJ to make fine adjustments to the internal reference. The input impedance of REFADJ is nominally 5kΩ. Use the circuit of Figure 7 to adjust the internal reference to ±1.5%.

External Reference

An external reference can be placed at either the input (REFADJ) or the output (REF) of the MAX1179/MAX1187/MAX1189's internal buffer amplifier. Using the buffered REFADJ input makes buffering the external reference unnecessary. The input impedance of REFADJ is typically 5kΩ. The internal buffer output must be bypassed at REF with a 10μF capacitor.

Connect REFADJ to AVDD to disable the internal buffer. Directly drive REF using an external 3.8V to 4.2V reference. During conversion, the external reference must be able to drive 100μA of DC load current and have an output impedance of 10Ω or less.

For optimal performance, buffer the reference through an op amp and bypass REF with a 10μF capacitor. Consider the MAX1179/MAX1187/MAX1189's equivalent input noise (0.6LSB) when choosing a reference.

Reading the Conversion Result

$\overline{EOC}$ flags the microprocessor when a conversion is complete. The falling edge of $\overline{EOC}$ signals that the data is valid and ready to be output to the bus. D0–D15 are the parallel outputs of the MAX1179/MAX1187/MAX1189. These three-state outputs allow for direct connection to a microcontroller I/O bus. The outputs remain high-impedance during acquisition and conversion. Data is loaded onto the bus with the third falling edge of $\overline{CS}$ with $R/\overline{C}$ high (after t_{DO}). Bringing $\overline{CS}$ high forces the output bus back to high impedance. The MAX1179/MAX1187/MAX1189 then wait for the next falling edge of $\overline{CS}$ to start the next conversion cycle (see Figure 2).

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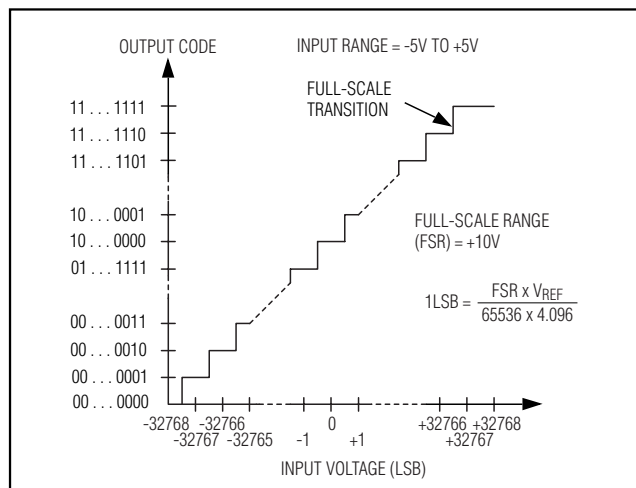


Figure 8. MAX1179 Transfer Function

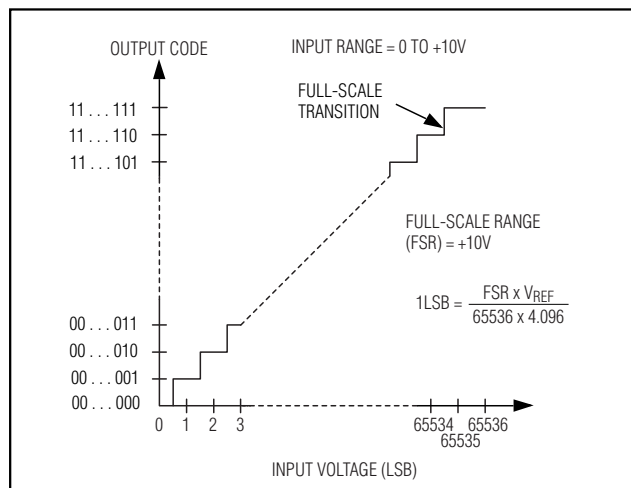


Figure 9. MAX1187 Transfer Function

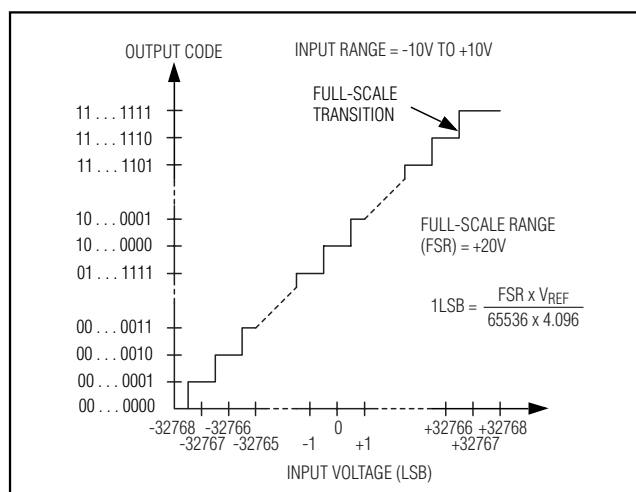


Figure 10. MAX1189 Transfer Function

Transfer Function

Figures 8, 9, and 10 show the MAX1179/MAX1187/MAX1189's output transfer functions. The MAX1179 and MAX1189 outputs are coded in offset binary, while the MAX1187 is coded in standard binary.

Input Buffer

Most applications require an input buffer amplifier to achieve 16-bit accuracy and prevent loading the source. Switch the channels immediately after acquisition, rather than near the end of or after a conversion when the input signal is multiplexed. This allows more time for the input buffer amplifier to respond to a large

step-change in input signal. The input amplifier must have a high enough slew rate to complete the required output voltage change before the beginning of the acquisition time. Figure 11 shows an example of this circuit using the MAX427.

Figures 12a and 12b show how the MAX1179 and MAX1189 analog input current varies depending on whether the chip is operating or powered down. The part is fully powered down between conversions if the voltage at R/C is set high during the second falling edge of $\overline{CS}$. The input current abruptly steps to the powered up value at the start of acquisition. This step in the input current can disrupt the ADC input, depending on the driving circuit's output impedance at high frequencies. If the driving circuit cannot fully settle by the end of acquisition time, the accuracy of the system can be compromised. To avoid this situation, increase the acquisition time, use a driving circuit that can settle within t_{ACQ} , or leave the MAX1179/MAX1189 powered up by setting the voltage at R/C low during the second falling edge of $\overline{CS}$.

Layout, Grounding, and Bypassing

For best performance, use printed circuit (PC) boards. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital ground planes with only one point connecting the two ground systems (analog and digital) as close to the device as possible.

Route digital signals far away from sensitive analog and reference inputs. If digital lines must cross analog lines, do so at right angles to minimize coupling digital noise

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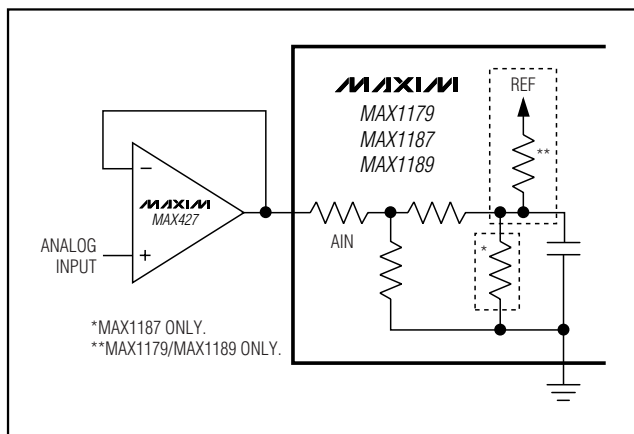


Figure 11. MAX1179/MAX1187/MAX1189 Fast-Settling Input Buffer

onto the analog lines. If the analog and digital sections share the same supply, isolate the digital and analog supply by connecting them with a low value (10Ω) resistor or ferrite bead.

The ADC is sensitive to high-frequency noise on the AV_{DD} supply. Bypass AV_{DD} to AGND with a $0.1\mu\text{F}$ capacitor in parallel with a $1\mu\text{F}$ to $10\mu\text{F}$ low-ESR capacitor with the smallest capacitor closest to the device. Keep capacitor leads short to minimize stray inductance.

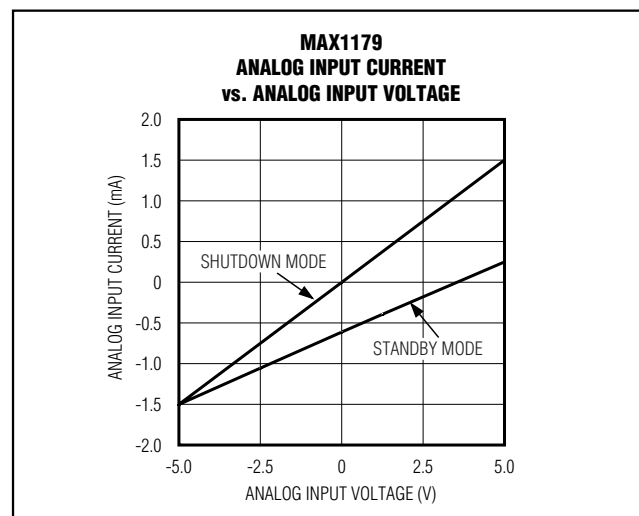


Figure 12a. MAX1179 Analog Input Current

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1179/MAX1187/MAX1189 are measured using the endpoint method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step-width and the ideal value of 1LSB. A DNL error specification of 1LSB guarantees no missing codes and a monotonic transfer function.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$\text{SNR} = ((6.02 \times N) + 1.76)\text{dB}$$

where $N = 16$ bits.

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter,

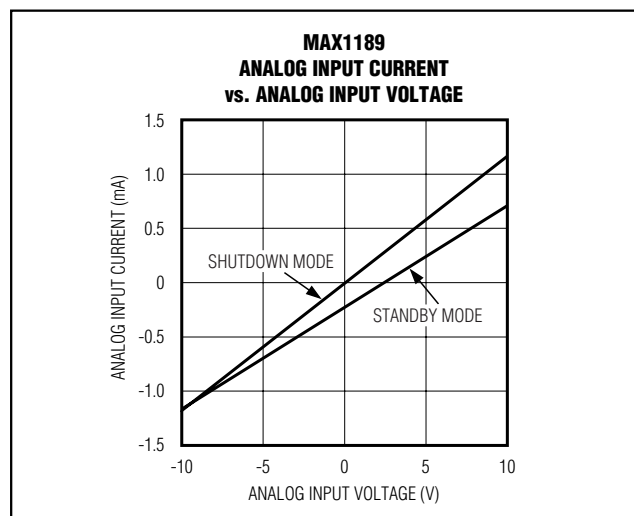


Figure 12b. MAX1189 Analog Input Current

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etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals.

$$\text{SINAD}(\text{db}) = 20 \times \log \left(\frac{\text{Signal}_{\text{RMS}}}{(\text{Noise} + \text{Distortion})_{\text{RMS}}} \right)$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$\text{ENOB} = \left(\frac{\text{SINAD} - 1.76}{6.02} \right)$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log \left(\frac{\left(\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2} \right)}{V_1} \right)$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest frequency component.

Chip Information

TRANSISTOR COUNT: 15,383

PROCESS: BiCMOS

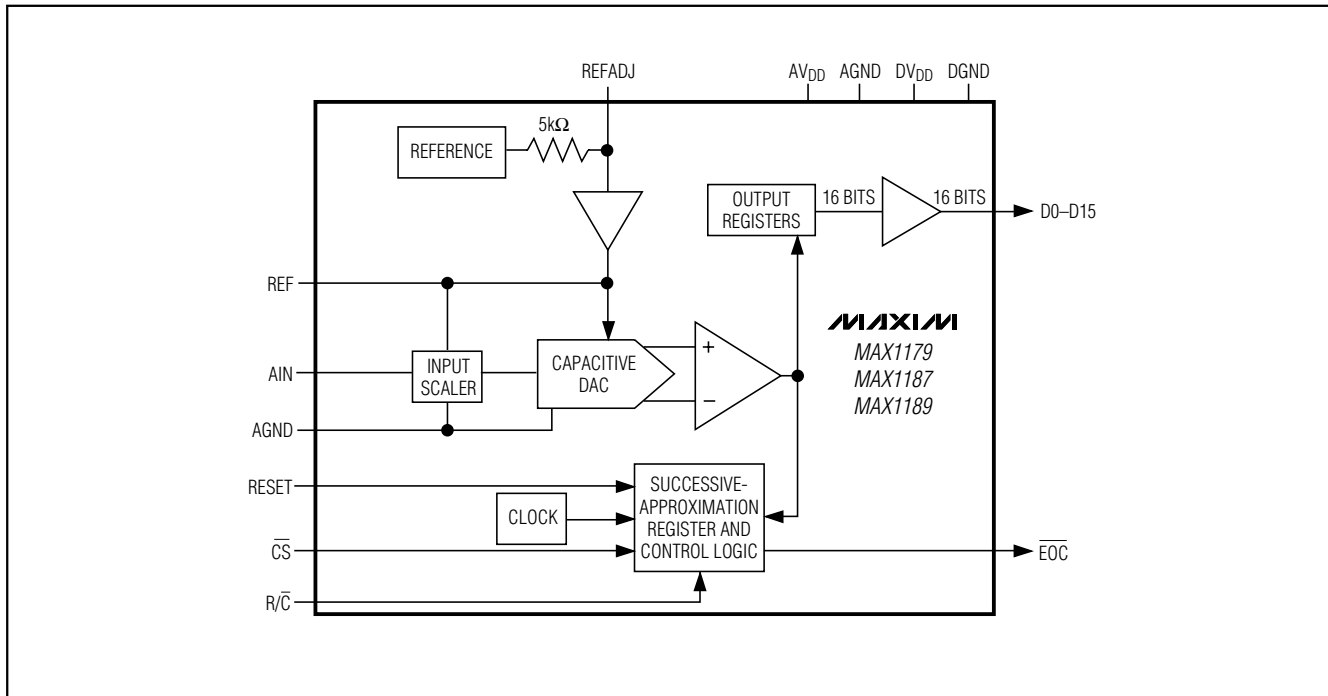
Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INPUT VOLTAGE RANGE	INL (LSB)
MAX1179CCUI	0°C to +70°C	28 TSSOP	±5V	±4
MAX1179AEUI	-40°C to +85°C	28 TSSOP	±5V	±2
MAX1179BEUI	-40°C to +85°C	28 TSSOP	±5V	±2
MAX1179CEUI	-40°C to +85°C	28 TSSOP	±5V	±4
MAX1187 ACUI	0°C to +70°C	28 TSSOP	0 to +10V	±2
MAX1187BCUI	0°C to +70°C	28 TSSOP	0 to +10V	±2
MAX1187CCUI	0°C to +70°C	28 TSSOP	0 to +10V	±4
MAX1187AEUI	-40°C to +85°C	28 TSSOP	0 to +10V	±2
MAX1187BEUI	-40°C to +85°C	28 TSSOP	0 to +10V	±2
MAX1187CEUI	-40°C to +85°C	28 TSSOP	0 to +10V	±4
MAX1189 ACUI	0°C to +70°C	28 TSSOP	±10V	±2
MAX1189BCUI	0°C to +70°C	28 TSSOP	±10V	±2
MAX1189CCUI	0°C to +70°C	28 TSSOP	±10V	±4
MAX1189AEUI*	-40°C to +85°C	28 TSSOP	±10V	±2
MAX1189BEUI*	-40°C to +85°C	28 TSSOP	±10V	±2
MAX1189CEUI*	-40°C to +85°C	28 TSSOP	±10V	±4

*Future product—contact factory for availability.

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Functional Diagram



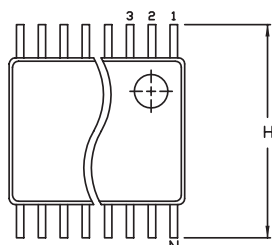
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Package Information

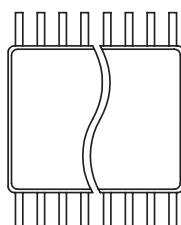
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

TSSOP 4.40mm EPS

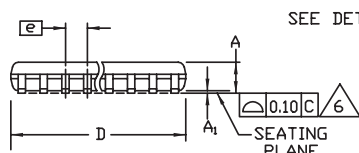
MAX1179/MAX1187/MAX1189



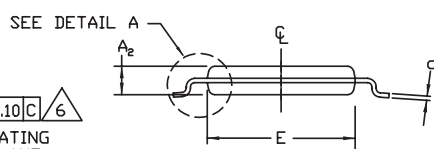
TOP VIEW



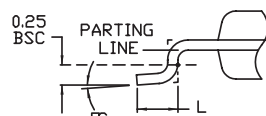
BOTTOM VIEW



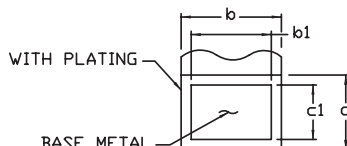
SIDE VIEW



END VIEW



DETAIL A



LEAD TIP DETAIL

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
 3. CONTROLLING DIMENSION: MILLIMETER
 4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
 5. "N" REFERS TO NUMBER OF LEADS
- THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [C-C-1]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [C-C-1] IN THE DIRECTION INDICATED

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	—	1.10	.043	—
A ₁	0.05	0.15	.002	.006
A ₂	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b ₁	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c ₁	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC	N		VARIATIONS			
			MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE:			
PACKAGE OUTLINE, TSSOP 4.40mm BODY			
APPROVAL	DOCUMENT CONTROL NO.	REV.	1/1
	21-0066	F	

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