TJA1100

100BASE-T1 PHY for Automotive Ethernet

Rev. 3 — 23 May 2017 Product data sheet

1. General description

The TJA1100 is a 100BASE-T1 compliant Ethernet PHY optimized for automotive use cases. The device provides 100 Mbit/s transmit and receive capability over a single Unshielded Twisted Pair (UTP) cable, supporting a cable length of up to at least 15 m. Optimized for automotive use cases such as IP camera links, driver assistance systems and back-bone networks, the TJA1100 has been designed to minimize power consumption and system costs, while still providing the robustness required for automotive use cases.

2. Features and benefits

2.1 Optimized for automotive use cases

- Transmitter optimized for capacitive coupling to unshielded twisted-pair cable
- Enhanced integrated PAM-3 pulse shaping for low RF emissions
- Adaptive receive equalizer optimized for automotive cable length of up to at least 15 m
- Reduced power consumption through configurable transmitter pulse amplitude adapted to cable length
- Dedicated PHY enable/disable input pin to minimize power consumption
- Low-power Sleep mode with local wake-up support
- Robust remote wake-up via the bus lines
- Gap-free supply undervoltage detection with fail-silent behavior
- EMC-optimized output driver strength for Media Independent Interface (MII) and Reduced MII (RMII)
- Diagnosis of cabling errors (shorts and opens)
- Small HVQFN-36 package for PCB space-constrained applications
- MDI pins protected against ESD to ±6kV HBM and ±6kV IEC61000-4-2
- MDI pins protected against transients in automotive environment
- Automotive-grade temperature range from −40 °C to +125 °C
- Automotive product qualification in accordance with AEC-Q100

2.2 Miscellaneous

- MII as well as RMII standard compliant interface
- Reverse MII mode for back-to-back connection of two PHYs
- 3V3 single supply operation with on-chip 1.8 V LDO regulators
- On-chip termination resistors for balanced UTP cable
- Jumbo frame support up to 16 kB
- Internal, external and remote loopback mode for diagnosis

- Bus pins short-circuit proof to battery voltage and ground (including common mode choke, 100 nF coupling capacitors)
- LED control output for link diagnosis

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1100HN	HVQFN36	plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 × 6 × 0.85 mm	SOT1092-2

4. Block diagram

A block diagram of the TJA1100 is shown in Figure 1. The 100BASE-T1 section contains the functional blocks specified in the 100BASE-T1 standard that make up the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) layer for both the transmit and receive signal paths. The MII/RMII interface (including the Serial Management Interface (SMI)) conforms to IEEE802.3 clause 22.

Additional blocks are defined for mode control, register configuration, interrupt control, system configuration, reset control, LED control, local wake-up and configuration control. A number of power supply related functional blocks are defined: Very Low Power (VLP) supply in Sleep mode, Reset circuit, supply monitoring and a 1.8 V regulator for the digital core. Pin strapping allows a number of default PHY settings (e.g. Master or Slave configuration) to be hardware-configured at power-up.

The clock signals needed for the operation of the PHY are generated in the PLL block, derived from an external crystal or an oscillator input signal.

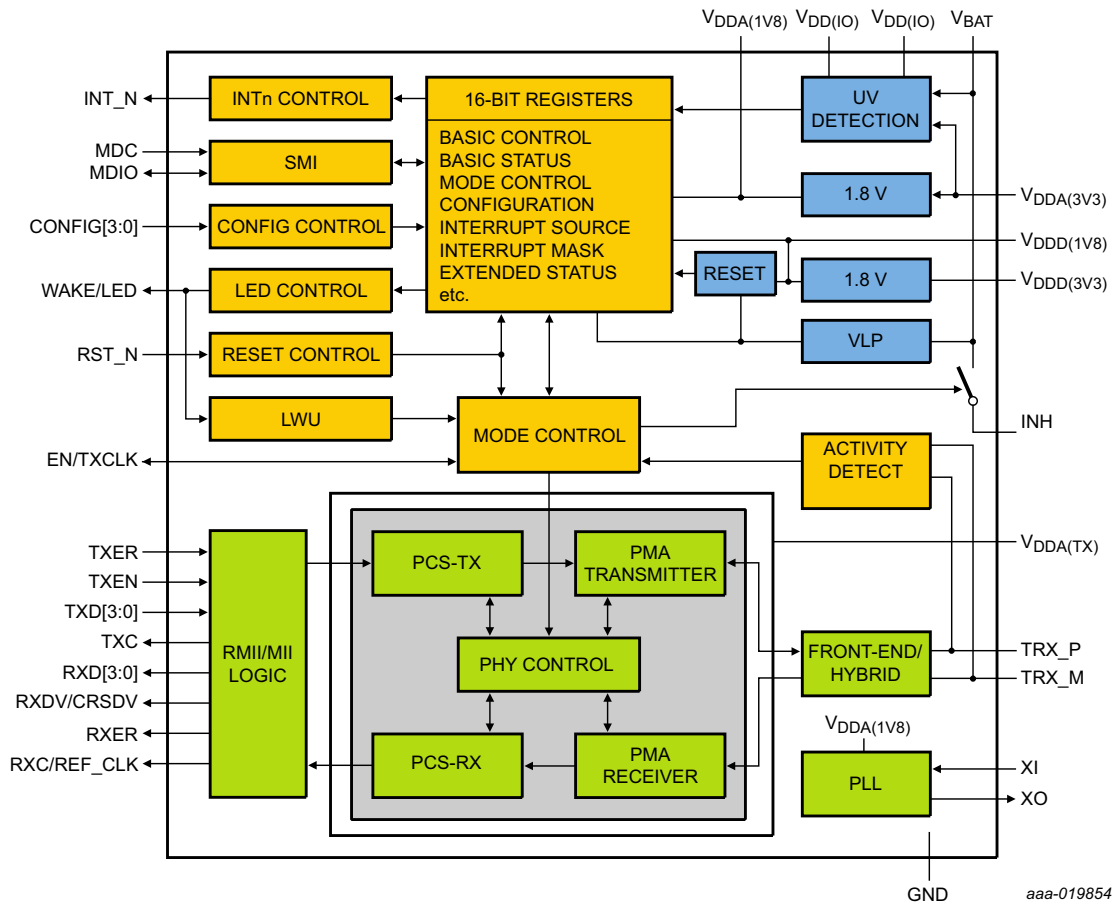


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

The pin configuration of the TJA1100 is shown in Figure 2. The following standard interfaces are provided by the TJA1100: MII/RMII (including SMI) and MDI. Since 100BASE-T1 allows for full-duplex bidirectional communication, the standard MII signals COL and CRS are not needed.

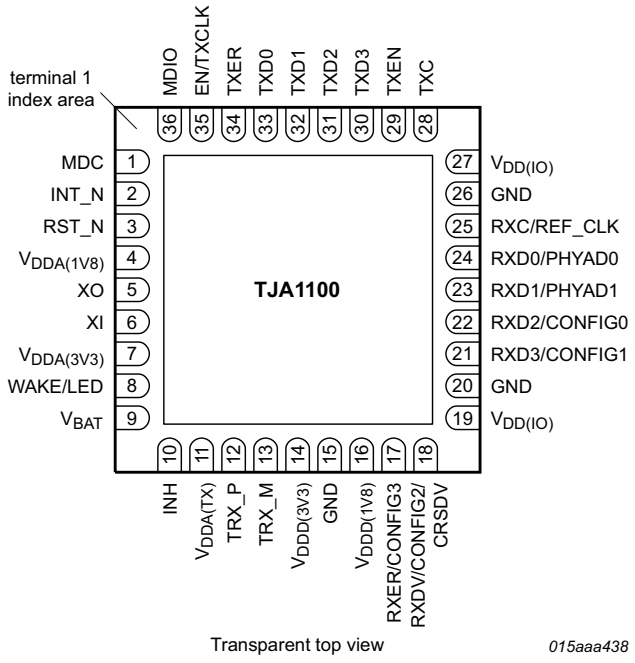


Fig 2. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
MDC	1	I	SMI clock input (weak pull-down)
INT_N	2	O	interrupt output (active-LOW, open-drain output)
RST_N	3	I	reset input (active-LOW)
$V_{DDA(1V8)}$	4	P	1.8 V analog supply voltage (internally generated; needs to be filtered externally)
XO	5	AO	crystal feedback - used in MII/RMII mode with 25 MHz crystal
XI	6	AI	crystal input - used in MII/RMII mode with 25 MHz crystal
$V_{DDA(3V3)}$	7	P	3.3 V analog supply voltage
LED	8	AO	LED open-drain output (when enabled: LED_ENABLE = 1)
WAKE	8	AI	local WAKE input (when LED output disabled: LED_ENABLE = 0)
V_{BAT}	9	P	battery supply voltage
INH	10	AO	inhibit output for voltage regulator control (V_{BAT}-related, active-HIGH)
$V_{DDA(TX)}$	11	P	3.3 V analog supply voltage for the transmitter
TRX_P	12	AIO	+ terminal for transmit/receive signal
TRX_M	13	AIO	– terminal for transmit/receive signal
$V_{DDD(3V3)}$	14	P	3.3 V digital supply voltage
GND[2]	15	G	ground reference
$V_{DDD(1V8)}$	16	P	1.8 V digital supply voltage (internally generated; needs to be filtered externally)
RXER	17	O	MII/RMII receive error output
CONFIG3	17	I	pin strapping configuration input 3
RXDV	18	O	MII/RMII receive data valid output
CONFIG2	18	I	pin strapping configuration input 2
CRSDV	18	O	RMII mode: carrier sense/receive data valid output
$V_{DD(IO)}$	19	P	3.3 V I/O supply voltage
GND[2]	20	G	ground reference
RXD3	21	O	MII mode: receive data output, bit 3 of RXD[3:0] nibble
CONFIG1	21	I	pin strapping configuration input 1
RXD2	22	O	MII mode: receive data output, bit 2 of RXD[3:0] nibble
CONFIG0	22	I	pin strapping configuration input 0
RXD1	23	O	MII mode: receive data output, bit 1 of RXD[3:0] nibble RMII mode: receive data output, bit 1 of RXD[1:0] nibble
PHYAD1	23	I	pin strapping configuration input for bit 1 of the PHY address used for the SMI address/Cipher scrambler
RXD0	24	O	MII mode: receive data output, bit 0 of RXD[3:0] nibble RMII mode: receive data output, bit 0 of RXD[1:0] nibble
PHYAD0	24	I	pin strapping configuration input for bit 0 of the PHY address used for the SMI address/Cipher scrambler
RXC	25	O	MII mode: 25 MHz receive clock output
		I	MII reverse mode: 25 MHz receive clock input

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
REF_CLK	25	I	RMII mode: 50 MHz oscillator clock input
		O	RMII mode: 50 MHz interface reference clock
GND[2]	26	G	ground reference
$V_{DD(IO)}$	27	P	3.3 V I/O supply voltage
TXC	28	IO	MII mode: 25 MHz transmit clock output MII reverse mode: 25 MHz transmit clock input
TXEN	29	I	MII/RMII mode: transmit enable input (active-HIGH, weak pull-down)
TXD3	30	I	MII mode: transmit data input, bit 3 of TXD[3:0] nibble
TXD2	31	I	MII mode: transmit data input, bit 2 of TXD[3:0] nibble
TXD1	32	I	MII mode: transmit data input, bit 1 of TXD[3:0] nibble RMII mode: transmit data input, bit 1 of TXD[1:0] nibble
TXD0	33	I	MII mode: transmit data input, bit 0 of TXD[3:0] nibble RMII mode: transmit data input, bit 0 of TXD[1:0] nibble
TXER	34	I	MII/RMII: transmit error input (weak pull-down)
EN	35	I	PHY enable input (active-HIGH)
TXCLK	35	O	transmit clock output in test mode and during slave jitter test
MDIO	36	IO	SMI data I/O (weak pull-up)

[1] AIO: analog input/output; AO: analog output; AI: analog input; I: digital input ($V_{DD(IO)}$ related); O: digital output ($V_{DD(IO)}$ related); IO: digital input/output ($V_{DD(IO)}$ related); P: power supply; G: ground.

[2] The HVQFN36 package die supply ground is connected to the GND pins and the exposed center pad. The GND pins must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended to connect the exposed center pad to board ground as well.

6. Functional description

6.1 System configuration

A 100BASE-T1 compliant Ethernet PHY, the TJA1100 provides 100 Mbit/s transmit and receive capability over a single unshielded twisted-pair cable, supporting a cable length of up to at least 15 m with a bit error rate less than or equal to 1E−10. It is optimized for capacitive signal coupling to the twisted-pair lines. To comply with automotive EMC requirements, a common-mode choke (CMC) is typically inserted into the signal path.

The TJA1100 is designed to provide a cost-optimized system solution for automotive Ethernet links. Communication with the Media Access Control (MAC) unit can be realized via the MII or the RMII.

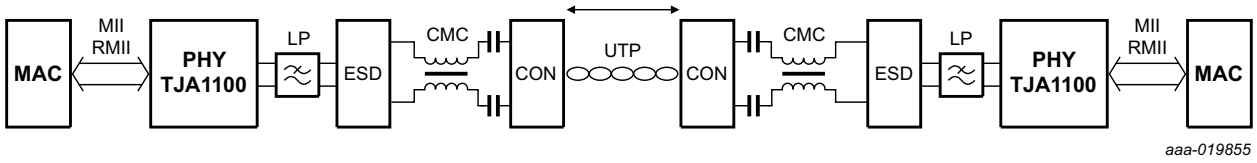


Fig 3. A system diagram showing capacitive coupling

6.2 MII and RMII

The TJA1100 contains MII and RMII interfaces to the MAC controller.

6.2.1 MII

6.2.1.1 Signaling and encoding

The connections between the PHY and the MAC are shown in more detail in Figure 4. Data is exchanged via 4-bit wide data nibbles on TXD[3:0] and RXD[3:0]. Transmit and receive data is synchronized with the transmit (TXC) and receive (RXC) clocks. Both clock signals are provided by the PHY and are typically derived from an external crystal running at a nominal frequency of 25 MHz (±100 ppm). Normal data transmission is initiated with a HIGH level on TXEN, while a HIGH level on RXDV indicates normal data reception.

MII encoding is described in Table 3 and Table 4.

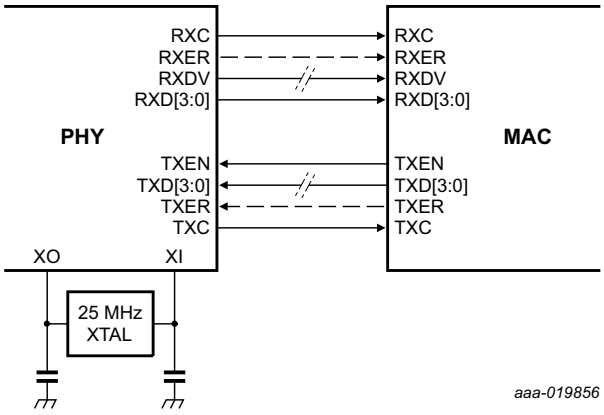


Fig 4. MII signaling

Table 3. MII encoding of TXD[3:0], TXEN and TXER

TXEN	TXER	TXD[3:0]	Indication
0	0	0000 through 1111	normal interframe
0	1	0000 through 1111	reserved
1	0	0000 through 1111	normal data transmission
1	1	0000 through 1111	transmit error propagation

Table 4. MII encoding of RXD[3:0], RXDV and RXER

RXDV	RXER	RXD[3:0]	Indication
0	0	0000 through 1111	normal interframe
0	1	0000	normal interframe
0	1	0001 through 1101	reserved
0	1	1110	false carrier indication
0	1	1111	reserved
1	0	0000 through 1111	normal data transmission
1	1	0000 through 1111	data reception with errors

Since 100BASE-T1 provides full-duplex communication, the standard signals COL and CRS are not needed.

6.2.2 RMII

6.2.2.1 Signaling and encoding

In the case of RMII, data is exchanged via 2-bit wide data nibbles on TXD[1:0] and RXD[1:0], as illustrated in Figure 5. To achieve the same data rate as MII, the interface is clocked at a nominal frequency of 50 MHz. A single clock signal, REF_CLK, is provided for both transmit and received data. This clock signal is provided by the PHY and is typically derived from an external 25 MHz (±100 ppm) crystal (see Figure 5). Alternatively, a 50 MHz clock signal (±50 ppm) generated by an external oscillator can be connected to pin REFCLK_IN (see Figure 6).

RMII encoding is described in Table 5 and Table 6.

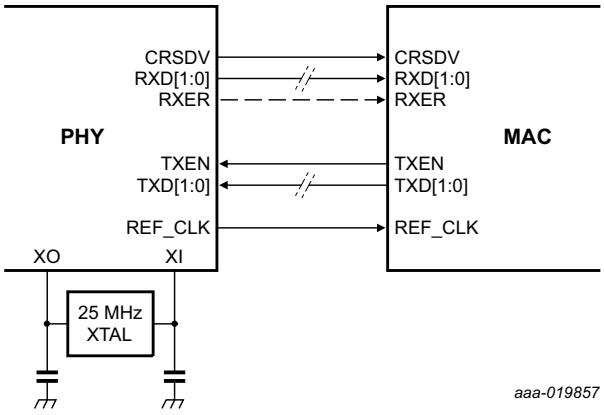


Fig 5. RMII signaling using an external crystal

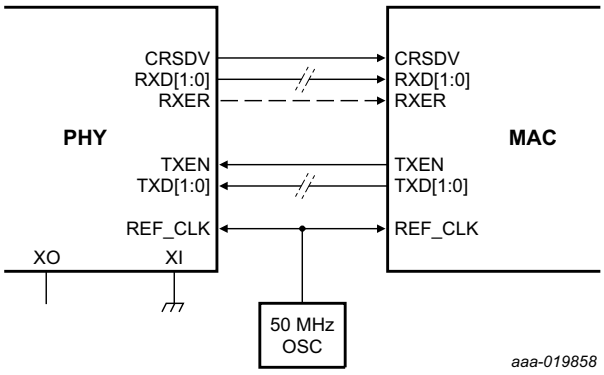


Fig 6. RMII signaling using an externally generated reference clock

Table 5. RMII encoding of TXD[1:0], TXEN

TXEN	TXD[1:0]	Indication
0	00 through 11	normal interframe
1	00 through 11	normal data transmission

Table 6. RMII encoding of RXD[1:0], CRSDV and RXER

CRSDV	RXER	RXD[1:0]	Indication
0	0	00 through 11	normal interframe
0	1	00	normal interframe
0	1	01 through 11	reserved
1	0	00 through 11	normal data transmission
1	1	00 through 11	data reception with errors

6.2.3 Reverse MII

In Reverse MII mode, two PHYs are connected back-to-back via the MII interface to realize a repeater function on the physical layer (see Figure 7). The MII signals are cross-connected: RX output signals from each PHY are connected to the TX inputs on the other PHY. For the PHY connected in Reverse MII mode, the TXC and RXC clock signals become inputs.

Since the MII interface is a standardized solution, two PHYs can be used to implement two different physical layers to realize, for example, a conversion from Fast Ethernet to 100BASE-T1 and vice versa. Another use case for such a repeater could be to double the link length up to 30 m.

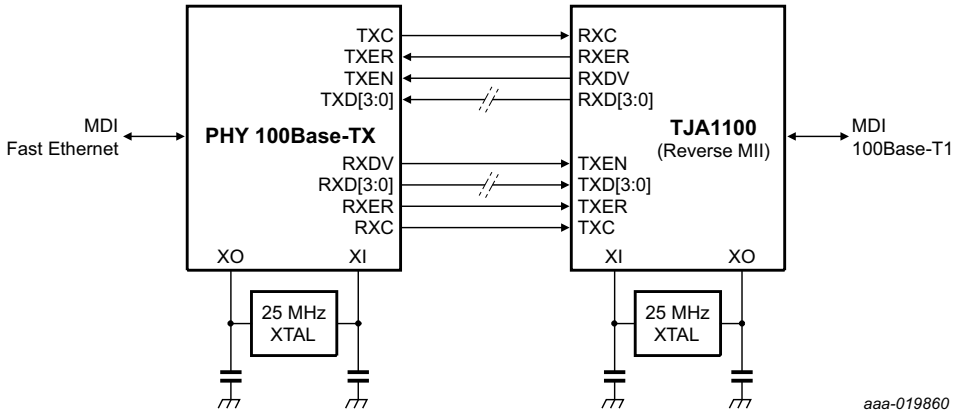


Fig 7. Fast Ethernet to 100BASE-T1 media converter with TJA1100 Reverse MII

6.3 System controller

6.3.1 Operating modes

6.3.1.1 Power-off mode

TJA1100 remains in Power-off mode as long as the voltage on pin V_{BAT} is below the power-on reset threshold. The analog blocks are disabled and the digital blocks are in a passive reset state in this mode.

6.3.1.2 Standby mode

At power-on, when the voltage on pin V_{BAT} rises above the under-voltage recovery threshold ($V_{uvr(VBAT)}$), the TJA1100 enters Standby mode, switching on the INH control output. This control signal may be used to activate the supply to the microcontroller in the ECU. Once the 3.3 V supply voltage is available, the internal 1.8 V regulators are activated and the PHY is configured according to the pin-strapping implemented on the CONFIGn and PHYADn pins. No SMI access takes place during the power-on settling time ($t_{s(pon)}$).

From an operating point of view, Standby mode corresponds to the IEEE 802.3 Power-down mode, where the transmit and receive functions (in the PHY) are disabled. Standby mode also acts as a fail-silent mode. The TJA1100 switches to Standby mode when an under-voltage condition is detected on $V_{DDA(3V3)}$, $V_{DDA(1V8)}$, $V_{DDD(1V8)}$ or $V_{DD(IO)}$.

6.3.1.3 Normal mode

To establish a communication link, the TJA1100 must be switched to Normal mode, either autonomously (AUTO_OP = 1; see Table 20) or via an SMI command (AUTO_OP = 0).

When the PHY is configured for autonomous operation, the TJA1100 will automatically enter Normal mode and activate the link on power-on.

When the PHY is host-controlled, the internal PLL starts running when the TJA1100 enters Normal mode and the transmit and receive functions (both PCS and PMA) are enabled. After a period of stabilization, $t_{init(PHY)}$, the TJA1100 is ready to set up a link. Once the LINK_CONTROL bit is set to 'ENABLE', the PHY configured as Master initiates the training sequence by transmitting idle pulses. The link is established when bit LINK_UP in the Communication Status register is set.

6.3.1.4 Disable mode

Whenever the Ethernet interface is not in use or must be disabled for fail-safe reasons, the PHY can be switched off by pulling pin EN LOW. The PHY is switched off completely in Disable mode, minimizing power consumption. The configuration register settings are maintained. To exit Disable mode, pin EN must be forced HIGH to activate the PHY.

6.3.1.5 Sleep mode

If the network management in a node decides to withdraw from the network because the functions of the node are no longer needed, it may power down the entire ECU via PHY Sleep mode. In Sleep mode, the transmit and receive functions are switched off and no signal is driven onto the twisted-pair lines. Transmit requests from the MII interface are ignored and the MII output pins are in a high-ohmic state. The SMI is also deactivated to minimize power consumption.

By releasing the INH output, the ECU is allowed to switch off its main power supply unit. Typically, the entire ECU is powered-down. The TJA1100 is kept partly alive by the permanent battery supply and can still react to activity on the Ethernet lines. Once valid Ethernet idle pulses are detected on the lines, the TJA1100 wakes up, switching on the main power unit via the INH control signal. As soon as the supply voltages are stable within their operating ranges, the TJA1100 can be switched to Normal mode via an SMI command and the communication link to the partner can be re-established. Sleep mode can be entered from Normal mode via the intermediate Sleep Request mode as well as from Standby mode, as shown in Figure 8. Note that the configuration register settings are maintained in Sleep mode.

6.3.1.6 Sleep Request mode

Sleep Request mode is an intermediate state used to introduce a transition to Sleep mode. The PHY sleep request timer starts when the TJA1100 enters Sleep Request mode. This timer determines how long the PHY remains in Sleep Request mode. When the timer expires (after $t_{to(req)sleep}$), the PHY switches to Sleep mode and INH is switched off. The PHY does not expect to receive Ethernet frames in Sleep Request mode. If any Ethernet frames are received at MDI or MII in Sleep Request mode, the PHY returns to Normal mode, the DATA_DET_WU flag in the General status register is set and a WAKEUP interrupt is generated.

Table 7 presents an overview of the status of TJA1100 functional blocks in each operating mode.

Table 7. Status of functional blocks in TJA1100 operating modes

Functional block	Normal	Standby[1]	Sleep Request	Sleep	Disable
MII	on	high-ohmic[2]	on	high-ohmic	high-ohmic
PMA/PCS-TX	on	off	on	off	off
PMA/PCS-RX	on	off	on	off	off
SMI	on	on	on	off	off
Activity detection	off	on	off	on	off
Crystal oscillator	on	off	on	off	off
LDO_1V8	on	on	on	off	off
RST_N input	on	on	on	off	on
EN input	on[3]	on	on	off	on
WAKE input	off	on/off[4]	on/off[4]	on/off[4]	off
INT_N output	on	on	on	high-ohmic	high-ohmic
LED output	on/off[4]	off	on/off[4]	off	off
INH output	on	on	on	off	on/off[5]
Temp detection	on	on	on	off	off

[1] Outputs RXD[3:0], RXER and RXDV are LOW in Standby mode; the other MII pins are configured as inputs via internal 100 kΩ pull-down resistors.

[2] Pins configured as outputs will be LOW in Standby mode.

[3] In Normal mode, this pin is used as the TXCLK output for the test modes and the slave jitter test (the PHY enable input is held HIGH internally during this time).

[4] The WAKE input is active in Standby, Sleep Request and Sleep modes if LED_ENABLE = 0; the LED output is active in Normal and Sleep Request modes if LED_ENABLE = 1.

[5] The behavior of the INH output in Disable mode is configurable.

6.3.1.7 Reset mode

The TJA1100 switches to Reset mode from any mode except Power-off when pin RST_N is held LOW for at least the maximum reset detection time ($t_{det(rst)(max)}$), provided the voltage on $V_{DD(IO)}$ is above the undervoltage threshold.

When RST_N goes HIGH again, or an undervoltage is detected on $V_{DD(IO)}$, the TJA1100, switches to Standby mode. All register bits are reset to their default values in Reset mode.

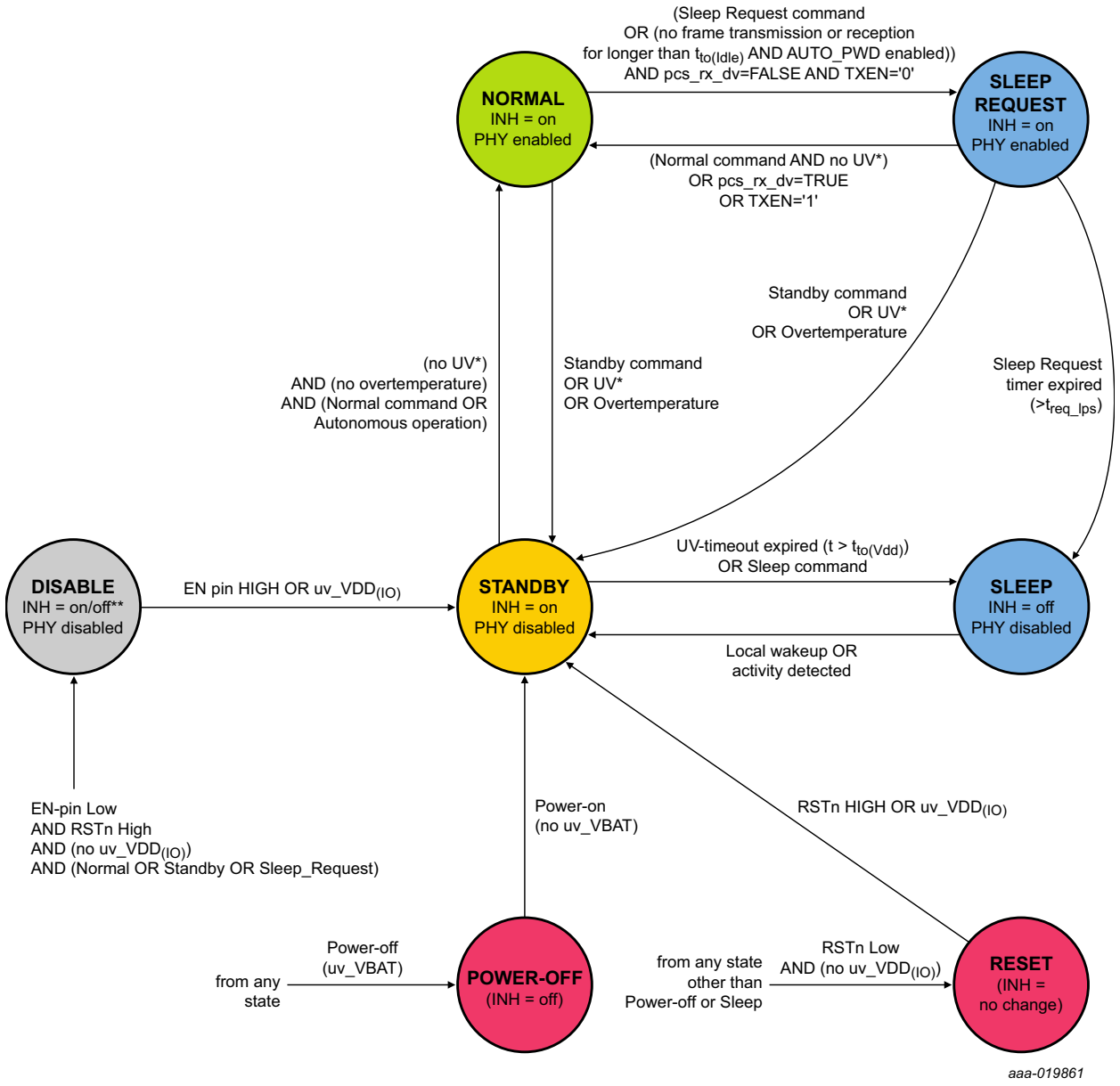
6.3.2 Transitions between operating modes

One of the key features of the TJA1100 is the possibility to put a link and its associated nodes into Sleep mode, while ensuring that the node can be woken up by activity on the Ethernet wires. A node can be switched to Sleep mode when link operation is not needed, minimizing power consumption.

Figure 8 shows the TJA1100 mode transition diagram. For a detailed description of the Sleep transition process, see the TJA1100 application hints [Ref. 1].

The following events, listed in order of priority, trigger mode transitions:

- Power on/off
- Undervoltage on $V_{DD(IO)}$ or $V_{DDD(1V8)}$
- RST_N input
- EN input
- Overtemperature or Undervoltage on $V_{DDA(3V3)}$, $V_{DDA(1V8)}$ or $V_{DDD(1V8)}$
- SMI command and wake-up (local or remote)



* UV means undervoltage on one of the power supply pins $V_{DD(IO)}$, $V_{DDA(3V3)}$, $V_{DDD(1V8)}$, $V_{DDA(1V8)}$
** INH can be configured to be on or off

Fig 8. Operating mode transitions

6.4 Wake-up request

A link that is in Sleep mode must be woken up before the link can be re-established. The node requesting the link can issue a wake request by sending idle symbols onto the link. The link partner detects the idle activity and wakes up.

For the Master PHY, it is only necessary to enable link control (LINK_CONTROL = 1). The training sequence is then detected as a wake-up request. For the Slave PHY, a link wake-up request is issued by setting bit WAKE_REQUEST in the Extended Control

register to 1 while the TJA1100 is in Normal mode with link control disabled (LINK_CONTROL = 0). The wake request phase lasts at least 5 ms to ensure a reliable wake-up. The TJA1100 aborts this wake request and stops sending idle symbols if bit WAKE_REQUEST is reset or link control is enabled.

6.5 Wake-up

When the TJA1100 detects a wake-up event, a WAKEUP interrupt is generated and the wake-up source is indicated in the General status register (status bits LOCAL_WU, REMOTE_WU and DATA_DET_WU; see Table 26). The wake-up source status bits are reset when the TJA1100 enters Sleep Request or Sleep mode. The TJA1100 distinguishes three wake-up sources:

6.5.1 Remote wake-up

In Standby and Sleep modes, any Ethernet activity on the MDI (idle pulses or Ethernet frames) triggers a remote wake-up.

6.5.2 Local wake-up

In Standby, Sleep Request and Sleep modes, a falling edge on pin WAKE (provided configuration bit LED_ENABLE = 0) triggers a local wake-up.

6.5.3 Wake-up by data detection

In Sleep Request mode, any Ethernet frame detected at the MDI or MII triggers wake-up by data detection.

6.6 Autonomous operation

If the PHY is configured for autonomous operation (either via pin strapping, see Section 6.11, or via bit AUTO_OP in Configuration register 1, see Table 20), the TJA1100 can operate and establish a link without further interaction with a host controller. On power-on or wake-up from Sleep mode, the TJA1100 goes directly to Normal mode once all supply voltages are available and the link-up process starts automatically. AUTO_OP must be reset when link or mode control are configured by the Host.

6.7 Autonomous power-down

If autonomous power-down is enabled via Configuration register 1 (AUTO_PWD = 1), the TJA1100 goes to Sleep Request mode automatically if no Ethernet frames have been received at the MDI and MII for the time-out time, $t_{to(pd)autn}$.

6.8 Transmitter amplitude

Power can be saved by adapting the amplitude of the transmitter output to the specific needs of a link. For example, a short link of up to 2 m does not need to operate on the same transmitter amplitude as a link of 15 m to achieve the same signal-to-noise ratio. The nominal transmitter output amplitude can be selected via bit TX_AMPLITUDE (see Table 20). The default value of 1000 mV can support a link of up to 15 m, while the lower values of 500 mV and 750 mV may be sufficient for shorter links of up to 2 m. The compliance, interoperability and EMC tests are performed at the default amplitude.

6.9 Test modes

Five test modes are supported. Only test modes 1, 2, 4 and 5 are included in 100BASE-T1 [Ref. 2]. The test modes can be individually selected via an SMI command in Normal mode while link control is disabled. The EN pin is used as a clock output in test modes that need a reference clock. The normal EN function is disabled in test modes.

6.9.1 Test mode 1

Test mode 1 is for testing the transmitter droop. In Test mode 1, the PHY transmits '+1' symbols for 600 ns followed by '–1' symbols for a further 600 ns. This sequence is repeated continuously.

6.9.2 Test mode 2

Test mode 2 is for testing the transmitter timing jitter in Master configuration. In test mode 2, the PHY transmits the data symbol sequence {+1, -1} repeatedly. The transmission of the symbols is synchronized with the local external oscillator.

6.9.3 Test mode 3

Test mode 3 is for testing the transmitter timing jitter in Slave configuration. In test mode 3, the PHY transmits the data symbol sequence {+1, -1} repeatedly. The transmission of the symbols is synchronized with the recovered receiver clock.

6.9.4 Test mode 4

Test mode 4 is for testing the transmitter distortion. In test mode 4, the PHY transmits the sequence of symbols generated by the scrambler polynomial gs1 = 1 + x9 + x11.

The bit sequence x0n, x1n is derived from the scrambler according to the following equations:

$$x0n = Scrn[0]$$
$$x1n = Scrn[1] \text{ XOR } Scrn[4]$$

This stream of 3-bit nibbles is mapped to a stream of ternary symbols according to Table 8.

Table 8. Symbol mapping in test mode 4

x1n	x0n	PAM-3 transmit symbol
0	0	0
0	1	+1
1	0	0
1	1	–1

6.9.5 Test mode 5

Test mode 5 is for testing the transmit PSD mask. In test mode 5, the PHY transmits a random sequence of PAM-3 symbols.

6.9.6 Slave jitter test

Selecting the 100BASE-T1 Slave jitter test (SLAVE_JITTER_TEST = 1; see Table 19) in Normal mode with LINK_CONTROL = 1 feeds the transmitter reference clock to pin EN. The normal EN function is disabled in this mode.

6.10 Error diagnosis

6.10.1 Undervoltage detection

Like state-of-the-art CAN and FlexRay transceivers, the TJA1100 monitors the status of the supply voltages continuously. Once a supply voltage drops below the specified minimum operating voltage, the TJA1100 enters the fail-silent Standby mode and communication is halted. A UV_ERR interrupt is generated and the source of the undervoltage ($V_{DDA(1V8)}$, $V_{DDD(1V8)}$ or $V_{DDA(3V3)}$) is indicated in the External status register (Table 27). The under-voltage detection/recovery range is positioned immediately next to the operating range, without a gap. Since parameters are specified down to the min. value of the under-voltage detection threshold, it is guaranteed that the behavior of the TJA1100 is fully specified and defined for all possible voltage condition on the supply pins.

6.10.2 Cabling errors

The TJA1100 can detect open and short circuits between the twisted-pair bus lines when neither of the link partners is transmitting (link control disabled). It may make sense to run the diagnostic before establishing the Ethernet link. When bit CABLE_TEST in the Extended Control register (Table 19) is set to 1, test pulses are transmitted onto the transmission medium with a repetition rate of 666.6 kHz. The TJA1100 evaluates the reflected signals and uses impedance mismatch data along the channel to determine the quality of the link. The results of the cable test are available in the External status register (Table 27) within $t_{to(cbl\_tst)}$. The tests performed and associated results are summarized in Table 9.

Table 9. Cable tests and results

The cable bus lines are designated BI_DA+ and BI_DA−, in alignment with 100BASE-T1 [Ref. 2].

BI_DA+	BI_DA-	Result
open	open	open detected
+ shorted to -	- shorted to +	short detected
shorted to V_{DD}	open	open detected
open	shorted to V_{DD}	open detected
shorted to V_{DD}	shorted to V_{DD}	short detected
shorted to GND	open	open detected
open	shorted to GND	open detected
shorted to GND	shorted to GND	short detected
connected to active link partner (master)	connected to active link partner (master)	short and open detected

6.10.3 Link stability

The signal-to-noise ratio is the parameter used to estimate link stability. The PMA Receive function monitors the signal-to-noise ratio continuously. Once the signal-to-noise ratio falls below a configurable threshold (SQI_FAILLIMIT), the link status is set to FAIL and communication is interrupted. The TJA1100 allows for adjusting the sensitivity of the PMA Receive function by configuring this threshold. The microcontroller can always check the current value of the signal-to-noise ratio via the SMI, allowing it to track a possible degradation in link stability.

6.10.4 Link-fail counter

High losses and/or a noisy channel may cause the link to shut down when reception is no longer reliable. In such cases, a LINK_STATUS_FAIL interrupt is generated by the PHY. Retraining of the link begins automatically provided link control is enabled (LINK_CONTROL = 1).

LOC_RCVR_COUNTER and REM_RCVR_COUNTER in the Link-fail counter register (Table 28) are incremented after every link fail event. Both counters are reset when this register is read.

6.10.5 Jabber detection

The Jabber detection function prevents the PHY being locked in the DATA state of the PCS Receive state diagram when the End-of-Stream Delimiters, ESD1 and ESD2, are not detected. The maximum time the PHY can reside in the DATA state is limited to $t_{to(PCS\text{-}RX)}$ (rcv_max_timer in 100BASE-T1; [Ref. 2]). After this time, the PCS-RX state machine is reset and a transition to PHY Idle state is triggered.

6.10.6 Polarity detection

When the TJA1100 is in Slave configuration, it can detect when the ternary symbols sent from the Master PHY are received with the wrong polarity. A polarity error would occur if the two signal wires of the UTP cable were mixed up at the Slave node connection. If the TJA1100 detects a polarity error in the Slave, it will correct it internally while setting the POLARITY_DETECT bit in the External status register (Table 27).

6.10.7 Interleave detection

A 100BASE-T1 PHY can send two different interleave sequences of ternary symbols, (TAn, TBn) or (TBn, TAn). The receiver in the TJA1100 is able to de-interleave both sequences. The order of the ternary symbols detected by the receiver is indicated by the INTERLEAVE_DETECT bit in the External status register (Table 27).

6.10.8 Loopback modes

The TJA1100 supports three loopback modes:

- Internal loopback (PCS loopback in accordance with 100BASE-T1)
- External loopback
- Remote loopback

6.10.8.1 Internal loopback

In Internal loopback mode, the PCS Receive function gets the ternary symbols A_n and B_n directly from the PCS Transmit function as shown in Figure 9. This action allows the MAC to compare packets sent through the MII transmit function with packets received from the MII receive function and, therefore, to validate the functionality of the 100BASE-T1 PCS function.

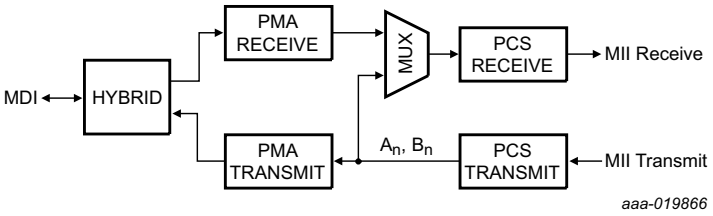


Fig 9. Internal loopback

6.10.8.2 External loopback

In external loopback mode, the PMA Receive function receives signals directly from the PMA Transmit function as shown in Figure 10. This external loopback test allows the MAC to compare packets sent through the MII transmit function with packets received from the MII receive function and, therefore, to validate the functionality of the 100BASE-T1 PCS and PMA functions.

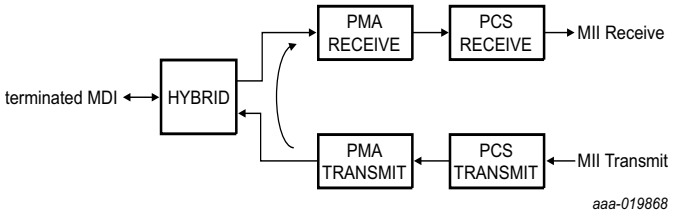


Fig 10. External loopback

6.10.8.3 Remote loopback

In Remote loopback mode, the packet received by the link partner at the MDI is passed through the PMA Receive and PCS Receive functions and forwarded to the PCS Transmit functions, which in turn sends it back to the link partner from where it came. The PCS receive data is made available at the MII. Remote loopback allows the MAC to compare the packets sent to the MDI with the packets received back from the MDI and thus to validate the functionality of the physical channel, including both 100BASE-T1 PHYs. To run the PHY in a loopback mode, the LOOPBACK control bit in the Basic control register should be set before enabling link control.

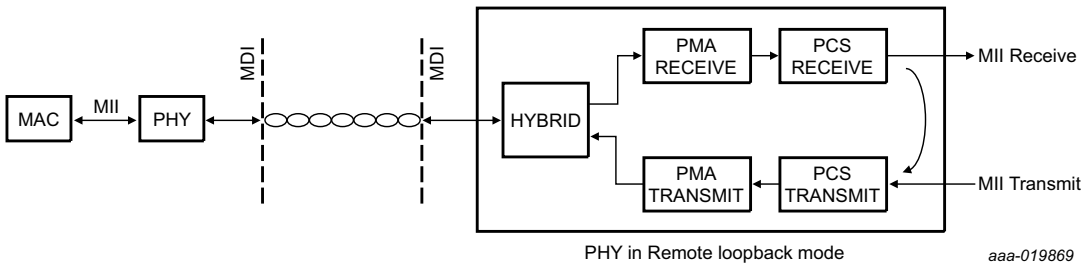


Fig 11. Remote loopback

6.11 Auto-configuration of the PHY during power-up via pin strapping

The logic levels on inputs PHYAD0, PHYAD1 and CONFIG0 to CONFIG3 determine the default configuration of the PHY at power-up or after a hardware reset. Pin strapping occurs during the power-on settling time ($t_{s(pon)}$), once all voltages (including 1V8) are available.

Pin strapping at pins 23 (PHYAD1) and 24 (PHYAD0) determine bits 1 and 0, respectively, of the PHY address used for the SMI address/Cipher scrambler. The PHY address cannot be changed once the PHY has been configured. Besides the address configured via pin strapping, the TJA1100 can always be accessed via address 0.

Table 10. Hardware configuration via CONFIG0 to CONFIG3 pin strapping during power-up

Pin	Value	Description
CONFIG0 (pin 22)	HIGH	PHY configured as Master
	LOW	PHY configured as Slave
CONFIG1 (pin 21)	HIGH	Autonomous operation
	LOW	Managed operation
CONFIG3/CONFIG2 (pin 17/pin 18)	LOW LOW	Normal MII mode
	LOW HIGH	RMII mode (external 50 MHz oscillator)
	HIGH LOW	RMII mode (25 MHz crystal)
	HIGH HIGH	Reverse MII mode

6.12 SMI registers

6.12.1 SMI register mapping

Table 11. SMI register mapping

Register index (dec)	Register name	Group
0	Basic control register	Basic
1	Basic status register	Basic
2	PHY identification register 1	Extended
3	PHY identification register 2	Extended
15	Extended status register	Extended
16	PHY identification register 3	NXP specific
17	Extended control register	NXP specific
18	Configuration register 1	NXP specific
19	Configuration register 2	NXP specific
20	Symbol error counter register	NXP specific
21	Interrupt source register	NXP specific
22	Interrupt enable register	NXP specific
23	Communication status register	NXP specific
24	General status register	NXP specific
25	External status register	NXP specific
26	Link-fail counter register	NXP specific

Table 12. Register notation

Notation	Description
R/W	Read/write
R	Read only
LH	Latched HIGH
LL	Latched LOW
SC	Self-clearing
CR	Cleared on reset

Table 13. Basic control register (Register 0)

Bit	Symbol	Access	Value	Description
15	RESET	R/W SC		software reset control:
			0[1]	normal operation
			1	PHY reset
14	LOOPBACK	R/W		loopback control:
			0[1]	normal operation
			1	loopback mode
13	SPEED_SELECT (LSB)	R/W	[2]	speed select (LSB):
			0	10 Mbit/s if SPEED_SELECT (MSB) = 0 1000 Mbit/s if SPEED_SELECT (MSB) = 1
			1[1]	100 Mbit/s if SPEED_SELECT (MSB) = 0 reserved if SPEED_SELECT (MSB) = 1
12	AUTONEG_EN	R/W SC	0[1]	Auto negotiation not supported; always 0; a write access is ignored.
11	POWER_DOWN	R/W		Standby power down enable:
			0[1]	normal operation (clearing this bit automatically triggers a transition to Normal mode; control bits POWER_MODE must be set to 0011 to select Normal mode, see Table 19)
			1	power down and switch to Standby mode (provided ISOLATE = 0; ignored if ISOLATE = 1 and CONTROL_ERR interrupt generated)
10	ISOLATE	R/W		PHY isolation:
			0[1]	normal operation
			1	isolate PHY from MII/RMII (provided POWER_DOWN = 0; ignored if POWER_DOWN = 1 and CONTROL_ERR interrupt generated)
9	RE_AUTONEG	R/W SC	0[1]	Auto negotiation not supported; always 0; a write access is ignored.
8	DUPLEX_MODE	R/W	1[1]	only full duplex supported; always 1; a write access is ignored.
7	COLLISION_TEST	R/W	0[1]	COL signal test not supported; always 0; a write access is ignored.
6	SPEED_SELECT (MSB)	R/W	[2]	speed select (MSB):
			0[1]	10 Mbit/s if SPEED_SELECT (LSB) = 0 100 Mbit/s if SPEED_SELECT (LSB) = 1
			1	1000 Mbit/s if SPEED_SELECT (LSB) = 0 reserved if SPEED_SELECT (LSB) = 1

Table 13. Basic control register (Register 0) *…continued*

Bit	Symbol	Access	Value	Description
5	UNIDIRECT_EN	R/W		unidirectional enable when bit 12 = 0 and bit 8 = 1:
			0[1]	enable transmit from MII only when the PHY has determined that a valid link has been established
			1	enable transmit from MII regardless of whether the PHY has determined that a valid link has been established
4:0	reserved	R/W	00000[1]	always write 00000; ignore on read

[1] Default value.

[2] Speed Select: 00: 10 Mbit/s; 01: 100 Mbit/s; 10: 1000 Mbit/s; 11: reserved; a write access value other than 01 is ignored.

Table 14. Basic status register (Register 1)

Bit	Symbol	Access	Value	Description
15	100BASE-T4	R	0[1]	PHY not able to perform 100BASE-T4
			1	PHY able to perform 100BASE-T4
14	100BASE-X_FD	R	0[1]	PHY not able to perform 100BASE-X full duplex
			1	PHY able to perform 100BASE-X full duplex
13	100BASE-X_HD	R	0[1]	PHY not able to perform 100BASE-X half duplex
			1	PHY able to perform 100BASE-X half duplex
12	10Mbps_FD	R	0[1]	PHY not able to perform 10 Mbit/s full duplex
			1	PHY able to perform 10 Mbit/s full duplex
11	10Mbps_HD	R	0[1]	PHY not able to perform 10 Mbit/s half duplex
			1	PHY able to perform 10 Mbit/s half duplex
10	100BASE-T2_FD	R	0[1]	PHY not able to perform 100BASE-T2 full duplex
			1	PHY able to perform 100BASE-T2 full duplex
9	100BASE-T2_HD	R	0[1]	PHY not able to perform 100BASE-T2 half duplex
			1	PHY able to perform 100BASE-T2 half duplex
8	EXTENDED_STATUS	R	0	no extended status information in register 15h
			1[1]	extended status information in register 15h
7	UNIDIRECT_ ABILITY	R	0	PHY able to transmit from MII only when the PHY has determined that a valid link has been established
			1[1]	PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	MF_PREAMBLE_SUPPRESSION	R	0	PHY will not accept management frames with preamble suppressed
			1[1]	PHY will accept management frames with preamble suppressed
5	AUTONEG_COMPLETE	R	0	Autonegotiation process not completed
			1[1]	Autonegotiation process completed
4	REMOTE_FAULT	R LH	0[1][2]	no remote fault condition detected
			1	remote fault condition detected
3	AUTONEG_ABILITY	R	0[1]	PHY not able to perform Autonegotiation
			1	PHY able to perform Autonegotiation
2	LINK_STATUS	R LL	0[1][2]	link is down
			1	link is up
1	JABBER_DETECT	R LH	0[1][2]	no jabber condition detected
			1	jabber condition detected
0	EXTENDED_CAPABILITY	R	0	basic register set capabilities only
			1[1]	extended register capabilities

[1] Default value.

[2] Reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 15. PHY identification register 1 (Register 2)

Bit	Symbol	Access	Value	Description
15:0	PHY_ID	R	0180h[1]	bits 3 to 18 of the Organizationally Unique IDentifier (OUI)[2]

[1] Default value.

[2] OUI = 00.60.37h (note that bits 1 and 2 of OUI are always 0).

Table 16. PHY identification register 2 (Register 3)

Bit	Symbol	Access	Value	Description
15:10	PHY_ID	R	110111[1]	bits 19 to 24 of the OUI[2]
9:4	TYPE_NO	R	000100[1]	six-bit manufacturer's type number
3:0	REVISION_NO	R	0001[1]	four-bit manufacturer's revision number

[1] Default value.

[2] OUI = 00.60.37h (note that bits 1 and 2 of OUI are always 0).

Table 17. Extended status register (Register 15)

Bit	Symbol	Access	Value	Description
15	1000BASE-X_FD	R	0[1]	PHY not able to perform 1000BASE-X full duplex
			1	PHY able to perform 1000BASE-X full duplex
14	1000BASE-X_HD	R	0[1]	PHY not able to perform 1000BASE-X half duplex
			1	PHY able to perform 1000BASE-X half duplex
13	1000BASE-T_FD	R	0[1]	PHY not able to perform 1000BASE-T full duplex
			1	PHY able to perform 1000BASE-T full duplex
12	1000BASE-T_HD	R	0[1]	PHY not able to perform 1000BASE-T half duplex
			1	PHY able to perform 1000BASE-T half duplex
11:8	reserved	R	-	
7	100BASE-T1	R	0	PHY not able to 1-pair 100BASE-T1 100 Mbit/s
			1[1]	PHY able to 1-pair 100BASE-T1 100 Mbit/s
6	1000BASE-T1	R	0[1]	PHY not able to perform 1000BASE-T1
			1	PHY able to perform 1000BASE-T1
5:0	reserved	R	-	

[1] Default value.

Table 18. PHY identification register 3 (Register 16)

Bit	Symbol	Access	Value	Description
15:8	reserved	R	-	
7:0	VERSION_NO	R	xxh	8-bit manufacturer's firmware revision number

Table 19. Extended control register (Register 17)

Bit	Symbol	Access	Value	Description
15	LINK_CONTROL	R/W	[1]	link control enable:
			0	link control disabled
			1	link control enabled
14:11	POWER_MODE	R/W	[2]	operating mode select:
			0000[3]	no change
			0011	Normal mode
			1100	Standby mode
			1011	Sleep Request mode
10	SLAVE_JITTER_TEST	R/W		enable/disable Slave jitter test
			0[3]	disable Slave jitter test
			1	enable Slave jitter test
9	TRAINING_RESTART	R/W SC		Autonegotiation process restart:
			0[3]	halts the training phase
			1	forces a restart of the training phase
8:6	TEST_MODE	R/W		test mode selection:
			000[3]	no test mode
			001	100BASE-T1 test mode 1
			010	100BASE-T1 test mode 2
			011	test mode 3
			100	100BASE-T1 test mode 4
			101	100BASE-T1 test mode 5
			110	scrambler and descrambler bypassed
			111	reserved
5	CABLE_TEST	R/W SC		TDR-based cable test:
			0[3]	stops TDR-based cable test
			1	forces TDR-based cable test
4:3	LOOPBACK_MODE	R/W		loopback mode select:
			00[3]	internal loopback
			01	external loopback
			10	external loopback
			11	remote loopback
2	CONFIG_EN	R/W		configuration register access:
			0[3]	configuration register access disabled
			1	configuration register access enabled
1	CONFIG_INH	R/W		INH configuration:
			0	INH switched off in Disable mode
			1[3]	INH switched on in Disable mode
0	WAKE_REQUEST[4]	R/W		wake-up request configuration:
			0[3]	no wake-up signal to be transmitted
			1	transmit idle symbols as bus wake-up request

[1] Default value is 0 when AUTO_OP = 0; default value is 1 when AUTO_OP = 1.

[2] Any other value generates a CONTROL_ERR interrupt.

[3] Default value.

[4] Link control must be disabled (LINK_CONTROL = 0) before WAKE_REQUEST is set.

Table 20. Configuration register 1 (Register 18)

Bit	Symbol	Access	Value	Description
15	MASTER_SLAVE	R/W	[1]	PHY Master/Slave configuration:
			0	PHY configured as Slave
			1	PHY configured as Master
14	AUTO_OP	R/W	[1]	managed/autonomous operation:
			0	managed operation
			1	autonomous operation
13	LINK_LENGTH	R/W	-	don't care (cable length)[2]
12	reserved	R/W	-	
11:10	TX_AMPLITUDE	R/W		nominal transmit amplitude:
			00	500 mV
			01	750 mV
			10[3]	1000 mV
			11	1250 mV
9:8	MII_MODE	R/W	[1]	MII mode:
			00	MII mode enabled
			01	RMII mode enabled (50 MHz input at REFCLK_IN)
			10	RMII mode enabled (25 MHz XTAL)
			11	Reverse MII mode
7	MII_DRIVER	R/W		MII output driver strength:
			0[3]	standard
			1	reduced
6	reserved	R/W	0	always write 0; ignore on read
5:4	LED_MODE	R/W		LED mode:
			00	link up (LED on when link OK: bit LINK_UP in the Communication Status Register = 1)
			01[3]	frame reception (LED on when BRreceive = true)
			10	symbol error[4]
			11	CRS signal
3	LED_ENABLE	R/W	[5]	LED enable:
			0[3]	LED output disabled; WAKE input enabled
			1	LED output enabled; WAKE input disabled
2	CONFIG_WAKE	R/W		local wake configuration:
			0[3]	absolute input threshold
			1	ratiometric input threshold ($V_{DD(IO)}$)

Table 20. Configuration register 1 (Register 18) *…continued*

Bit	Symbol	Access	Value	Description
1	AUTO_PWD	R/W		autonomous power down:
			0[3]	autonomous power-down disabled
			1	autonomous power-down enabled
0	reserved	R/W	0	always write 0; ignore on read

[1] Default value determined by pin strapping (see Section 6.11).

[2] Function is obsolete due to improved echo cancelation; default value is 0.

[3] Default value.

[4] The active state of the LED output will be lengthened by $t_{w(LED)}$.

[5] The WAKE input is enabled in Sleep, Sleep Request and Standby modes if LED_ENABLE = 0.

Table 21. Configuration register 2 (Register 19)

Bit	Symbol	Access	Value	Description
15:11	PHYAD[4:0]	R	[1]	PHY address used for the SMI address and for initializing the Cipher scrambler key; PHYAD[1:0] is predetermined by the hardware configuration straps on pins 23 and 24; PHYAD[4:2] set to 001
10:9	SQI_AVERAGING	R/W	[2]	Signal Quality Indicator (SQI) averaging:
			00	SQI averaged 32 symbols
			01[3]	SQI averaged 64 symbols
			10	SQI averaged 128 symbols
			11	SQI averaged 256 symbols
8:6	SQI_WLIMIT	R/W		SQI warning limit:
			000	no warning limit
			001[3]	class A SQI warning limit
			010	class B SQI warning limit
			011	class C SQI warning limit
			100	class D SQI warning limit
			101	class E SQI warning limit
			110	class F SQI warning limit
			111	class G SQI warning limit
5:3	SQI_FAILLIMIT	R/W		SQI fail limit:
			000[3]	no fail limit
			001	class A SQI fail limit
			010	class B SQI fail limit
			011	class C SQI fail limit
			100	class D SQI fail limit
			101	class E SQI fail limit
			110	class F SQI fail limit
			111	class G SQI fail limit
2	JUMBO_ENABLE	R/W		Jumbo packet support:
			0	packets up to 4 kB supported
			1[3]	packets up to 16 kB supported

Table 21. Configuration register 2 (Register 19) *…continued*

Bit	Symbol	Access	Value	Description
1:0	SLEEP_REQUEST_TO	R/W		sleep request time-out:
			00	0.4 ms
			01[3]	1 ms
			10	4 ms
			11	16 ms

[1] Default value determined by pin strapping.

[2] The SQI is derived from the actual internal slicer margin and includes filtering. Averaging the SQI value itself does not, therefore, have any added value.

[3] Default value.

Table 22. Symbol error counter register 2 (Register 20)

Bit	Symbol	Access	Value	Description
15:0	SYM_ERR_CNT	R	0000h[1]	The symbol error counter is incremented when an invalid code symbol is received (including idle symbols). The counter is incremented only once per packet, even when the received packet contains more than one symbol error. This counter increments up to 2^{16}. When the counter overflows, the value FFFFh is retained. The counter is reset when the register is read.

[1] Default value. Bits NOT reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 23. Interrupt status register (Register 21)

Bit	Symbol	Access	Value	Description
15	PWON	R LH	0[1]	power-on not detected
			1	power-on detected
14	WAKEUP	R LH	0[1]	no local or remote wake-up detected
			1	local or remote wake-up detected
13:12	reserved	R	-	
11	PHY_INIT_FAIL	R LH	0[1]	no PHY initialization error detected
			1	PHY initialization error detected
10	LINK_STATUS_FAIL	R LH	0[1][2]	link status not changed
			1	link status bit LINK_UP changed from ‘link OK’ to ‘link fail’
9	LINK_STATUS_UP	R LH	0[1][2]	link status not changed
			1	link status bit LINK_UP changed from ‘link fail’ to ‘link OK’
8	SYM_ERR	R LH	0[1][2]	no symbol error detected
			1	symbol error detected
7	TRAINING_FAILED	R LH	0[1]	no training phase failure detected
			1	training phase failure detected
6	SQI_WARNING	R LH	0[1][2]	SQI value above warning limit
			1	SQI value below warning limit and bit LINK_UP set
5	CONTROL_ERR	R LH	0[1]	no SMI control error detected
			1	SMI control error detected
4	reserved	R	-	
3	UV_ERR	R LH	0[1]	no undervoltage detected
			1	undervoltage detected on $V_{DD(IO)}$, $V_{DDA(1V8)}$, $V_{DDD(1V8)}$ or $V_{DDA(3V3)}$
2	UV_RECOVERY	R LH	0[1]	no undervoltage recovery detected
			1	undervoltage recovery detected
1	TEMP_ERR	R LH	0[1]	no overtemperature error detected
			1	overtemperature error detected
0	SLEEP_ABORT	R LH	0[1]	no transition from Sleep Request back to Normal when pcs_rx_dv changes from FALSE to TRUE or TXEN goes HIGH
			1	transition from Sleep Request back to Normal mode when pcs_rx_dv changes from FALSE to TRUE or TXEN goes HIGH

[1] Default value.

[2] Interrupts LINK_STATUS_FAIL, LINK_STATUS_UP, SYM_ERR and SQI_WARNING are cleared on entering Sleep Request mode, on entering Standby mode due to an undervoltage and when an undervoltage is detected in Standby mode.

Table 24. Interrupt enable register (Register 22)

Bit	Symbol	Access	Value	Description
15	PWON_EN	R/W	0	PWON interrupt disabled
			1[1]	PWON interrupt enabled
14	WAKEUP_EN	R/W	0[1]	WAKEUP interrupt disabled
			1	WAKEUP interrupt enabled
13:12	reserved	R/W	00[1]	always write 00; ignore on read
11	PHY_INIT_FAIL_EN	R/W	0[1]	PHY_INIT_FAIL interrupt disabled
			1	PHY_INIT_FAIL interrupt enabled
10	LINK_STATUS_FAIL_EN	R/W	0[1]	LINK_STATUS_FAIL interrupt disabled
			1	LINK_STATUS_FAIL interrupt enabled
9	LINK_STATUS_UP_EN	R/W	0[1]	LINK_STATUS_UP interrupt disabled
			1	LINK_STATUS_UP interrupt enabled
8	SYM_ERR_EN	R/W	0[1]	SYM_ERR interrupt disabled
			1	SYM_ERR interrupt enabled
7	TRAINING_FAILED_EN	R/W	0[1]	TRAINING_FAILED interrupt disabled
			1	TRAINING_FAILED interrupt enabled
6	SQI_WARNING_EN	R/W	0[1]	SQI_WARNING interrupt disabled
			1	SQI_WARNING interrupt enabled
5	CONTROL_ERR_EN	R/W	0[1]	CONTROL_ERR interrupt disabled
			1	CONTROL_ERR interrupt enabled
4	reserved	R/W	0[1]	always write 0; ignore on read
3	UV_ERR_EN	R/W	0[1]	UV_ERR interrupt disabled
			1	UV_ERR interrupt enabled
2	UV_RECOVERY_EN	R/W	0[1]	UV_RECOVERY interrupt disabled
			1	UV_RECOVERY interrupt enabled
1	TEMP_ERR_EN	R/W	0[1]	TEMP_ERR interrupt disabled
			1	TEMP_ERR interrupt enabled
0	SLEEP_ABORT_EN	R/W	0[1]	SLEEP_ABORT interrupt disabled
			1	SLEEP_ABORT interrupt enabled

[1] Default value.

Table 25. Communication status register (Register 23)

Bit	Symbol	Access	Value	Description
15	LINK_UP	R	0[1][2]	link failure
			1	link OK
14:13	TX_MODE	R	00[1][2]	transmitter disabled
			01	transmitter in SEND_N mode
			10	transmitter in SEND_I mode
			11	transmitter in SEND_Z mode
12	LOC_RCVR_STATUS	R LL	0[1][2]	local receiver not OK
			1	local receiver OK
11	REM_RCVR_STATUS	R LL	0[1][2]	remote receiver not OK
			1	remote receiver OK
10	SCR_LOCKED	R	0[1][2]	descrambler unlocked
			1	descrambler locked
9	SSD_ERR	R LH	0[1][2]	no SSD error detected
			1	SSD error detected
8	ESD_ERR	R LH	0[1][2]	no ESD error detected
			1	ESD error detected
7:5	SQI	R	000[1][2]	worse than class A SQI (unstable link)
			001	class A SQI (unstable link)
			010	class B SQI (unstable link)
			011	class C SQI (good link)
			100	class D SQI (good link; bit error rate < 1e−10)
			101	class E SQI (good link)
			110	class F SQI (very good link)
			111	class G SQI (very good link)
4	RECEIVE_ERR	R LH	0[1][2]	no receive error detected
			1	receive error detected since register last read
3	TRANSMIT_ERR	R LH	0[1][2]	no transmit error detected
			1	transmit error detected since register last read
2:0	PHY_STATE	R	000[1]	PHY Idle
			001	PHY Initializing
			010	PHY Configured
			011	PHY Offline
			100	PHY Active
			101	PHY Isolate
			110	PHY Cable test
			111	PHY Test mode

[1] Default value.

[2] Reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 26. General status register (Register 24)

Bit	Symbol	Access	Value	Description
15	INT_STATUS	R	0[1]	all interrupts cleared
			1	unmasked interrupt pending
14	PLL_LOCKED	R LL	0[1]	PLL unstable and not locked
			1	PLL stable and locked
13	LOCAL_WU	R LH	0[1]	no local wake-up detected
			1	local wake-up detected
12	REMOTE_WU	R LH	0[1]	no remote wake-up detected
			1	remote wake-up detected
11	DATA_DET_WU	R LH	0[1]	no 100BASE-T1 data detected at MDI or MII in Sleep Request mode
			1	100BASE-T1 data detected at MDI (pcs_rx_dv = TRUE; see Ref. 2) or MII (TXEN = HIGH) in Sleep Request mode
10	EN_STATUS	R LH	0[1]	EN HIGH
			1	EN switched LOW since register last read
9	RESET_STATUS	R	0[1]	no hardware reset detected
			1	hardware reset detected since register last read
8	reserved	R	-	
7:3	LINKFAIL_CNT	R	00000[2]	number of link fails since register last read.
2:0	reserved	R	-	

[1] Default value.

[2] Default value; bits NOT reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 27. External status register (Register 25)

Bit	Symbol	Access	Value	Description
15	reserved	R	-	
14	UV_VDDA_3V3	R LH	0[1]	no undervoltage detected on pin $V_{DDA(3V3)}$
			1	undervoltage detected on pin $V_{DDA(3V3)}$
13	UV_VDDD_1V8	R LH	0[1]	no undervoltage detected on pin $V_{DDD(1V8)}$
			1	undervoltage detected on pin $V_{DDD(1V8)}$
12	UV_VDDA_1V8	R LH	0[1]	no undervoltage detected on pin $V_{DDA(1V8)}$
			1	undervoltage detected on pin $V_{DDA(1V8)}$
11	UV_VDDIO	R LH	0[1]	no undervoltage detected on pin $V_{DD(IO)}$
			1	undervoltage detected on pin $V_{DD(IO)}$
10	TEMP_HIGH	R LH	0[1]	temperature below high level
			1	temperature above high level
9	TEMP_WARN	R LH	0[1]	temperature below warning level
			1	temperature above warning level
8	SHORT_DETECT	R LH	0[2]	no short circuit detected
			1	short circuit detected since register last read
7	OPEN_DETECT	R LH	0[2]	no open circuit detected
			1	open circuit detected since register last read

Table 27. External status register (Register 25) *…continued*

Bit	Symbol	Access	Value	Description
6	POLARITY_DETECT	R	0[2]	no polarity inversion detected at MDI
			1	polarity inversion detected at MDI
5	INTERLEAVE_DETECT	R	0[1]	interleave order of detected ternary symbols: TAn, TBn [2]
			1	interleave order of detected ternary symbols: TBn, TAn
4:0	reserved	R	-	

[1] Default value.

[2] Default value; bit NOT reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 28. Link fail counter register (Register 26)

Bit	Symbol	Access	Value	Description
15:8	LOC_RCVR_CNT	R	00h[1]	The counter is incremented when local receiver is NOT_OK; when the counter overflows, the value FFh is retained. The counter is reset when the register is read.
7:0	REM_RCVR_CNT	R	00h[1]	The counter is incremented when remote receiver is NOT_OK; when the counter overflows, the value FFh is retained. The counter is reset when the register is read.

[1] Default value; bits NOT reset to default value when link control is disabled (LINK_CONTROL = 0).

7. Limiting values

Table 29. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	voltage on pin x	DC value			
		on pin V_{BAT}	−0.3	+40	V
		on pin INH	−0.3	V_{BAT} + 0.3	V
		on pins WAKE, LED	−36	+42	V
		on pins $V_{DDA(TX)}$, $V_{DDD(3V3)}$, $V_{DD(IO)}$, TRX_P, TRX_M	−0.3	+4.6	V
		on pin $V_{DDA(3V3)}$			
		V_{BAT} < 3.1 V; 9 hours at an equivalent junction temperature of 150 °C; activation energy of 0.78 eV	−0.3	+3.6	V
		$V_{BAT} \geq 3.1$ V	−0.3	+4.6	V
		on pins MDC, MDIO, RST_N, INT_N, EN and MII digital input and output pins	−0.3	min($V_{DD(IO)}$ + 0.3, +4.6)	V
		on pins $V_{DDA(1V8)}$, $V_{DDD(1V8)}$, XI, XO	−0.3	+2.5	V
I_{EN}	current on pin EN		-	250	µA
I_{RST_N}	current on pin RST_N		-	250	µA
I_{INH}	current on pin INH	no time limit	−2	-	mA
I_{LED}	current on pin LED	no time limit; LED_ENABLE = 1	-	10	mA
V_{trt}	transient voltage	on pins WAKE, V_{BAT}, TRX_P, TRX_M [1]			
		pulse 1	−100	-	V
		pulse 2a	-	75	V
		pulse 3a	−150	-	V
		pulse 3b	-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; 150 pF, 330 Ω			
		on pins TRX_P, TRX_M to GND [2][3]	−6.0	+6.0	kV
		on pins WAKE, LED to GND [2][4]	−6.0	+6.0	kV
		on pin V_{BAT} to GND [2][5]	−6.0	+6.0	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ			
		on pins TRX_P, TRX_M to GND [6]	−6.0	+6.0	kV
		on pins WAKE, LED to GND [7]	−6.0	+6.0	kV
		on pin V_{BAT} to GND [8]	−6.0	+6.0	kV
		on any other pin [6]	−2.0	+2.0	kV
		Charged Device Model (CDM); 1 Ω [9]			
		on any pin	−500	+500	V
T_{amb}	ambient temperature		−40	+125	°C
T_{stg}	storage temperature		−55	+150	°C

[1] According to ISO7637, class C; verified by an external test house.

[2] Verified by external test house; test result must be equal to or better than ±6 kV.

[3] Tested with a common mode choke and 100 nF coupling capacitors.

[4] Tested with 10 nF capacitor to GND and 10 kΩ in series between the capacitor and the WAKE/LED pin.

[5] Tested with 100 nF from V_{BAT} to GND.

[6] According to AEC-Q100-002.

[7] According to AEC-Q100-002 with 10 nF capacitor to GND and 10 kΩ in series between the capacitor and the WAKE/LED pin.

[8] According to AEC-Q100-002 with 100 nF from V_{BAT} to GND.

[9] According to AEC-Q100-011.

8. Thermal characteristics

Table 30. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient [1]	in free air	31	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	in free air	8	K/W

[1] TJA1100 mounted on a JEDEC 2s2p board with 25 vias between layer 1 and layer 2; via diameter: 0.5 mm, wall thickness: 18 μm.

9. Static characteristics

Table 31. Static characteristics

T_{vj} = −40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{BAT}	battery supply voltage	operating range	3.1	-	36	V
I_{BAT}	battery supply current	all modes except Sleep; V_{BAT} < 36 V; I_{INH} = 0 μA	-	-	1.5	mA
		Sleep mode; $T_{vj} \leq 85$ °C; 7.4 V < V_{BAT} < 30 V	-	30	70	μA
		V_{BAT} < 40 V; I_{INH} = 0 μA	-	-	5	mA
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin V_{BAT}		2.8	-	-	V
$V_{uvr(VBAT)}$	undervoltage recovery voltage on pin V_{BAT}		-	-	3.1	V
$V_{uvhys(VBAT)}$	undervoltage hysteresis voltage on pin V_{BAT}		15	100	-	mV
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	operating range	3.1	3.3	3.5	V
$I_{DDA(3V3)}$	analog supply current (3.3 V)	Normal/Sleep Request modes	-	21	27	mA
		Standby mode	-	110	250	μA
		Disable/Reset modes	-	4	20	μA
$V_{DDA(TX)}$	transmitter analog supply voltage	operating range	3.1	3.3	3.5	V
$I_{DDA(TX)}$	transmitter analog supply current	Normal/Sleep Request modes; amplitude transmitter = 1 V	-	60	75	mA
		Standby/Disable/Reset modes	-	0	50	μA
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)	operating range	3.1	3.3	3.5	V

Table 31. Static characteristics *…continued*

T_{vj} = −40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDD(3V3)}$	digital supply current (3.3 V)	Normal/Sleep Request modes	-	47	56	mA
		Standby mode; T_{vj} = 25 °C;	-	150	700	µA
		Standby mode; T_{vj} = 125 °C;	-	0.4	6	mA
		Disable/Reset modes	-	0	10	µA
$V_{uvd(VDDA3V3)}$	undervoltage detection voltage on pin $V_{DDA(3V3)}$		2.9	-	-	V
$V_{uvr(VDDA3V3)}$	undervoltage recovery voltage on pin $V_{DDA(3V3)}$		-	-	3.1	V
$V_{uvhys(VDDA3V3)}$	undervoltage hysteresis voltage on pin $V_{DDA(3V3)}$		50	80	-	mV
$V_{DD(IO)}$	input/output supply voltage	operating range	3.1	3.3	3.5	V
$I_{DD(IO)}$	input/output supply current	Normal/Sleep Request modes; C_{load} on MII pins = 15 pF [1]	-	-	9	mA
		Standby/Disable modes; no currents in pull-up resistors on digital inputs	-	-	20	µA
		Reset mode; no currents in pull-up resistors on digital inputs [1]	-	35	70	µA
$V_{uvd(VDDIO)}$	undervoltage detection voltage on pin $V_{DD(IO)}$		2.9	-	-	V
$V_{uvr(VDDIO)}$	undervoltage recovery voltage on pin $V_{DD(IO)}$		-	-	3.1	V
$V_{uvhys(VDDIO)}$	undervoltage hysteresis voltage on pin $V_{DD(IO)}$		50	80	-	mV
P	power dissipation	Normal/Sleep Request modes	-	455	640	mW
SMI interface: pins MDC and MDIO						
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
C_i	input capacitance	pin MDC [1]	-	-	8	pF
		pin MDIO [1]	-	-	10	pF
V_{OH}	HIGH-level output voltage	pin MDIO; I_{OH} = −4 mA	$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	pin MDIO; I_{OL} = 4 mA	-	-	0.4	V
I_{IH}	HIGH-level input current	V_{IH} = $V_{DD(IO)}$	-	-	20	µA
I_{IL}	LOW-level input current	pin MDC; V_{IL} = 0 V	−20	-	-	µA
		pin MDIO; 0 V ≤ V_i ≤ $V_{DD(IO)}$	−3800	-	−20	µA
R_{pd}	pull-down resistance	on pin MDC	262.5	500	-	kΩ
R_{pu}	pull-up resistance	on pin MDIO	70	100	130	kΩ
(R)MII interface: pins TXER, TXEN, TXDx, TXC, RXDx, RXDV, RXER, RXC						
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
C_i	input capacitance	[1]	-	-	8	pF

Table 31. Static characteristics *…continued*

T_{vj} = −40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{IH}	HIGH-level input current	V_{IH} = $V_{DD(IO)}$	-	-	200	µA
I_{IL}	LOW-level input current	V_{IL} = 0 V	−20	-	-	µA
R_{pd}	pull-down resistance	on pins TXER, TXEN, TXDx	70	100	130	kΩ
		on pin TXC; reverse MII mode	70	100	130	kΩ
pins RST_N, EN						
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
$V_{hys(i)}$	input hysteresis voltage		0.36	0.5	-	V
C_i	input capacitance	[1]	-	-	8	pF
I_{IH}	HIGH-level input current	at pin RST_N; V_{IH} = $V_{DD(IO)}$	-	-	20	µA
I_{IL}	LOW-level input current	at pin EN; V_{IL} = 0 V	−20	-	-	µA
R_{pd}	pull-down resistance	on pin EN	70	100	130	kΩ
R_{pu}	pull-up resistance	on pin RST_N	70	100	130	kΩ
pin TXCLK						
V_{OH}	HIGH-level output voltage	TEST_MODE = 001, 010, 011 or 100 or SLAVE_JITTER_TEST = 1 (see Table 19); I_{OH} = −4 mA	$V_{DD(IO)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	TEST_MODE = 001, 010, 011 or 100 or SLAVE_JITTER_TEST = 1 (see Table 19); I_{OL} = 4 mA	-	-	0.4	V
pins RXD[3:0], RXER and RXDV during pin strapping						
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
pin WAKE (LED_ENABLE = 0)						
V_{IH}	HIGH-level input voltage	CONFIG_WAKE = 0 (see Table 20)	2.8	-	4.1	V
		CONFIG_WAKE = 1	0.44 × $V_{DD(IO)}$	-	0.64 × $V_{DD(IO)}$	V
V_{IL}	LOW-level input voltage	CONFIG_WAKE = 0	2.4	-	3.75	V
		CONFIG_WAKE = 1	0.38 × $V_{DD(IO)}$	-	0.55 × $V_{DD(IO)}$	V
$V_{hys(i)}$	input hysteresis voltage	CONFIG_WAKE = 0	0.25	-	0.8	V
		CONFIG_WAKE = 1	0.025 × $V_{DD(IO)}$	-	0.2 × $V_{DD(IO)}$	V
I_i	input current	LED driver off	−5	-	+5	µA
pin LED (LED_ENABLE = 1)						
V_{OL}	LOW-level output voltage	LED driver on; I_{LED} = 0.8 mA	-	-	1.4	V
		LED driver on; I_{LED} = 3 mA	-	-	2	V
$I_{O(sc)}$	short-circuit output current	V_{LED} = 40 V			20	mA

Table 31. Static characteristics *…continued*

T_{vj} = −40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
pin INT_N						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	-	-	0.4	V
pin INH						
V_{OH}	HIGH-level output voltage	all modes except Sleep, Power-off; I_{INH} = −1 mA	V_{BAT} − 1	-	V_{BAT}	V
I_{OL}	LOW-level output current	all modes except Sleep, Power-off; V_{INH} = 0 V	−15	−7	−2	mA
I_L	leakage current	Sleep, Power-off modes	−5	-	+5	µA
pins XI, Xo						
C_i	input capacitance	pin XI [1]	-	3.5	-	pF
		pin XO [1]	-	2	-	pF
$g_{m(DC)}$	DC transconductance	Normal, Sleep Request modes; MII_MODE = 00, 01 or 11	13.3	25	47	mA/V
Transmitter test results						
V_{droop}/V_M	droop voltage to peak voltage ratio	100BASE-T1 test mode 1; with respect to initial peak value [1]	−45	-	+45	%
$V_{dist(M)}$	peak distortion voltage	100BASE-T1 test mode 4 [1]	-	-	15	mV
PSDM	power spectral density mask	100BASE-T1 test mode 5				
		f = 1 MHz [1]	−30.9	-	−23.3	dBm
		f = 20 MHz [1]	−35.8	-	−24.8	dBm
		f = 40 MHz [1]	−49.2	-	−28.5	dBm
		f = 57 MHz to 200 MHz [1]	-	-	−36.5	dBm
Transmitter output amplitude						
$V_{oM(TX)}$	transmitter peak output voltage	TX_AMPLITUDE = 00 (see Table 20); $R_{L(dif)}$ = 100 Ω	-	500	-	mV
		TX_AMPLITUDE = 01; $R_{L(dif)}$ = 100 Ω	-	750	-	mV
		TX_AMPLITUDE = 10; $R_{L(dif)}$ = 100 Ω	-	1000	-	mV
		TX_AMPLITUDE = 11; $R_{L(dif)}$ = 100 Ω	-	1250	-	mV
$R_{term(TRX\_P)}$	termination resistance on pin TRX_P	Normal, Sleep Request modes	47.5	50	52.5	Ω
		Standby, Sleep, Disable modes [1]	30	67	85	Ω
$R_{term(TRX\_M)}$	termination resistance on pin TRX_M	Normal, Sleep Request modes	47.5	50	52.5	Ω
		Standby, Sleep, Disable modes [1]	30	67	85	Ω
Temperature protection						
$T_{j(sd)}$	shutdown junction temperature		180	-	200	°C
$T_{j(sd)rel}$	release shutdown junction temperature		147	-	167	°C

Table 31. Static characteristics *…continued*

T_{vj} = −40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(warn)}$	warning junction temperature		155	-	175	°C
$T_{j(warn)rel}$	release warning junction temperature		147	-	167	°C
$T_{j(warn)hys}$	warning junction temperature hysteresis		2	8	-	°C

[1] Guaranteed by design.

10. Dynamic characteristics

Table 32. Dynamic characteristics

T_{vj} = −40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MII transmit timing[1]; see Figure 12						
$T_{clk(TXC)}$	TXC clock period		-	40	-	ns
δ_{TXC}	TXC duty cycle		35	-	65	%
$t_{WH(TXC)}$	TXC pulse width HIGH		14	20	-	ns
$t_{WL(TXC)}$	TXC pulse width LOW		14	20	-	ns
$t_{su(TXD)}$	TXD set-up time	to rising edge on TXC	10	-	-	ns
$t_{su(TXEN)}$	TXEN set-up time	to rising edge on TXC	10	-	-	ns
$t_{su(TXER)}$	TXER set-up time	to rising edge on TXC; transmit coding error	10	-	-	ns
$t_{h(TXD)}$	TXD hold time	from rising edge on TXC	0	-	-	ns
$t_{h(TXEN)}$	TXEN hold time	from rising edge on TXC	0	-	-	ns
$t_{h(TXER)}$	TXER hold time	from rising edge on TXC; transmit coding error	0	-	-	ns
MII receive timing[1]; Figure 13						
$T_{clk(RXC)}$	RXC clock period		-	40	-	ns
δ_{RXC}	RXC duty cycle		35	-	65	%
$t_{WH(RXC)}$	RXC pulse width HIGH		14	20	-	ns
$t_{WL(RXC)}$	RXC pulse width LOW		14	20	-	ns
$t_{d(RXC-RXD)}$	delay time from RXC to RXD	from rising edge on RXC	15	-	25	ns
$t_{d(RXC-RXDV)}$	delay time from RXC to RXDV	from rising edge on RXC	15	-	25	ns
$t_{d(RXC-RXER)}$	delay time from RXC to RXER	from rising edge on RXC	15	-	25	ns
RMII transmit and receive timing[1]; see Figure 14 and Figure 15						
$T_{clk(REF\_CLK)}$	REF_CLK clock period		-	20	-	ns
δ_{REF_CLK}	REF_CLK duty cycle		35	-	65	%
$t_{WH(REF\_CLK)}$	REF_CLK pulse width HIGH		7	10	-	ns
$t_{WL(REF\_CLK)}$	REF_CLK pulse width LOW		7	10	-	ns

Table 32. Dynamic characteristics *...continued*

T_{vj} = −40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(TXD)}$	TXD set-up time	to rising edge on REF_CLK	4	-	-	ns
$t_{su(TXEN)}$	TXEN set-up time	to rising edge on REF_CLK	4	-	-	ns
$t_{h(TXD)}$	TXD hold time	from rising edge on REF_CLK	2	-	-	ns
$t_{h(TXEN)}$	TXEN hold time	from rising edge on REF_CLK	2	-	-	ns
$t_{d(REF\_CLK-RXD)}$	delay time from REF_CLK to RXD	from rising edge on REF_CLK	4	-	13	ns
$t_{d(REF\_CLK-RXER)}$	delay time from REF_CLK to RXER	from rising edge on REF_CLK	4	-	13	ns
$t_{d(REF\_CLK-CRSDV)}$	delay time from REF_CLK to CRSDV	from rising edge on REF_CLK	4	-	13	ns
(R)MII interface timing[1]						
t_f	fall time	from 2 V to 0.8 V				
		MII output pins; C_L = 15 pF; MII mode; MII_DRIVER = 0;	1.3	-	5	ns
		MII output pins; reduced EMC; MII mode; MII_DRIVER = 1; C_L = 7.5 pF	2	-	7.7	ns
		RMII output pins; C_L = 15 pF; RMII mode; MII_DRIVER = 0	0.7	-	2.5	ns
		RMII output pins; reduced EMC; RMII mode; MII_DRIVER = 1; C_L = 7.5 pF	0.9	-	3.4	ns
t_r	rise time	from 0.8 V to 2 V				
		MII output pins; C_L = 15 pF; MII mode; MII_DRIVER = 0	1.3	-	5	ns
		MII output pins; reduced EMC; MII mode; MII_DRIVER = 1; C_L = 7.5 pF	2	-	7.7	ns
		RMII output pins; C_L = 15 pF; RMII mode; MII_DRIVER = 0	0.7	-	2.5	ns
		RMII output pins; reduced EMC; RMII mode; MII_DRIVER = 1; C_L = 7.5 pF	0.9	-	3.4	ns
TXCLK timing[1]						
t_f	fall time	from 2 V to 0.8 V; TEST_MODE = 001, 010, 011 or 100 or SLAVE_JITTER_TEST = 1 (see Table 19); C_L = 15 pF	0.7	-	2.5	ns
t_r	rise time	from 0.8 V to 2 V; TEST_MODE = 001, 010, 011 or 100 or SLAVE_JITTER_TEST = 1 (see Table 19); C_L = 15 pF	0.7	-	2.5	ns
SMI timing[1]; see Figure 16						
$T_{clk(MDC)}$	MDC clock period		400	-	-	ns
$t_{WH(MDC)}$	MDC pulse width HIGH		160	-	-	ns

Table 32. Dynamic characteristics *...continued*

T_{vj} = −40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{WL(MDC)}$	MDC pulse width LOW		160	-	-	ns
$t_{su(MDIO)}$	MDIO set-up time	to rising edge on MDC	10	-	-	ns
$t_{h(MDIO)}$	MDIO hold time	from rising edge on MDC	10	-	-	ns
$t_{d(MDC-MDIO)}$	delay time from MDC to MDIO	from rising edge on MDC; read from PHY	0	-	300	ns
WAKE timing; pin WAKE						
$t_{det(wake)}$	wake-up detection time		10	-	40	µs
$t_{to(PCS-RX)}$ [2]	PCS-RX time-out time	Normal and Sleep Request modes				
		JUMBO_ENABLE = 0	-	1.1	-	ms
		JUMBO_ENABLE = 1	-	2.2	-	ms
Cable test timing						
$t_{to(cbl\_tst)}$	cable test time-out time	Normal mode; CABLE_TEST = 1	-	100	-	µs
LED timing [1]; pin LED						
$t_{on(LED)}$	turn-on time on pin LED	R_L = 1 kΩ; C_L = 100 pF	-	-	10	µs
$t_{off(LED)}$	turn-off time on pin LED	R_L = 1 kΩ; C_L = 100 pF	-	-	10	µs
$t_{w(LED)}$	LED pulse width	R_L = 1 kΩ; C_L = 100 pF; LED_MODE = 10	4	5	10	ms
INH timing [1]; pin INH						
$t_{on(INH)}$	turn-on time on pin INH	R_L = 100 kΩ; C_L = 50 pF; $V_{th(INH)}$ = 2 V	0	2	50	µs
$t_{off(INH)}$	turn-off time on pin INH	R_L = 100 kΩ; C_L = 50 pF; $V_{th(INH)}$ = 2 V	5	50	65	µs
interrupt timing [1]; pin INT_N						
$t_{on(INTN)}$	turn-on time on pin INT_N	R_{pu} = 10 kΩ; C_L = 15 pF	8	-	20	µs
$t_{off(INTN)}$	turn-off time on pin INT_N	R_{pu} = 10 kΩ; C_L = 15 pF	8	-	20	µs
pins RST_N, EN						
$t_{det(rst)}$	reset detection time	on pin RSTN; $V_{uvd(VDDIO)} < V_{DD(IO)} \leq 3.5$ V	5	-	20	µs
$t_{det(EN)}$	detection time on pin EN	$V_{uvd(VDDIO)} < V_{DD(IO)} \leq 3.5$ V	5	-	20	µs
Transmitter test results						
$t_{jit(RMS)}$	RMS jitter time	Master mode	-	-	50	ps
		Slave mode (with link); SLAVE_JITTER_TEST = 1 [1] [3]	-	-	150	ps
Undervoltage detection						
$t_{det(uv)(VBAT)}$	undervoltage detection time on pin V_{BAT}	V_{BAT} = 2.7 V [1]	0	-	30	µs
$t_{det(uv)VDDA(3V3)}$	undervoltage detection time on pin $V_{DDA(3V3)}$	$V_{DDA(3V3)}$ = 2.8 V [1]	2	-	30	µs
$t_{rec(uv)VDDA(3V3)}$	undervoltage recovery time on pin $V_{DDA(3V3)}$	$V_{DDA(3V3)}$ = 3.2 V [1]	2	-	30	µs
$t_{det(uv)VDD(IO)}$	undervoltage detection time on pin $V_{DD(IO)}$	$V_{DD(IO)}$ = 2.8 V [1]	2	-	30	µs

Table 32. Dynamic characteristics *...continued*

T_{vj} = −40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{rec(uv)VDD(IO)}$	undervoltage recovery time on pin $V_{DD(IO)}$	$V_{DD(IO)}$ = 3.2 V [1]	2	-	30	µs
$t_{to(uvd)}$	undervoltage detection time-out time	Normal, Standby, Sleep Request and Disable modes	300		670	ms
General timing parameters						
$t_{s(pon)}$	power-on settling time	from power-on to Standby mode	-	-	2	ms
$t_{init(PHY)}$	PHY initialization time	from Standby mode to Normal mode	-	-	2	ms
$t_{to(req)sleep}$	sleep request time-out time	SLEEP_REQUEST_TO = 00	360	-	500	µs
		SLEEP_REQUEST_TO = 01	900	-	1150	µs
		SLEEP_REQUEST_TO = 10	3.6	-	4.4	ms
		SLEEP_REQUEST_TO = 11	14.4	-	17.6	ms
$t_{det(wake)}$	wake-up detection time	on bus pins TRX_P and TRX_M	-	-	0.7	ms
$t_{to(pd)autn}$	autonomous power-down time-out time	Normal mode; AUTO_PWD = 1	1	-	2	s
t_{PD}	propagation delay	from MII to MDI; Normal mode [1]	140	-	300	ns
		from MDI to MII; Normal mode [1]	760	-	920	ns
		from RMII to MDI; Normal mode [1]	190	-	540	ns
		from MDI to RMII; Normal mode [1]	700	-	1070	ns

[1] Guaranteed by design.

[2] rcv_max_timer in 100BASE-T1; Ref. 2.

[3] Measured at the EN pin, representing the transmit clock (TX_CLK).

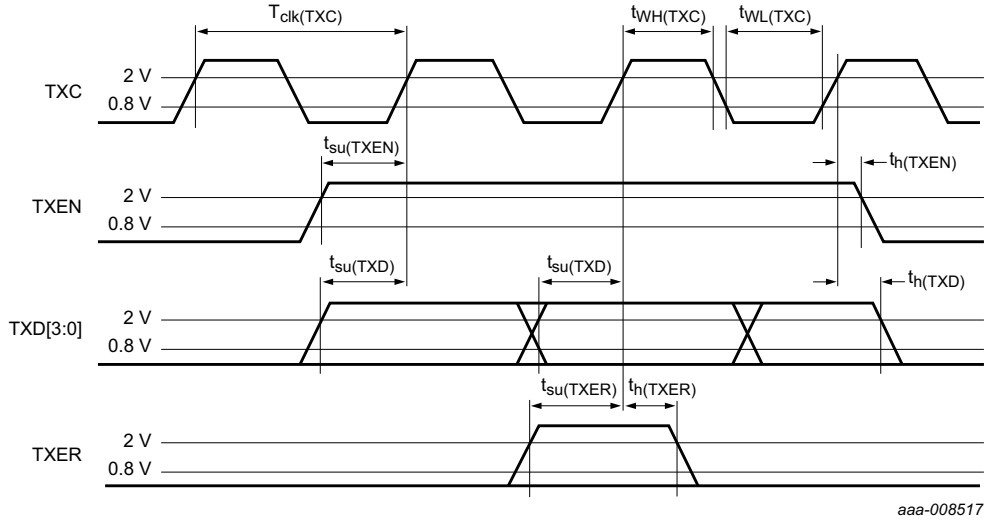


Fig 12. MII transmit timing diagram

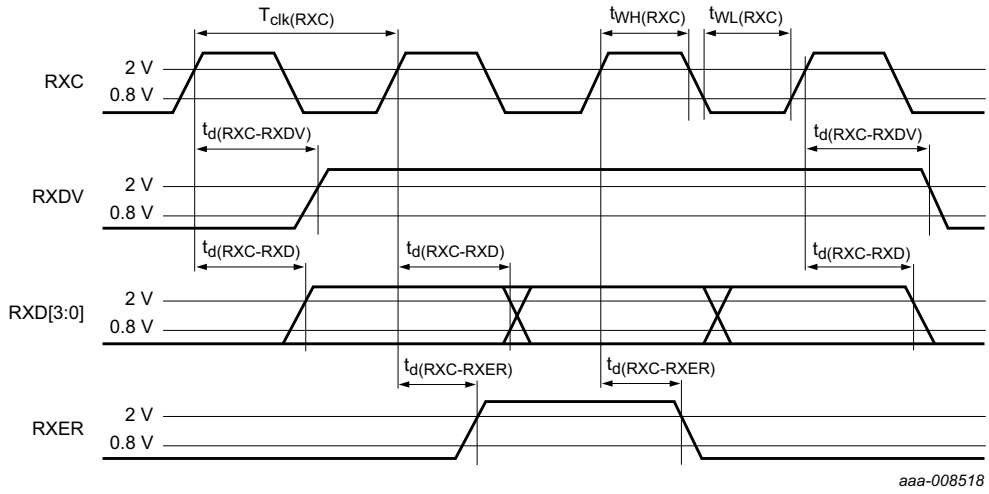


Fig 13. MII receive timing diagram

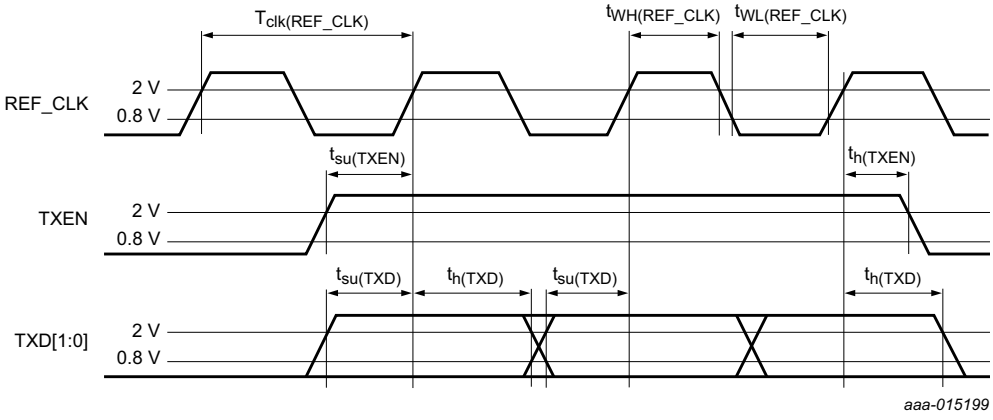


Fig 14. RMII transmit timing diagram

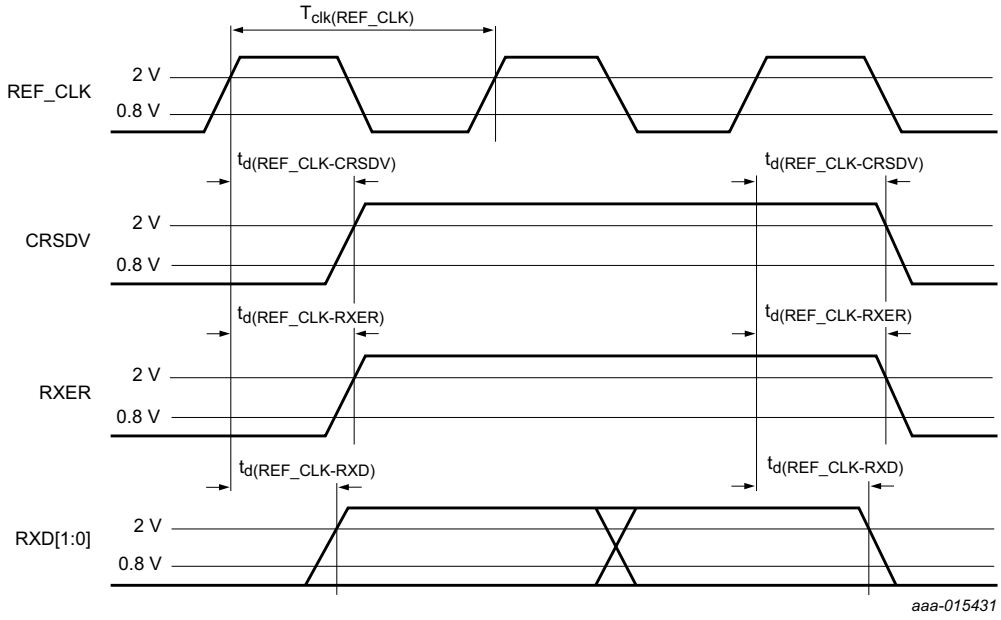


Fig 15. RMII receive timing diagram

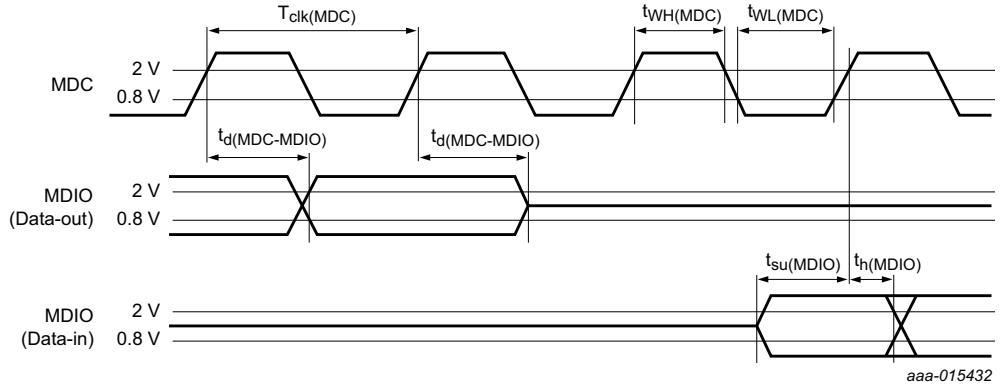


Fig 16. SMI timing diagram

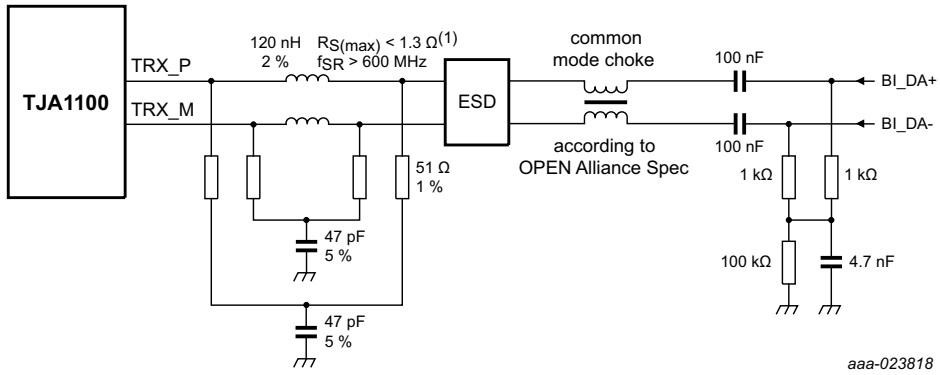
11. Application information

The MDI interface connects the PHY to the twisted pair cable and consists of the following elements, illustrated from left to right in Figure 17:

- low-pass filter
- ESD protection
- common-mode choke
- capacitive coupling
- common-mode termination (optional)
- connector head/plug

Minimum requirements for these components are shown. Robustness requirements depend on the application. Further information can be found in the TJA1100 application hints [Ref. 1].

The MDI interface acts as termination for the transmission line of the balanced 100 Ω cable. Any deviation from the nominal 100 Ω at the MDI interface will cause a portion of the incoming signal to be reflected. The amount of reflected signal is measured by the Return Loss parameter (over frequency) and must not exceed the limits specified in 100BASE-T1 [Ref. 2].



(1) $R_{S(max)}$ = maximum series resistance; f_{SR} = self resonant frequency

Fig 17. MDI application diagram

It is advised to use a PESD2ETH diode to protect against shorts to bus lines greater than 5 V. The supply terminal of the diode should be connected to a 3.3 V domain that is available when the TJA1100 is active. The diode layout should be symmetrical, as shown in the routing scheme example in Figure 18.

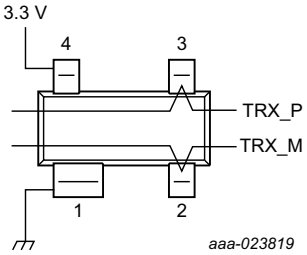


Fig 18. ESD diode trace routing

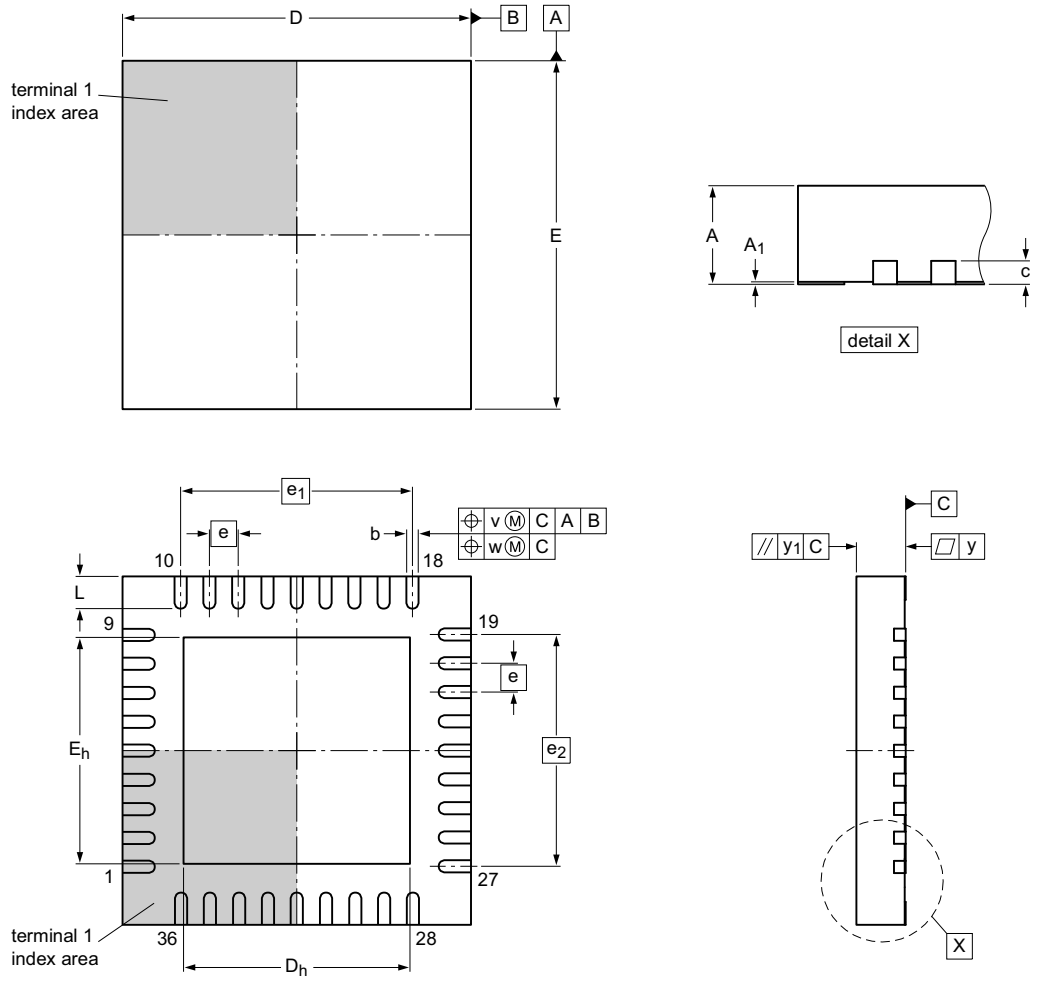
Further details on ESD protection, along with additional recommendations, can be found in the TJA1100 applications hints, Ref. 1.

12. Package information

The TJA1100 comes in the HVQFN-36 package as shown in Figure 19. Measuring just 36 mm^2 with a pitch of 0.5 mm, it is particularly suitable for use in PCB space-constrained applications, such as an integrated IP camera module. The package features wettable sides/flanks to allow for optical inspection of the soldering process. The exposed die pad shown in the package diagram should be connected to ground.

13. Package outline

HVQFN36: plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 x 6 x 0.85 mm **SOT1092-2**



Dimensions

Unit		A(1)	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
	max	1.00	0.05	0.30		6.1	4.05	6.1	4.05				0.65				
mm	nom	0.85	0.02	0.21	0.2	6.0	3.90	6.0	3.90	0.5	4	4	0.55	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	3.75	5.9	3.75				0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1092-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1092-2		---	---			~~09-02-23~~ 09-02-24

Fig 19. Package outline SOT1092-2 (HVQFN36)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 20) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 33 and 34

Table 33. SnPb eutectic process (from J-STD-020D)

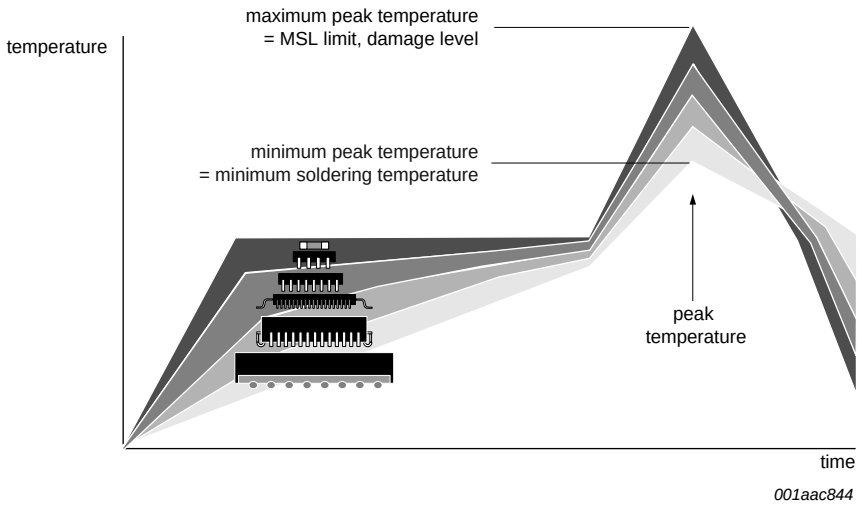
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 34. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 20.



MSL: Moisture Sensitivity Level

Fig 20. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. References

[1] AH1310 TJA1100 Application Hints

[2] IEEE Std 802.3bw-2015, 26 October 2015

16. Revision history

Table 35. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1100 v.3	20170523	Product data sheet	-	TJA1100 v.2.2
Modifications:	• Compliance with 100BASE-T1 IEEE 802.3bw instead of OPEN Alliance BroadR-Reach (OABR): – old specification replaced with new throughout document – reference to BroadR-Reach removed from Figure 1 – Section 6.9: text of 1st paragraph revised – Table 17: text of bit 6 revised – Table 20: text of bit 13 revised – TX Enable removed: Table 23: bit 4 TXEN_CLAMPED removed; bit now reserved Table 24: bit 4 TXEN_CLAMPED_EN removed; bit now reserved Table 32: parameter $t_{detCL(TXEN)}$ removed – Table 32: value of parameter t_{PD} changed • text 'SNR'/'signal-to-noise ratio' replaced by 'SQI'/ 'Signal Quality Indicator' throughout the document • Figure 1 revised: pin names corrected/added • Table 2, Figure 2: TXCLK functionality added to pin 35; associated Table note 3 added in Table 7; description text amended for pins 4 and 16 • Figure 3: low-pass filter (LP) and ESD stages added at input and output • LPS/WUR functions removed as not in line with new TC10 Sleep/Wake-up specification – Section 6.3.2: text of first two paragraphs amended; Figure 9 deleted – Section 6.4: final paragraph deleted – Table 20: bits 0 and 6 now reserved; Table note 4 added – Table 23, Table 24: bits 13 and 12 now reserved (interrupts removed) • Section 6.10.2: 2nd paragraph deleted, replaced by Table 9 • Section 6.10.6: polarity detection re-introduced; POLARITY_DETECT added (bit 6) in Table 27 • Section 6.10.8 restructured/revised – Section 6.10.8.2: reference to open link in Figure 10 replaced with 'terminated MDI', and text in preceding paragraph changed accordingly • PHY identification register 3 for manufacturer's firmware revision number added: – register 16 added to Table 11 – Table 18 added • Table 16: value of bits REVISION_NO changed • Table 21: Table note 2 added • Table 23: description of bit 0 clarified • Table 25: changed description for bits 7:5 • Table 31: parameter values/conditions changed - I_{BAT}, $V_{DDD(3V3)}$, P; V_{OH} and V_{OL} parameters added for pin TXCLK • Table 32: parameter values/conditions changed - (R)MII rise and fall times (t_r and t_f); INT_N timing parameters added, $t_{w(LED)}$ added, t_f and t_r parameters added for pin TXCLK • Figure 17 amended (Ethernet terminal connections added; text 'optional' removed) • Figure 18 and associated text amended			

Table 35. Revision history *…continued*

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1100 v.2.2	20160721	Product data sheet	-	TJA1100 v.1
TJA1100 v.1	20160104	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

19. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 23 May 2017
Document identifier: TJA1100

Общество с ограниченной ответственностью «МосЧип» ИНН 7719860671 / КПП 771901001
Адрес: 105318, г.Москва, ул.Щербаковская д.3, офис 1107

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

http://moschip.ru/get-element

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:
moschip.ru
moschip.ru_4
moschip.ru_6
moschip.ru_9