

74CBTLV3257-Q100

Quad 1-of-2 multiplexer/demultiplexer

Rev. 3 — 9 April 2019

Product data sheet

1. General description

The 74CBTLV3257-Q100 provides a quad 1-of-2 high-speed multiplexer/demultiplexer with common select (S) and output enable (\overline{OE}) inputs. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. When pin \overline{OE} = LOW, one of the two switches is selected (low-impedance ON-state) with pin S. When pin \overline{OE} = HIGH, all switches are in the high-impedance OFF-state, independent of pin S. To ensure the high-impedance OFF-state during power-up or power-down, \overline{OE} should be tied to the V_{CC} through a pull-up resistor. The current-sinking capability of the driver determines the minimum value of the resistor.

Schmitt trigger action at control input, makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|--------------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74CBTLV3257D-Q100 | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74CBTLV3257PW-Q100 | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74CBTLV3257BQ-Q100 | -40 °C to +125 °C | DHVQFN16 | plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm | SOT763-1 |

4. Functional diagram

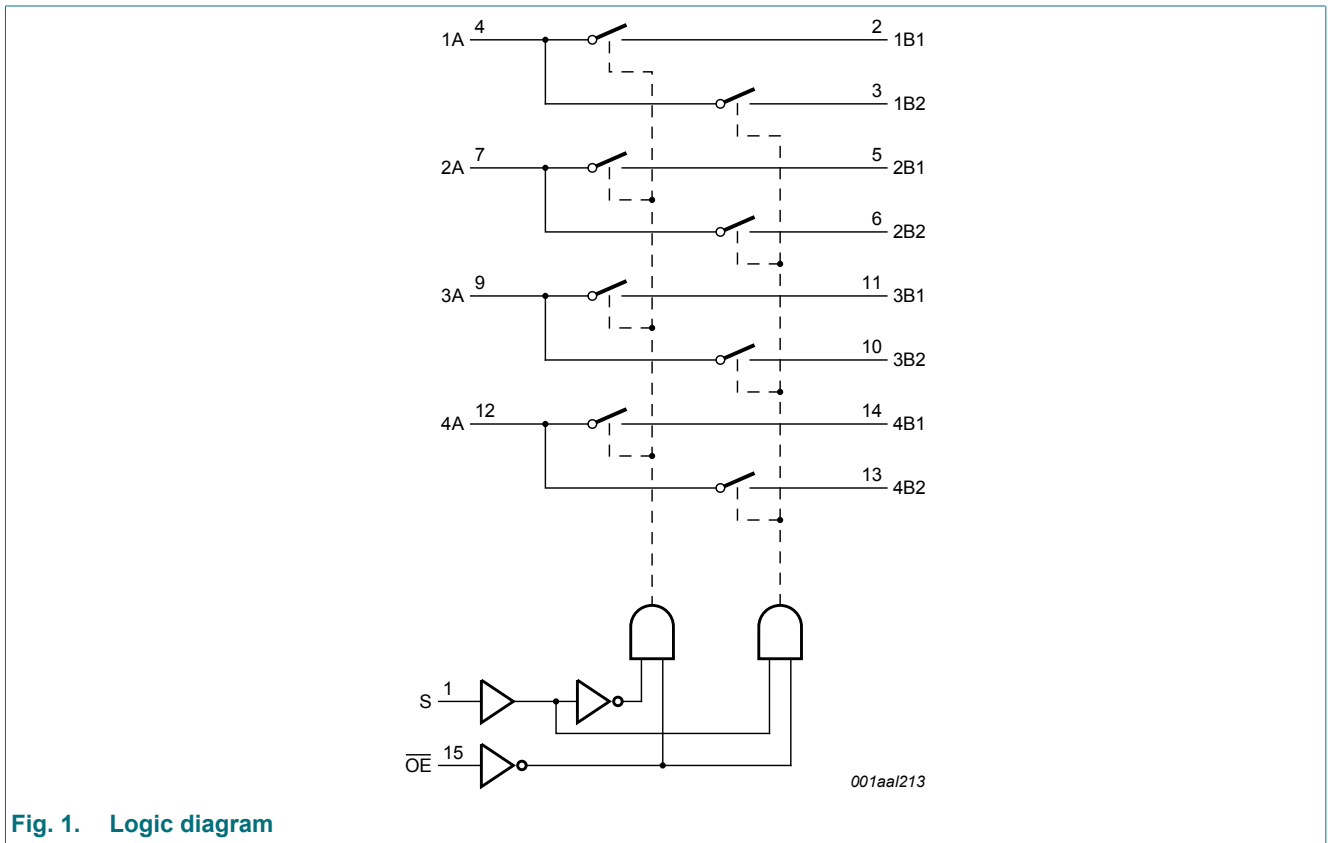


Fig. 1. Logic diagram

5. Pinning information

5.1. Pinning

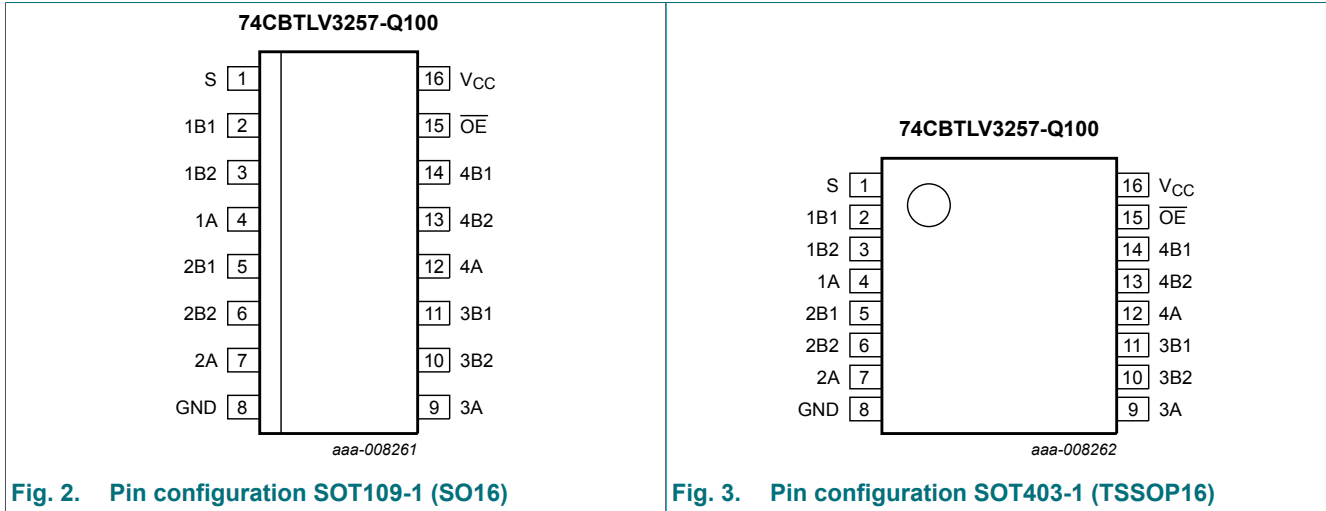


Fig. 2. Pin configuration SOT109-1 (SO16)

Fig. 3. Pin configuration SOT403-1 (TSSOP16)

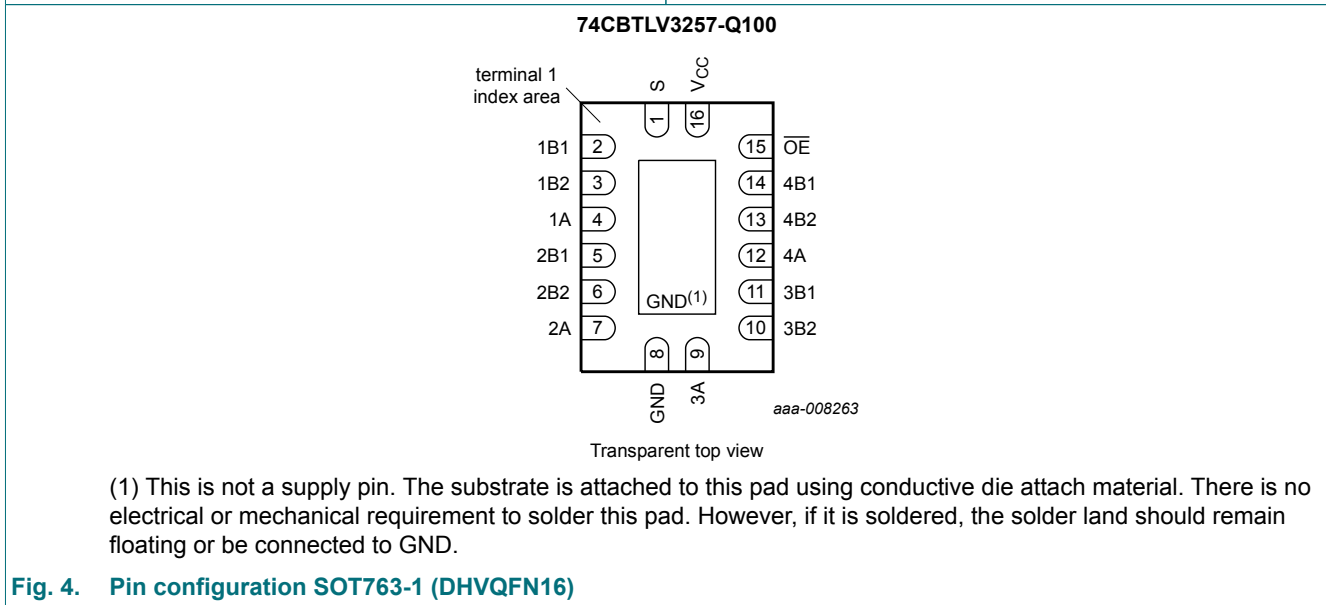


Fig. 4. Pin configuration SOT763-1 (DHVQFN16)

5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------|----------------------------------|
| S | 1 | select input |
| 1B1 to 4B1 | 2, 5, 11, 14 | B1 input/output |
| 1B2 to 4B2 | 3, 6, 10, 13 | B2 input/output |
| 1A to 4A | 4, 7, 9, 12 | A input/output |
| GND | 8 | ground (0 V) |
| OE | 15 | output enable input (active LOW) |
| V _{CC} | 16 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care

| Inputs | | Function switch |
|--------|---|-----------------------|
| OE | S | |
| L | L | nA = nB1 |
| L | H | nA = nB2 |
| H | X | disconnect nA and nBn |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|------|-----------------------|------|
| V _{CC} | supply voltage | | -0.5 | +4.6 | V |
| V _I | input voltage | control inputs [1] | -0.5 | +4.6 | V |
| V _{SW} | switch voltage | enable and disable mode [2] | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | input clamping current | V _I < -0.5 V | -50 | - | mA |
| I _{SK} | switch clamping current | V _I < -0.5 V | -50 | - | mA |
| I _{SW} | switch current | V _{SW} = 0 V to V _{CC} | - | ±128 | mA |
| I _{CC} | supply current | | - | +100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C [3] | - | 500 | mW |

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.

[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed

[3] For TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------------------|--------------------------------------|-----|-----------------|------|
| V _{CC} | supply voltage | | 2.3 | 3.6 | V |
| V _I | input voltage | | 0 | 3.6 | V |
| V _{SW} | switch voltage | enable and disable mode | 0 | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.3 V to 3.6 V [1] | 0 | 200 | ns/V |

[1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

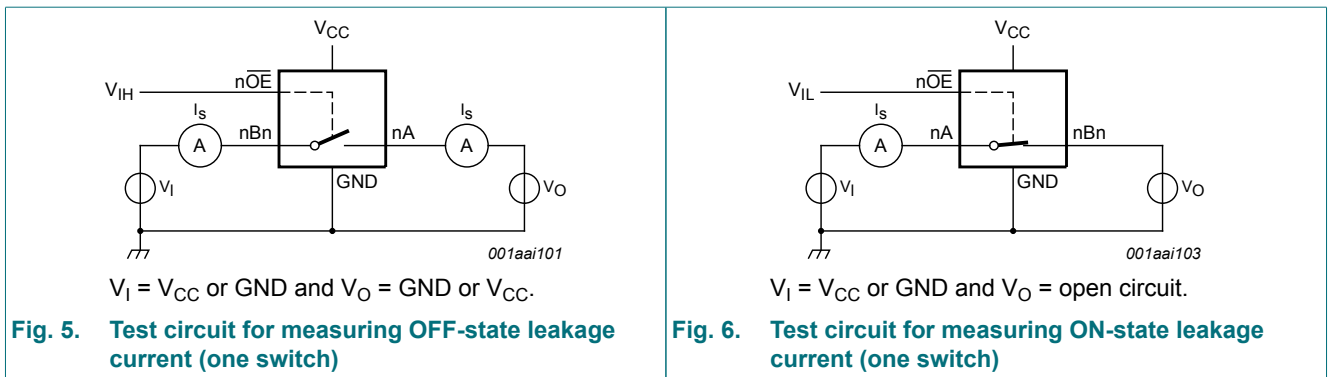
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|---------------------|---------------------------|---|-------------------------------------|--------|-----|--------------------------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | V _{CC} = 3.0 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | V _{CC} = 3.0 V to 3.6 V | - | - | 0.9 | - | 0.9 | V |
| I _I | input leakage current | pin $\overline{\text{OE}}$, S; V _{CC} = 3.6 V; V _I = GND to V _{CC} | - | - | ±1 | - | ±20 | µA |
| I _{S(OFF)} | OFF-state leakage current | V _{CC} = 3.6 V; see Fig. 5 | - | - | ±1 | - | ±20 | µA |
| I _{S(ON)} | ON-state leakage current | V _{CC} = 3.6 V; see Fig. 6 | - | - | ±1 | - | ±20 | µA |
| I _{OFF} | power-off leakage current | V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V | - | - | ±10 | - | ±50 | µA |
| I _{CC} | supply current | V _I = GND or V _{CC} ; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V; I _O = 0 A | - | - | 10 | - | 50 | µA |
| ΔI _{CC} | additional supply current | pin $\overline{\text{OE}}$, S; V _{CC} = 3.6 V; V _I = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC} | [2] | - | 300 | - | 2000 | µA |
| C _I | input capacitance | pin $\overline{\text{OE}}$, S; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V | - | 0.9 | - | - | - | pF |
| C _{S(OFF)} | OFF-state capacitance | V _{CC} = 3.3 V; V _I = 0 V to 3.3 V | - | 5.2 | - | - | - | pF |
| C _{S(ON)} | ON-state capacitance | V _{CC} = 3.3 V; V _I = 0 V to 3.3 V | - | 14.3 | - | - | - | pF |

[1] All typical values are measured at T_{amb} = 25 °C.

[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1. Test circuits



9.2. ON resistance

Table 7. Resistance R_{ON}

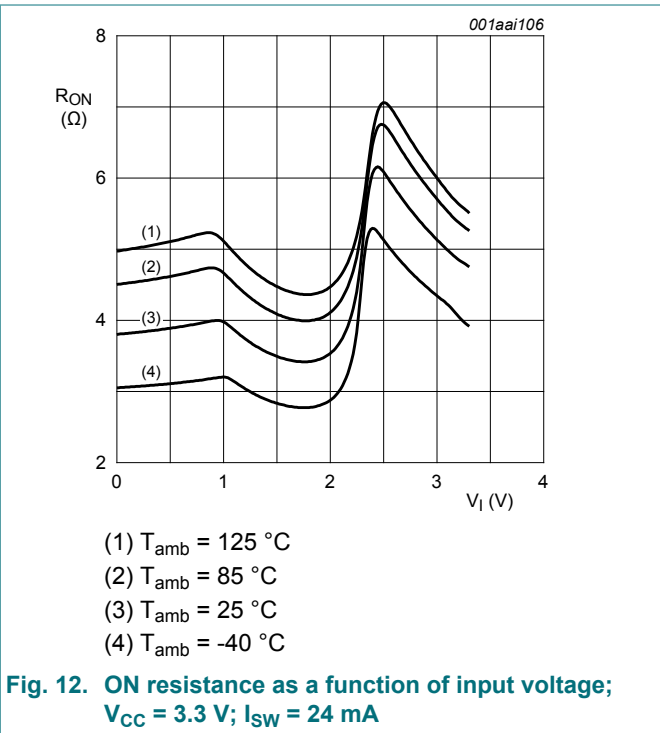
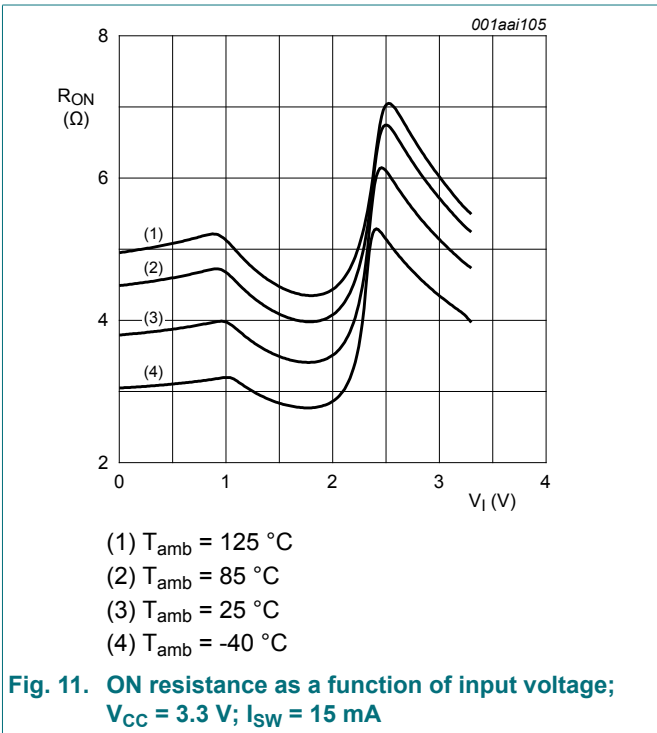
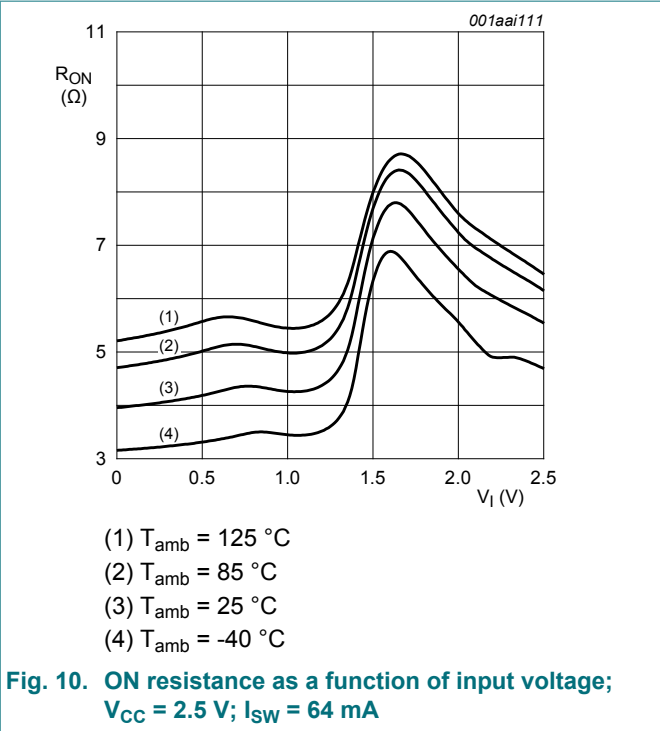
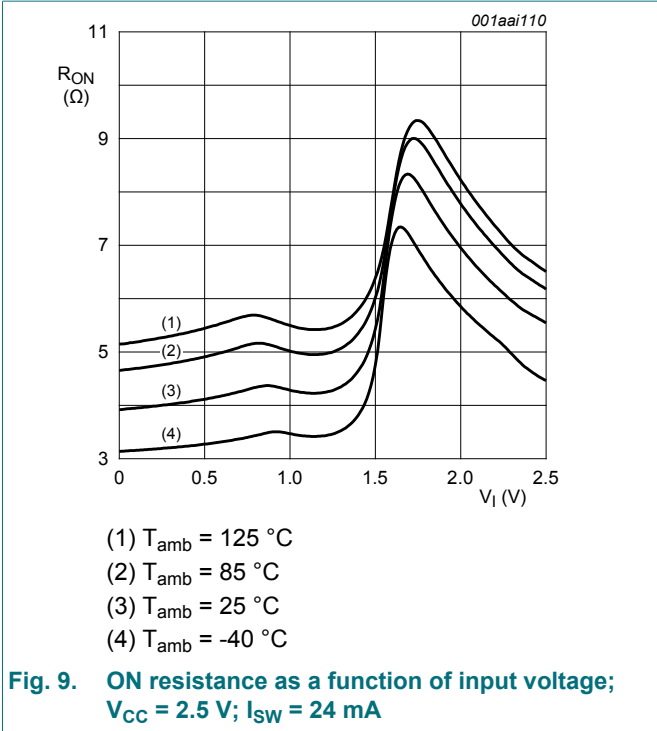
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

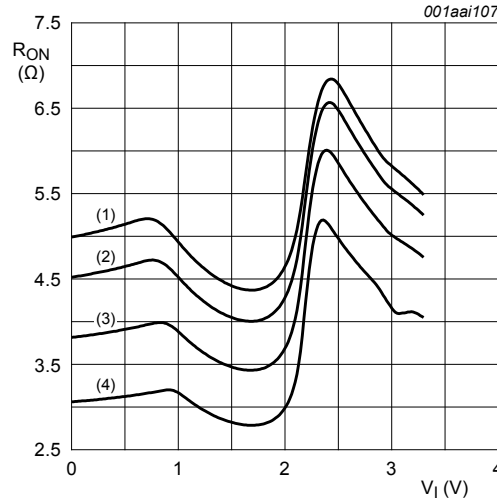
| Symbol | Parameter | Conditions | $T_{amb} = -40\text{ °C to }+85\text{ °C}$ | | | $T_{amb} = -40\text{ °C to }+125\text{ °C}$ | | Unit | |
|----------|---------------|--|---|--------|------|---|------|----------|----------|
| | | | Min | Typ[1] | Max | Min | Max | | |
| R_{ON} | ON resistance | $V_{CC} = 2.3\text{ V to }2.7\text{ V};$ see Fig. 8 to Fig. 10 | [2] | | | | | | |
| | | | $I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$ | - | 4.2 | 8.0 | - | 15.0 | Ω |
| | | | $I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$ | - | 4.2 | 8.0 | - | 15.0 | Ω |
| | | $I_{SW} = 15\text{ mA}; V_I = 1.7\text{ V}$ | - | 8.4 | 40.0 | - | 60.0 | Ω | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V};$ see Fig. 11 to Fig. 13 | $I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$ | - | 4.0 | 7.0 | - | 11.0 | Ω |
| | | | $I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$ | - | 4.0 | 7.0 | - | 11.0 | Ω |
| | | | $I_{SW} = 15\text{ mA}; V_I = 2.4\text{ V}$ | - | 6.2 | 15.0 | - | 25.5 | Ω |

- [1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and nominal V_{CC} .
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.3. ON resistance test circuit and graphs







- (1) $T_{amb} = 125\text{ °C}$
- (2) $T_{amb} = 85\text{ °C}$
- (3) $T_{amb} = 25\text{ °C}$
- (4) $T_{amb} = -40\text{ °C}$

Fig. 13. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$; $I_{SW} = 64\text{ mA}$

10. Dynamic characteristics

Table 8. Dynamic characteristics

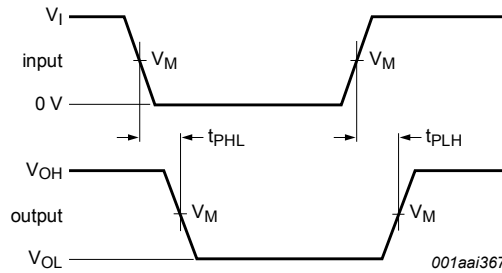
$GND = 0\text{ V}$; for test circuit see Fig. 16

| Symbol | Parameter | Conditions | $T_{amb} = -40\text{ °C to }+85\text{ °C}$ | | | $T_{amb} = -40\text{ °C to }+125\text{ °C}$ | | Unit |
|----------|-------------------|---|--|--------|------|---|------|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| t_{pd} | propagation delay | nA to nBn or nBn to nA; see Fig. 14 [2] [3] | | | | | | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | - | - | 0.15 | - | 0.25 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | - | 0.15 | - | 0.25 | ns |
| | | S to nA; see Fig. 14 [3] | | | | | | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.0 | 3.8 | 6.1 | 1.0 | 6.7 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | 3.2 | 5.3 | 1.0 | 5.8 | ns |
| t_{en} | enable time | \overline{OE} to nA or nBn; see Fig. 15 [4] | | | | | | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.0 | 2.2 | 5.6 | 1.0 | 6.2 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | 2.0 | 5.0 | 1.0 | 5.5 | ns |
| | | S to nBn; see Fig. 15 [4] | | | | | | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.0 | 3.5 | 6.1 | 1.0 | 6.7 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | 3.0 | 5.3 | 1.0 | 5.8 | ns |

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|--------|-----------|------------|-------------------------------------|--------------|--|--------------------------------------|-----|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| | | | t _{dis} | disable time | \overline{OE} to nA or nBn; see Fig. 15 [5] V _{CC} = 2.3 V to 2.7 V V _{CC} = 3.0 V to 3.6 V S to nBn; see Fig. 15 [5] V _{CC} = 2.3 V to 2.7 V V _{CC} = 3.0 V to 3.6 V | | | |
| | | | 1.0 | 2.6 | 5.5 | 1.0 | 6.1 | ns |
| | | | 1.0 | 3.1 | 5.5 | 1.0 | 6.1 | ns |
| | | | 1.0 | 2.6 | 4.8 | 1.0 | 5.3 | ns |
| | | | 1.0 | 3.2 | 4.5 | 1.0 | 5.0 | ns |

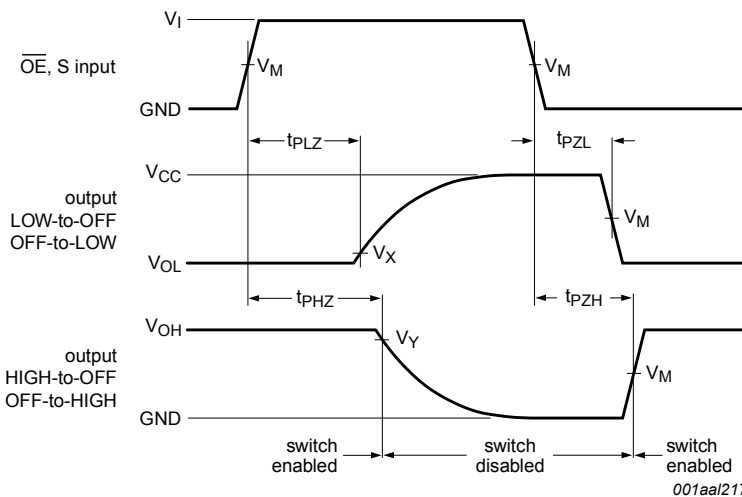
- [1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.
- [2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- [3] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [4] t_{en} is the same as t_{PZH} and t_{PZL}.
- [5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

10.1. Waveforms and test circuit



Measurement points are given in Table 9.
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 14. The data input (nA or nBn) to output (nBn or nA) propagation delays

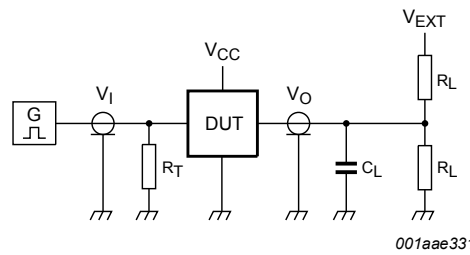


Measurement points are given in Table 9.
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 15. Enable and disable times

Table 9. Measurement points

| Supply voltage | Input | | | Output | | |
|-----------------|--------------------|-----------------|---------------------------------|--------------------|--------------------------|--------------------------|
| V _{CC} | V _M | V _I | t _r = t _f | V _M | V _X | V _Y |
| 2.3 V to 2.7 V | 0.5V _{CC} | V _{CC} | ≤ 2.0 ns | 0.5V _{CC} | V _{OL} + 0.15 V | V _{OH} - 0.15 V |
| 3.0 V to 3.6 V | 0.5V _{CC} | V _{CC} | ≤ 2.0 ns | 0.5V _{CC} | V _{OL} + 0.3 V | V _{OH} - 0.3 V |



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Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 16. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Load | | V _{EXT} | | |
|-----------------|----------------|----------------|-------------------------------------|-------------------------------------|-------------------------------------|
| V _{CC} | C _L | R _L | t _{PLH} , t _{PHL} | t _{PZH} , t _{PHZ} | t _{PZL} , t _{PLZ} |
| 2.3 V to 2.7 V | 30 pF | 500 Ω | open | GND | 2V _{CC} |
| 3.0 V to 3.6 V | 50 pF | 500 Ω | open | GND | 2V _{CC} |

10.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = GND$ or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5$ ns.

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | Unit |
|---------------------|--------------------------|---|--------------------------|-----|-----|------|
| | | | Min | Typ | Max | |
| f _(-3dB) | -3 dB frequency response | V _{CC} = 3.3 V; R _L = 50 Ω; see Fig. 17 [1] | - | 398 | - | MHz |

[1] f_i is biased at 0.5V_{CC}.



Fig. 17. Test circuit for measuring the frequency response when channel is in ON-state

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|------------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note

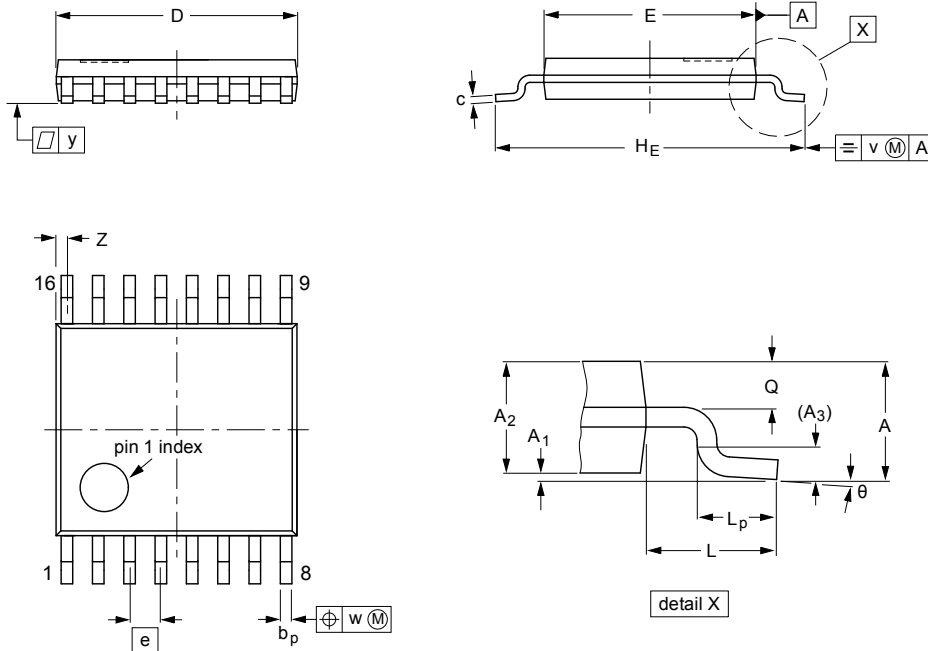
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | 99-12-27 03-02-19 |

Fig. 18. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|---|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.40 0.06 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|--|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | 99-12-27 03-02-18 |

Fig. 19. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

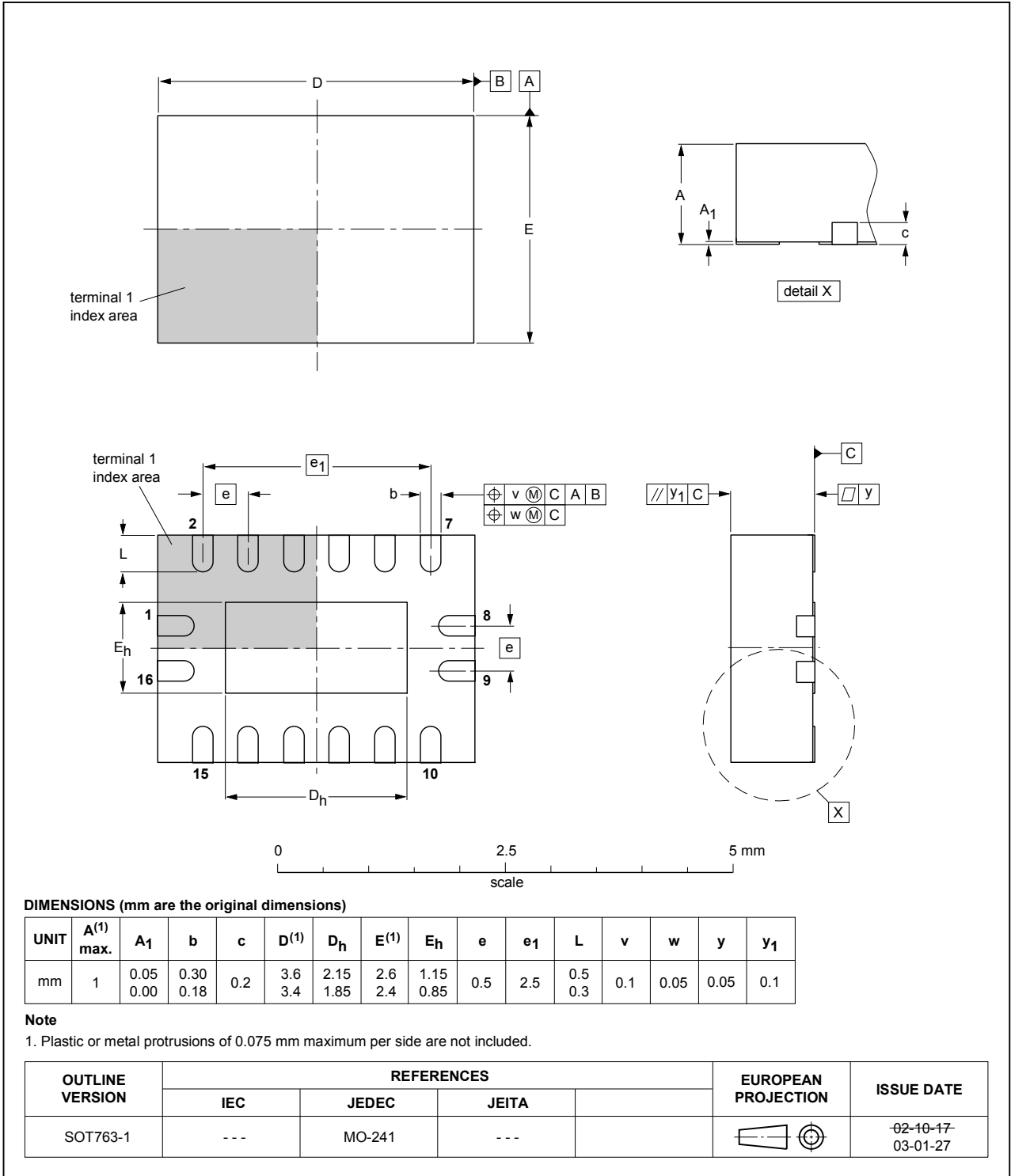


Fig. 20. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |

13. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------------|--|--------------------|---------------|----------------------|
| 74CBTLV3257_Q100 v.3 | 20190409 | Product data sheet | - | 74CBTLV3257_Q100 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74CBTLV3257DS-Q100 (SSOP16/SOT519-1) removed. | | | |
| 74CBTLV3257_Q100 v.2 | 20161110 | Product data sheet | - | 74CBTLV3257_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none"> Section 10.2 added. | | | |
| 74CBTLV3257_Q100 v.1 | 20130704 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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