

BUK7K12-60E

Dual N-channel 60 V, 9.3 m Ω standard level MOSFET

11 December 2013

Product data sheet

1. General description

Dual standard level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with V_{GS(th)} of greater than 1 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	60	V	
I _D	drain current	V _{GS} = 10 V; Tmb = 25 °C; <u>Fig. 1</u>	[1]	-	-	40	Α	
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	68	W	
Static characte	Static characteristics FET1 and FET2							
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11		-	7.64	9.3	mΩ	
Dynamic characteristics FET1 and FET2								
Q_{GD}	gate-drain charge	$I_D = 10 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ °C}; \underline{\text{Fig. 13}}; \underline{\text{Fig. 14}}$		-	11	-	nC	

[1] Continuous current is limited by package.



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Pinning information

Table 2. **Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	8 7 6 5	D1 D1 D2 D2
2	G1	gate1	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		mbk725
7	D1	drain1	1 2 3 4 LFPAK56D (SOT1205)	
8	D1	drain1		

Ordering information

Table 3. **Ordering information**

Type number	Package				
	Name	Description	Version		
BUK7K12-60E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205		

Marking 7.

Marking codes Table 4.

Type number	Marking code
BUK7K12-60E	71260E

Limiting values 8.

Limiting values Table 5.

In accordance with the Absolute Maximum Rating System (IEC 60134).

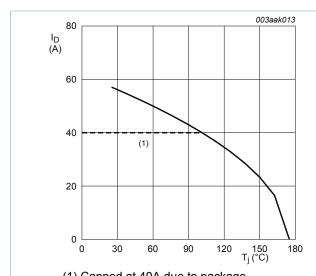
Symbol	Parameter	Conditions		Min	Max	Unit	
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	60	V	
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω		-	60	V	
V _{GS}	gate-source voltage	T _j ≤ 175 °C; DC		-20	20	V	
I _D	drain current	V _{GS} = 10 V; Tmb = 25 °C; <u>Fig. 1</u>	[1]	-	40	Α	
		T _{mb} = 100 °C; V _{GS} = 10 V; <u>Fig. 1</u>	[1]	-	40	Α	
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 4		-	228	Α	
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	68	W	
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Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I _S	source current	T _{mb} = 25 °C	[1]	-	40	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	228	Α
Avalanche Ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 40 A; $V_{sup} \le 60 \text{ V}$; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; Fig. 3	[2][3]	-	103	mJ

- [1] Continuous current is limited by package.
- [2] Refer to application note AN10273 for further information
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



(1) Capped at 40A due to package

Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 10V$$

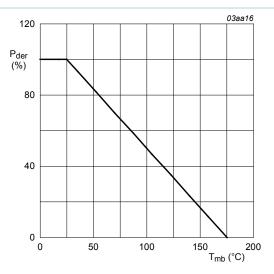


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

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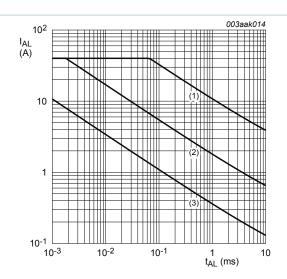
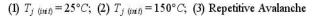


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time



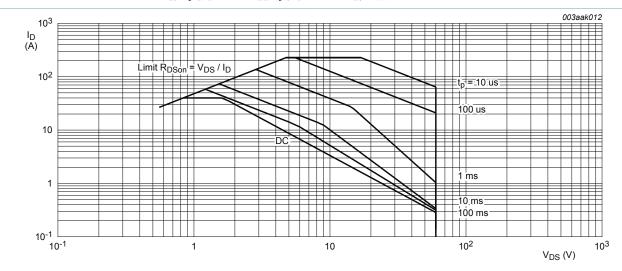


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

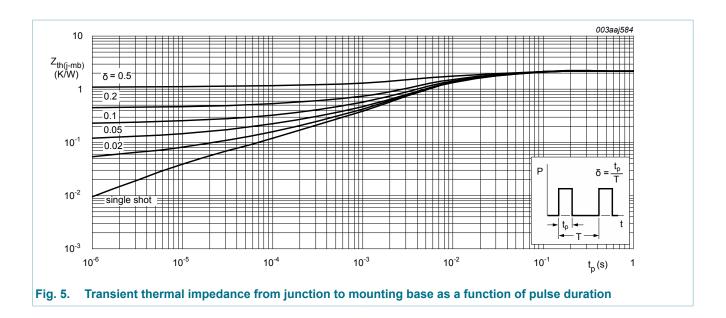
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	2.21	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics FET1 and FET2					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	54	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9; Fig. 10	2.4	3	4	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; Fig. 9; Fig. 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9; Fig. 10	-	-	4.5	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; Fig. 11	-	7.64	9.3	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _j = 175 °C; Fig. 11; Fig. 12	-	17.1	20.8	mΩ
Dynamic ch	naracteristics FET1 and FE	ET2		'		
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 48 V; V _{GS} = 10 V;	-	34.2	-	nC
Q _{GS}	gate-source charge	T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>	-	6.7	-	nC
Q _{GD}	gate-drain charge	1	-	11	-	nC

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;		-	1761	2348	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>		-	247	297	pF
C _{rss}	reverse transfer capacitance			-	155	213	pF
t _{d(on)}	turn-on delay time	V_{DS} = 48 V; R_{L} = 5 Ω ; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω ; T_{j} = 25 °C; I_{D} = 10 A		-	9.1	-	ns
t _r	rise time			-	12.5	-	ns
t _{d(off)}	turn-off delay time			-	23	-	ns
t _f	fall time			-	15	-	ns
Source-dra	ain diode FET1 and FET2		1		'	'	,
V_{SD}	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$		-	0.78	1.2	V
t _{rr}	reverse recovery time	I_S = 10 A; dI_S/dt = -100 A/ μ s; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C		-	25	-	ns
Q _r	recovered charge			-	24	-	nC

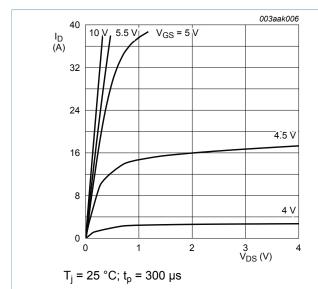


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

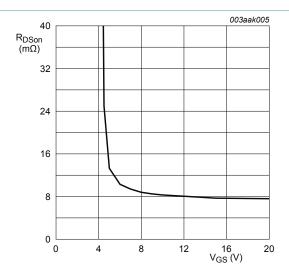


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; I_D = 10A$$

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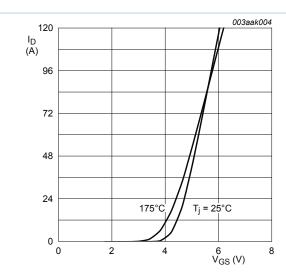


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



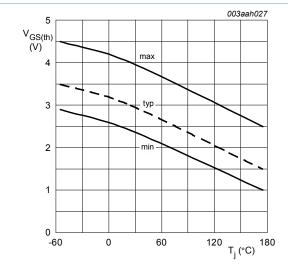


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$$

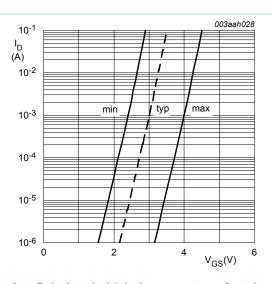


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^{\circ}C; \ V_{DS} = 5V$$

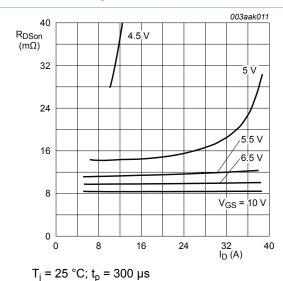


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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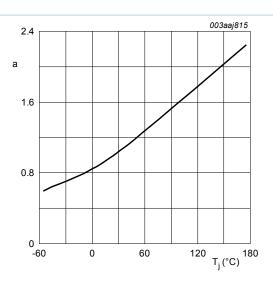


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon (25^{\circ}C)}}$$

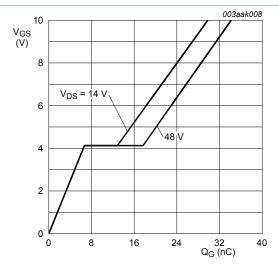


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25$$
°C; $I_D = 10A$

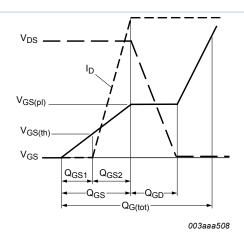


Fig. 13. Gate charge waveform definitions

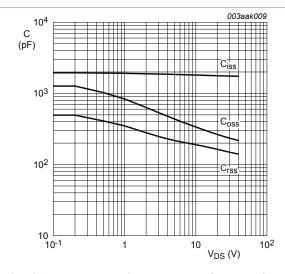


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = \mathbf{0}V; f = \mathbf{1}MHz$$

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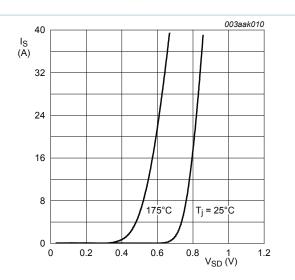


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

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11. Package outline

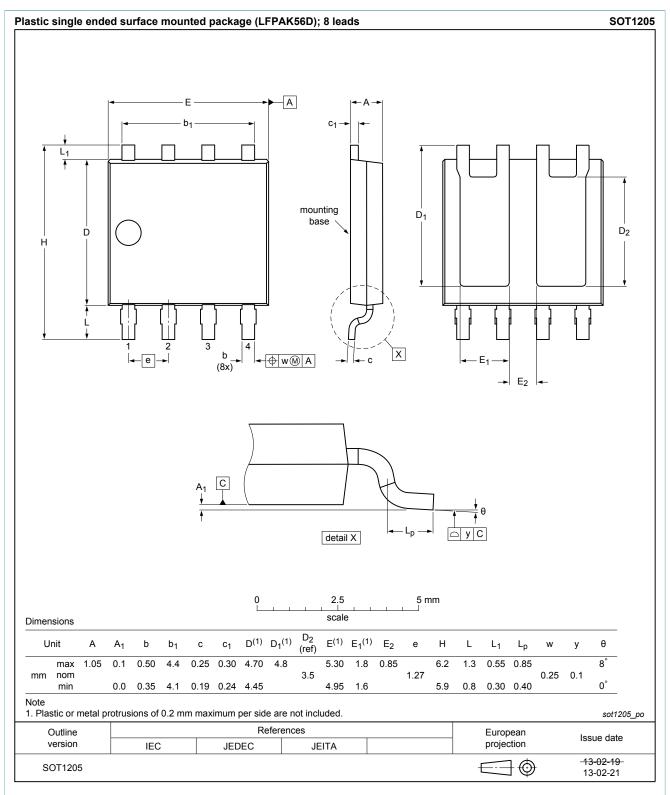


Fig. 17. Package outline LFPAK56D (SOT1205)

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