



PBSS4160PANS

60 V, 1 A NPN/NPN low V_{CEsat} (BISS) transistor

11 February 2015

Product data sheet

1. General description

NPN/NPN low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a leadless medium power DFN2020D-6 (SOT1118D) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

NPN/PNP complement: PBSS4160PANPS. PNP/PNP complement: PBSS5160PAPS.

2. Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- Reduced Printed-Circuit Board (PCB) requirements
- Exposed heat sink for excellent thermal and electrical conductivity
- High energy efficiency due to less heat generation
- Suitable for Automatic Optical Inspection (AOI) of solder joints
- AEC-Q101 qualified

3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- LED lighting
- Power switches (e.g. motors, fans)

4. Quick reference data

Table 1. Quick reference data

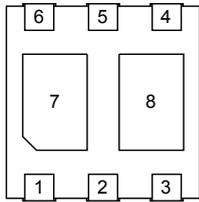
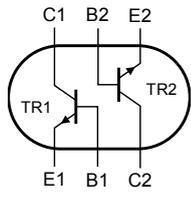
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	60	V
I_C	collector current		-	-	1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	1.5	A



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
R _{CEsat}	collector-emitter saturation resistance	I _C = 0.5 A; I _B = 50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-	240	mΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 <p>Transparent top view DFN2020D-6 (SOT1118D)</p>	 <p><i>sym140</i></p>
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4160PANS	DFN2020D-6	DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118D

7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4160PANS	3F

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CBO}	collector-base voltage	open emitter		-	60	V
V _{CEO}	collector-emitter voltage	open base		-	60	V
V _{EBO}	emitter-base voltage	open collector		-	7	V
I _C	collector current			-	1	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms		-	1.5	A
I _B	base current			-	0.3	A
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms		-	1	A
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
			[5]	-	450	mW
			[6]	-	760	mW
			[7]	-	700	mW
			[8]	-	1450	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
			[5]	-	620	mW
			[6]	-	1040	mW
			[7]	-	960	mW
			[8]	-	2000	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.

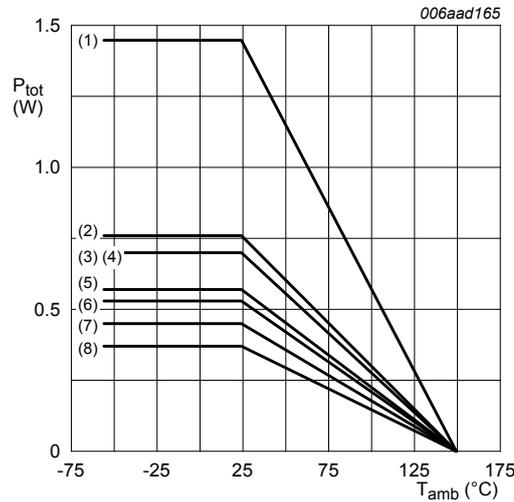
[2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.

[4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm².

[5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.

- [6] Device mounted on an FR4 PCB, single-sided 70 μm copper strip line, tin-plated, mounting pad for collector 1 cm².
- [7] Device mounted on 4-layer PCB 70 μm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 μm copper strip line, tin-plated, mounting pad for collector 1 cm².



- (1) 4-layer PCB 70 μm, mounting pad for collector 1 cm²
- (2) FR4 PCB 70 μm, mounting pad for collector 1 cm²
- (3) 4-layer PCB 70 μm, standard footprint
- (4) 4-layer PCB 35 μm, mounting pad for collector 1 cm²
- (5) FR4 PCB 35 μm, mounting pad for collector 1 cm²
- (6) 4-layer PCB 35 μm, standard footprint
- (7) FR4 PCB 70 μm, standard footprint
- (8) FR4 PCB 35 μm, standard footprint

Fig. 1. Per transistor: power derating curves

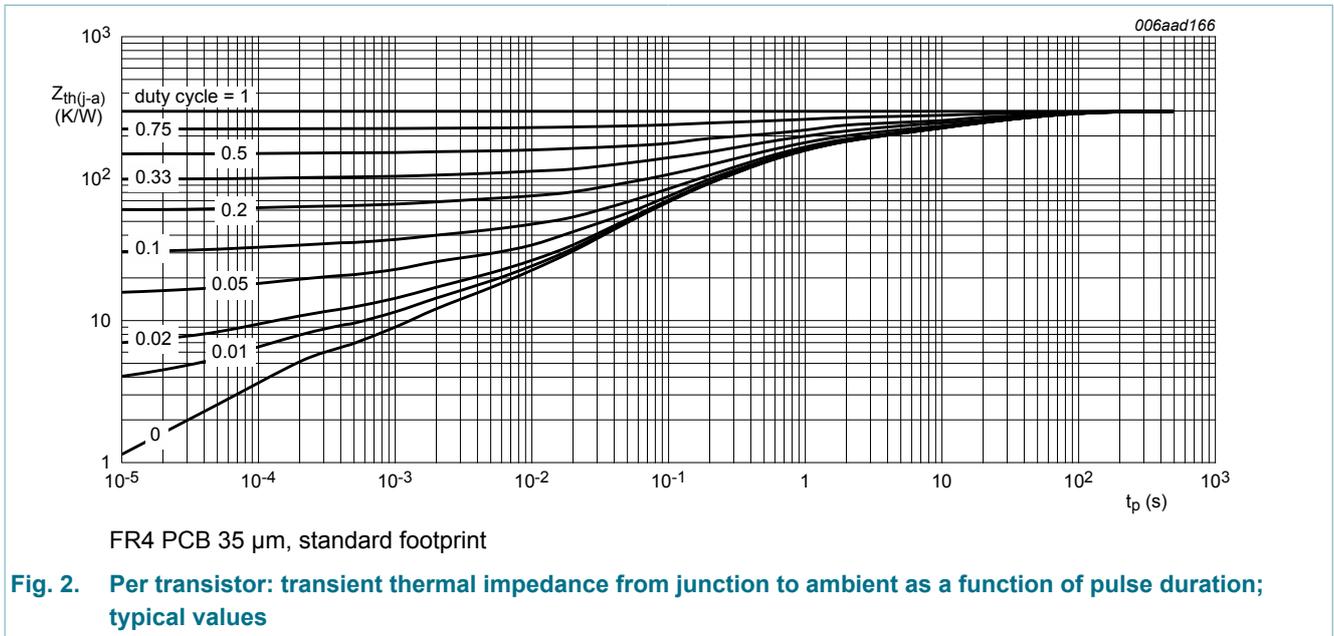
9. Thermal characteristics

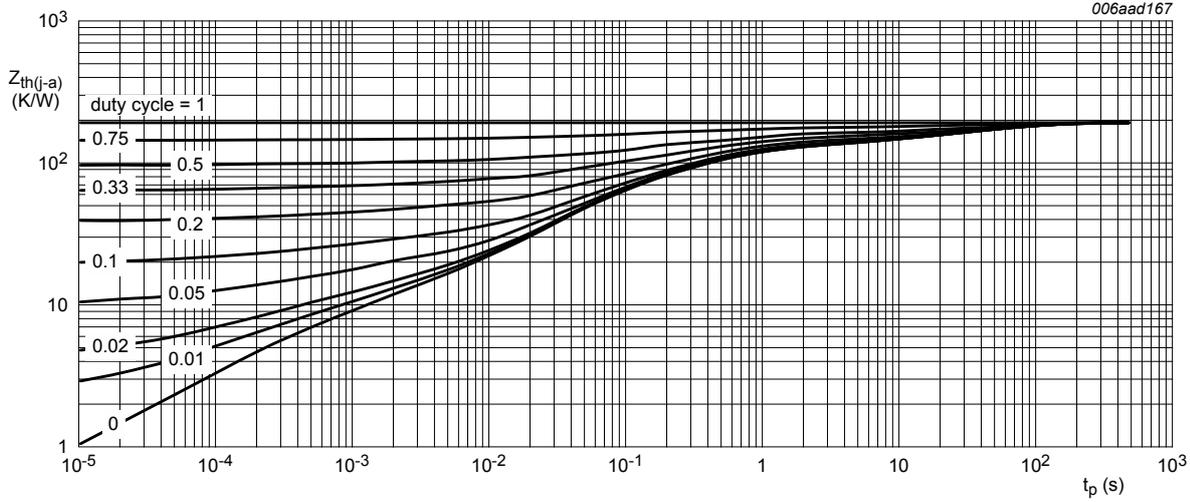
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
			[5]	-	-	278	K/W
			[6]	-	-	164	K/W
			[7]	-	-	179	K/W
			[8]	-	-	86	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	30	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	245	K/W
			[2]	-	-	160	K/W
			[3]	-	-	171	K/W
			[4]	-	-	130	K/W
			[5]	-	-	202	K/W
			[6]	-	-	120	K/W
			[7]	-	-	130	K/W
			[8]	-	-	63	K/W

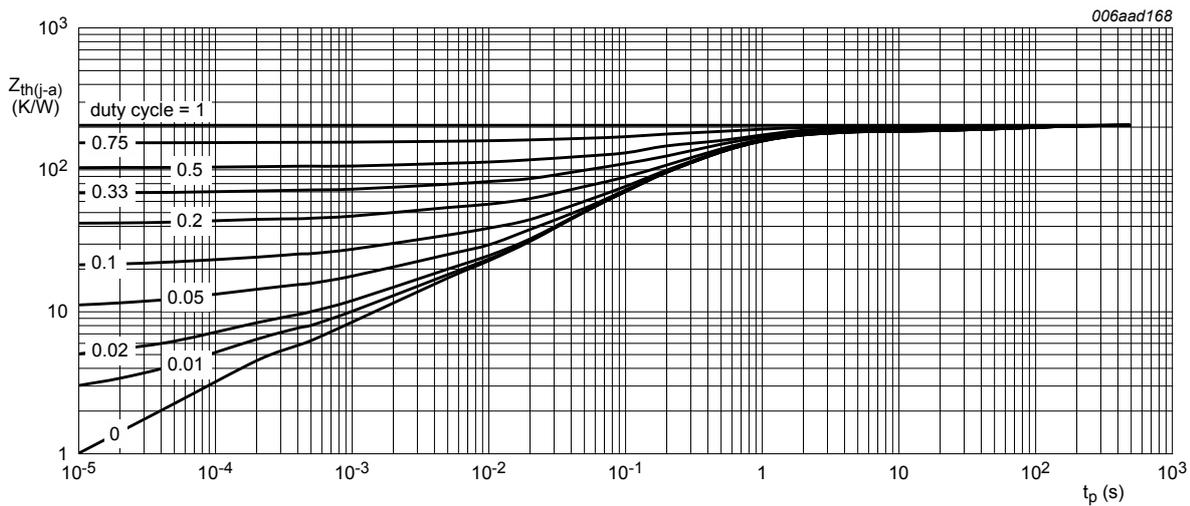
- [1] Device mounted on an FR4 PCB, single-sided 35 μm copper strip line, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided 35 μm copper strip line, tin-plated, mounting pad for collector 1 cm^2 .
- [3] Device mounted on 4-layer PCB 35 μm copper strip line, tin-plated and standard footprint.
- [4] Device mounted on 4-layer PCB 35 μm copper strip line, tin-plated, mounting pad for collector 1 cm^2 .
- [5] Device mounted on an FR4 PCB, single-sided 70 μm copper strip line, tin-plated and standard footprint.
- [6] Device mounted on an FR4 PCB, single-sided 70 μm copper strip line, tin-plated, mounting pad for collector 1 cm^2 .
- [7] Device mounted on 4-layer PCB 70 μm copper strip line, tin-plated and standard footprint.
- [8] Device mounted on 4-layer PCB 70 μm copper strip line, tin-plated, mounting pad for collector 1 cm^2 .





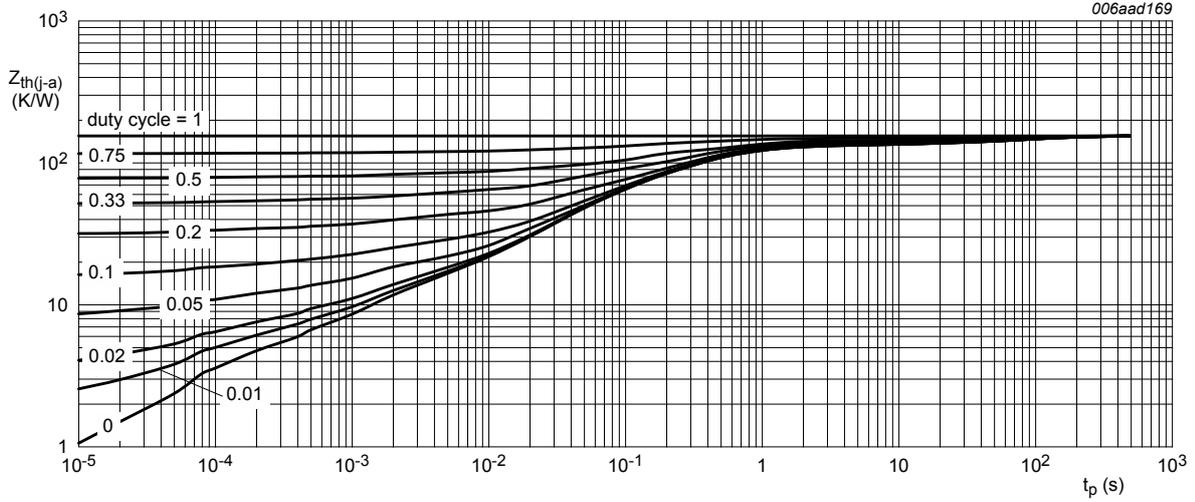
FR4 PCB 35 μ m, mounting pad for collector 1 cm²

Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



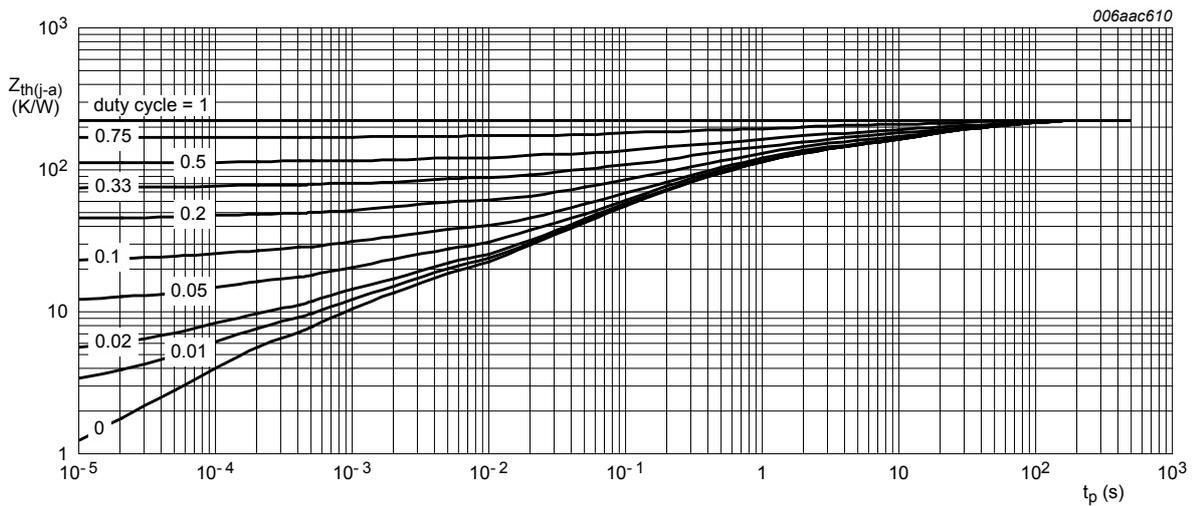
4-layer PCB 35 μ m, standard footprint

Fig. 4. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



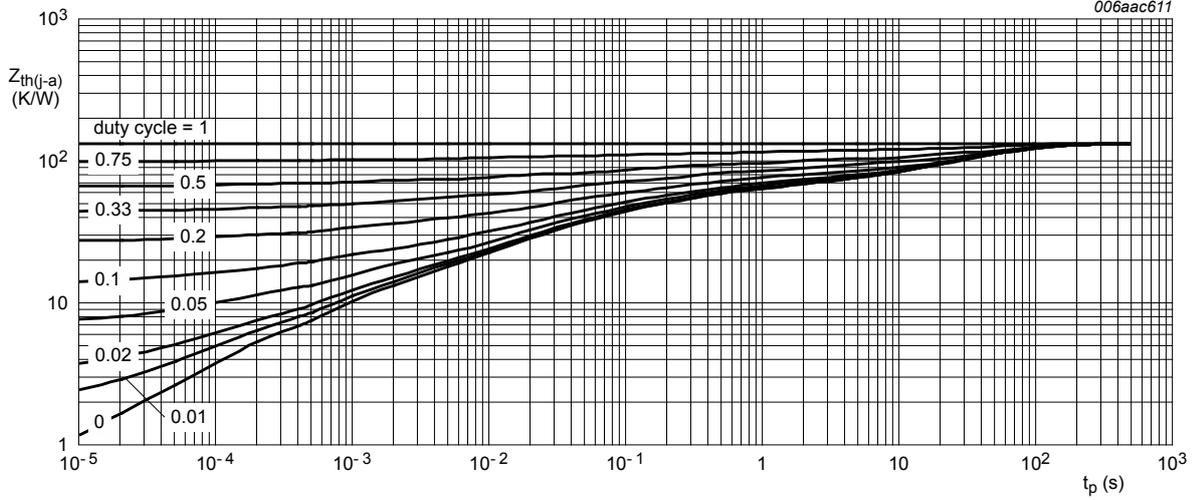
4-layer PCB 35 μm , mounting pad for collector 1 cm^2

Fig. 5. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



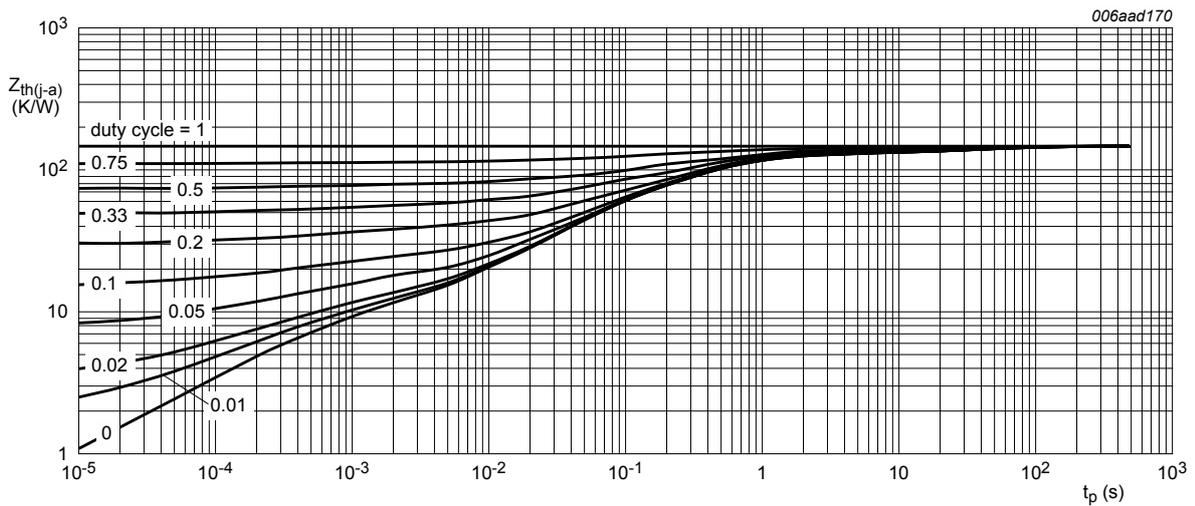
FR4 PCB 70 μm , standard footprint

Fig. 6. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



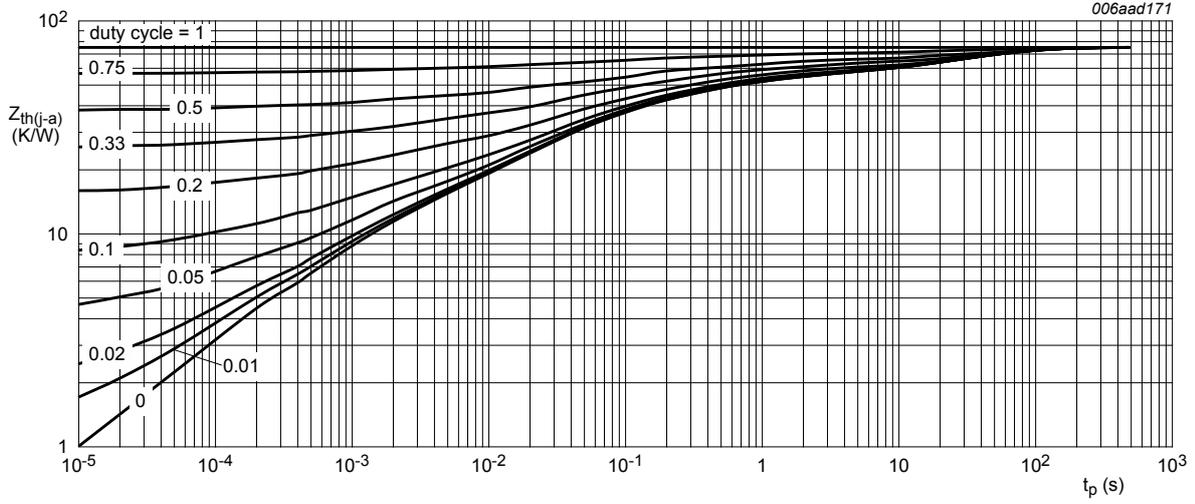
FR4 PCB 70 μm, mounting pad for collector 1 cm²

Fig. 7. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



4-layer PCB 70 μm, standard footprint

Fig. 8. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



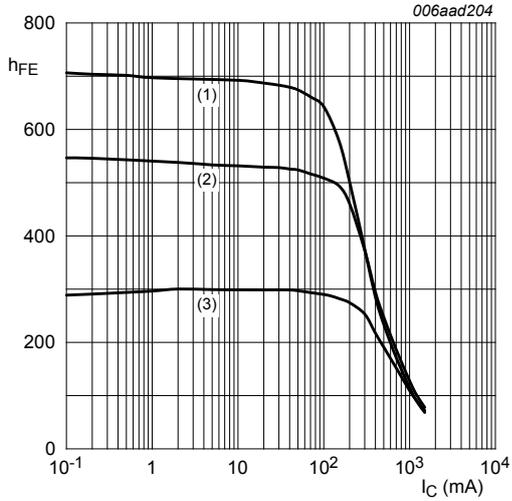
4-layer PCB 70 μm , mounting pad for collector 1 cm^2

Fig. 9. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

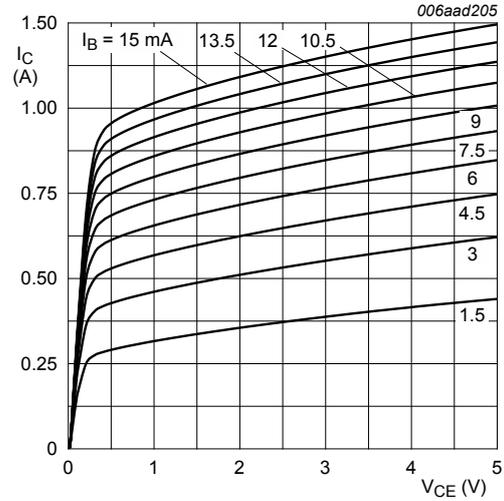
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
I _{CBO}	collector-base cut-off current	V _{CB} = 48 V; I _E = 0 A; T _{amb} = 25 °C	-	-	100	nA
		V _{CB} = 48 V; I _E = 0 A; T _j = 150 °C	-	-	50	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C	-	-	100	nA
h _{FE}	DC current gain	V _{CE} = 2 V; I _C = 100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	290	430	-	
		V _{CE} = 2 V; I _C = 500 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	150	220	-	
		V _{CE} = 2 V; I _C = 1 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	70	110	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 500 mA; I _B = 50 mA; T _{amb} = 25 °C	-	90	120	mV
		I _C = 1 A; I _B = 50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	185	240	mV
		I _C = 1 A; I _B = 100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	175	220	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = 0.5 A; I _B = 50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-	240	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = 500 mA; I _B = 50 mA; T _{amb} = 25 °C	-	-	1	V
		I _C = 1 A; I _B = 50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-	1.1	V
		I _C = 1 A; I _B = 100 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-	1.1	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = 2 V; I _C = 0.5 A; pulsed; t _p ≤ 300 μs; δ ≤ 0.02; T _{amb} = 25 °C	-	-	0.9	V
t _d	delay time	V _{CC} = 10 V; I _C = 500 mA; I _{Bon} = 25 mA; I _{Boff} = -25 mA; T _{amb} = 25 °C	-	15	-	ns
t _r	rise time		-	90	-	ns
t _{on}	turn-on time		-	105	-	ns
t _s	storage time		-	410	-	ns
t _f	fall time		-	130	-	ns
t _{off}	turn-off time		-	540	-	ns
f _T	transition frequency		V _{CE} = 10 V; I _C = 50 mA; f = 100 MHz; T _{amb} = 25 °C	90	175	-
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C	-	4	6	pF



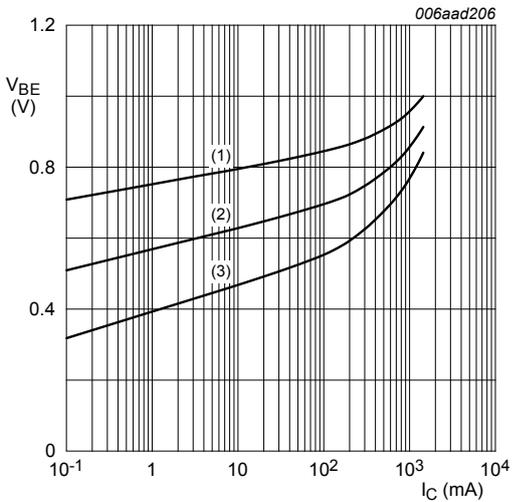
$V_{CE} = 2 V$
 (1) $T_{amb} = 100^\circ C$
 (2) $T_{amb} = 25^\circ C$
 (3) $T_{amb} = -55^\circ C$

Fig. 10. DC current gain as a function of collector current; typical values



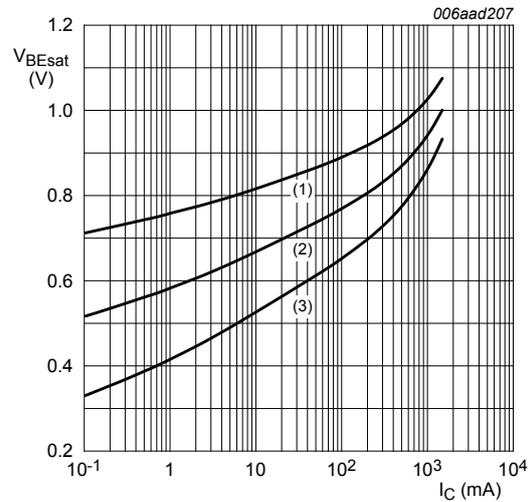
$T_{amb} = 25^\circ C$

Fig. 11. Collector current as a function of collector-emitter voltage; typical values



$V_{CE} = 2 V$
 (1) $T_{amb} = -55^\circ C$
 (2) $T_{amb} = 25^\circ C$
 (3) $T_{amb} = 100^\circ C$

Fig. 12. Base-emitter voltage as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = -55^\circ C$
 (2) $T_{amb} = 25^\circ C$
 (3) $T_{amb} = 100^\circ C$

Fig. 13. Base-emitter saturation voltage as a function of collector current; typical values

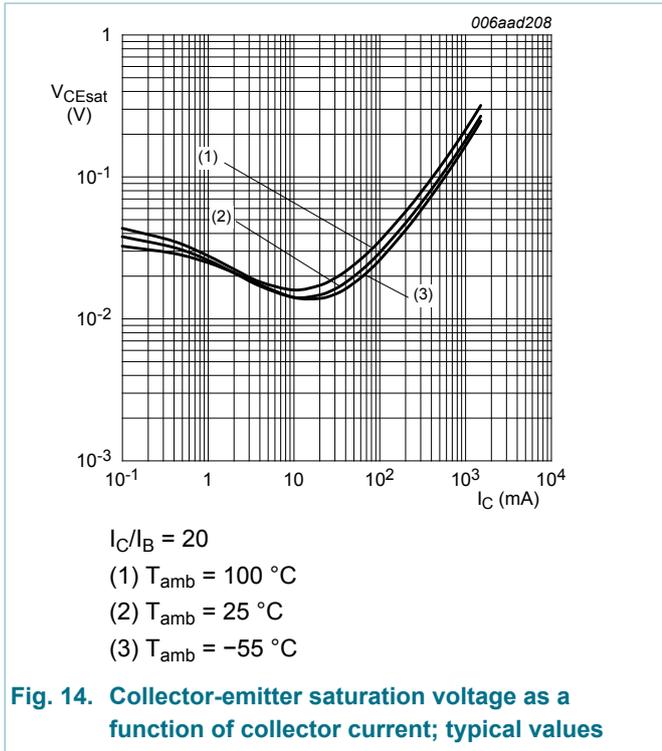


Fig. 14. Collector-emitter saturation voltage as a function of collector current; typical values

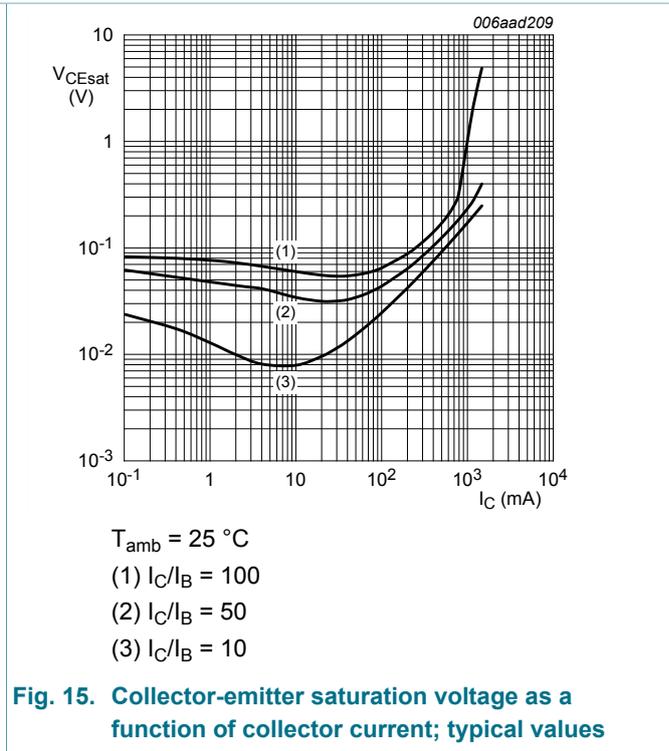


Fig. 15. Collector-emitter saturation voltage as a function of collector current; typical values

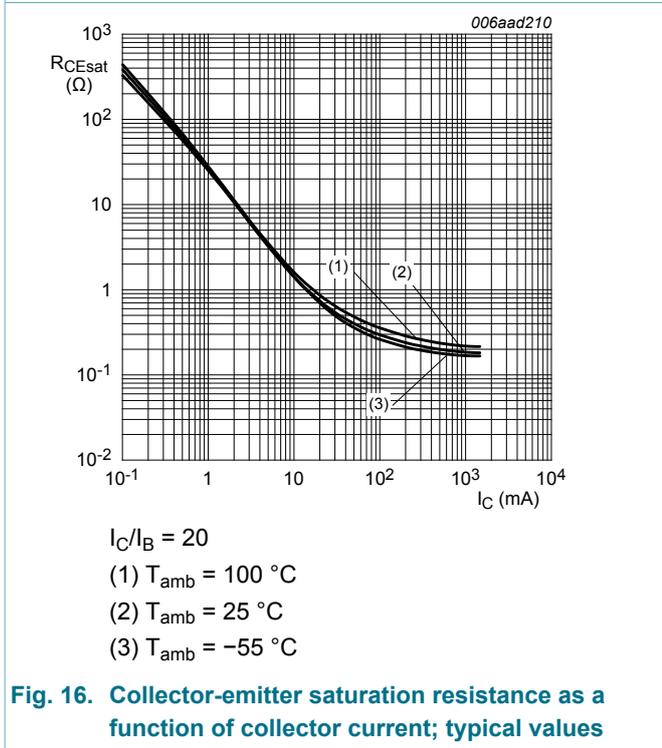


Fig. 16. Collector-emitter saturation resistance as a function of collector current; typical values

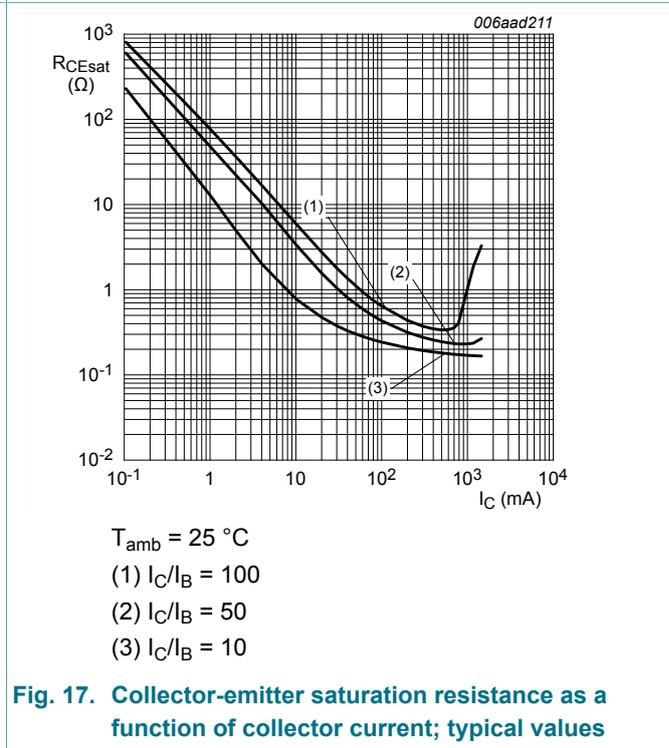


Fig. 17. Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

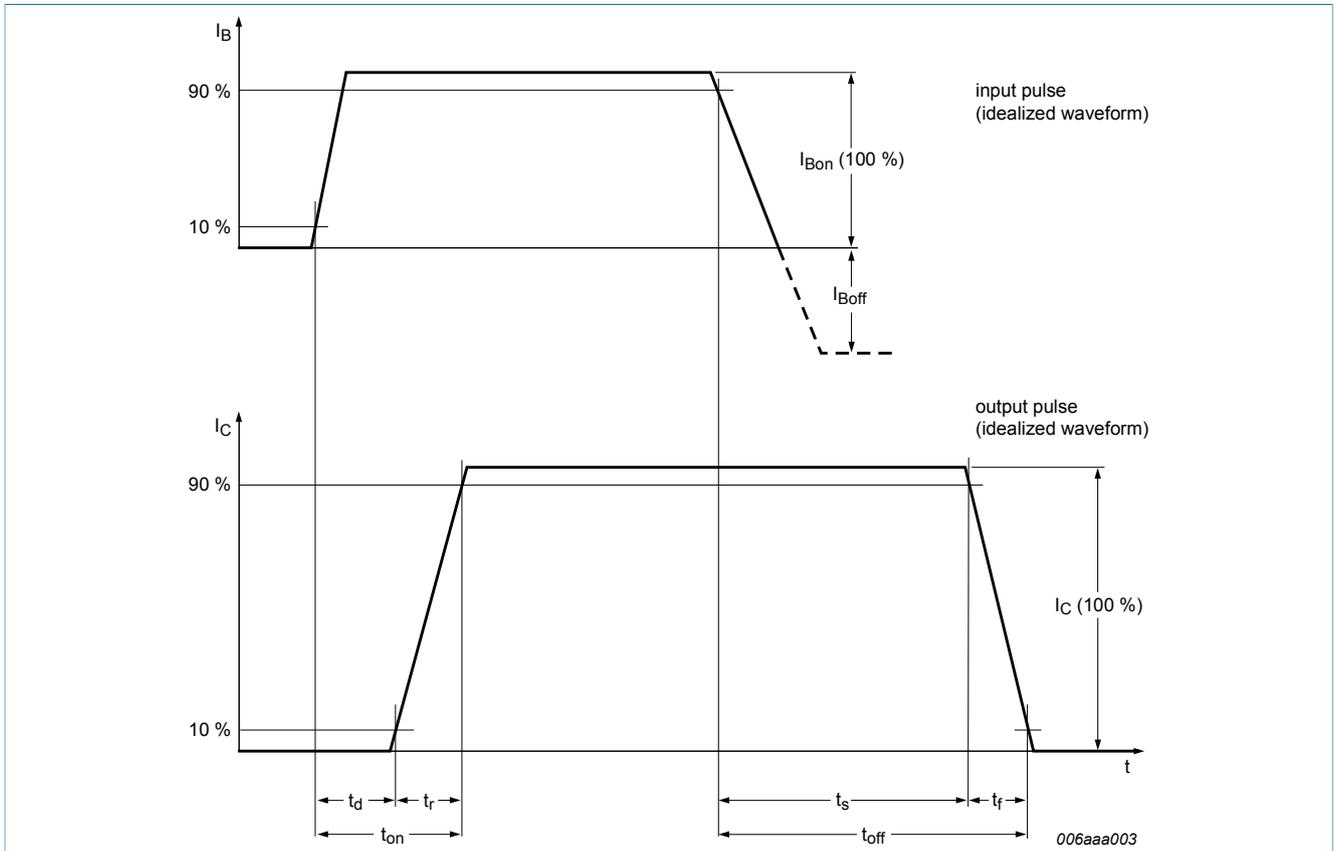


Fig. 18. BISS transistor switching time definition

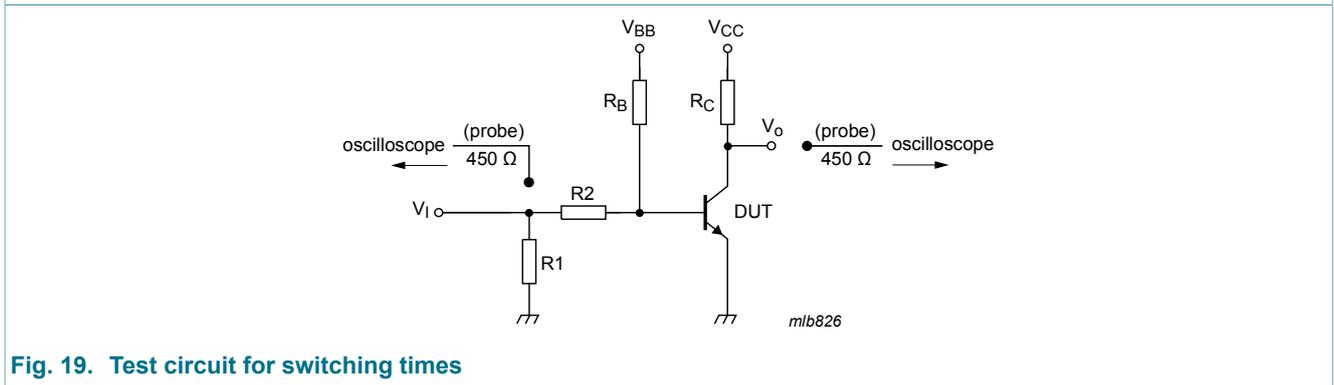


Fig. 19. Test circuit for switching times

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm

SOT1118D

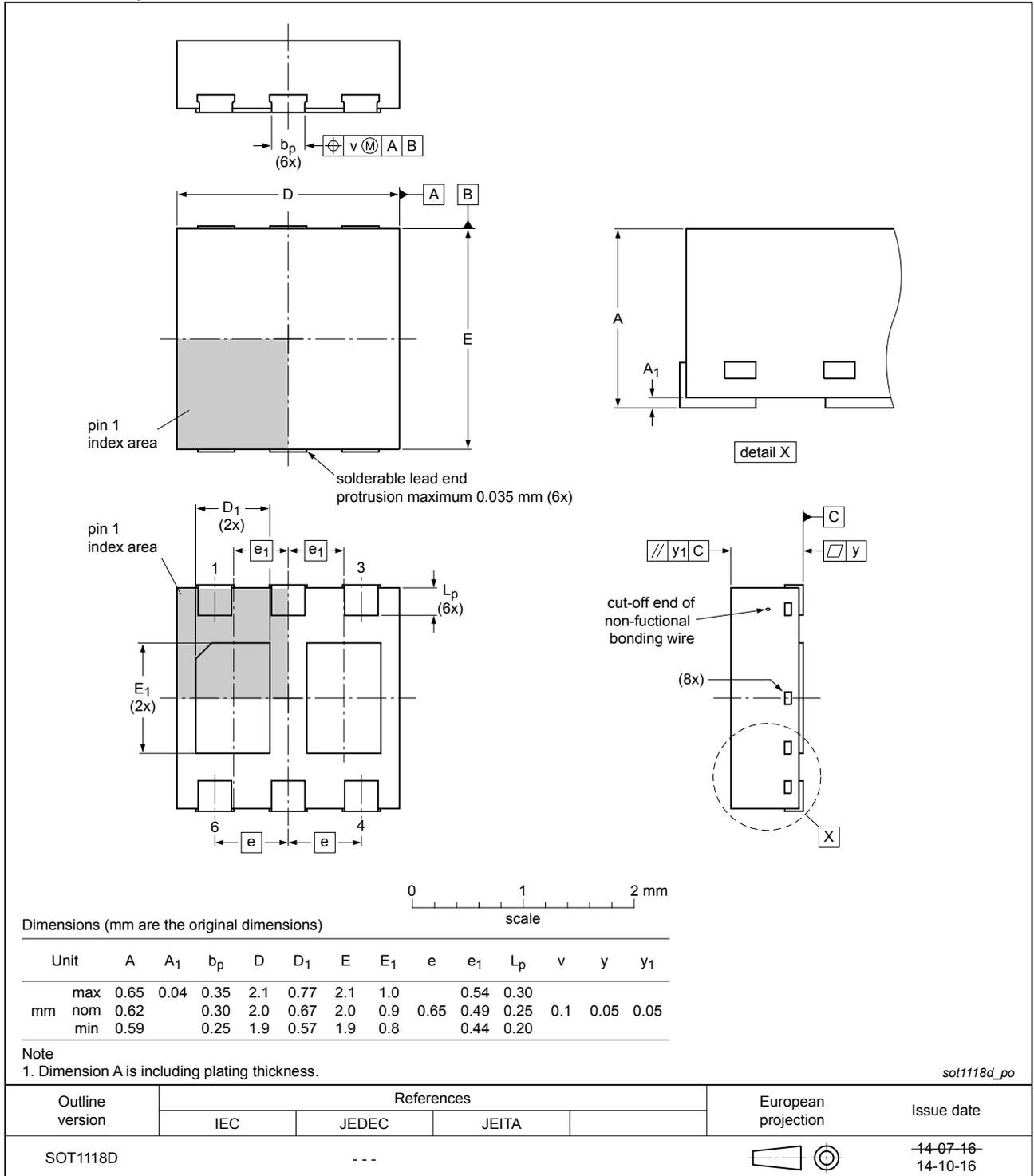


Fig. 20. Package outline DFN2020D-6 (SOT1118D)

13. Soldering

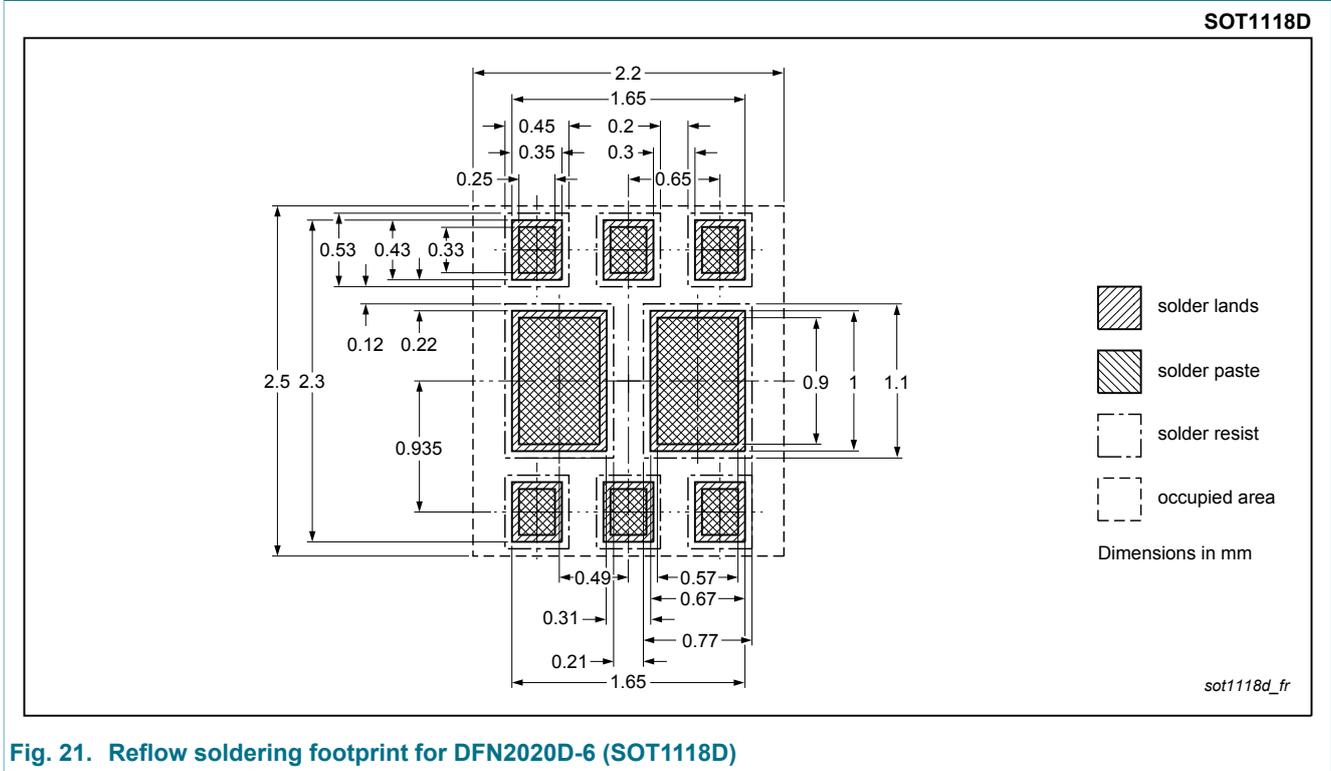


Fig. 21. Reflow soldering footprint for DFN2020D-6 (SOT1118D)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4160PANS v.1	20150211	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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