

NB100LVEP17

2.5V / 3.3V Quad Differential Driver/Receiver

Description

The NB100LVEP17 is a 4-bit differential line receiver. The design incorporates two stages of gain, internal to the device, making it an excellent choice for use in high bandwidth amplifier applications.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

Inputs of unused gates can be left open and will not affect the operation of the rest of the device.

Features

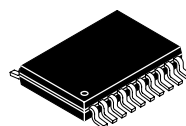
- Maximum Input Clock Frequency > 2.5 GHz Typical
- Maximum Input Data Rate > 2.5 Gb/s Typical
- 250 ps Typical Propagation Delay
- Low Profile QFN Package
- PECL Mode Operating Range: $V_{CC} = 2.375$ V to 3.8 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.8 V
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- V_{BB} Output
- Pb-Free Packages are Available



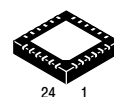
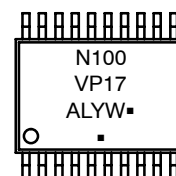
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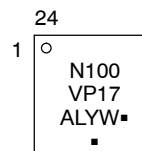
MARKING DIAGRAMS*



TSSOP-20
DT SUFFIX
CASE 948E



24 PIN QFN
MN SUFFIX
CASE 485L



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

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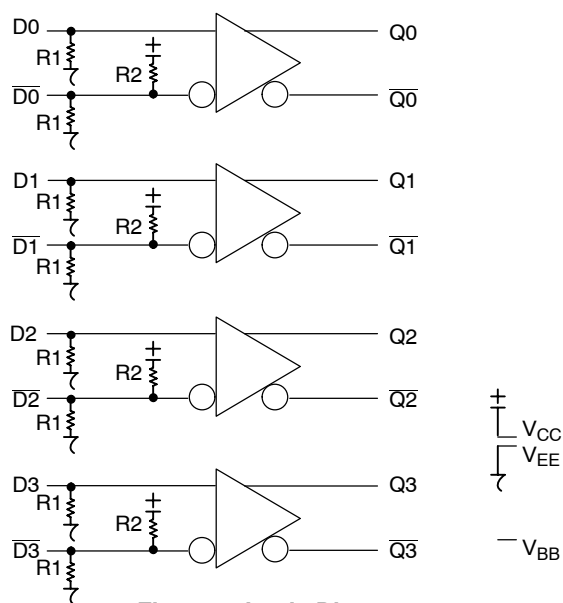


Figure 1. Logic Diagram

Table 1. PIN DESCRIPTION

| Pin | | Name | I/O | Default State | Description |
|-------------|----------------|---------------------|------------|---------------|--|
| TSSOP | QFN | | | | |
| 1,20 | 13,18,21,22,23 | V_{CC} | - | - | Positive Supply Voltage. All V_{CC} Pins Must be Externally Connected to Power Supply to Guarantee Proper Operation. |
| 11 | 10 | V_{EE} | - | - | Negative Supply Voltage. All V_{EE} Pins Must be Externally Connected to Power Supply to Guarantee Proper Operation. |
| 10 | 9 | V_{BB} | - | - | ECL Reference Voltage Output. |
| 2,4,6,8 | 1,3,5,7 | $D[0:3]$ | ECL Input | Low | Noninverted Differential Inputs [0:3]. Internal $75\text{ k}\Omega$ to V_{EE} . |
| 3,5,7,9 | 2,4,6,8 | $\overline{D}[0:3]$ | ECL Input | High | Inverted Differential Inputs [0:3]. Internal $75\text{ k}\Omega$ to V_{EE} and $37\text{ k}\Omega$ to V_{CC} . |
| 19,17,15,13 | 12,15,17,20 | $Q[0:3]$ | ECL Output | - | Noninverted Differential Outputs [0:3]. Typically Terminated with $50\ \Omega$ to $V_{TT} = V_{CC} - 2\text{ V}$. |
| 18,16,14,12 | 11,14,16,19 | $\overline{Q}[0:3]$ | ECL Output | - | Inverted Differential Outputs [0:3]. Typically Terminated with $50\ \Omega$ to $V_{TT} = V_{CC} - 2\text{ V}$. |
| N/A | 24 | NC | - | - | No Connect. The NC Pin is Electrically Connected to the Die and "MUST BE" Left Open. |
| N/A | - | EP | - | - | Exposed Pad. (Note 1) |

1. All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation. The thermally conductive expose pad on the package bottom (see case drawing) must be attached to a heat-sinking conduit.

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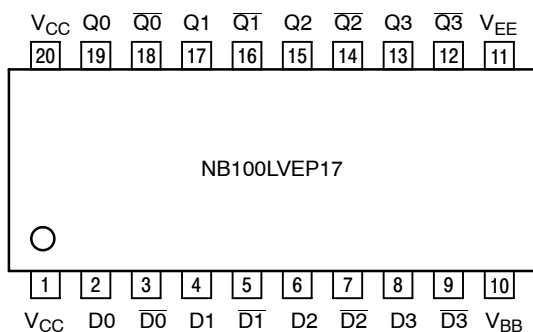


Figure 2. TSSOP-20 Lead Pinout (Top View)

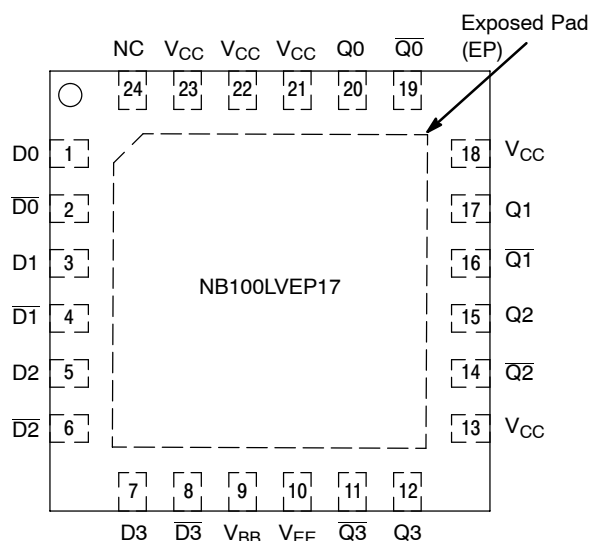


Figure 3. QFN-24 Lead Pinout (Top View)

Table 2. ATTRIBUTES

| Characteristics | | Value | |
|---|---|-----------------------------|--------------------|
| Internal Input Pulldown Resistor | (R1) | 75 kΩ | |
| Internal Input Pullup Resistor | (R2) | 37 kΩ | |
| ESD Protection | Human Body Model Machine Model Charged Device Model | > 2 kV > 150 V > 2 kV | |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | | Pb Pkg | Pb-Free Pkg |
| | TSSOP-20 QFN-24 | Level 1 Level 1 | Level 1 Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in | |
| Transistor Count | | 274 Devices | |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | | |

1. For additional information, see Application Note AND8003/D.

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Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|----------------|--------------|
| V _{CC} | Positive Mode Power Supply | V _{EE} = 0 V | | 6 | V |
| V _{EE} | Negative Mode Power Supply | V _{CC} = 0 V | | -6 | V |
| V _I | Positive Mode Input Voltage Negative Mode Input Voltage | V _{EE} = 0 V V _{CC} = 0 V | V _I ≤ V _{CC} V _I ≥ V _{EE} | 6 -6 | V V |
| I _{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| I _{BB} | V _{BB} Sink/Source | | | ±0.5 | mA |
| T _A | Operating Temperature Range | | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) JEDEC 51-3 (1S - Single Layer Test Board) | 0 lfpm 500 lfpm | 20 TSSOP 20 TSSOP | 140 50 | °C/W °C/W |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) JEDEC 51-6 (2S2P Multilayer Test Board) with Filled Thermal Vias | 0 lfpm 500 lfpm | 24 QFN 24 QFN | 37 32 | °C/W °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | 20 TSSOP 24 QFN | 23 to 41 11 | °C/W °C/W |
| T _{sol} | Wave Solder Pb Pb-Free | | | 265 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 4. DC CHARACTERISTICS, PECL V_{CC} = 2.5 V; V_{EE} = 0 V (Note 2)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------|--|--------|-------------|------|-------------|------|------|-------------|------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I _{EE} | Negative Power Supply Current | 30 | 40 | 50 | 30 | 40 | 50 | 30 | 40 | 55 | mA |
| V _{OH} | Output HIGH Voltage (Note 3) | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| V _{OL} | Output LOW Voltage (Note 3) | 555 | 775 | 900 | 555 | 775 | 900 | 555 | 775 | 900 | mV |
| V _{IH} | Input HIGH Voltage (Single-Ended) (Note 4) | 1335 | | 1620 | 1335 | | 1620 | 1275 | | 1620 | mV |
| V _{IL} | Input LOW Voltage (Single-Ended) (Note 4) | 555 | | 875 | 555 | | 875 | 555 | | 875 | mV |
| V _{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5) | 1.2 | | 2.5 | 1.2 | | 2.5 | 1.2 | | 2.5 | V |
| I _{IH} | Input HIGH Current (@ V _{IH}) | | | 150 | | | 150 | | | 150 | μA |
| I _{IL} | Input LOW Current (@ V _{IL}) | D D | 0.5 -150 | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary -0.125 V to +1.3 V.
- All loading with 50 Ω to V_{EE} = V_{CC} - 2.0 V.
- Do not use V_{BB} at V_{CC} < 3.0 V.
- V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 5. DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$; $V_{EE} = 0\text{ V}$ (Note 6)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|--------|-------------|------|-------------|------|------|-------------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Negative Power Supply Current | 30 | 40 | 50 | 30 | 40 | 50 | 30 | 40 | 55 | mA |
| V_{OH} | Output HIGH Voltage (Note 7) | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| V_{OL} | Output LOW Voltage (Note 7) | 1355 | 1575 | 1700 | 1355 | 1575 | 1700 | 1355 | 1575 | 1700 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 1355 | | 1675 | 1355 | | 1675 | 1355 | | 1675 | mV |
| V_{BB} | ECL Output Reference Voltage (Note 8) | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9) | 1.2 | | 3.3 | 1.2 | | 3.3 | 1.2 | | 3.3 | V |
| I_{IH} | Input HIGH Current (@ V_{IH}) | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current (@ V_{IL}) | D D | 0.5 -150 | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary + 0.5 V to -0.3 V.

7. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

8. Single ended input operation is limited $V_{CC} \geq 3.0\text{ V}$ in PECL mode.

9. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$, $V_{EE} = -2.375\text{ V}$ to -3.8 V (Note 10)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|---|----------------|-------------|-------|----------------|-------|-------|----------------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Negative Power Supply Current | 30 | 40 | 50 | 30 | 40 | 50 | 30 | 40 | 55 | mA |
| V_{OH} | Output HIGH Voltage (Note 11) | -1145 | -1020 | -895 | -1145 | -1020 | -895 | -1145 | -1020 | -895 | mV |
| V_{OL} | Output LOW Voltage (Note 11) | -1945 | -1725 | -1600 | -1945 | -1725 | -1600 | -1945 | -1725 | -1600 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1945 | | -1600 | -1945 | | -1600 | -1945 | | -1600 | mV |
| V_{BB} | ECL Output Reference Voltage (Note 12) | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | mV |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) | $V_{EE} + 1.2$ | | 0.0 | $V_{EE} + 1.2$ | | 0.0 | $V_{EE} + 1.2$ | | 0.0 | V |
| I_{IH} | Input HIGH Current (@ V_{IH}) | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current (@ V_{IL}) | D D | 0.5 -150 | | 0.5 -150 | | | 0.5 -150 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Input and output parameters vary 1:1 with V_{CC} .

11. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$.

12. Single ended input operation is limited $V_{EE} \leq -3.0\text{ V}$ in NECL mode.

13. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 7. AC CHARACTERISTICS $V_{CC} = 0\text{ V}$; $V_{EE} = -2.375\text{ V}$ to -3.8 V or $V_{CC} = 2.375\text{ V}$ to 3.8 V ; $V_{EE} = 0\text{ V}$ (Note 14)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|--------------------------|---|-------|---------------|-----------------|------|---------------|-----------------|------|---------------|-----------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OUTPP} | Output Voltage Amplitude (See Figures 4, 5) | | | | | | | | | | |
| | $f_{in} < 1\text{ GHz}$ | 600 | 700 | | 600 | 700 | | 550 | 700 | | mV |
| | $f_{in} = 2\text{ GHz}$ | 400 | 500 | | 325 | 500 | | 300 | 500 | | |
| | $f_{in} = 2.5\text{ GHz}$ | 300 | 400 | | 250 | 400 | | 200 | 400 | | |
| t_{PLH} , t_{PHL} | Propagation Delay to Output Differential D to Q, \bar{Q} | 200 | 250 | 325 | 200 | 250 | 325 | 225 | 300 | 350 | ps |
| t_{Skew} | Pulse Skew (Note 15) Within Device Skew (Note 17) Device-to-Device Skew (Note 17) | | 5 5 25 | 25 25 100 | | 5 5 25 | 25 25 100 | | 5 5 25 | 25 25 100 | ps |
| t_{JITTER} | RMS Random Clock Jitter (Note 18) Peak-to-Peak Data Dependent Jitter (Note 19) | | 0.5 5 5 | 1 15 15 | | 0.5 5 5 | 1 15 15 | | 0.5 5 5 | 1 15 15 | ps |
| V_{INPP} | Input Voltage Swing (Differential Configuration) (Note 20) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r t_f | Output Rise/Fall Times @ 50 MHz (20% – 80%) | 125 | 175 | 225 | 140 | 190 | 240 | 150 | 200 | 250 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

14. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to $V_{CC} - 2.0\text{ V}$. Input edge rates 150 ps (20% – 80%).

15. Pulse Skew = $|t_{PLH} - t_{PHL}|$

16. Worst case difference between Q0 and Q1 outputs.

17. Skew is measured between outputs under identical transitions.

18. Additive RMS jitter with 50% Duty Cycle Clock Signal at 2.5 GHz.

19. Peak-to-Peak jitter with input NRZ data at PRBS $2^{31}-1$ at 2.5 Gb/s with all inputs active.

20. Input voltage swing is a single-ended measurement operating in differential mode, with minimum propagation change of 50 ps.

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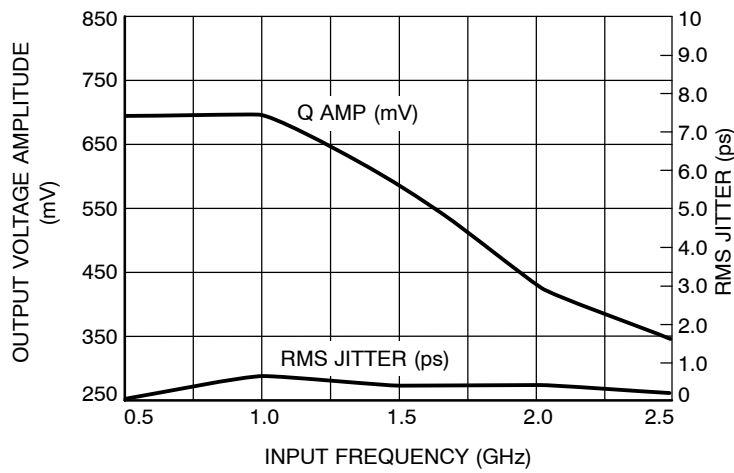


Figure 4. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at $V_{CC} = 2.5$ V, Ambient Temperature

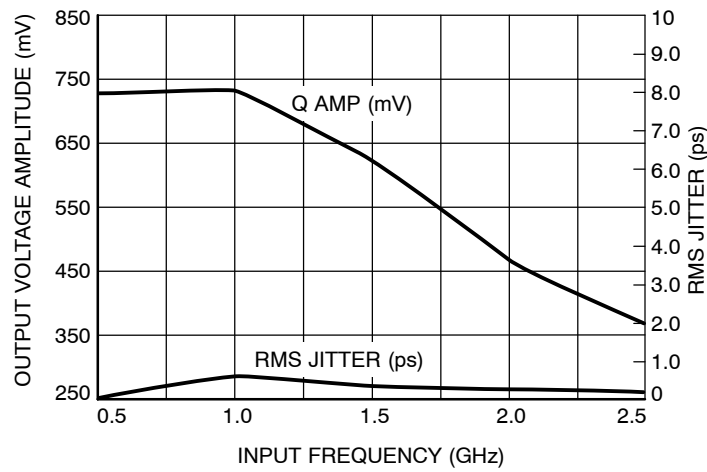


Figure 5. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at $V_{CC} = 3.3$ V, Ambient Temperature

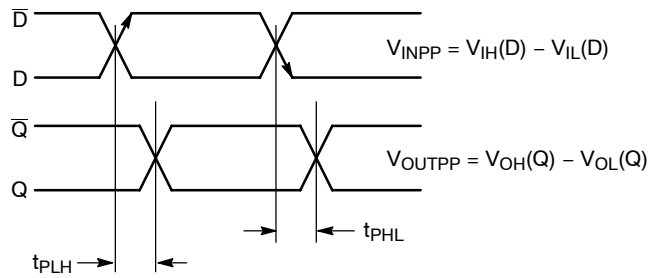


Figure 6. AC Reference Measurement

NB100LVEP17

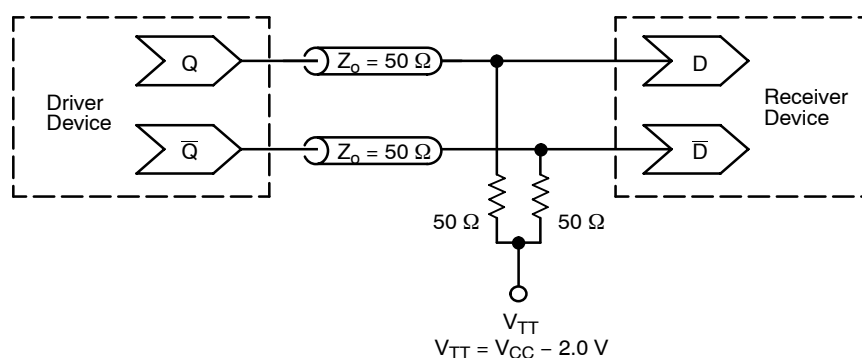


Figure 7. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

| Device | Package | Shipping† |
|------------------|---------------------|------------------|
| NB100LVEP17DT | TSSOP-20* | 75 Units / Rail |
| NB100LVEP17DTG | TSSOP-20* | 75 Units / Rail |
| NB100LVEP17DTR2 | TSSOP-20* | 2500 Tape & Reel |
| NB100LVEP17DTR2G | TSSOP-20* | 2500 Tape & Reel |
| NB100LVEP17MN | QFN-24 | 92 Units / Rail |
| NB100LVEP17MNG | QFN-24 (Pb-Free) | 92 Units / Rail |
| NB100LVEP17MNR2 | QFN-24 | 3000 Tape & Reel |
| NB100LVEP17MNR2G | QFN-24 (Pb-Free) | 3000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

*This package is inherently Pb-Free.

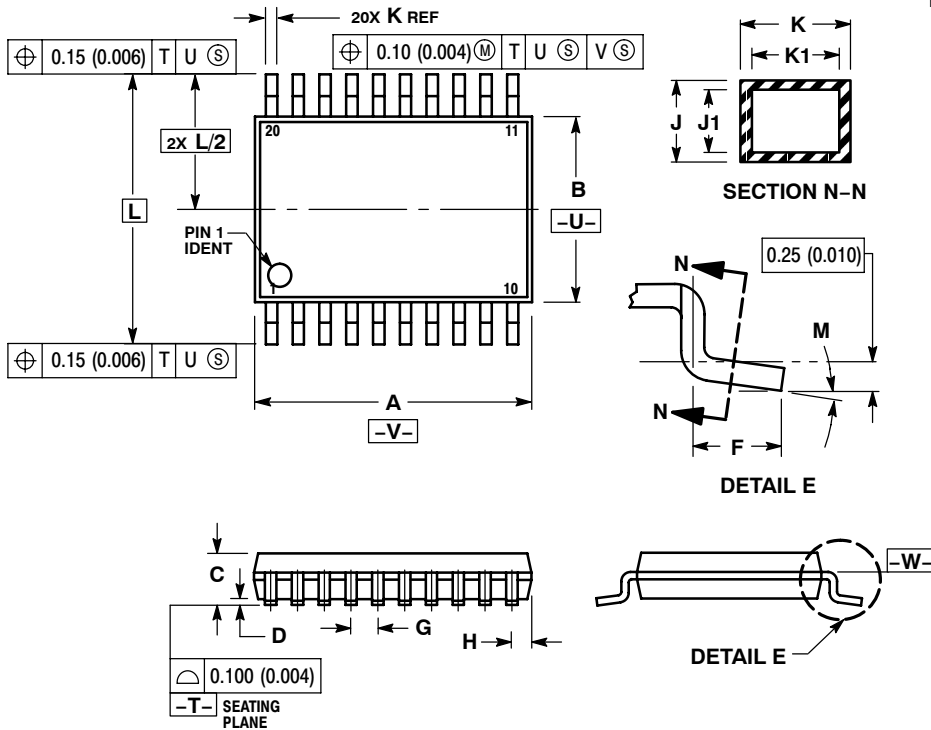
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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PACKAGE DIMENSIONS

TSSOP-20
CASE 948E-02
ISSUE C

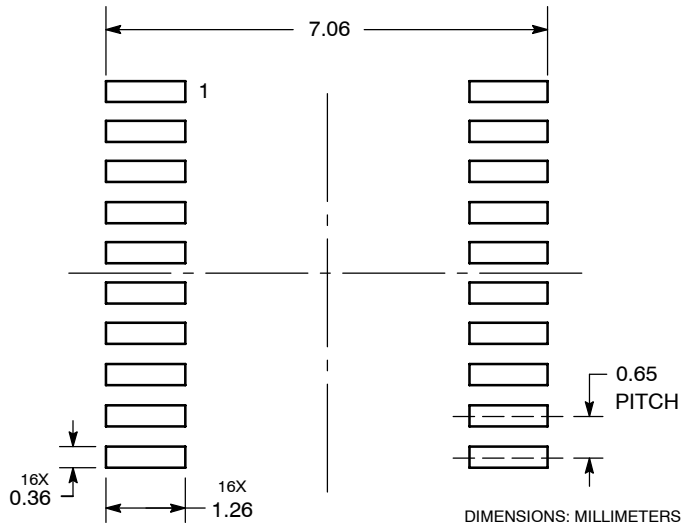


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*

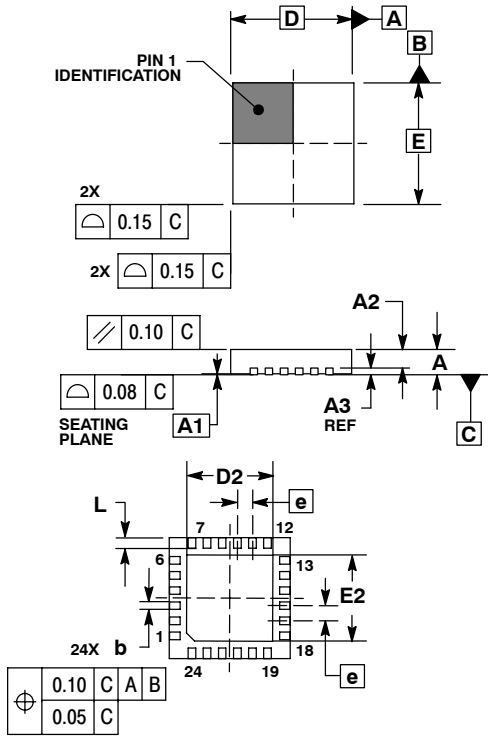


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

QFN 24
MN SUFFIX
 24 PIN QFN, 4x4
 CASE 485L-01
 ISSUE O




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A2 | 0.60 | 0.80 |
| A3 | 0.20 | REF |
| b | 0.23 | 0.28 |
| D | 4.00 | BSC |
| D2 | 2.70 | 2.90 |
| E | 4.00 | BSC |
| E2 | 2.70 | 2.90 |
| e | 0.50 | BSC |
| L | 0.35 | 0.45 |

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Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

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