### **General Description**

The MAX6443–MAX6452 low-current microprocessor reset circuits feature single or dual manual reset inputs with an extended setup period. Because of the extended setup period, short switch closures (nuisance resets) are ignored.

On all devices, the reset output asserts when any of the monitored supply voltages drops below its specified threshold. The reset output remains asserted for the reset timeout period (210ms typ) after all monitored supplies exceed their reset thresholds. The reset output is one-shot pulse asserted for the reset timeout period (140ms min) when selected manual reset input(s) are held low for an extended setup timeout period. These devices ignore manual reset transitions of less than the extended setup timeout period.

The MAX6443–MAX6448 are single fixed-voltage  $\mu P$  supervisors. The MAX6443/MAX6444 have a single extended manual reset input. The MAX6445/MAX6446 have two extended manual reset inputs. The MAX6447/MAX6448 have one extended and one immediate manual reset input.

The MAX6449–MAX6452 have one fixed-threshold  $\mu P$  supervisor and one adjustable-threshold  $\mu P$  supervisor. The MAX6449/MAX6450 have two delayed manual reset inputs. The MAX6451/MAX6452 have one delayed and one immediate manual reset input.

The MAX6443–MAX6452 have an active-low RESET with push-pull or open-drain output logic options. These devices, offered in small SOT packages, are fully guaranteed over the extended temperature range (-40°C to +85°C).

### **Applications**

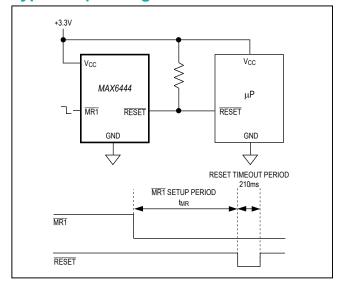
- Set-Top Boxes
- Consumer Electronics
- DVD Players
- Cable/DSL Modems
- MP3 Players
- Industrial Equipment
- Automotive
- Medical Devices

#### **Features**

- Single or Dual-Supply Voltage Monitors
- Precision Factory-Set Reset Thresholds from 1.6V to 4.6V
- Adjustable Threshold to Monitor Voltages Down to 0.63V (MAX6449–MAX6452)
- Single or Dual Manual Reset Inputs with Extended Setup Period
- Optional Short Setup Time Manual Reset Input (MAX6447/MAX6448 and MAX6451/MAX6452)
- Immune to Short Voltage Transients
- Low 6µA Supply Current
- Guaranteed Valid Reset Down to V<sub>CC</sub> = 1.0V
- Active-Low RESET (Push-Pull or Open-Drain) Outputs
- 140ms (min) Reset Timeout Period
- Small SOT143 and SOT23 Packages
- AEC-Q100 Qualified (MAX6444US16K/V+T)

Ordering Information at end of data sheet.

## **Typical Operating Circuit**





## **Absolute Maximum Ratings**

(All voltages referenced to GND.)	
V <sub>CC</sub>	0.3V to +6V
Open-Drain RESET	0.3V to +6V
Push-Pull RESET0.3V to	$(V_{CC} + 0.3V)$
MR1, MR2, MR2, RSTIN	0.3V to +6V
Input Current, All Pins	±20mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
4-Pin SOT143 (derate 4.0mW/°C above +70°C)	320mW
5-Pin SOT23 (derate 7.1mW/°C above +70°C)	571mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C)	696mW

Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	
Lead(Pb)-free	+260°C
Containing lead	+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **Electrical Characteristics**

 $(V_{CC} = 1.0V \text{ to } 5.5V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise specified. Typical values are at } T_A = +25^{\circ}\text{C.})$  (Note 1)

PARAMETER	SYMBOL	COND	ITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V <sub>CC</sub>					5.5	V
V Summer Cumment		V <sub>CC</sub> = 5.5V, no load			7	20	
V <sub>CC</sub> Supply Current	Icc	V <sub>CC</sub> = 3.6V, no load			6	16	μA
		46		4.50	4.63	4.75	
		44		4.25	4.38	4.50	
		31		3.00	3.08	3.15	
		29		2.85	2.93	3.00	
V <sub>CC</sub> Reset Threshold	V <sub>TH</sub>	26		2.55	2.63	2.70	V
		23		2.25	2.32	2.38	
		22		2.12	2.19	2.25	]
		17		1.62	1.67	1.71	
		16		1.52	1.58	1.62	1
Reset Threshold Tempco					60		ppm/°C
Reset Threshold Hysteresis					2 × V <sub>TH</sub>		mV
DCTINI Threehold	V <sub>TH-RSTIN</sub>	MAX6449-MAX6452	T <sub>A</sub> = 0°C to +85°C	0.615	0.630	0.645 V	
RSTIN Threshold			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	0.610		0.650	7 V
RSTIN Threshold Hysteresis	V <sub>HYST</sub>	MAX6449-MAX6452			2.5		mV
RSTIN Input Current	I <sub>RSTIN</sub>	MAX6449-MAX6452		-25		+25	nA
RSTIN to Reset Output Delay		MAX6449–MAX6452, V <sub>RSTIN</sub> falling at 1mV/μs			15		μs
Reset Timeout Period	t <sub>RP</sub>			140	210	280	ms
V <sub>CC</sub> to RESET Output Delay	t <sub>RD</sub>	V <sub>CC</sub> falling at 1mV/µs		20		μs	
<u> </u>		K		6.72	10.08	13.44	
Manual Reset Minimum Setup		L		4.48	6.72	8.96	1 _
Period Pulse Width	t <sub>MR</sub>	S		2.24	3.36	4.48	s
		Т		1.12	1.68	2.24	1

## **Electrical Characteristics (continued)**

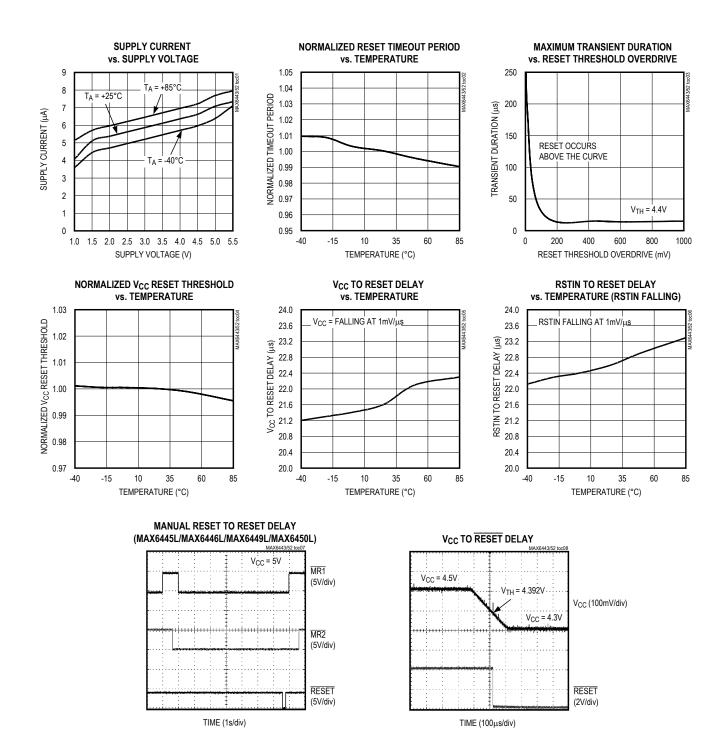
 $(V_{CC} = 1.0V \text{ to } 5.5V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, \text{ unless otherwise specified. Typical values are at } T_A = +25^{\circ}\text{C.})$  (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP MAX	UNITS
MR2 Minimum Setup Period Pulse Width		MAX6447/MAX6448/MAX6451/MAX6452	1		μs
MR2 Glitch Rejection		MAX6447/MAX6448/MAX6451/MAX6452		100	ns
MR2 to RESET Delay		MAX6447/MAX6448/MAX6451/MAX6452		200	ns
Manual Reset Timeout Period	t <sub>MRP</sub>		140	210 280	ms
MR1 to V <sub>CC</sub> Pullup Impedance			25	50 75	kΩ
MR2 to V <sub>CC</sub> Pullup Impedance		MAX6445/MAX6446/MAX6449/MAX6450	25	50 75	kΩ
RESET Output Low (Open Drain or Push-Pull)		V <sub>CC</sub> ≥ 1.00V, I <sub>SINK</sub> = 50μA, RESET asserted		0.3	
		V <sub>CC</sub> ≥ 1.20V, I <sub>SINK</sub> = 100μA, <del>RESET</del> asserted	0.3		
	V <sub>OL</sub>	V <sub>CC</sub> ≥ 2.55V, I <sub>SINK</sub> = 1.2mA, <del>RESET</del> asserted		0.3	V
		V <sub>CC</sub> ≥ 4.25V, I <sub>SINK</sub> = 3.2mA, <del>RESET</del> asserted		0.4	
		V <sub>CC</sub> ≥ 1.80V, I <sub>SOURCE</sub> = 200µA, RESET deasserted	0.8 × V <sub>CC</sub>		
RESET Output High (Push-Pull)	V <sub>OH</sub>	V <sub>CC</sub> ≥ 3.15V, I <sub>SOURCE</sub> = 500μA, RESET deasserted	0.8 × V <sub>CC</sub>		V
		V <sub>CC</sub> ≥ 4.75V, I <sub>SOURCE</sub> = 800μA, <del>RESET</del> deasserted	0.8 × V <sub>CC</sub>		
RESET Open-Drain Leakage Current	lkg	RESET deasserted		1	μA
MR1, MR2, MR2 Input Low Voltage	V <sub>IL</sub>			0.3 × V <sub>0</sub>	c V
MR1, MR2, MR2 Input High Voltage	V <sub>IH</sub>		0.7 × V <sub>CC</sub>		V

**Note 1:** Devices production tested at  $T_A = +25$ °C. Overtemperature limits are guaranteed by design.

# **Typical Operating Characteristics**

( $V_{CC}$  = 3.3V,  $T_A$  = +25°C, unless otherwise noted.)



### **Pin Description**

PIN						
MAX6443 MAX6444	MAX6445 MAX6446	MAX6447 MAX6448	MAX6449 MAX6450	MAX6451 MAX6452	NAME	FUNCTION
1	2	2	2	2	GND	Ground
2	1	1	1	1	RESET	Active-Low Push-Pull or Open-Drain Output. $\overline{RESET}$ changes from high to low when $V_{CC}$ or RSTIN drops below its selected reset threshold and remains low for the 210ms reset timeout period after all monitored power-supply inputs exceed their selected reset thresholds. $\overline{RESET}$ is one-shot pulsed low for the reset timeout period (140ms min) after selected manual reset inputs are asserted longer than the specified setup period. For the open-drain output, use a minimum $20k\Omega$ pullup resistor to $V_{CC}$ .
3	_	3	_	3	MD1	Manual Reset Input, Active Low. Internal $50 k\Omega$ pullup to $V_{CC}$ . Pull $\overline{MR1}$ low for the typical input pulse width ( $t_{MR}$ ) to one-shot pulse $\overline{RESET}$ for the reset timeout period.
_	3	_	3	MR1		$\begin{array}{c} \underline{\text{Manual Reset Input, Active Low. Pull both } \overline{\text{MR1}} \text{ and} \\ \overline{\text{MR2}} \text{ low for the typical input pulse width } (t_{MR}) \text{ to one-shot pulse } \overline{\text{RESET}} \text{ for the reset timeout period.} \end{array}$
4	4	4	4	4	V <sub>CC</sub>	$\ensuremath{\text{V}_{\text{CC}}}$ Voltage Input. Power supply and input for the primary microprocessor voltage reset monitor.
_	5	_	6	_	MR2	Manual Reset Input, Active Low. Internal $50k\Omega$ pullup to $V_{CC}$ . Pull both MR1 and MR2 low for the typical input pulse width (t <sub>MR</sub> ) to one-shot pulse RESET for the reset timeout period.
_	_	5	_	6	MR2	Manual Reset Input. Pull the MR2 high to immediately one-shot pulse RESET for the reset timeout period.
_	_	_	5	5	RSTIN	Reset Input. High-impedance input to the adjustable reset comparator. Connect RSTIN to the center point of an external resistor-divider to set the threshold of the externally monitored voltage.

## **Detailed Description**

### **Reset Output**

The reset output is typically connected to the reset input of a microprocessor ( $\mu P$ ). A  $\mu P$ 's reset input starts or restarts the  $\mu P$  in a known state. The MAX6443–MAX6452  $\mu P$  supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down and brownout conditions (see the *Typical Operating Circuit*).

 $\overline{\text{RESET}}$  changes from high to low whenever the monitored voltages (RSTIN or  $V_{CC}$ ) drop below the reset

threshold voltages. Once  $V_{RSTIN}$  and  $V_{CC}$  exceed their respective reset threshold voltages,  $\overline{RESET}$  remains low for the reset timeout period and then goes high.  $\overline{RESET}$  is one-shot pulsed whenever selected manual reset inputs are asserted.  $\overline{RESET}$  stays asserted for the normal reset timeout period (140ms min).

RESET is guaranteed to be in the proper output logic state for  $V_{CC}$  inputs  $\geq$  1V. For applications requiring valid reset logic when  $V_{CC}$  is less than 1V, see the *Ensuring a Valid RESET Output Down to V\_{CC} = 0V* section.

### Manual Reset Input Options

Unlike typical manual reset functions associated with supervisors, each device in the MAX6443–MAX6452 family includes at least one manual reset input, which must be held logic-low for an extended setup period ( $t_{MR}$ ) before the  $\overline{RESET}$  output asserts. When valid manual reset input conditions/setup periods are met, the  $\overline{RESET}$  output is one-shot pulse asserted low for a fixed reset timeout period (140ms min). Existing front-panel pushbutton switches (i.e., power on/off, channel up/down, or mode select) can be used to drive the manual reset inputs. The extended manual reset setup period prevents nuisance system resets during normal front-panel usage or resulting from inadvertent short-term pushbutton closure.

The MAX6443/MAX6444, MAX6447/MAX6448, and MAX6451/MAX6452 include a single manual reset input with extended setup period ( $\overline{\text{MR1}}$ ). The MAX6445/MAX6446 and MAX6449/MAX6450 include two manual reset inputs ( $\overline{\text{MR1}}$  and  $\overline{\text{MR2}}$ ) with extended setup periods. For dual  $\overline{\text{MR1}}$ ,  $\overline{\text{MR2}}$  devices, both inputs must be held low simultaneously for the extended setup period ( $t_{\text{MR}}$ ) before the reset output is pulse asserted. The dual extended setup provides greater protection from nuisance resets. (For example, the user or service technician is informed to simultaneously push both the on/off button and the channel-select button for 6.72s (L suffix) to reset the system.)

The MAX6443/MAX6452 RESET output is pulse asserted once for the reset timeout period after each valid manual reset input condition. At least one manual reset input must be released (go high) and then be driven low for the extended setup period before RESET asserts again. Internal timing circuitry debounces low-to-high manual reset logic transitions, so no external circuitry is required. Figure 1 illustrates the single manual reset function of the MAX6443/MAX6444 single-voltage monitors, and Figure 2 represents the dual manual reset function of the MAX6445/MAX6446 and MAX6449/MAX6450.

The MAX6447/MAX6448 and MAX6451/MAX6452 include both an extended setup period and immediate setup period manual reset inputs. A low-to-high MR2 rising edge transition immediately pulse asserts the RESET output for the reset timeout period (140ms min). If the MAX6447/MAX6448 and MAX6451/MAX6452 MR2 input senses another rising edge before the end of the 140ms timeout period (Figure 3), the internal timer clears and begins counting again. If no rising edges are detected within the 210ms timeout period, RESET deasserts. The high-to-low transition on MR2 input is internally debounced for 210ms to ensure that

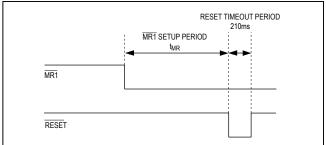


Figure 1. MAX6443/MAX6444 Manual Reset Timing Diagram

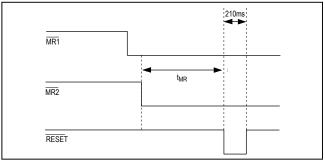


Figure 2. MAX6445/MAX6446/MAX6449/MAX6450 Manual Reset Timing Diagram

there are no false RESET assertions when MR2 is driven from high to low (Figure 4). The MR2 input can be used for system test purposes or smart-card-detect applications (see the *Applications Information* section).

### Adjustable Input Voltage (RSTIN)

The MAX6449–MAX6452 monitor the voltage on RSTIN using an adjustable reset threshold set with an external resistor voltage-divider (Figure 5). Use the following formula to calculate the externally monitored voltage (VMON-TH):

$$V_{MON-TH} = V_{TH-RSTIN} \times (R1 + R2)/R2$$

where  $V_{MON-TH}$  is the desired reset threshold voltage and  $V_{TH-RSTIN}$  is the reset input threshold (0.63V). Resistors R1 and R2 can have very high values to minimize current consumption because of low leakage currents. Set R2 to some conveniently high value (250k $\Omega$ , for example), and calculate R1 based on the desired reset threshold voltage, using the following formula:

R1 = R2 × 
$$(V_{MON-TH}/V_{TH-RSTIN} - 1) \Omega$$

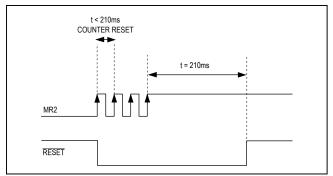


Figure 3. MAX6447/MAX6448/MAX6451/MAX6452 MR2 Assertion DebouncingTiming Diagram

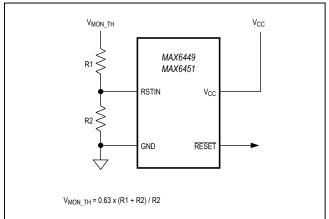


Figure 5. Calculating the Monitored Threshold Voltages

## **Applications Information**

### **Interrupt Before Reset**

To minimize data loss and speed system recovery, many applications interrupt the processor or reset only portions of the system before a processor hard reset is asserted. The extended setup time of the MAX6443–MAX6452 manual reset inputs allows the same pushbutton (connected to both the processor interrupt and the extended  $\overline{\text{MR1}}$  input, as shown in Figure 6) to control both the interrupt and hard reset functions. If the pushbutton is closed for less than  $t_{MR}$ , the processor is only interrupted. If the system still does not respond properly, the pushbutton (or two buttons for the dual manual reset) can be closed for the full extended setup period to hard reset the processor. If desired, connect an LED to the  $\overline{\text{RESET}}$  output to blink off (or on) for the reset timeout period to signify when the pushbutton is

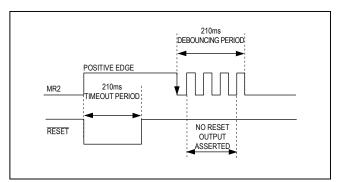


Figure 4. MAX6447/MAX6448/MAX6451/MAX6452 MR2 Deassertion Debouncing Timing Diagram

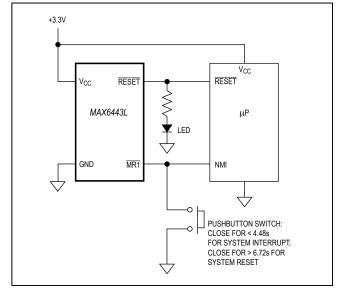


Figure 6. Interrupt Before Reset Application Circuit

closed long enough for a hard reset (the same LED might be used as the front-panel power-on display).

### **Smart Card Insertion/Removal**

The MAX6447/MAX6448/MAX6451/MAX6452 dual manual resets are useful in applications in which both an extended and immediate setup periods are needed. Figure 7 illustrates the insertion and removal of a smart card.  $\overline{\text{MR1}}$  monitors a front-panel pushbutton. When closed for  $t_{\text{MR}}$ ,  $\overline{\text{RESET}}$  one-shot pulses low for 140ms min. Because  $\overline{\text{MR1}}$  is internally pulled to  $V_{\text{CC}}$  through a  $50 \text{k}\Omega$  resistor, the front-panel switch can be connected to a microprocessor for general-purpose I/O control. MR2 monitors a switch to detect when a smart card is inserted. When the switch is closed high (card inserted),

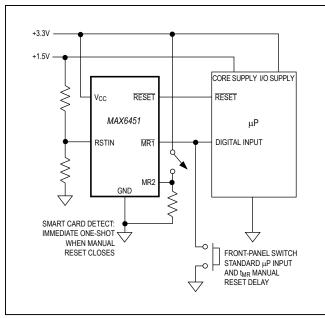


Figure 7. MAX6451/MAX6452 Application Circuit

RESET one-shot pulses low for 140ms. MR2 is internally debounced for 210ms to prevent false resets when the smart card is removed.

# Interfacing to Other Voltages for Logic Compatibility

The open-drain  $\overline{RESET}$  output can be used to interface to a  $\mu P$  with other logic levels. As shown in Figure 8, the open-drain output can be connected to voltages from 0 to 6V.

Generally, the pullup resistor connected to the  $\overline{\text{RESET}}$  connects to the supply voltage that is being monitored at the IC's  $V_{CC}$  pin. However, some systems may use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 8). Keep in mind that as the supervisor's  $V_{CC}$  decreases toward 1V, so does the IC's ability to sink current at  $\overline{\text{RESET}}$ .  $\overline{\text{RESET}}$  is pulled high as  $V_{CC}$  decays toward 0. The voltage where this occurs depends on the pullup resistor value and the voltage to which it is connected.

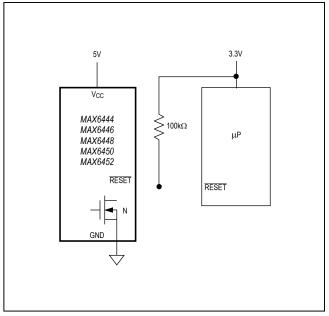


Figure 8. Interfacing to Other Voltage Levels

# Ensuring a Valid RESET Down to V<sub>CC</sub> = 0V (Push-Pull RESET)

When  $V_{CC}$  falls below 1V,  $\overline{RESET}$  current-sinking capabilities decline drastically. The high-impedance CMOS-logic inputs connected to  $\overline{RESET}$  can drift to undetermined voltages. This presents no problems in most applications, because most  $\mu Ps$  and other circuitry do not operate with  $V_{CC}$  below 1V.

In applications in which  $\overline{\text{RESET}}$  must be valid down to 0V, add a pulldown resistor between  $\overline{\text{RESET}}$  and GND for the push-pull outputs. The resistor sinks any stray leakage currents, holding  $\overline{\text{RESET}}$  low (Figure 9). The value of the pulldown resistor is not critical;  $100\text{k}\Omega$  is large enough not to load  $\overline{\text{RESET}}$  and small enough to pull  $\overline{\text{RESET}}$  to ground. The external pulldown cannot be used with the open-drain reset outputs.

#### Transient Immunity

In addition to issuing a reset to the  $\mu P$  during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration falling transients (glitches). The graph Maximum Transient Duration vs. Reset Threshold Overdrive in the *Typical Operating Characteristics* section shows this relationship.

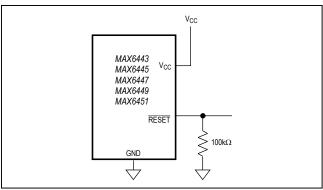


Figure 9. Ensuring  $\overline{RESET}$  Valid to  $V_{CC} = 0V$ 

Table 1. Reset Voltage Threshold

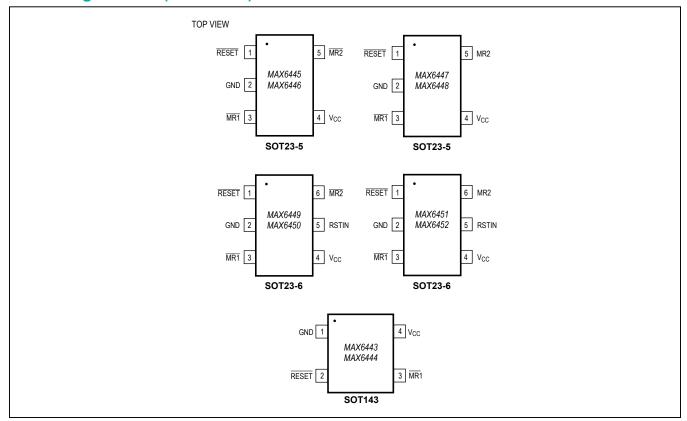
PART NO. SUFFIX	VCC NOMINAL VOLTAGE THRESHOLD (V)				
46	4.625				
44	4.375				
31	3.075				
29	2.925				
26	2.625				
23	2.313				
22	2.188				
17	1.665				
16	1.575				

Table 2. Manual Reset Setup Period (t<sub>MR</sub>)

PART NO. SUFFIX	MANUAL RESET SETUP PERIOD (s)
K	10.08
L	6.72
S	3.36
Т	1.68

The area below the curves of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a falling pulse applied to  $V_{CC}$ , starting above the actual reset threshold  $(V_{TH})$  and ending below it by the magnitude indicated (reset threshold overdrive). As the magnitude of the transient increases ( $V_{CC}$  goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a  $V_{CC}$  transient that goes 100mV below the reset threshold and lasts 20 $\mu$ s or less does not cause a reset pulse to be asserted.

## **Pin Configurations (continued)**



### **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE
MAX6443US+T	-40°C to +85°C	4 SOT143
MAX6444US+T	-40°C to +85°C	4 SOT143
MAX6444US/V+T*	-40°C to +85°C	4 SOT143
MAX6444US16K/V+T	-40°C to +85°C	4 SOT143
MAX6445UK+T	-40°C to +85°C	5 SOT23
MAX6446UK+T	-40°C to +85°C	5 SOT23
MAX6447UK+T	-40°C to +85°C	5 SOT23
MAX6448UK+T	-40°C to +85°C	5 SOT23
MAX6449UT+T	-40°C to +85°C	6 SOT23
MAX6450UT+T	-40°C to +85°C	6 SOT23
MAX6451UT+T	-40°C to +85°C	6 SOT23
MAX6452UT+T	-40°C to +85°C	6 SOT23

Note: The first "\_\_" is a placeholder for the threshold voltage level of the devices. A desired threshold level is set by the two-number suffix found in Table 1. The third "\_" is a placeholder for the manual reset setup period of the devices. A desired setup period is set by the letter suffix found in Table 2. All devices are available in tapeand-reel only. There is a 2500-piece minimum order increment for standard versions (Table 2). Sample stock is typically held on standard versions only. Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability.

Most devices are available in lead(Pb)-free packaging only. See Ordering Information for devices available in both leaded and lead(Pb)-free packaging.

N denotes an automotive qualified part.

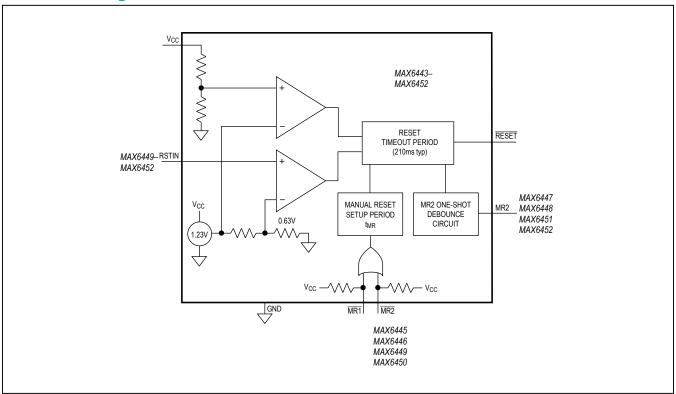
\*Future product—contact factory for availability.

+Denotes Lead(Pb)-free packages and - denotes leaded packages. For top mark information, please go to https://www.maximintegrated.com/en/design/packaging/topmark/.

### **Selector Guide**

PART	MR1 EXT. SETUP	MR2 (NO SETUP)	MR2 EXT. SETUP	RSTIN	PUSH-PULL RESET	OPEN-DRAIN RESET
MAX6443	~	_	_	_	~	_
MAX6444	~	_	_	_	_	V
MAX6445	~	_	~	_	V	_
MAX6446	~	_	~	_	_	~
MAX6447	~	~	_	_	V	_
MAX6448	~	~	_	_	_	~
MAX6449	~	_	~	~	V	_
MAX6450	~	_	~	~	_	V
MAX6451	~	~	_	~	~	_
MAX6452	~	~	_	~	_	V

## **Functional Diagram**



## MAX6443-MAX6452

# μP Reset Circuits with Long Manual Reset Setup Period

## **Chip Information**

PROCESS: BICMOS

## **Package Information**

For the latest package outline information and land patterns (footprints), go to <a href="www.maximintegrated.com/packages">www.maximintegrated.com/packages</a>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
4 SOT143	U4+1	<u>21-0052</u>	<u>90-0183</u>
5 SOT23	U5+1, U5-1	<u>21-0057</u>	<u>90-0174</u>
6 SOT23	U6+1	<u>21-0058</u>	<u>90-0175</u>

### MAX6443-MAX6452

# μP Reset Circuits with Long Manual Reset Setup Period

## **Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/02	Initial release	_
3	6/10	Revised the General Description, Features, Applications, Ordering Information, Absolute Maximum Ratings, Electrical Characteristics, Typical Operating Characteristics, Pin Description, the Manual Reset Input Options, Interrupt Before Reset, and Smart Card Insertion/Removal sections, Functional Diagram, Typical Operating Circuit, Selector Guide, Figures 1, 6, and 7, as well as Tables 2 and 3 to add extended setup timeout specifications	1, 2, 4, 5–12
4	3/14	Added the automotive MAX6444US/V+T to the Ordering Information table	1
5	12/15	Added lead-free package part numbers, removed top mark table and added reference to top mark information on website	1, 10, 12
6	3/18	Updated Ordering Information table and Benefits and Features section	1. 10

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