NLSF302

Quad 2-Input NOR Gate

The NLSF302 is an advanced high speed CMOS 2-input NOR gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.



• High Speed: $t_{PD} = 3.6 \text{ ns}$ (Typ) at $V_{CC} = 5.0 \text{ V}$

• Low Power Dissipation: $I_{CC} = 2.0 \mu A$ (Max) at $T_A = 25^{\circ}C$

• High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$

• Power Down Protection Provided on Inputs

• Balanced Propagation Delays

• Designed for 2.0 V to 5.5 V Operating Range

• Low Noise: $V_{OLP} = 0.8 \text{ V (Max)}$

• Function Compatible with Other Standard Logic Families

• QFN-16 Package

• Latchup Performance Exceeds 300 mA

• ESD Performance: Human Body Model; > 2000 V,

Machine Model > 200 V

• Chip Complexity: 40 FETs or 10 Equivalent Gates

• Pb-Free Package is Available*

FUNCTION TABLE

Inp	uts	Output		
Α	В	Υ		
L	L	Н		
L	Н	L		
Н	L	L		
Н	Н	L		



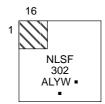
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QFN-16 MN SUFFIX CASE 485G

MARKING DIAGRAM



NLSF302 = Device Code

A = Assembly Location

L = Wafer Lot Y = Year W = Work Week

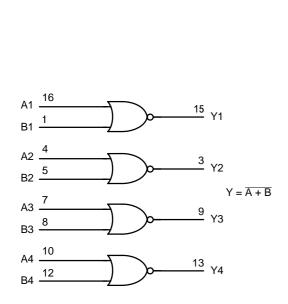
■ = Pb-Free Package (Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NLSF302MNR2	QFN-16	3000/Tape & Reel
NLSF302MNR2G	QFN-16 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



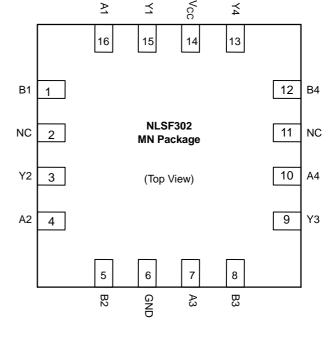


Figure 1. LOGIC DIAGRAM

Figure 2. PIN ASSIGNMENT (QFN-16)

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
DC Supply Voltage	V _{CC}	- 0.5 to + 7.0	V
DC Input Voltage	V _{in}	- 0.5 to + 7.0	V
DC Output Voltage	V _{out}	-0.5 to V_{CC} + 0.5	V
Input Diode Current	I _{IK}	- 20	mA
Output Diode Current	lok	± 20	mA
DC Output Current, per Pin	l _{out}	± 25	mA
DC Supply Current, V _{CC} and GND Pins	Icc	± 50	mA
Power Dissipation in Still Air	P _D	450	mW
Storage Temperature	T _{stg}	- 65 to + 150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Parame	Symbol	Min	Max	Unit	
DC Supply Voltage		V _{CC}	2.0	5.5	V
DC Input Voltage		V _{in}	0	5.5	V
DC Output Voltage		V _{out}	0	V _{CC}	V
Operating Temperature		T _A	-40	+85	°C
Input Rise and Fall Time	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V} $ $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	t _r , t _f	0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

		V _{CC}		V _{CC} T _A = 25°C		$T_A = -40$			
Parameter	Test Conditions	Symbol	V	Min	Тур	Max	Min	Max	Unit
Minimum High-Level Input Voltage		V _{IH}	2.0 3.0 to 5.5	1.50 V _{CC} x 0.7			1.50 V _{CC} x 0.7		V
Maximum Low-Level Input Voltage		V _{IL}	2.0 3.0 to 5.5			0.50 V _{CC} x 0.3		0.50 V _{CC} x 0.3	V
Minimum High–Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu\text{A}$	V _{OH}	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$		3.0 4.5	2.58 3.94			2.48 3.80		
Maximum Low–Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu\text{A}$	V _{OL}	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
	V _{in} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA		3.0 4.5			0.36 0.36		0.44 0.44	
Maximum Input Leakage Current	V _{in} = 5.5 V or GND	I _{in}	0 to 5.5			± 0.1		± 1.0	μΑ
Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	I _{CC}	5.5			2.0		20.0	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_f = t_f = 3.0 \text{ns}$)

				$T_A = 25^{\circ}C$		$T_A = -40$) to 85°C	
Parameter	Test Conditions	Symbol	Min	Тур	Max	Min	Max	Unit
Maximum Propagation Delay, Input A or B to Output Y	$V_{CC} = 3.3 \pm 0.3 \text{ V C}_{L} = 15 \text{ pF}$ $C_{L} = 50 \text{ pF}$	t _{PLH} , t _{PHL}		5.6 8.1	7.9 11.4	1.0 1.0	9.5 13.0	ns
	$V_{CC} = 5.0 \pm 0.5 \text{ V C}_{L} = 15 \text{ pF}$ $C_{L} = 50 \text{ pF}$			3.6 5.1	5.5 7.5	1.0 1.0	6.5 8.5	
Maximum Input Capacitance		C _{in}		4	10		10	pF
				Typical (@ 25°C, V _C	_C = 5.0 V		
Power Dissipation Capacitance	(Note 1)	C _{PD}			15			pF

C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per gate). C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$, $C_L = 50 \text{ pF}$, $V_{CC} = 5.0 \text{V}$)

		T _A = 25°C		
Characteristic	Symbol	Тур	Max	Unit
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	0.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	- 0.3	- 0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}		3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}		1.5	V

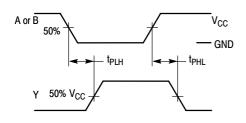
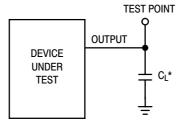


Figure 3. Switching Waveforms



*Includes all probe and jig capacitance

Figure 4. Test Circuit

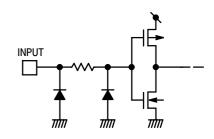
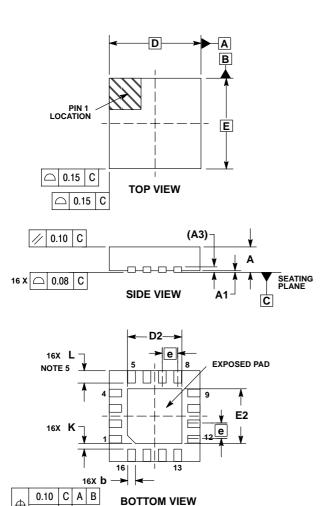


Figure 5. Input Equivalent Circuit

NLSF302

PACKAGE DIMENSIONS

16 PIN QFN CASE 485G-01 ISSUE C



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION 6 APPLIES TO PLATED
 TERMINAL AND IS MEASURED BETWEEN
- 12.5 AND 0.30 MM FROM TERMINAL.
 COPLANARITY APPLIES TO THE EXPOSED
 PAD AS WELL AS THE TERMINALS.
 L_{max} CONDITION CAN NOT VIOLATE 0.2 MM
 MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS				
DIM	MIN	MAX			
Α	0.80	1.00			
A1	0.00	0.05			
А3	0.20	REF			
b	0.18 0.30				
D	3.00	BSC			
D2	1.65	1.85			
E	3.00	BSC			
E2	1.65	1.85			
е	0.50 BSC				
K	0.18 TYP				
L	0.30	0.50			

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