Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MC56F847XX
Rev. 3, 08/2012

MC56F847XX

MC56F847xx

Supports the 56F84789VLL, 56F84786VLK, 56F84769VLL, 56F84766VLK, 56F84763VLH

Features

- This family of digital signal controllers (DSCs) is based on the 32-bit 56800EX core. Each device combines, on a single chip, the processing power of a DSP and the functionality of an MCU with a flexible set of peripherals to support many target applications:
  - Industrial control
  - Home appliances
  - Smart sensors
  - Fire and security systems
  - Switched-mode power supply and power management
  - Uninterruptible Power Supply (UPS)
  - Solar and wind power generator
  - Power metering
  - Motor control (ACIM, BLDC, PMSM, SR, stepper)
  - Handheld power tools
  - Circuit breaker
  - Medical device/equipment
  - Instrumentation
  - Lighting

- DSC based on 32-bit 56800EX core
  - Up to 100 MIPS at 100 MHz core frequency
  - DSP and MCU functionality in a unified, C-efficient architecture

- On-chip memory
  - Up to 288 KB (256 KB + 32 KB) flash memory, including up to 32 KB FlexNVM
  - Up to 32 KB RAM
  - Up to 2 KB FlexRAM with EEE capability
  - 100 MHz program execution from both internal flash memory and RAM
  - On-chip flash memory and RAM can be mapped into both program and data memory spaces

- Analog
  - Two high-speed, 8-channel, 12-bit ADCs with dynamic x2, x4 programmable amplifier
  - One 20-channel, 16-bit ADC
  - Four analog comparators with integrated 6-bit DAC references
  - One 12-bit DAC

- PWMs and timers
  - Two eFlexPWM modules with up to 24 PWM outputs, one including 8 channels with high resolution NanoEdge placement
  - Two 16-bit quad timer (2 x 4 16-bit timers)
  - Two Periodic Interval Timers (PITs)
  - One Quadrature Decoder
  - Two Programmable Delay Blocks (PDBs)

- Communication interfaces
  - Three high-speed queued SCI (QSCI) modules with LIN slave functionality
  - Up to three queued SPI (QSPI) modules
  - Two SMBus-compatible I2C ports
  - One flexible controller area network (FlexCAN) module

- Security and integrity
  - Cyclic Redundancy Check (CRC) generator
  - Computer operating properly (COP) watchdog
  - External Watchdog Monitor (EWM)

- Clocks
  - Two on-chip relaxation oscillators: 8 MHz (400 kHz at standby mode) and 32 kHz
  - Crystal / resonator oscillator

- System
  - DMA controller
  - Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
  - Inter-module crossbar connection
  - JTAG/enhanced on-chip emulation (EOnCE) for unobtrusive, real-time debugging

- Operating characteristics
  - Single supply: 3.0 V to 3.6 V
  - 5 V–tolerant I/O (except RESETB pin)

- LQFP packages:
  - 64-pin
  - 80-pin
  - 100-pin

Table of Contents

1 Overview

1.1 MC56F844x/5x/7x Product Family

The following table highlights major features, including features that differ among members of the family. Features not listed are shared by all members of the family.

Table 1. 56F844x/5x/7x Family

Part Number	MC56F84																	
	789	**786**	**769**	**766**	**763**	**553**	**550**	**543**	**540**	**587**	**585**	**567**	**565**	**462**	**452**	**451**	**442**	**441**
Core freq. (MHz)	100	100	100	100	100	80	80	80	80	80	80	80	80	60	60	60	60	60
Flash memory (KB)	256	256	128	128	128	96	96	64	64	256	256	128	128	128	96	96	64	64
FlevNVM/ FlexRAM (KB)	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2	32/2
Total flash memory (KB)[1]	288	288	160	160	160	128	128	96	96	288	288	160	160	160	128	128	96	96
RAM (KB)	32	32	24	24	24	16	16	8	8	32	32	24	24	24	16	16	8	8
Memory resource protection	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Watchdog	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
12-bit Cyclic ADC channels	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (300 ns)	2x5 (300 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x8 (600 ns)	2x5 (600 ns)	2x8 (600 ns)	2x5 (600 ns)
16-bit SAR ADC (with Temp Sensor) channels	1x 16	1x 10	1x 16	1x 10	1x8	1x8	0	1x8	0	1x 16	1x 10	1x 16	1x 10	0	1x8	0	1x8	0
PWMA with input capture:																		
High-resolution channels	1x8	1x8	1x8	1x8	1x8	1x8	1x6	1x8	1x6	0	0	0	0	0	0	0	0	0
Standard channels	4	1	4	1	1	1	0	1	0	2x 12	1x 12, 1x9	2x 12	1x 12, 1x9	1x9	1x9	1x6	1x9	1x6

Table continues on the next page...

Table 1. 56F844x/5x/7x Family (continued)

Part Number	MC56F84																	
	789	786	769	766	763	553	550	543	540	587	585	567	565	462	452	451	442	441
PWMB with input capture: Standard channels	1x 12	1x7	1x 12	1x7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12-bit DAC	1	1	1	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0
Quad Decoder	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DMA	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
CMP	4	4	4	4	4	4	3	4	3	4	4	4	4	4	4	3	4	3
QSCI	3	3	3	3	2	2	2	2	2	3	3	3	3	2	2	2	2	2
QSPI	3	2	3	2	2	2	2	2	2	3	2	3	2	2	2	2	2	2
I2C/SMBus	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
FlexCAN	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
LQFP package pin count	100	80	100	80	64	64	48	64	48	100	80	100	80	64	64	48	64	48

1. This total includes FlexNVM and assumes no FlexNVM is used with FlexRAM for EEPROM.

1.2 56800EX 32-bit Digital Signal Controller Core

- Efficient 32-bit 56800EX Digital Signal Processor (DSP) engine with modified dual Harvard architecture
  - Three internal address buses
  - Four internal data buses: two 32-bit primary buses, one 16-bit secondary data bus, and one 16-bit instruction bus
  - 32-bit data accesses
  - Support for concurrent instruction fetches in the same cycle and dual data accesses in the same cycle
  - 20 addressing modes
- As many as 100 million instructions per second (MIPS) at 100 MHz core frequency
- 162 basic instructions
- Instruction set supports both fractional arithmetic and integer arithmetic
- 32-bit internal primary data buses supporting 8-bit, 16-bit, and 32-bit data movement, addition, subtraction, and logical operation
- Single-cycle 16 × 16-bit -> 32-bit and 32 x 32-bit -> 64-bit multiplier-accumulator (MAC) with dual parallel moves
- 32-bit arithmetic and logic multi-bit shifter
- Four 36-bit accumulators, including extension bits

- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Bit reverse address mode, effectively supporting DSP and Fast Fourier Transform algorithms
- Full shadowing of the register stack for zero-overhead context saves and restores: nine shadow registers corresponding to the R0, R1, R2, R3, R4, R5, N, N3, and M01 address registers
- Instruction set supporting both DSP and controller functions
- Controller-style addressing modes and instructions for compact code
- Enhanced bit manipulation instruction set
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- Priority level setting for interrupt levels
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging that is independent of processor speed

1.3 Operation Parameters

- Up to 100 MHz operation at -40 °C to 105 °C ambient temperature
- Single 3.3 V power supply
- Supply range: V_{DD} - V_{SS} = 2.7 V to 3.6 V, V_{DDA} - V_{SSA} = 2.7 V to 3.6 V

1.4 On-Chip Memory and Memory Protection

- Modified dual Harvard architecture permits as many as three simultaneous accesses to program and data memory
- Internal flash memory with security and protection to prevent unauthorized access
- Memory resource protection (MRP) unit to protect supervisor programs and resources from user programs
- Programming code can reside in flash memory during flash programming
- The dual-ported RAM controller supports concurrent instruction fetches and data accesses, or dual data accesses, by the DSC core.
  - Concurrent accesses provide increased performance.
  - The data and instruction arrive at the core in the same cycle, reducing latency.
- On-chip memory
  - Up to 144 KW program/data flash memory, including FlexNVM
  - Up to 16 KW dual port data/program RAM

- Up to 16 KW FlexNVM, which can be used as additional program or data flash memory
- Up to 1 KW FlexRAM, which can be configured as enhanced EEPROM (used in conjunction with FlexNVM) or used as additional RAM

1.5 Interrupt Controller

- Five interrupt priority levels
  - Three user programmable priority levels for each interrupt source: level 0, 1, 2
  - Unmaskable level 3 interrupts include: illegal instruction, hardware stack overflow, misaligned data access, SWI3 instruction
  - Maskable level 3 interrupts include: EOnCE step counter, EOnCE breakpoint unit, EOnCE trace buffer
  - Lowest-priority software interrupt: level LP
- Support for nested interrupt: higher priority level interrupt request can interrupt lower priority interrupt subroutine
- Masking of interrupt priority level managed by the 56800EX core
- Two programmable fast interrupts that can be assigned to any interrupt source
- Notification to System Integration Module (SIM) to restart clock when in wait and stop states
- Ability to relocate interrupt vector table

1.6 Peripheral highlights

1.6.1 Enhanced Flex Pulse Width Modulator (eFlexPWM)

- PWM module contains four identical submodules with up to three outputs per submodule
- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- PWMA with NanoEdge high resolution
  - Fractional delay for enhanced resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - 312 ps PWM frequency and duty-cycle resolution when NanoEdge functionality is enabled
- PWMB with supporting accumulative fractional clock calculation
  - Accumulative fractional clock calculation improves the resolution of the PWM period and edge placement
  - Arbitrary PWM edge placement
  - Equivalent to 312 ps PWM frequency and duty-cycle resolution on average

- PWM outputs can be configured as complementary output pairs or independent outputs
- Dedicated time-base counter with period and frequency control per submodule
- Independent top and bottom deadtime insertion for each complementary pair
- Independent control of both edges of each PWM output
- Enhanced input capture and output compare functionality on each input
  - Channels not used for PWM generation can be used for buffered output compare functions
  - Channels not used for PWM generation can be used for input capture functions
  - Enhanced dual edge capture functionality
- Synchronization of submodule to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half-cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware
- Support for double switching PWM outputs
- Up to eight fault inputs can be assigned to control multiple PWM outputs
  - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software control of each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event
- PWMX pin can optionally output a third PWM signal from each submodule
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - Crossbar module outputs
  - External ADC input, taking into account values set in ADC high and low limit registers

1.6.2 12-bit Analog-to-Digital Converter (Cyclic type)

- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 8-channel external inputs
  - Built-in x1, x2, x4 programmable gain pre-amplifier
  - Maximum ADC clock frequency is up to 20 MHz with as low as 50 ns period
  - Single conversion time of 8.5 ADC clock cycles
  - Additional conversion time of 6 ADC clock cycles
- Support of analog inputs for single-ended and differential conversions
- Sequential, parallel, and independent scan mode
- First 8 samples have offset, limit and zero-crossing calculation supported
- ADC conversions can be synchronized by any module connected to internal crossbar module, such as PWM and timer modules and GPIO and comparators

- Support for simultaneous and software triggering conversions
- Support for multi-triggering mode with a programmable number of conversions on each trigger
- Each ADC has ability to scan and store up to 8 conversion results
- Current injection protection

1.6.3 Inter-Module Crossbar and AND-OR-INVERT logic

- Provides generalized connections between and among on-chip peripherals: ADCs, 12-bit DAC, Comparators, Quad Timers, eFlexPWMs, PDBs, EWM, Quadrature Decoder, and select I/O pins
- User-defined input/output pins for all modules connected to crossbar
- DMA request and interrupt generation from crossbar
- Write-once protection for all registers
- AND-OR-INVERT function that provides a universal Boolean function generator using a four-term sum-of-products expression, with each product term containing true or complement values of the four selected inputs (A, B, C, D).

1.6.4 Comparator

- Full rail-to-rail comparison range
- Support for high speed mode and low speed mode
- Selectable input source includes external pins and internal DACs
- Programmable output polarity
- 6-bit programmable DAC as voltage reference per comparator
- Three programmable hysteresis levels
- Selectable interrupt on rising edge, falling edge, or toggle of comparator output

1.6.5 12-bit Digital-to-Analog Converter

- 12-bit resolution
- Powerdown mode
- Automatic mode allows the DAC to automatically generate pre-programmed output waveforms including square, triangle, and sawtooth waveforms for applications such as slope compensation
- Programmable period, update rate, and range
- Output can be routed to an internal comparator, ADC, or optionally off chip

1.6.6 Quad Timer

- Four 16-bit up/down counters with programmable prescaler for each counter
- Operation modes: edge count, gated count, signed count, capture, compare, PWM, signal shot, single pulse, pulse string, cascaded, quadrature decode
- Programmable input filter
- Counting start can be synchronized across counters

1.6.7 Queued Serial Communications Interface (QSCI) Modules

- Operating clock up to two times CPU operating frequency
- Four-word-deep FIFOs available on both transmit and receive buffers
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit integer and 3-bit fractional baud rate selection
- Full-duplex or single-wire operation
- Programmable 8-bit or 9-bit data format
- Error detection capability
- Two receiver wakeup methods:
  - Idle line
  - Address mark
- 1/16 bit-time noise detection

1.6.8 Queued Serial Peripheral Interface (QSPI) Modules

- Maximum 25 Mbps baud rate
- Selectable baud rate clock sources for low baud rate communication
- Baud rate as low as Baudrate_Freq_in / 8192
- Full-duplex operation
- Master and slave modes
- Double-buffered operation with separate transmit and receive registers
- Four-word-deep FIFOs available on transmit and receive buffers
- Programmable length transmissions (2 bits to 16 bits)
- Programmable transmit and receive shift order (MSB as first bit transmitted)

1.6.9 Inter-Integrated Circuit (I2C)/System Management Bus (SMBus) Modules

- Compatible with I2C bus standard
- Support for System Management Bus (SMBus) specification, version 2
- Multi-master operation

- General call recognition
- 10-bit address extension
- Start/Repeat and Stop indication flags
- Support for dual slave addresses or configuration of a range of slave addresses
- Programmable glitch input filter

1.6.10 Flex Controller Area Network (FlexCAN) Module

- Clock source from PLL or XOSC/CLKIN
- Implementation of the CAN protocol Version 2.0 A/B
- Standard and extended data frames
- 0-to-8 bytes data length
- Programmable bit rate up to 1 Mbps
- Support for remote frames
- Sixteen Message Buffers, each configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask Registers per Message Buffer
- Internal timer for time-stamping of received and transmitted messages
- Listen-only mode capability
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Global network time, synchronized by a specific message
- Low power modes, with programmable wakeup on bus activity

1.6.11 Computer Operating Properly (COP) Watchdog

- Programmable timeout period
- Support for operation in all power modes: run mode, wait mode, stop mode
- Causes loss of reference reset 128 cycles after loss of reference clock to the PLL is detected
- Selectable reference clock source in support of EN60730 and IEC61508
- Selectable clock sources:
  - External crystal oscillator/external clock source
  - On-chip low-power 32 kHz oscillator
  - System bus (IPBus up to 100 MHz)
  - 8 MHz / 400 kHz ROSC
- Support for interrupt triggered when the counter reaches the timeout value

1.6.12 Power Supervisor

- Power-on reset (POR) to reset CPU, peripherals, and JTAG/EOnCE controllers (VDD > 2.1 V)
- Brownout reset (VDD < 1.9 V)
- Critical warn low voltage interrupt (LVI2.0)
- Peripheral low voltage interrupt (LVI2.7)

1.6.13 Phase Locked Loop

- Wide programmable output frequency: 240 MHz to 400 MHz
- Input reference clock frequency: 8 MHz to 16 MHz
- Detection of loss of lock and loss of reference clock
- Ability to power down

1.6.14 Clock sources

1.6.14.1 On-Chip Oscillators

- Tunable 8 MHz relaxation oscillator with 400 kHz at standby mode (divide-by-two output)
- 32 kHz low frequency clock as secondary clock source for COP, EWM, PIT

1.6.14.2 Crystal Oscillator

- Support for both high ESR crystal oscillator (greater than 100-ohm ESR) and ceramic resonator
- 4 MHz to 16 MHz operating frequency

1.6.15 Cyclic Redundancy Check (CRC) Generator

- Hardware 16/32-bit CRC generator
- High-speed hardware CRC calculation
- Programmable initial seed value
- Programmable 16/32-bit polynomial
- Error detection for all single, double, odd, and most multi-bit errors

- Option to transpose input data or output data (CRC result) bitwise or bytewise,[1] which is required for certain CRC standards
- Option for inversion of final CRC result

1.6.16 General Purpose I/O (GPIO)

- 5 V tolerance
- Individual control of peripheral mode or GPIO mode for each pin
- Programmable push-pull or open drain output
- Configurable pullup or pulldown on all input pins
- All pins except JTAG and RESETB pins default to be GPIO inputs
- 2 mA / 9 mA source/sink capability
- Controllable output slew rate

1.7 Block Diagrams

The 56800EX core is based on a modified dual Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

The device's basic architecture appears in Figure 1 and Figure 2. Figure 1 illustrates how the 56800EX system buses communicate with internal memories and the IPBus interface and the internal connections among each unit of the 56800EX core. Figure 2 shows the peripherals and control blocks connected to the IPBus bridge. See the specific device’s Reference Manual for details.

1. A bytewise transposition is not possible when accessing the CRC data register via 8-bit accesses. In this case, user software must perform the bytewise transposition.

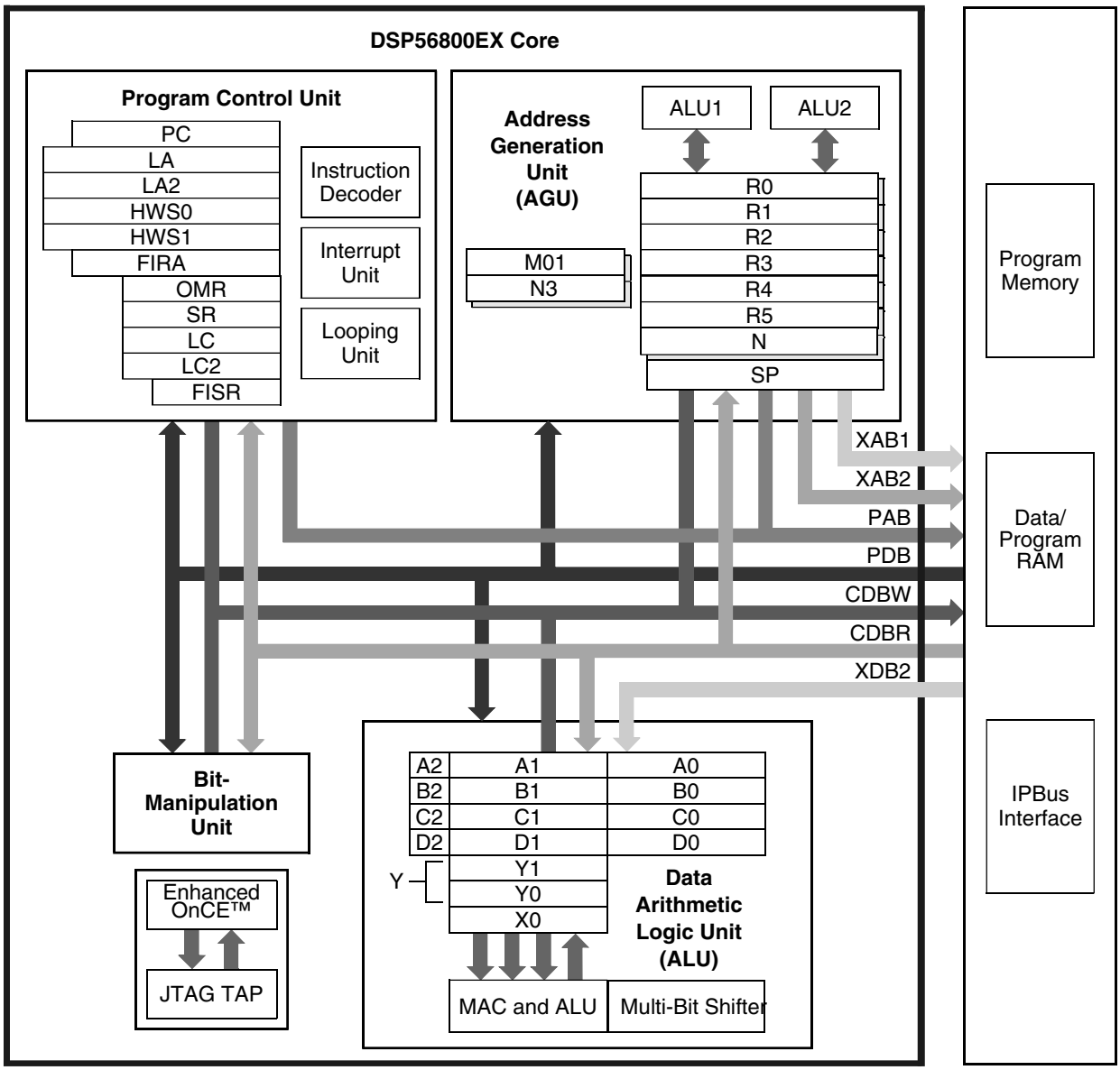


Figure 1. 56800EX Basic Block Diagram

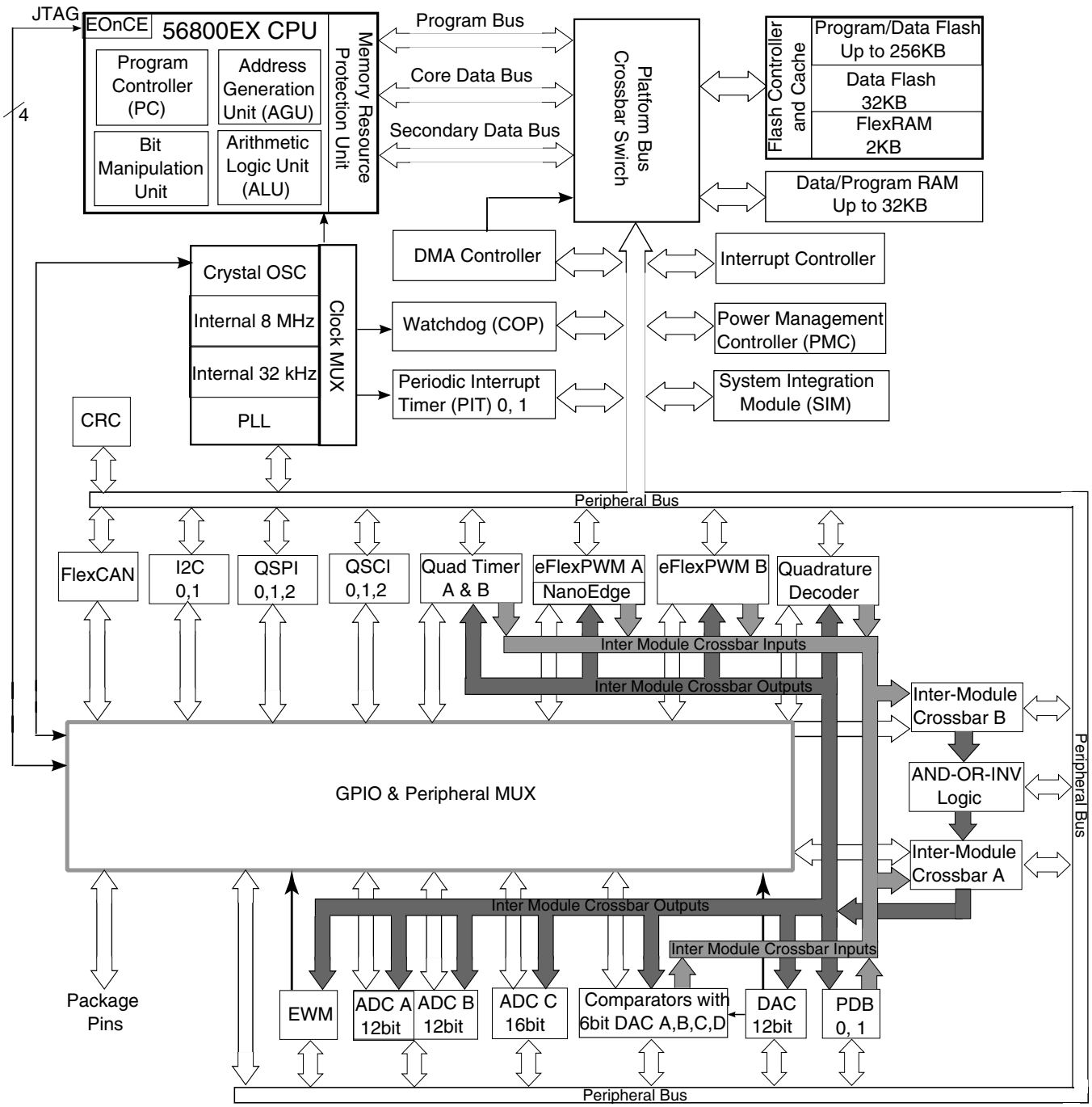


Figure 2. System Diagram

2 Signal groups

The input and output signals of the MC56F84xxx are organized into functional groups, as detailed in Table 2.

Table 2. Functional Group Pin Allocations

Functional Group	Number of Pins in 48LQFP	Number of Pins in 64LQFP	Number of Pins in 80LQFP	Number of Pins in 100LQFP
Power Inputs (V_{DD}, V_{DDA}, V_{CAP})	5	6	6	6
Ground (V_{SS}, V_{SSA})	4	4	4	4
Reset	1	1	1	1
eFlexPWM with NanoEdge ports, not including fault pins	6	8	8	8
eFlexPWM without NanoEdge ports, not including fault pins	0	1	7	16
Queued Serial Peripheral Interface (QSPI) ports	5	6	8	15
Queued Serial Communications Interface (QSCI) ports	6	9	13	15
Inter-Integrated Circuit (I^2C) interface ports	4	6	6	6
12-bit Analog-to-Digital Converter (Cyclic ADC) inputs	10	16	16	16
16-bit Analog-to-Digital Converter (SAR ADC) inputs	2	8	10	16
Analog Comparator inputs/outputs	10/4	13/6	13/6	16/6
12-bit Digital-to-Analog output	1	1	1	1
Quad Timer Module (TMR) ports	6	9	11	13
Controller Area Network (FlexCAN)	2	2	2	2
Inter-Module Crossbar inputs/outputs	12/2	16/6	19/17	25/19
Clock inputs/outputs	2/2	2/2	2/3	2/3
JTAG / Enhanced On-Chip Emulation (EOnCE)	4	4	4	4

3 Ordering parts

3.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device numbers: MC56F84

4 Part identification

4.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

4.2 Format

Part numbers for this device have the following format: Q 56F8 4 C F P T PP N

4.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• MC = Fully qualified, general market flow • PC = Prequalification
56F8	DSC family with flash memory and DSP56800/ DSP56800E/DSP56800EX core	• 56F8
4	DSC subfamily	• 4
C	Maximum CPU frequency (MHz)	• 4 = 60 MHz • 5 = 80 MHz • 7 = 100 MHz
F	Primary program flash memory size	• 4 = 64 KB • 5 = 96 KB • 6 = 128 KB • 8 = 256 KB
P	Pin count	• 0 and 1 = 48 • 2 and 3 = 64 • 4, 5, and 6 = 80 • 7, 8, and 9 = 100
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LF = 48LQFP • LH = 64LQFP • LK = 80LQFP • LL = 100LQFP
N	Packaging type	• R = Tape and reel • (Blank) = Trays

4.4 Example

This is an example part number: MC56F84789VLL

5 Terminology and guidelines

5.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

5.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

5.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

5.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

5.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

5.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

5.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

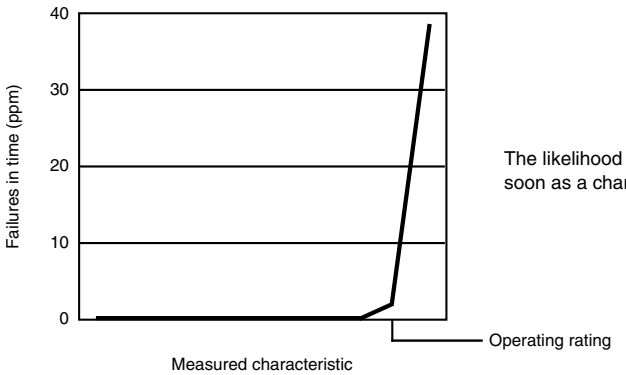
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

5.4.1 Example

This is an example of an operating rating:

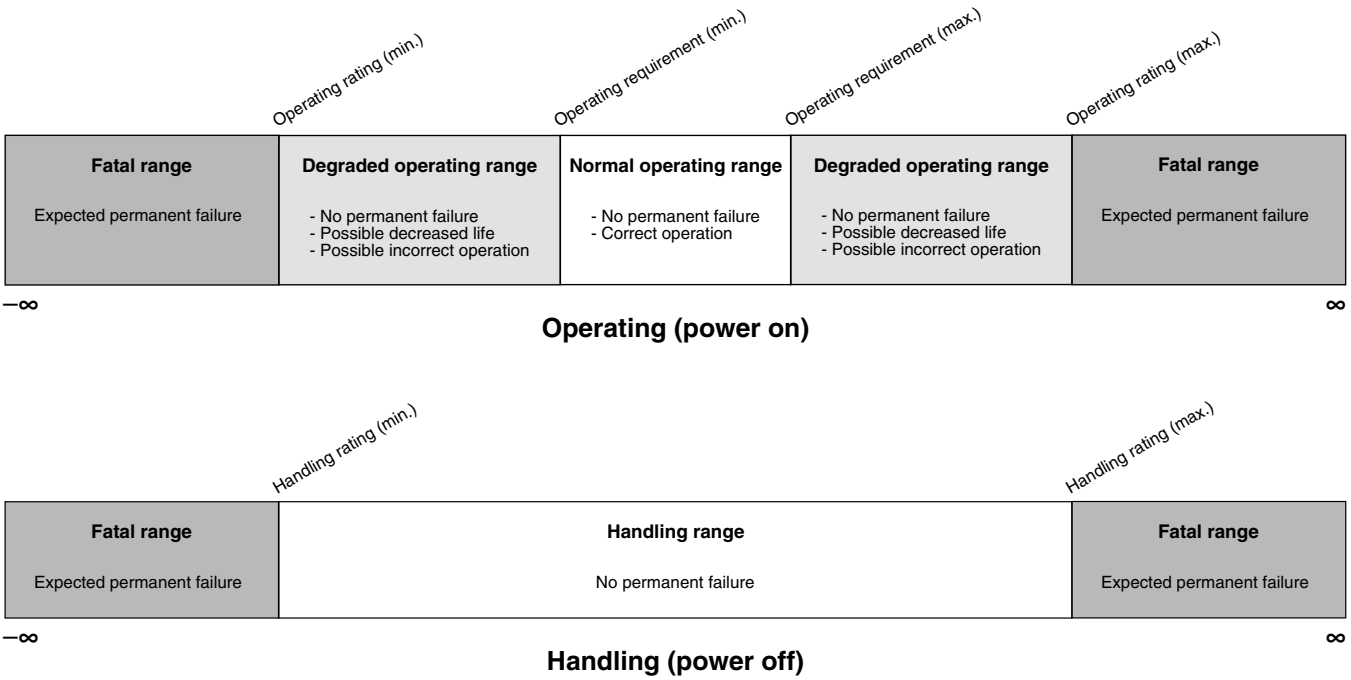
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

5.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

5.6 Relationship between ratings and operating requirements



5.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

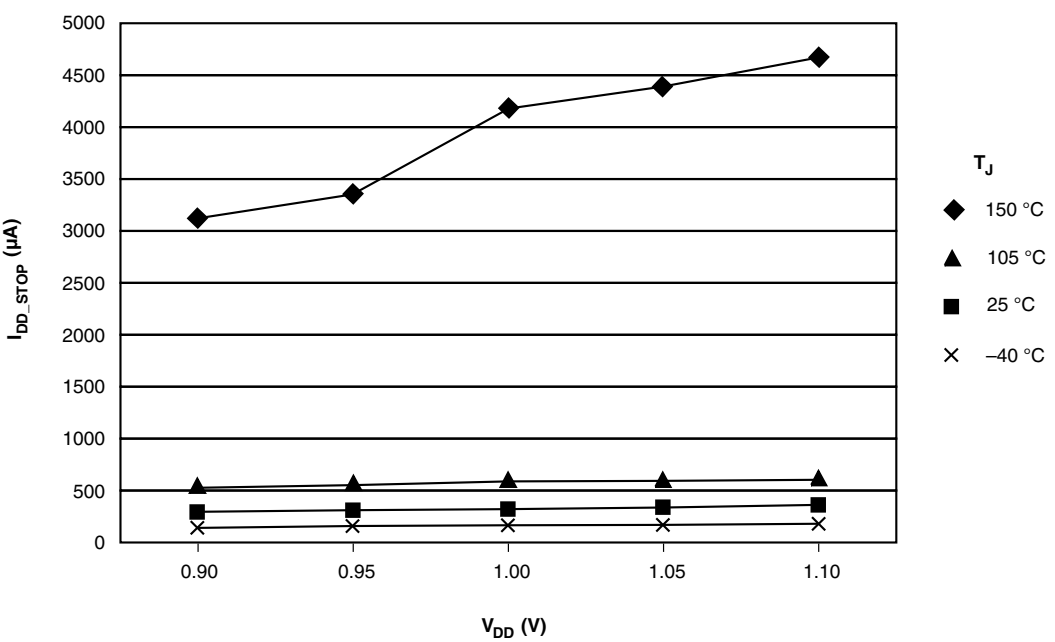
5.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

5.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



5.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

6 Ratings

6.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

6.3 ESD handling ratings

Although damage from electrostatic discharge (ESD) is much less common on these devices than on early CMOS circuits, use normal handling precautions to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with AEC-Q100 Stress Test Qualification. During the device qualification ESD stresses were performed for the human body model (HBM), the machine model (MM), and the charge device model (CDM).

All latch-up testing is in conformity with AEC-Q100 Stress Test Qualification.

A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 3. ESD/Latch-up Protection

Characteristic[1]	Min	Max	Unit
ESD for Human Body Model (HBM)	–2000	+2000	V
ESD for Machine Model (MM)	–200	+200	V
ESD for Charge Device Model (CDM)	–500	+500	V
Latch-up current at TA= 85°C (I_{LAT})	–100	+100	mA

1. Parameter is achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted.

6.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device.

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Supply Voltage Range	V_{DD}		-0.3	4.0	V
Analog Supply Voltage Range	V_{DDA}		-0.3	4.0	V
ADC High Voltage Reference	V_{REFHx}		-0.3	4.0	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}		-0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}		-0.3	0.3	V

Table continues on the next page...

Table 4. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V) (continued)

Characteristic	Symbol	Notes[1]	Min	Max	Unit
Digital Input Voltage Range	V_{IN}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Input Voltage Range	V_{IN_RESET}	Pin Group 2	-0.3	4.0	V
Oscillator Input Voltage Range	V_{OSC}	Pin Group 4	-0.4	4.0	V
Analog Input Voltage Range	V_{INA}	Pin Group 3	-0.3	4.0	V
Input clamp current, per pin (V_{IN} < V_{SS} - 0.3 V)[2, 3]	V_{IC}		—	-5.0	mA
Output clamp current, per pin[4]	V_{OC}		—	±20.0	mA
Contiguous pin DC injection current—regional limit sum of 16 contiguous pins	I_{ICont}		-25	25	mA
Output Voltage Range (normal push-pull mode)	V_{OUT}	Pin Group 1, 2	-0.3	4.0	V
Output Voltage Range (open drain mode)	V_{OUTOD}	Pin Group 1	-0.3	5.5	V
$\overline{\text{RESET}}$ Output Voltage Range	V_{OUTOD_RESET}	Pin Group 2	-0.3	4.0	V
DAC Output Voltage Range	V_{OUT_DAC}	Pin Group 5	-0.3	4.0	V
Ambient Temperature Industrial	T_A		-40	105	°C
Storage Temperature Range (Extended Industrial)	T_{STG}		-55	150	°C

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
2. Continuous clamp current
3. All 5 volt tolerant digital I/O pins are internally clamped to VSS through a ESD protection diode. There is no diode connection to VDD. If VIN greater than VDIO_MIN (=VSS-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required.
4. I/O is configured as push-pull mode.

7 General

7.1 General Characteristics

The device is fabricated in high-density, low-power CMOS with 5 V–tolerant TTL-compatible digital inputs, except for the $\overline{\text{RESET}}$ pin which is 3.3 V only. The term “5 V–tolerant” refers to the capability of an I/O pin, built on a 3.3 V–compatible process technology, to withstand a voltage up to 5.5 V without damaging the device.

5 V–tolerant I/O is desirable because many systems have a mixture of devices designed for 3.3 V and 5 V power supplies. In such systems, a bus may carry both 3.3 V– and 5 V–compatible I/O voltage levels (a standard 3.3 V I/O is designed to receive a maximum

voltage of 3.3 V ± 10% during normal operation without causing damage). This 5 V–tolerant capability therefore offers the power savings of 3.3 V I/O levels combined with the ability to receive 5 V levels without damage.

Absolute maximum ratings in Table 4 are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

Unless otherwise stated, all specifications within this chapter apply over the temperature range of -40°C to 105°C ambient temperature over the following supply ranges: VSS = VSSA = 0 V, VDD = VDDA = 3.0 V to 3.6 V, CL ≤ 50 pF, f_{OP} = 100 MHz.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

7.2 AC Electrical Characteristics

Tests are conducted using the input levels specified in Table 7. Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured between the 10% and 90% points, as shown in Figure 3.

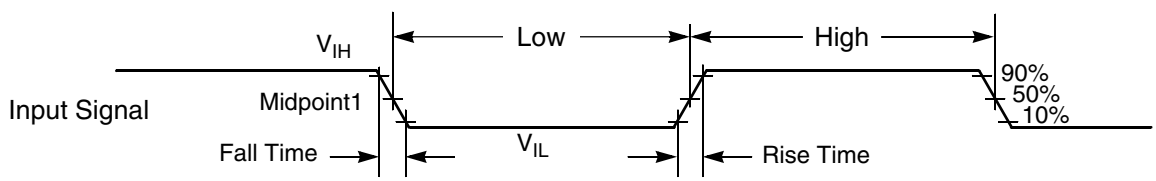


Figure 3. Input Signal Measurement References

Figure 4 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

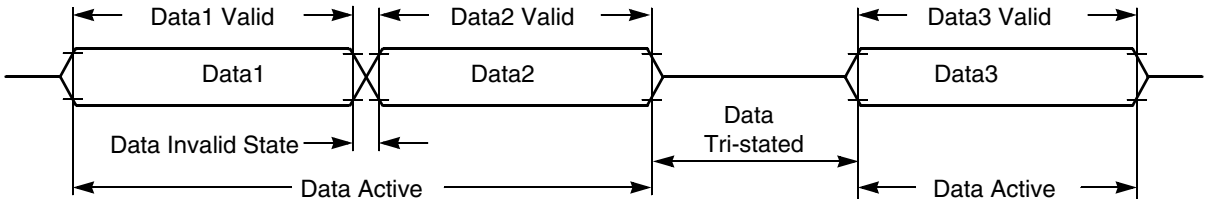


Figure 4. Signal States

7.3 Nonswitching electrical specifications

7.3.1 Voltage and current operating requirements

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 5. Recommended Operating Conditions (V_{REFLx} = 0 V, V_{SSA} = 0 V, V_{SS} = 0 V)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit
Supply voltage[2]	V_{DD}, V_{DDA}		2.7	3.3	3.6	V
ADC (Cyclic) Reference Voltage High	V_{REFHA} V_{REFHB}		3.0		V_{DDA}	V
ADC (SAR) Reference Voltage High	V_{REFHC}		2.0		V_{DDA}	V
Voltage difference V_{DD} to V_{DDA}	ΔVDD		-0.1	0	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔVSS		-0.1	0	0.1	V
Input Voltage High (digital inputs)	V_{IH}	Pin Group 1	0.7 x V_{DD}		5.5	V
$\overline{\text{RESET}}$ Voltage High	V_{IH_RESET}	Pin Group 2	0.7 x V_{DD}	—	V_{DD}	V
Input Voltage Low (digital inputs)	V_{IL}	Pin Groups 1, 2			0.35 x V_{DD}	V
Oscillator Input Voltage High XTAL driven by an external clock source	V_{IHOSC}	Pin Group 4	2.0		V_{DD} + 0.3	V
Oscillator Input Voltage Low	V_{ILOSC}	Pin Group 4	-0.3		0.8	V
Output Source Current High (at V_{OH} min.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OH}	 Pin Group 1 Pin Group 1	 — —		 -2 -9	 mA
Output Source Current Low (at V_{OL} max.)[3, 4] • Programmed for low drive strength • Programmed for high drive strength	I_{OL}	 Pin Groups 1, 2 Pin Groups 1, 2	 — —		 2 9	 mA

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$

- Pin Group 3: ADC and Comparator Analog Inputs
- Pin Group 4: XTAL, EXTAL
- Pin Group 5: DAC analog output

2. ADC (Cyclic) specifications are not guaranteed when V_{DDA} is below 3.0 V.
3. Total chip source or sink current cannot exceed 75 mA.
4. Contiguous pin DC injection current of regional limit—includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins—is 25 mA.

7.3.2 LVD and POR operating requirements

Table 6. PMC Low-Voltage Detection (LVD) and Power-On Reset (POR) Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
POR Assert Voltage[1]	POR		2.0		V
POR Release Voltage[2]	POR		2.7		V
LVI_2p7 Threshold Voltage			2.73		V
LVI_2p2 Threshold Voltage			2.23		V

1. During 3.3-volt V_{DD} power supply ramp down
2. During 3.3-volt V_{DD} power supply ramp up (gated by LVI_2p7)

7.3.3 Voltage and current operating behaviors

The following table provides information about power supply requirements and I/O pin characteristics.

Table 7. DC Electrical Characteristics at Recommended Operating Conditions

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit	Test Conditions
Output Voltage High	V_{OH}	Pin Group 1	V_{DD} - 0.5	—	—	V	$I_{OH} = I_{OHmax}$
Output Voltage Low	V_{OL}	Pin Groups 1, 2	—	—	0.5	V	$I_{OL} = I_{OLmax}$
Digital Input Current High	I_{IH}	Pin Group 1	—	0	+/- 2.5	µA	V_{IN} = 2.4 V to 5.5 V
pull-up enabled or disabled		Pin Group 2					V_{IN} = 2.4 V to V_{DD}
Comparator Input Current High	I_{IHC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Oscillator Input Current High	I_{IHOSC}	Pin Group 3	—	0	+/- 2	µA	$V_{IN} = V_{DDA}$
Internal Pull-Up Resistance	$R_{Pull-Up}$		20	—	50	kΩ	—
Internal Pull-Down Resistance	$R_{Pull-Down}$		20	—	50	kΩ	—

Table continues on the next page...

Table 7. DC Electrical Characteristics at Recommended Operating Conditions (continued)

Characteristic	Symbol	Notes[1]	Min	Typ	Max	Unit	Test Conditions
Comparator Input Current Low	I_{ILC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
Oscillator Input Current Low	I_{ILOSC}	Pin Group 3	—	0	+/- 2	µA	V_{IN} = 0V
DAC Output Voltage Range	V_{DAC}	Pin Group 5	Typically V_{SSA} + 40mV	—	Typically V_{DDA} - 40mV	V	R_{LD} = 3 kΩ ll C_{LD} = 400 pf
Output Current[1] High Impedance State	I_{OZ}	Pin Groups 1, 2	—	0	+/- 1	µA	—
Schmitt Trigger Input Hysteresis	V_{HYS}	Pin Groups 1, 2	0.06 x V_{DD}	—	—	V	—

1. **Default Mode**
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC

7.3.4 Power mode transition operating behaviors

Parameters listed are guaranteed by design.

NOTE

All address and data buses described here are internal.

Table 8. Reset, Stop, Wait, and Interrupt Timing

Characteristic	Symbol	Typical Min	Typical Max	Unit	See Figure
Minimum $\overline{\text{RESET}}$ Assertion Duration	t_{RA}	16[1]	—	ns	—
$\overline{\text{RESET}}$ deassertion to First Address Fetch	t_{RDA}	865 x T_{OSC} + 8 x T		ns	—
Delay from Interrupt Assertion to Fetch of first instruction (exiting Stop)	t_{IF}	361.3	570.9	ns	—

1. If the $\overline{\text{RESET}}$ pin filter is enabled by setting the RST_FLT bit in the SIM_CTRL register to 1, the minimum pulse assertion must be greater than 21 ns.

NOTE

In the Table 8, T = system clock cycle and T_{OSC} = oscillator clock cycle. For an operating frequency of 100 MHz, T = 10 ns. At 4 MHz (used coming out of reset and stop modes), T = 250 ns.

7.3.5 Power consumption operating behaviors

Table 9. Current Consumption

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
RUN	100 MHz	• 100 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Continuous MAC instructions with fetches from Program Flash • All peripheral modules enabled. • TMRs and SCIs using 1X Clock • NanoEdge within PWMA using 1X clock • ADC/DAC powered on and clocked at 5 MHz[2] • Comparator powered on	63.7 mA	16.7 mA	101 mA	32 mA
WAIT	100 MHz	• 100 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered on • Processor Core in WAIT state • All Peripheral modules enabled. • TMRs and SCIs using 1X Clock • NanoEdge within PWMA using 2X clock • ADC/DAC/Comparator powered off	43.5 mA	1.4 µA	80 mA	6.8 µA
STOP	4 MHz	• 4 MHz Device Clock • Regulators are in full regulation • Relaxation Oscillator on • PLL powered off • Processor Core in STOP state • All peripheral module and core clocks are off • ADC/DAC/Comparator powered off	10.1 mA	—	37 mA	—
LPRUN (LsRUN)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator (ROSC) • ROSC in standby mode • Regulators are in standby • PLL disabled • Repeat NOP instructions • All peripheral modules enabled, except NanoEdge and cyclic ADCs[3] • Simple loop with running from platform instruction buffer	2.30 mA	2.73 mA	30 mA	5.9 mA
LPWAIT (LsWAIT)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator (ROSC) • ROSC in standby mode • Regulators are in standby • PLL disabled • All peripheral modules enabled, except NanoEdge and cyclic ADCs[3] • Processor core in wait mode	2.29 mA	2.73 mA	30 mA	5.9 mA

Table continues on the next page...

Table 9. Current Consumption (continued)

Mode	Maximum Frequency	Conditions	Typical at 3.3 V, 25°C		Maximum at 3.6 V, 105°C	
			I_{DD}[1]	I_{DDA}	I_{DD}[1]	I_{DDA}
LPSTOP (LsSTOP)	2 MHz	• 200 kHz Device Clock from Relaxation Oscillator (ROSC) • ROSC in standby mode • Regulators are in standby • PLL disabled • Only PITs and COP enabled; other peripheral modules disabled and clocks gated off[3] • Processor core in stop mode	1.55 mA	—	29 mA	—
VLPRUN	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • Repeat NOP instructions • All peripheral modules, except COP and EWM, disabled and clocks gated off • Simple loop running from platform instruction buffer	1.18 mA	522 nA	27 mA	8.5 µA
VLPWAIT	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in wait mode	1.10 mA	506 nA	26 mA	8.5 µA
VLPSTOP	200 kHz	• 32 kHz Device Clock • Clocked by a 32 kHz external clock source • Oscillator in power down • All ROSCs disabled • Large regulator is in standby • Small regulator is disabled • PLL disabled • All peripheral modules, except COP, disabled and clocks gated off • Processor core in stop mode	1.03 mA	—	26 mA	—

1. No output switching, all ports configured as inputs, all inputs low, no DC loads
2. ADC power consumption at higher frequency can be found in Table 26
3. In all chip LP modes and flash memory VLP modes, the maximum frequency for flash memory operation is 500 kHz due to the fixed frequency ratio of 1:4 between the CPU clock and the flash clock.

7.3.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

7.3.7 Capacitance attributes

Table 10. Capacitance attributes

Description	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	—	10	—	pF
Output capacitance	C_{OUT}	—	10	—	pF

7.4 Switching specifications

7.4.1 Device clock specifications

Table 11. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYSCLK}	Device (system and core) clock frequency • using relaxation oscillator • using external clock source	 0.001 0	 100 100	MHz	
f_{IPBUS}	IP bus clock	—	100	MHz	

7.4.2 General Switching Timing

Table 12. Switching Timing

Symbol	Description	Min	Max	Unit	Notes
	GPIO pin interrupt pulse width[1] Synchronous path	1.5		IP Bus Clock Cycles	2
	Port rise and fall time (high drive strength), Slew disabled 2.7 ≤ V_{DD} ≤ 3.6V.	5.5	15.1	ns	3
	Port rise and fall time (high drive strength), Slew enabled 2.7 ≤ V_{DD} ≤ 3.6V.	1.5	6.8	ns	3

Table continues on the next page...

Table 12. Switching Timing (continued)

Symbol	Description	Min	Max	Unit	Notes
	Port rise and fall time (low drive strength). Slew disabled . 2.7 ≤ V_{DD} ≤ 3.6V	8.2	17.8	ns	4
	Port rise and fall time (low drive strength). Slew enabled . 2.7 ≤ V_{DD} ≤ 3.6V	3.2	9.2	ns	4

1. Applies to a pin only when it is configured as GPIO and configured to cause an interrupt by appropriately programming GPIOn_IPOLR and GPIOn_IENR.
2. The greater synchronous and asynchronous timing must be met.
3. 75 pF load
4. 15 pF load

7.5 Thermal specifications

7.5.1 Thermal operating requirements

Table 13. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature (extended industrial)	–40	105	°C

7.5.2 Thermal attributes

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To account for $P_{I/O}$ in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

See Thermal Design Considerations for more detail on thermal design considerations.

Board type	Symbol	Description	64 LQFP	80 LQFP	100 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	64	55	62	°C/W	1, 2

Table continues on the next page...

Board type	Symbol	Description	64 LQFP	80 LQFP	100 LQFP	Unit	Notes
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	46	40	49	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	44	52	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	39	34	43	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	28	24	35	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	15	12	17	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	3	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
5. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
6. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

8 Peripheral operating requirements and behaviors

8.1 Core modules

8.1.1 JTAG Timing

Table 14. JTAG Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
TCK frequency of operation	f_{OP}	DC	SYS_CLK/16	MHz	Figure 5
TCK clock pulse width	t_{PW}	50	—	ns	Figure 5
TMS, TDI data set-up time	t_{DS}	5	—	ns	Figure 6
TMS, TDI data hold time	t_{DH}	5	—	ns	Figure 6
TCK low to TDO data valid	t_{DV}	—	30	ns	Figure 6
TCK low to TDO tri-state	t_{TS}	—	30	ns	Figure 6

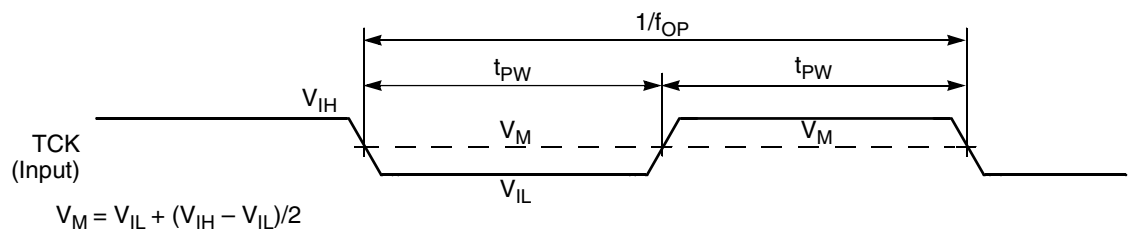


Figure 5. Test Clock Input Timing Diagram

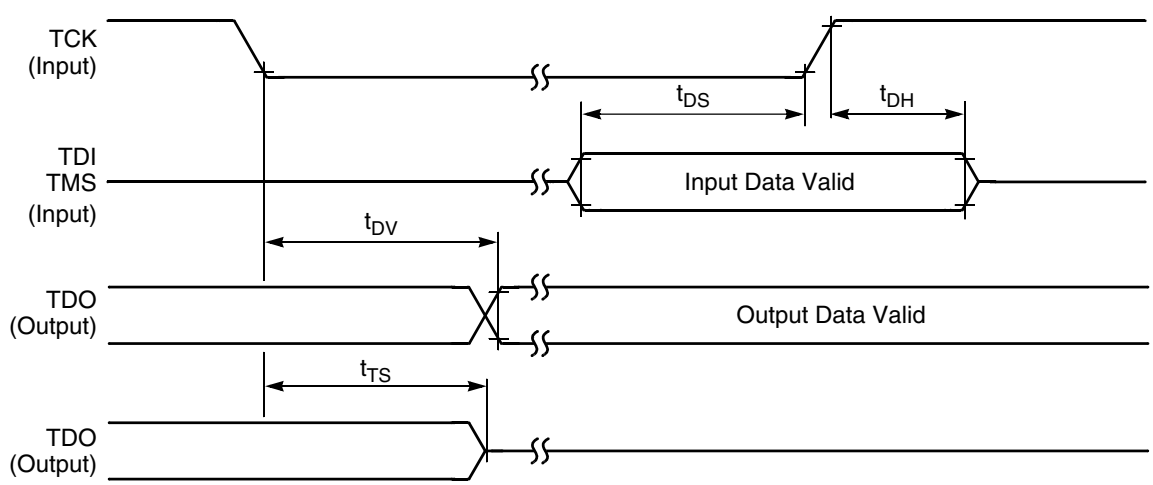


Figure 6. Test Access Port Timing Diagram

8.2 System modules

8.2.1 Voltage Regulator Specifications

The regulator supplies approximately 1.2 V to the MC56F84xxx's core logic. This regulator requires an external 2.2 µF capacitor on each V_{CAP} pin for proper operation. Ceramic and tantalum capacitors tend to provide better performance tolerances. The output voltage can be measured directly on the V_{CAP} pin. The specifications for this regulator are shown in Table 15.

Table 15. Regulator 1.2 V Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage[1]	V_{CAP}	—	1.22	—	V
Short Circuit Current[2]	I_{SS}	—	600		mA
Short Circuit Tolerance (V_{CAP} shorted to ground)	T_{RSC}	—	—	30	Minutes

1. Value is after trim
2. Guaranteed by design

Table 16. Bandgap Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Reference Voltage (after trim)	V_{REF}	—	1.21	—	V

8.3 Clock modules

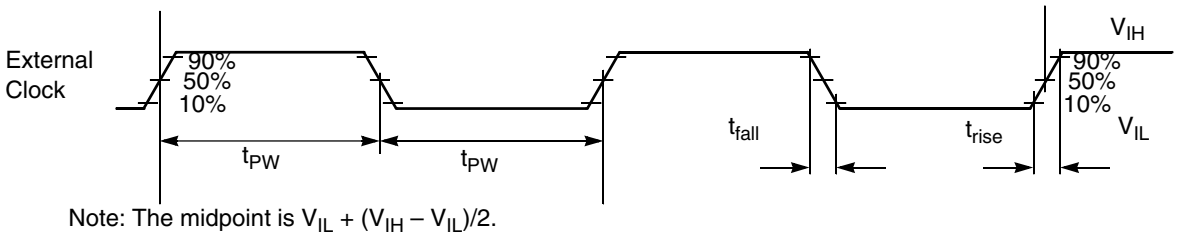
8.3.1 External Clock Operation Timing

Parameters listed are guaranteed by design.

Table 17. External Clock Operation Timing Requirements

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	—	—	50	MHz
Clock pulse width[2]	t_{PW}	8			ns
External clock input rise time[3]	t_{rise}	—	—	1	ns
External clock input fall time[4]	t_{fall}	—	—	1	ns
Input high voltage overdrive by an external clock	V_{ih}	0.85VDD	—	—	V
Input low voltage overdrive by an external clock	V_{il}	—	—	$0.3V_{DD}$	V

1. See Figure 7 for detail on using the recommended connection of an external clock driver.
2. The chip may not function if the high or low pulse width is smaller than 6.25 ns.
3. External clock input rise time is measured from 10% to 90%.
4. External clock input fall time is measured from 90% to 10%.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 7. External Clock Timing

8.3.2 Phase Locked Loop Timing

Table 18. Phase Locked Loop Timing

Characteristic	Symbol	Min	Typ	Max	Unit
PLL input reference frequency[1]	f_{ref}	8	8	16	MHz
PLL output frequency[2]	f_{op}	240	—	400	MHz
PLL lock time[3]	t_{plls}	35.5		73.2	µs
Allowed Duty Cycle of input reference	t_{dc}	40	50	60	%

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8 MHz input.
2. The frequency of the core system clock cannot exceed 100 MHz. If the NanoEdge PWM is available, the PLL output must be set to 400 MHz.
3. This is the time required after the PLL is enabled to ensure reliable operation.

8.3.3 External Crystal or Resonator Requirement

Table 19. Crystal or Resonator Requirement

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation	f_{XOSC}	4	8	16	MHz

8.3.4 Relaxation Oscillator Timing

Table 20. Relaxation Oscillator Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
8 MHz Output Frequency[1] RUN Mode • 0°C to 105°C • -40°C to 105°C Standby Mode (IRC trimmed @ 8 MHz) • -40°C to 105°C		 7.84 7.76 266.8	 8 8 402	 8.16 8.24 554.3	 MHz kHz
8 MHz Frequency Variation RUN Mode Due to temperature • 0°C to 105°C • -40°C to 105°C			 +/- 1.5 +/- 1.5	 +/-2 +/-3	 %
32 kHz Output Frequency[2] RUN Mode • -40°C to 105°C		 30.1	 32	 33.9	 kHz
32 kHz Output Frequency Variation RUN Mode Due to temperature • -40°C to 105°C			 +/-2.5	 +/-4	 %
Stabilization Time • 8 MHz output[3] • 32 kHz output[4]	tstab		 0.12 14.4	 0.4 16.2	 µs
Output Duty Cycle		48	50	52	%

1. Frequency after application of 8 MHz trim
2. Frequency after application of 32 kHz trim
3. Standby to run mode transition
4. Power down to run mode transition

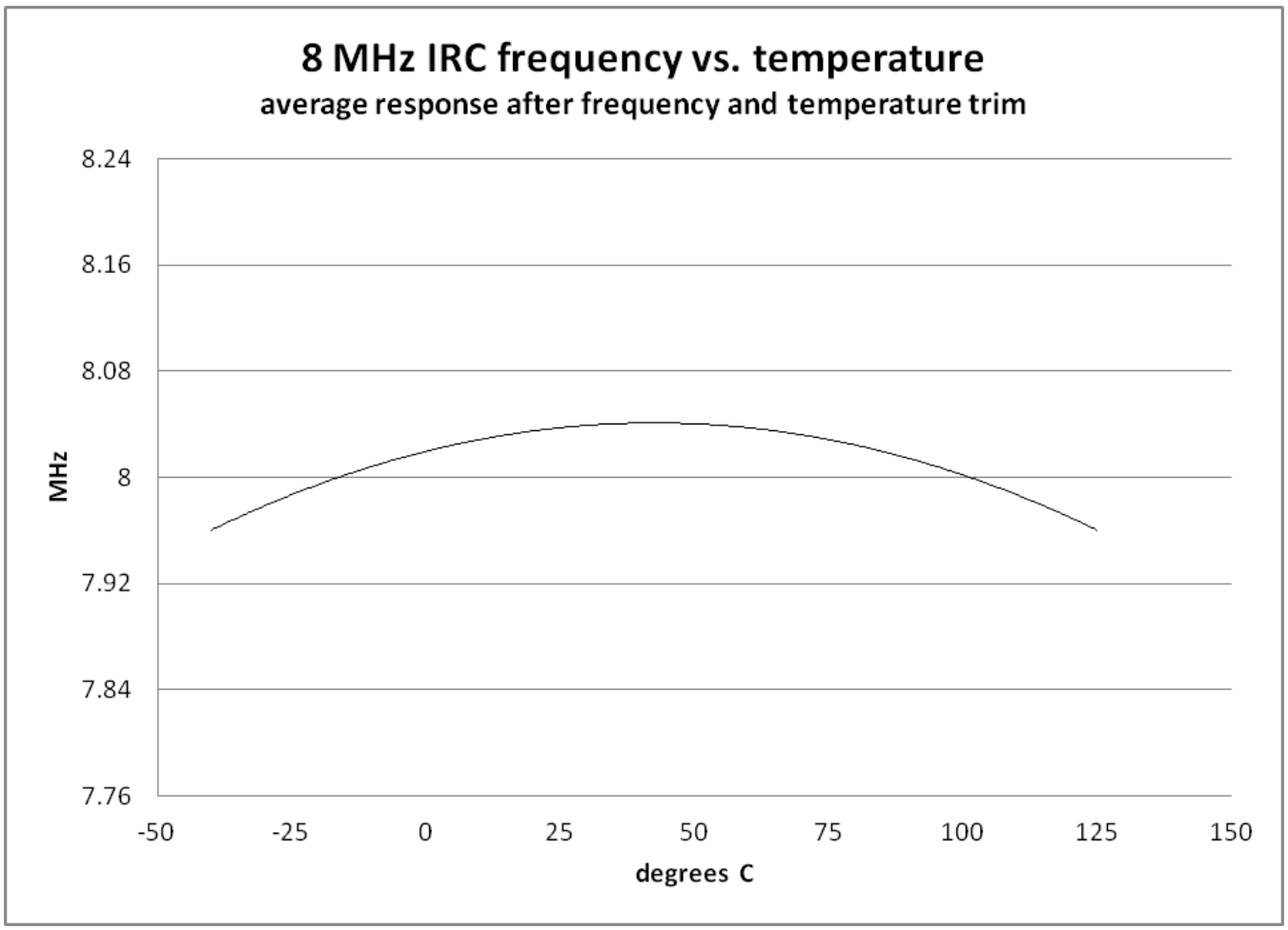


Figure 8. Relaxation Oscillator Temperature Variation (Typical) After Trim (Preliminary)

8.4 Memories and memory interfaces

8.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

8.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 21. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	

Table continues on the next page...

Table 21. NVM program/erase timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk32k}$	Erase Block high-voltage time for 32 KB	—	52	452	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.4.1.2 Flash timing specifications — commands

Table 22. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.5	ms	
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (data flash sector)	—	—	60	µs	1
$t_{rd1sec2k}$	Read 1s Section execution time (program flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1
t_{pgm4}	Program Longword execution time	—	65	145	µs	
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	55	465	ms	
$t_{ersblk256k}$	• 256 KB program flash	—	122	985	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512p}$	• 512 B program flash	—	2.4	—	ms	
$t_{pgmsec512d}$	• 512 B data flash	—	4.7	—	ms	
$t_{pgmsec1kp}$	• 1 KB program flash	—	4.7	—	ms	
$t_{pgmsec1kd}$	• 1 KB data flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	175	1500	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	

Table continues on the next page...

Table 22. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	µs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
	Byte-write to FlexRAM for EEPROM operation					
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	µs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Word-write to FlexRAM for EEPROM operation					
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	µs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b8k}$	• 8 KB EEPROM backup	—	340	1700	µs	
$t_{eewr16b16k}$	• 16 KB EEPROM backup	—	385	1800	µs	
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	475	2000	µs	
	Longword-write to FlexRAM for EEPROM operation					
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	µs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b8k}$	• 8 KB EEPROM backup	—	545	1950	µs	
$t_{eewr32b16k}$	• 16 KB EEPROM backup	—	630	2050	µs	
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

8.4.1.3 Flash high voltage current behaviors

Table 23. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

8.4.1.4 Reliability specifications

Table 24. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{nvmwree8k}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

8.5 Analog

8.5.1 12-bit Cyclic Analog-to-Digital Converter (ADC) Parameters

Table 25. 12-bit ADC Electrical Specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	V_{DDA}	2.7	3.3	3.6	V
Vrefh Supply Voltage[2]	Vrefhx	3.0		V_{DDA}	V
ADC Conversion Clock[3]	f_{ADCCLK}	0.6		20	MHz
Conversion Range	R_{AD}	V_{REFL}		V_{REFH}	V

Table continues on the next page...

Table 25. 12-bit ADC Electrical Specifications (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage Range External Reference Internal Reference	V_{ADIN}	 V_{REFL} V_{SSA}		 V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time	t_{ADC}		6		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block) • at 600 kHz ADC Clock, LP mode • ≤ 8.33 MHz ADC Clock, 00 mode • ≤ 12.5 MHz ADC Clock, 01 mode • ≤ 16.67 MHz ADC Clock, 10 mode • ≤ 20 MHz ADC Clock, 11 mode	I_{ADRUN}		1 5 9 15 19		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.02		µA
V_{REFH} Current	I_{VREFH}		0.001		µA
Accuracy (DC or Absolute)					
Integral non-Linearity[4]	I_{NL}		+/- 3	+/- 5	LSB[5]
Differential non-Linearity[4]	DNL		+/- 0.6	+/- 1	LSB[5]
Monotonicity					
Offset[6] • ≤15 MHz ADC Clock Internal/External Reference • >15 MHz ADC Clock Internal/External Reference	V_{OFFSET}	 +/- 4.03 +/- 7.25	 +/- 8.86 +/- 13.70		mV
Gain Error	E_{GAIN}		0.801 to 0.809	0.798 to 0.814	
AC Specifications[7]					
Signal to Noise Ratio	SNR		59		dB
Total Harmonic Distortion	THD		64		dB
Spurious Free Dynamic Range	SFDR		65		dB
Signal to Noise plus Distortion	SINAD		59		dB
Effective Number of Bits	ENOB		9.5		bits
ADC Inputs					
Input Leakage Current	I_{IN}		0	+/-2	µA
Input Injection Current [8]	I_{INJ}			+/-3	mA
Input Capacitance Sampling Capacitor	C_{ADI}		 4.8		pF

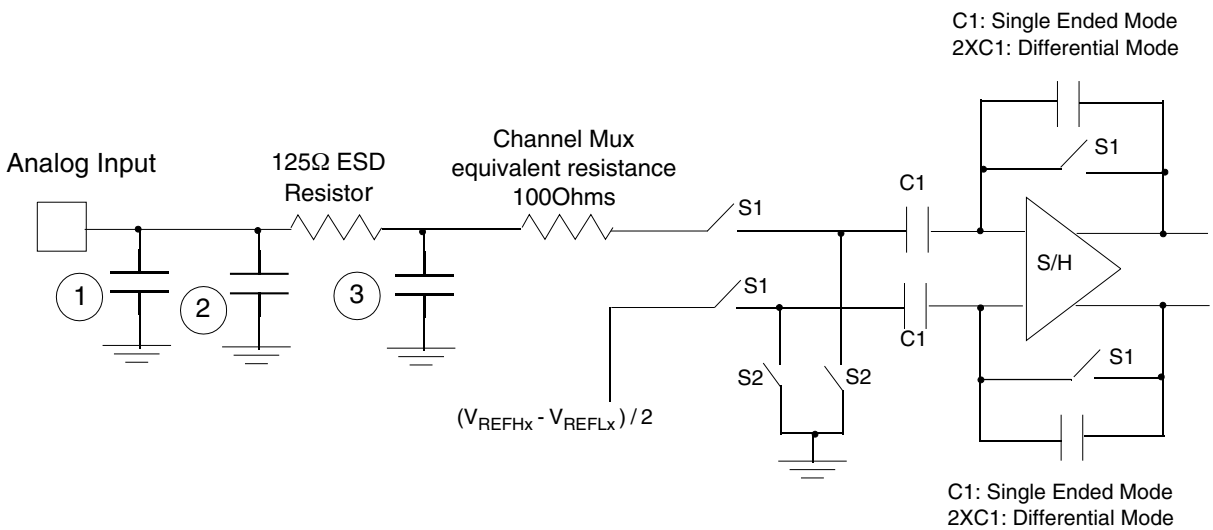
1. If the ADC's reference is from V_{DDA}: When V_{DDA} is below 3.0 V, the ADC functions but ADC specifications are not guaranteed.
2. When the input is at the V_{refl} level, the resulting output will be all zeros (hex 000), plus any error contribution due to offset and gain error. When the input is at the V_{refh} level the output will be all ones (hex FFF), minus any error contribution due to offset and gain error.
3. ADC clock duty cycle min/max is 45/55%

4. I_{NL} measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$.
5. LSB = Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 Gain Setting
6. Offset over the conversion range of 0025 to 4080
7. Measured converting a 1 kHz input Full Scale sine wave
8. The current that can be injected into or sourced from an unselected ADC input without affecting the performance of the ADC

8.5.1.1 Equivalent Circuit for ADC Inputs

The following figure illustrates the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases and operate at the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 1.4 \times 10^{-12}} + 100ohm + 125ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. 8 pF noise damping capacitor
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time of 4.8pF
5. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency

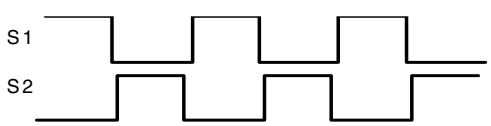


Figure 9. Equivalent Circuit for A/D Loading

8.5.2 16-bit SAR ADC electrical specifications

8.5.2.1 16-bit ADC operating conditions

Table 26. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD}-V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} - V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high	Absolute	V_{DDA}	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low	Absolute	V_{SSA}	V_{SSA}	V_{SSA}	V	4
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-/10-/12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	6
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	6
C_{rate}	ADC conversion rate	≤ 12 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	7
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	7

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. V_{REFH} is internally tied to V_{DDA}.
4. V_{REFL} is internally tied to V_{SSA}.
5. This resistance is external to MCU. The analog source resistance must be kept as low as possible to achieve the best results. The results in this data sheet were derived from a system which has < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1ns.
6. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
7. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

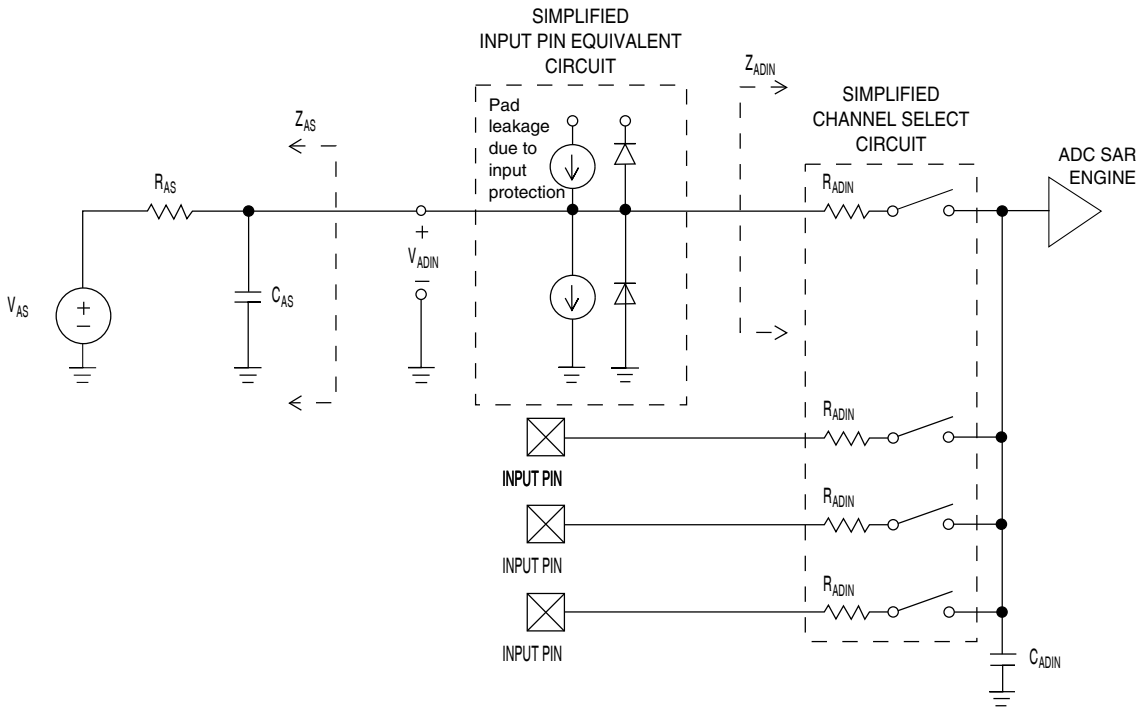


Figure 10. ADC input impedance equivalency diagram

8.5.2.2 16-bit ADC electrical characteristics

Table 27. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current			—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0 • ADLPC=1, ADHSC=1 • ADLPC=0, ADHSC=0 • ADLPC=0, ADHSC=1	1.2 3.0 2.4 4.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz MHz MHz MHz	t_{ADACK} = 1/ f_{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12 bit modes • <12 bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 16 bit modes • 12 bit modes • <12 bit modes	— — —	-1 to +4 ±0.7 ±0.2	— — -0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 16 bit modes • 12 bit modes • <12 bit modes	— — —	±7.0 ±1.0 ±0.5	— -2.7 to +1.9 -0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12 bit modes • <12 bit modes	— —	-4 -1.4	-5.4 -1.8	LSB[4]	V_{ADIN} = V_{DDA} 5

Table continues on the next page...

Table 27. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
E_Q	Quantization error	• 16 bit modes • 12 bit modes	— —	-1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16 bit single-ended mode • Avg=32 • Avg=4 12 bit single-ended mode • Avg=32 • Avg=1	 12.2 11.4 	 13.9 13.1 10.8 10.2	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16 bit single-ended mode • Avg=32 12 bit single-ended mode • Avg=32	 — —	 -85 -74	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16 bit single-ended mode • Avg=32 12 bit single-ended mode • Avg=32	 78 	 90 78	 — —	 dB dB	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the device's voltage and current operating ratings)
	Temp sensor slope	–40°C to 105°C	—	1.715	—	mV/°C	
V_{TEMP25}	Temp sensor voltage	25°C	—	722	—	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit should be set, the HSC bit should be clear with 1MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock <16MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock <12MHz.

7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.
8. System Clock = 4 MHz, ADC Clock = 2 MHz, AVG = Max, Long Sampling = Max

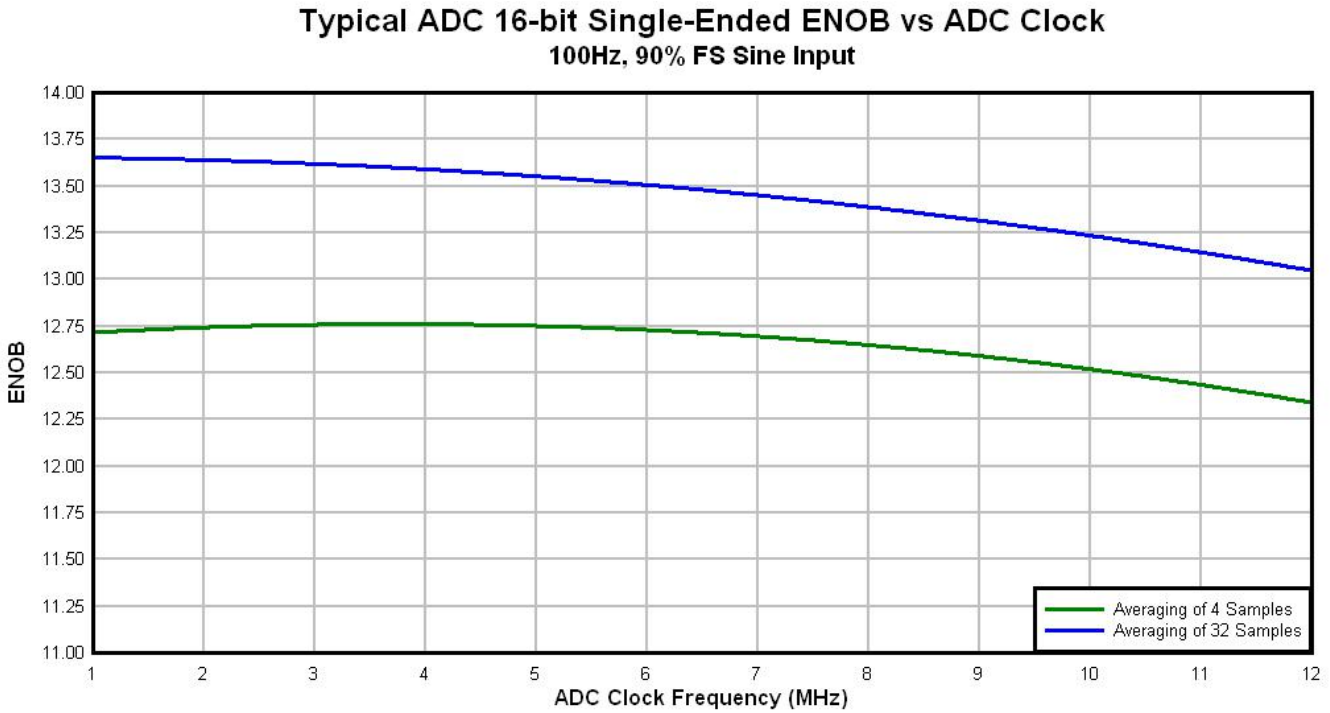


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

8.5.3 12-bit Digital-to-Analog Converter (DAC) Parameters

Table 28. DAC Parameters

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
DC Specifications						
Resolution			12	12	12	bits
Settling time[1]	At output load RLD = 3 kΩ CLD = 400 pf		—	1		µs
Power-up time	Time from release of PWRDWN signal until DACOUT signal is valid	t_{DAPU}	—	—	11	µs
Accuracy						
Integral non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	INL	—	+/- 3	+/- 4	LSB[3]
Differential non-linearity[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	DNL	—	+/- 0.8	+/- 0.9	LSB[3]

Table continues on the next page...

Table 28. DAC Parameters (continued)

Parameter	Conditions/Comments	Symbol	Min	Typ	Max	Unit
Monotonicity	> 6 sigma monotonicity, < 3.4 ppm non-monotonicity			guaranteed		—
Offset error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	V_{OFFSET}	—	+ 25	+ 35	mV
Gain error[2]	Range of input digital words: 410 to 3891 ($19A - $F33) 5% to 95% of full range	E_{GAIN}	—	+/- 0.5	+/- 1.5	%
DAC Output						
Output voltage range	Within 40 mV of either V_{SSA} or V_{DDA}	V_{OUT}	V_{SSA} + 0.04 V	—	V_{DDA} - 0.04 V	V
AC Specifications						
Signal-to-noise ratio		SNR	—	85	—	dB
Spurious free dynamic range		SFDR	—	-72	—	dB
Effective number of bits		ENOB	—	11	—	bits

1. Settling time is swing range from V_{SSA} to V_{DDA}
2. No guaranteed specification within 5% of V_{DDA} or V_{SSA}
3. LSB = 0.806mV

8.5.4 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	2.7	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	13	mV
	• CR0[HYSTCTR] = 01	—	10	48	mV
	• CR0[HYSTCTR] = 10	—	20	105	mV
	• CR0[HYSTCTR] = 11	—	30	148	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)[2]		50		ns

Table continues on the next page...

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)		250		ns
	Analog comparator initialization delay[3]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
	6-bit DAC reference inputs, Vin1 and Vin2 There are two reference input options selectable (via VRSEL control bit). The reference options must fall within this range.	V_{DDA}	—	V_{DD}	V
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[4]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Signal swing is 100 mV
3. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
4. 1 LSB = $V_{reference}$/64

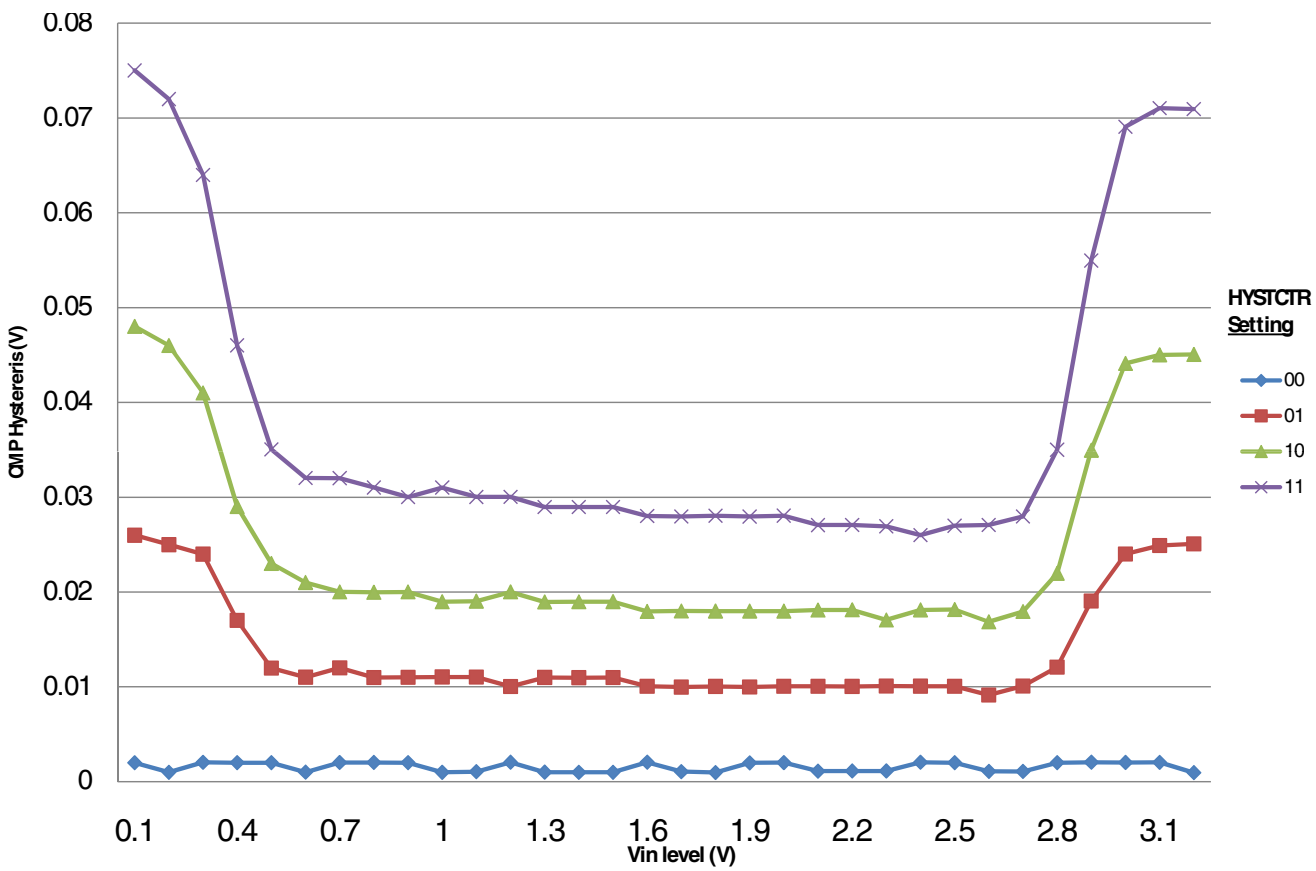


Figure 12. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

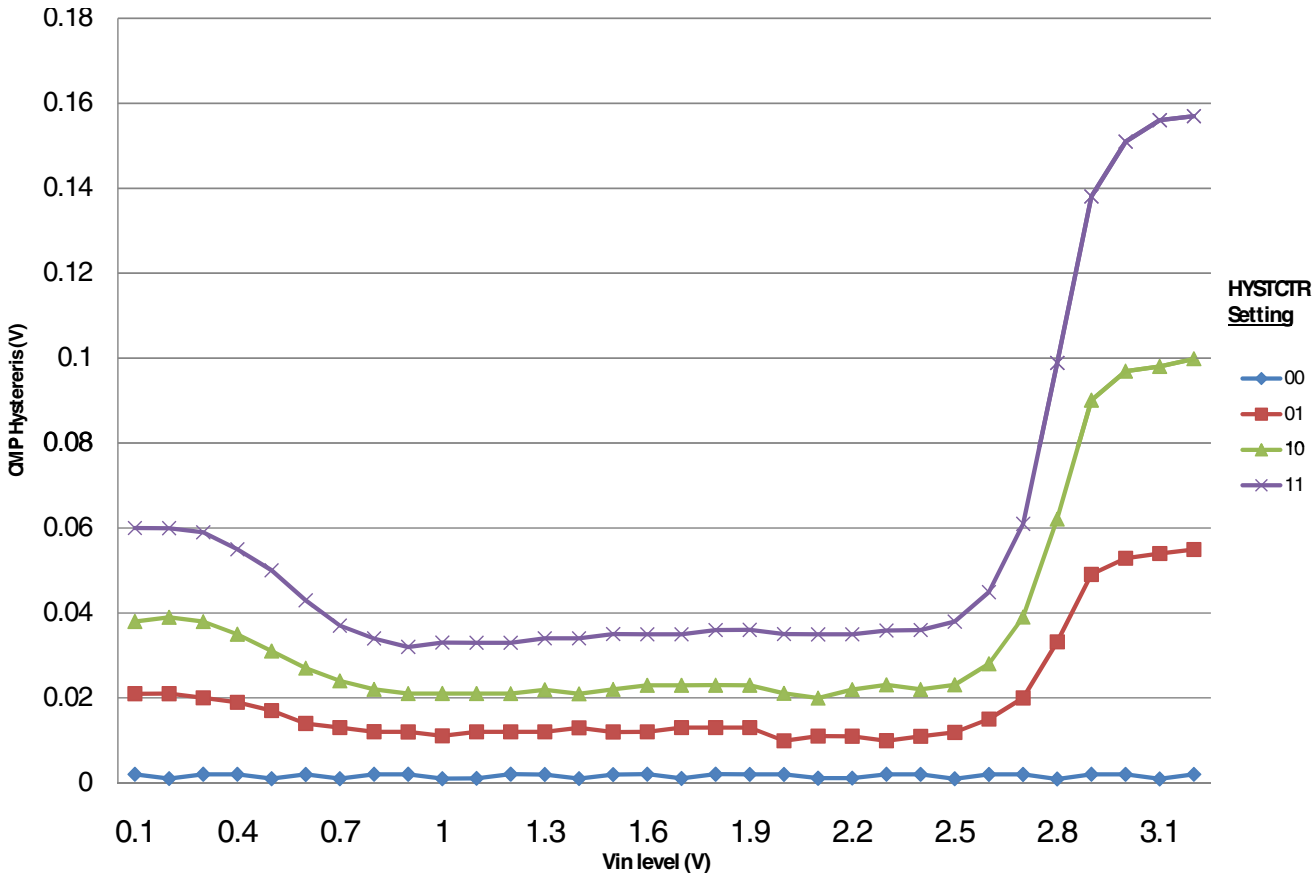


Figure 13. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

8.6 PWMs and timers

8.6.1 Enhanced NanoEdge PWM Characteristics

Table 30. NanoEdge PWM Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
PWM clock frequency		80	100	100	MHz
NanoEdge Placement (NEP) Step Size[1, 2]	pwmp	307	312	317	ps
Delay for fault input activating to PWM output deactivated	—	1	—		ns
Power-up Time[3]	t_{pu}		25		µs

1. Reference IPbus clock of 100 MHz in NanoEdge Placement mode.
2. Temperature and voltage variations do not affect NanoEdge Placement step size.
3. Powerdown to NanoEdge mode transition.

8.6.2 Quad Timer Timing

Parameters listed are guaranteed by design.

Table 31. Timer Timing

Characteristic	Symbol	Min[1]	Max	Unit	See Figure
Timer input period	P_{IN}	2T + 6	—	ns	Figure 14
Timer input high/low period	P_{INHL}	1T + 3	—	ns	Figure 14
Timer output period	P_{OUT}	20	—	ns	Figure 14
Timer output high/low period	P_{OUTHL}	10	—	ns	Figure 14

1. T = clock cycle. For 100 MHz operation, T = 10 ns.

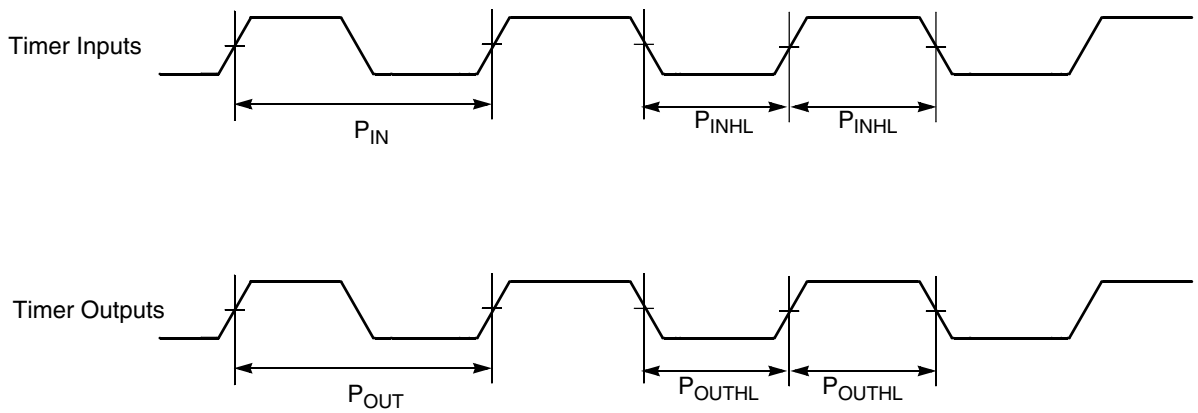


Figure 14. Timer Timing

8.7 Communication interfaces

8.7.1 Queued Serial Peripheral Interface (SPI) Timing

Parameters listed are guaranteed by design.

Table 32. SPI Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time	t_C				Figure 15
Master		35	—	ns	Figure 16
Slave		35	—	ns	Figure 17
					Figure 18

Table continues on the next page...

Table 32. SPI Timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Enable lead time	t_{ELD}				Figure 18
Master		—	—	ns	
Slave		17.5	—	ns	
Enable lag time	t_{ELG}				Figure 18
Master		—	—	ns	
Slave		17.5	—	ns	
Clock (SCK) high time	t_{CH}				Figure 15
Master		16.6	—	ns	Figure 16
Slave		16.6	—	ns	Figure 17
					Figure 18
Clock (SCK) low time	t_{CL}				Figure 18
Master		16.6	—	ns	
Slave		16.6	—	ns	
Data set-up time required for inputs	t_{DS}				Figure 15
Master		16.5	—	ns	Figure 16
Slave		1	—	ns	Figure 17
					Figure 18
Data hold time required for inputs	t_{DH}				Figure 15
Master		1	—	ns	Figure 16
Slave		3	—	ns	Figure 17
					Figure 18
Access time (time to data active from high-impedance state)	t_A				Figure 18
Slave		5	—	ns	
Disable time (hold time to high-impedance state)	t_D				Figure 18
Slave		5	—	ns	
Data valid for outputs	t_{DV}				Figure 15
Master		—	5	ns	Figure 16
Slave (after enable edge)		—	15	ns	Figure 17
					Figure 18
Data invalid	t_{DI}				Figure 15
Master		0	—	ns	Figure 16
Slave		0	—	ns	Figure 17
					Figure 18

Table continues on the next page...

Table 32. SPI Timing (continued)

Characteristic	Symbol	Min	Max	Unit	See Figure
Rise time	t_R				Figure 15
Master		—	1	ns	Figure 16
Slave		—	1	ns	Figure 17
					Figure 18
Fall time	t_F				Figure 15
Master		—	1	ns	Figure 16
Slave		—	1	ns	Figure 17
					Figure 18

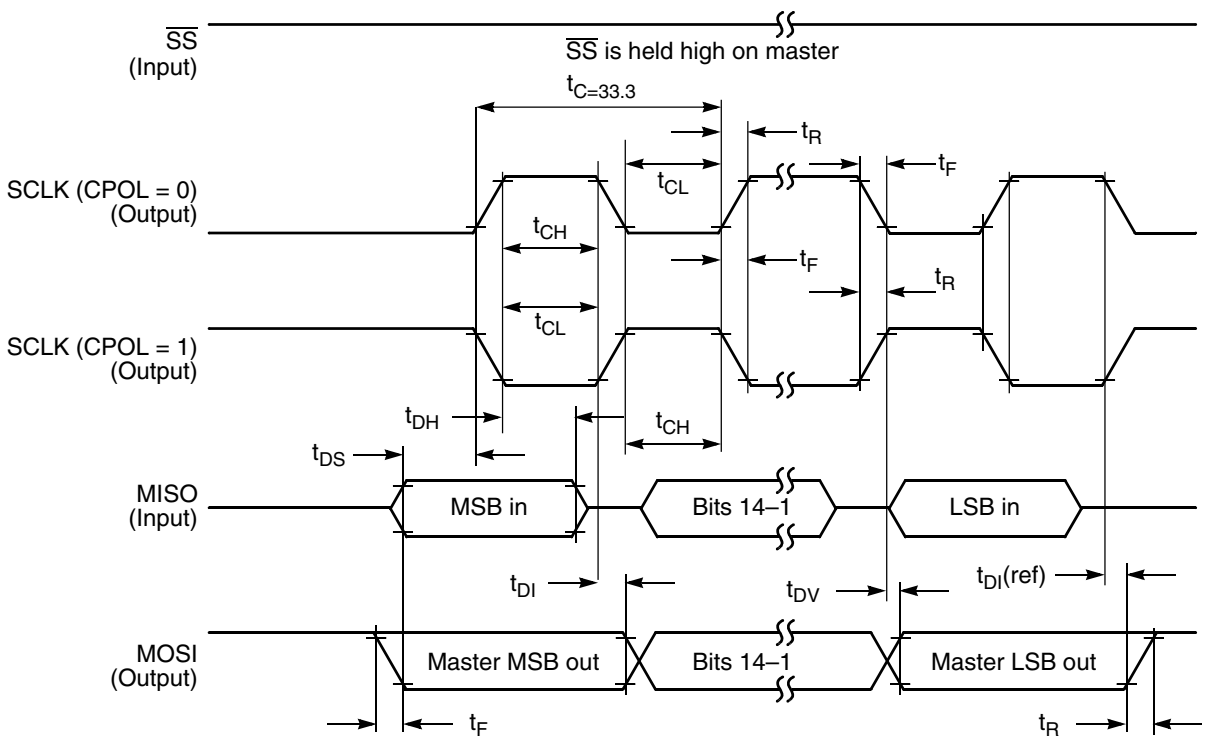


Figure 15. SPI Master Timing (CPHA = 0)

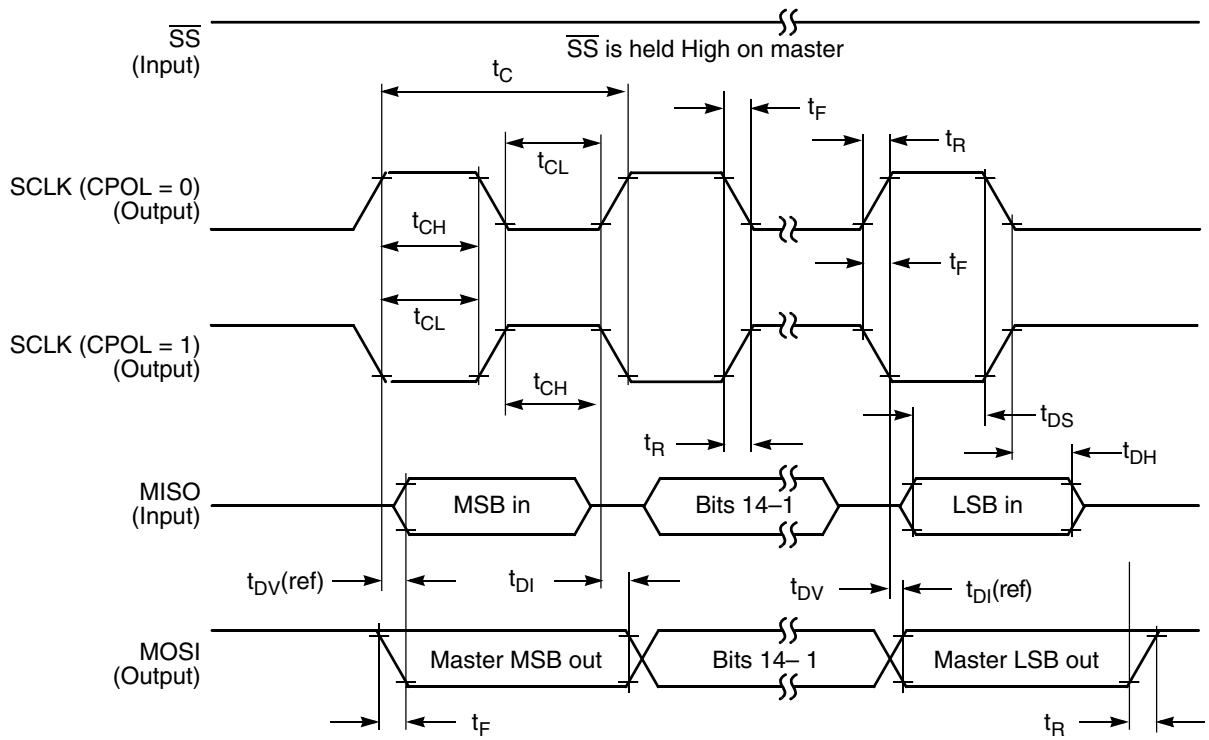


Figure 16. SPI Master Timing (CPHA = 1)

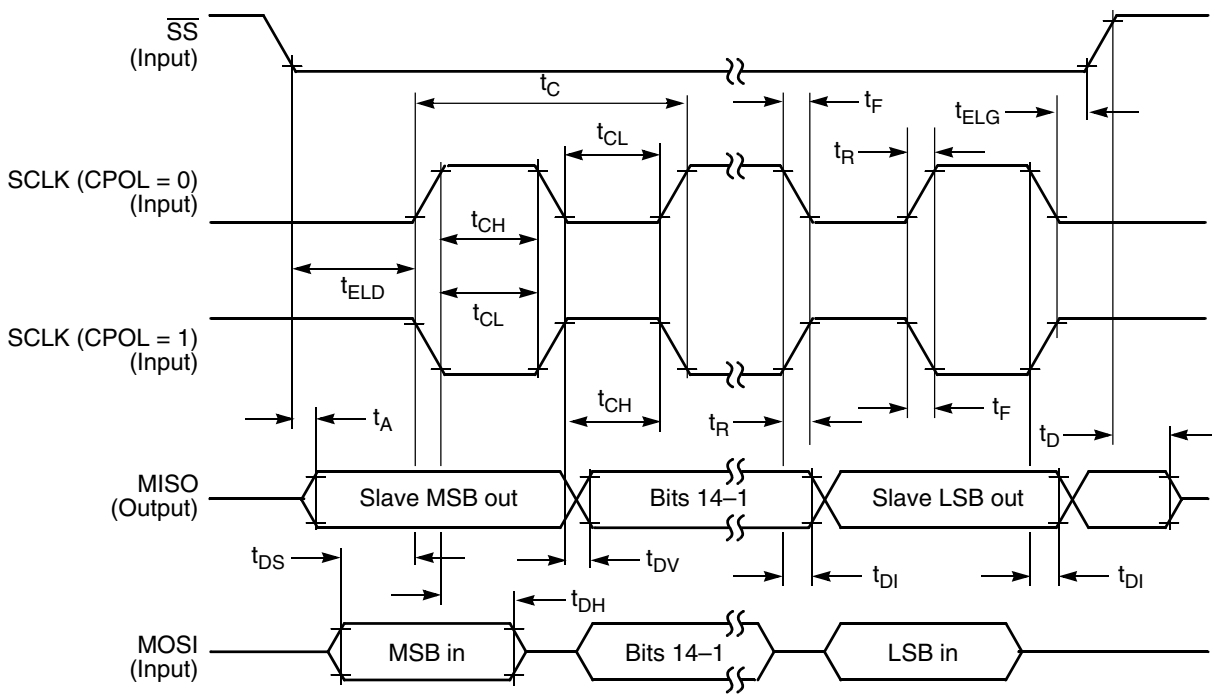


Figure 17. SPI Slave Timing (CPHA = 0)

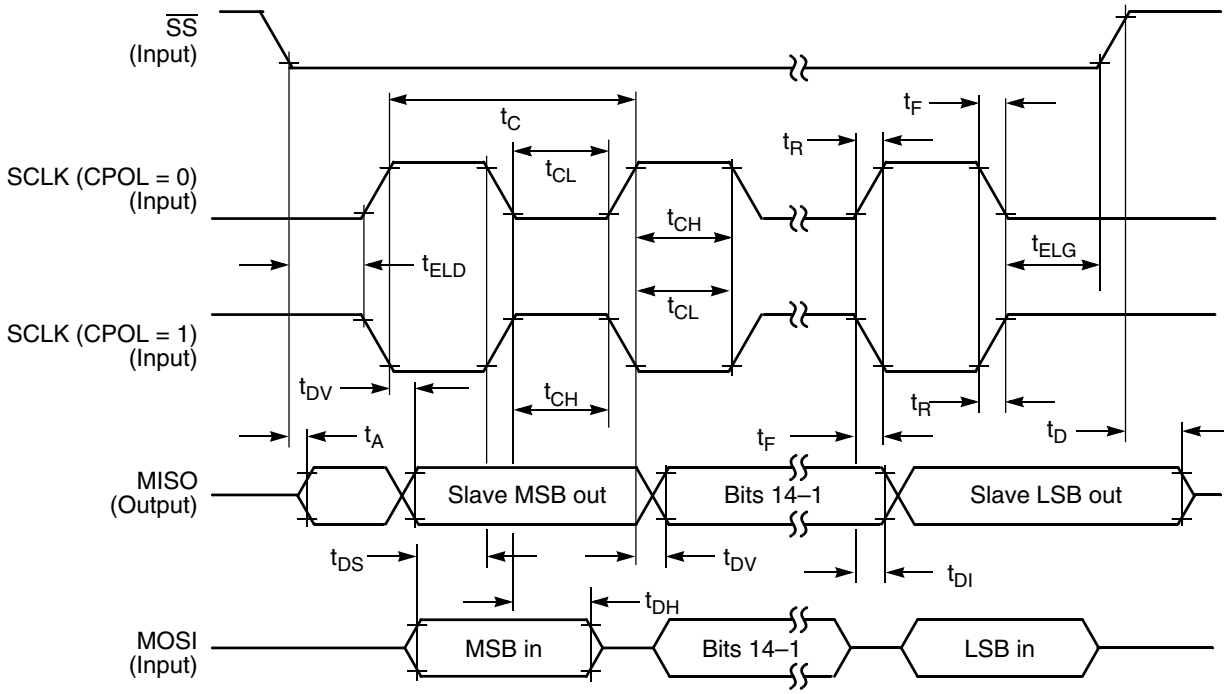


Figure 18. SPI Slave Timing (CPHA = 1)

8.7.2 Queued Serial Communication Interface (SCI) Timing

Parameters listed are guaranteed by design.

Table 33. SCI Timing

Characteristic	Symbol	Min	Max	Unit	See Figure
Baud rate[1]	BR	—	(f_{MAX}/16)	Mbps	—
RXD pulse width	RXD_{PW}	0.965/BR	1.04/BR	ns	Figure 19
TXD pulse width	TXD_{PW}	0.965/BR	1.04/BR	ns	Figure 20
LIN Slave Mode					
Deviation of slave node clock from nominal clock rate before synchronization	$F_{TOL\_UNSYNCH}$	-14	14	%	—
Deviation of slave node clock relative to the master node clock after synchronization	F_{TOL_SYNCH}	-2	2	%	—
Minimum break character length	T_{BREAK}	13	—	Master node bit periods	—
		11	—	Slave node bit periods	—

1. f_{MAX} is the frequency of operation of the SCI clock in MHz, which can be selected as the bus clock (max. 200 MHz depending on part number) or 2x bus clock (max. 200 MHz) for the devices.

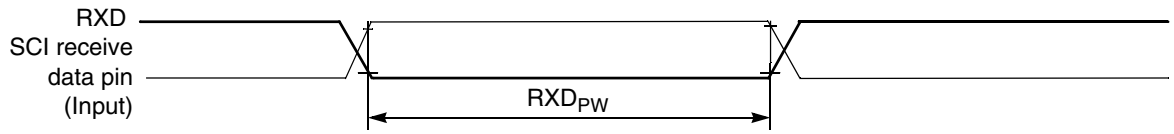


Figure 19. RXD Pulse Width

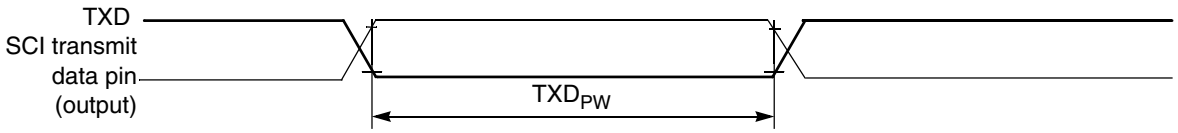


Figure 20. TXD Pulse Width

8.7.3 Freescale's Scalable Controller Area Network (FlexCAN)

Table 34. FlexCAN Timing Parameters

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
CAN Wakeup dominant pulse filtered	T_{WAKEUP}	—	2	µs
CAN Wakeup dominant pulse pass	T_{WAKEUP}	5	—	µs

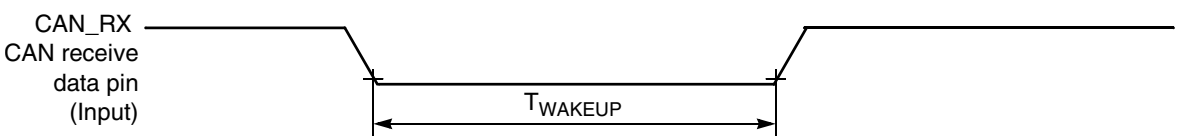


Figure 21. Bus Wake-up Detection

8.7.4 Inter-Integrated Circuit Interface (I^2C) Timing

Table 35. I^2C Timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t_{HD}; STA	4	—	0.6	—	µs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	µs
Set-up time for a repeated START condition	t_{SU}; STA	4.7	—	0.6	—	µs
Data hold time for I_2C bus devices	t_{HD}; DAT	0[1]	3.45[2]	0[3]	0.9[1]	µs
Data set-up time	t_{SU}; DAT	250[4]	—	100[2, 5]	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	20 +0.1C_b[6]	300	ns

Table continues on the next page...

Table 35. I ^{2}C Timing (continued)

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Fall time of SDA and SCL signals	t_f	—	300	20 +0.1C_b[5]	300	ns
Set-up time for STOP condition	t_{SU}; STO	4	—	0.6	—	µs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	µs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I^{2}C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I^{2}C bus device can be used in a Standard mode I2C bus system, but the requirement $t_{SU;\ DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;\ DAT} = 1000 + 250 = 1250$ ns (according to the Standard mode I^{2}C bus specification) before the SCL line is released.
6. C_b = total capacitance of the one bus line in pF.

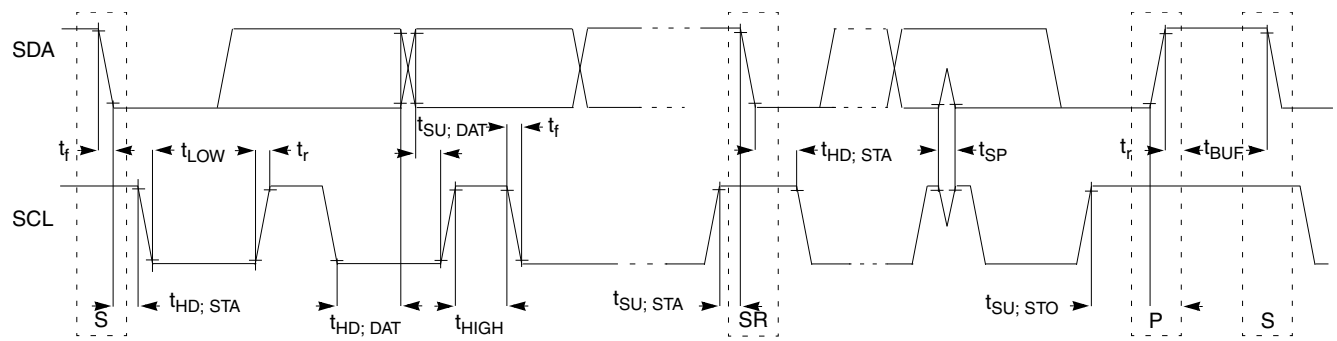


Figure 22. Timing Definition for Fast and Standard Mode Devices on the I^{2}C Bus

9 Design Considerations

9.1 Thermal Design Considerations

An estimation of the chip junction temperature, TJ, can be obtained from the equation:

$$T_J = T_A + (R_{\Theta JA} \times P_D)$$

Where,

T_A = Ambient temperature for the package (°C)

$R_{\Theta JA}$ = Junction-to-ambient thermal resistance (°C/W)

P_D = Power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single-layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low-power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$$

Where,

$R_{\Theta JA}$ = Package junction-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ = Package junction-to-case thermal resistance (°C/W)

$R_{\Theta CA}$ = Package case-to-ambient thermal resistance (°C/W)

$R_{\Theta JC}$ is device related and cannot be adjusted. You control the thermal environment to change the case to ambient thermal resistance, $R_{\Theta CA}$. For instance, you can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (YJT) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

Where,

T_T = Thermocouple temperature on top of package (°C/W)

Ψ_{JT} = hermal characterization parameter (°C/W)

P_D = Power dissipation in package (W)

The thermal characterization parameter is measured per JESD51–2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over

about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

9.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation of the device:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place 0.01–0.1µF capacitors positioned as near as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better tolerances.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are as short as possible.
- Bypass the V_{DD} and V_{SS} with approximately 100 µF, plus the number of 0.1 µF ceramic capacitors.
- PCB trace lengths should be minimal for high-frequency signals.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA}, and V_{SSA} pins.

- Using separate power planes for V_{DD} and V_{DDA} and separate ground planes for V_{SS} and VSSA are recommended. Connect the separate analog and digital power and ground planes as near as possible to power supply outputs. If an analog circuit and digital circuit are powered by the same power supply, you should connect a small inductor or ferrite bead in serial with V_{DDA} and V_{SSA} traces.
- Physically separate analog components from noisy digital components by ground planes. Do not place an analog trace in parallel with digital traces. Place an analog ground trace around an analog signal trace to isolate it from digital traces.
- Because the flash memory is programmed through the JTAG/EOnCE port, SPI, SCI, or I^2C, the designer should provide an interface to this port if in-circuit flash programming is desired.
- If desired, connect an external RC circuit to the $\overline{\text{RESET}}$ pin. The resistor value should be in the range of 4.7 kΩ–10 kΩ; the capacitor value should be in the range of 0.22 µF–4.7 µF.
- Configuring the $\overline{\text{RESET}}$ pin to GPIO output in normal operation in a high-noise environment may help to improve the performance of noise transient immunity.
- Add a 2.2 kΩ external pullup on the TMS pin of the JTAG port to keep EOnCE in a restate during normal operation if JTAG converter is not present.
- During reset and after reset but before I/O initialization, all I/O pins are at tri-state.
- To eliminate PCB trace impedance effect, each ADC input should have a no less than 33 pF 10Ω RC filter.

10 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

Drawing for package	Document number to be used
64-pin LQFP	98ASS23234W
80-pin LQFP	98ASS23174W
100-pin LQFP	98ASS23308W

11 Pinout

11.1 Signal Multiplexing and Pin Assignments

This section shows the signals available on each package pin and the locations of these pins on the devices supported by this document. The SIM's GPS registers are responsible for selecting which ALT functionality is available on most pins.

NOTE

The RESETB pin is a 3.3 V pin only.

NOTE

If the GPIOC1 pin is used as GPIO, the XOSC should be powered down.

NOTE

PWMB signals—including PWMB_2A, PWMB_2B, and PWMB_3X—are not available on the 64 LQFP package.

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
1	1	1	TCK	TCK	GPIOD2			
2	2	2	RESETB	RESETB	GPIOD4			
3	3	3	GPIOC0	GPIOC0	EXTAL	CLKIN0		
4	4	4	GPIOC1	GPIOC1	XTAL			
5	5	5	GPIOC2	GPIOC2	TXD0	TB0	XB_IN2	CLKO0
6	6	6	GPIOF8	GPIOF8	RXD0	TB1	CMPD_O	
7	—	—	VDD	VDD				
8	—	—	VSS	VSS				
9	7	—	GPIOD6	GPIOD6	TXD2	XB_IN4	XB_OUT8	
10	8	—	GPIOD5	GPIOD5	RXD2	XB_IN5	XB_OUT9	
11	9	7	GPIOC3	GPIOC3	TA0	CMPA_O	RXD0	CLKIN1
12	10	8	GPIOC4	GPIOC4	TA1	CMPB_O	XB_IN8	EWM_OUT_B
13	—	—	GPIOA10	GPIOA10	ANC18&CMPD_IN3			
14	—	—	GPIOA9	GPIOA9	ANC17&CMPD_IN2			
15	11	—	VSS	VSS				
16	12	—	VCAP	VCAP				
17	13	9	GPIOA7	GPIOA7	ANA7&ANC11			
18	—	—	GPIOA8	GPIOA8	ANC16&CMPD_IN1			
19	14	10	GPIOA6	GPIOA6	ANA6&ANC10			
20	15	11	GPIOA5	GPIOA5	ANA5&ANC9			
21	16	12	GPIOA4	GPIOA4	ANA4&ANC8&CMPD_IN0			
22	17	13	GPIOA0	GPIOA0	ANA0&CMPA_IN3	CMPC_O		
23	18	14	GPIOA1	GPIOA1	ANA1&CMPA_IN0			
24	19	15	GPIOA2	GPIOA2	ANA2&VREFHA&CMPA_IN1			

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
25	20	16	GPIOA3	GPIOA3	ANA3&VREFLA&CMPA_IN2			
26	21	17	GPIOB7	GPIOB7	ANB7&ANC15&CMPB_IN2			
27	22	18	GPIOC5	GPIOC5	DACO	XB_IN7		
28	23	19	GPIOB6	GPIOB6	ANB6&ANC14&CMPB_IN1			
29	24	20	GPIOB5	GPIOB5	ANB5&ANC13&CMPC_IN2			
30	25	21	GPIOB4	GPIOB4	ANB4&ANC12&CMPC_IN1			
31	26	22	VDDA	VDDA				
32	27	23	VSSA	VSSA				
33	28	24	GPIOB0	GPIOB0	ANB0&CMPB_IN3			
34	29	25	GPIOB1	GPIOB1	ANB1&CMPB_IN0			
35	30	26	VCAP	VCAP				
36	31	27	GPIOB2	GPIOB2	ANB2&VREFHB&CMPC_IN3			
37	32	—	GPIOA11	GPIOA11	ANC19&VREFHC			
38	33	—	GPIOB8	GPIOB8	ANC20&VREFLC			
39	—	—	GPIOB9	GPIOB9	ANC21	XB_IN9	MISO2	
40	—	—	GPIOB10	GPIOB10	ANC22	XB_IN8	MOSI2	
41	—	—	GPIOB11	GPIOB11	ANC23	XB_IN7	SCLK2	
42	34	28	GPIOB3	GPIOB3	ANB3&VREFLB&CMPC_IN0			
43	35	29	VDD	VDD				
44	36	30	VSS	VSS				
45	—	—	GPIOF11	GPIOF11	TXD0	XB_IN11		
46	—	—	GPIOF15	GPIOF15	RXD0	XB_IN10		
47	37	—	GPIOD7	GPIOD7	XB_OUT11	XB_IN7	MISO1	
48	38	—	GPIOG11	GPIOG11	TB3	CLKO0	MOSI1	
49	39	31	GPIOC6	GPIOC6	TA2	XB_IN3	CMP_REF	
50	40	32	GPIOC7	GPIOC7	SS0_B	TXD0		
51	—	—	GPIOG10	GPIOG10	PWMB_2X	PWMA_2X	XB_IN8	SS2_B
52	41	33	GPIOC8	GPIOC8	MISO0	RXD0	XB_IN9	
53	42	34	GPIOC9	GPIOC9	SCLK0	XB_IN4		
54	43	35	GPIOC10	GPIOC10	MOSI0	XB_IN5	MISO0	
55	44	36	GPIOF0	GPIOF0	XB_IN6	TB2	SCLK1	
56	45	—	GPIOF10	GPIOF10	TXD2	PWMA_FAULT6	PWMB_FAULT6	XB_OUT10
57	46	—	GPIOF9	GPIOF9	RXD2	PWMA_FAULT7	PWMB_FAULT7	XB_OUT11
58	47	37	GPIOC11	GPIOC11	CANTX	SCL1	TXD1	
59	48	38	GPIOC12	GPIOC12	CANRX	SDA1	RXD1	
60	49	39	GPIOF2	GPIOF2	SCL1	XB_OUT6		
61	50	40	GPIOF3	GPIOF3	SDA1	XB_OUT7		
62	51	41	GPIOF4	GPIOF4	TXD1	XB_OUT8		
63	52	42	GPIOF5	GPIOF5	RXD1	XB_OUT9		

100 LQFP	80 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3
64	—	—	GPIOG8	GPIOG8	PWMB_0X	PWMA_0X	TA2	XB_OUT10
65	—	—	GPIOG9	GPIOG9	PWMB_1X	PWMA_1X	TA3	XB_OUT11
66	53	43	VSS	VSS				
67	54	44	VDD	VDD				
68	55	45	GPIOE0	GPIOE0	PWMA_0B			
69	56	46	GPIOE1	GPIOE1	PWMA_0A			
70	57	—	GPIOG2	GPIOG2	PWMB_0B	XB_OUT4		
71	58	—	GPIOG3	GPIOG3	PWMB_0A	XB_OUT5		
72	—	—	GPIOE8	GPIOE8	PWMB_2B	PWMA_FAULT0		
73	—	—	GPIOE9	GPIOE9	PWMB_2A	PWMA_FAULT1		
74	59	47	GPIOE2	GPIOE2	PWMA_1B			
75	60	48	GPIOE3	GPIOE3	PWMA_1A			
76	61	49	GPIOC13	GPIOC13	TA3	XB_IN6	EWM_OUT_B	
77	62	50	GPIOF1	GPIOF1	CLKO1	XB_IN7	CMPD_O	
78	63	—	GPIOG0	GPIOG0	PWMB_1B	XB_OUT6		
79	64	—	GPIOG1	GPIOG1	PWMB_1A	XB_OUT7		
80	—	—	GPIOG4	GPIOG4	PWMB_3B	PWMA_FAULT2		
81	—	—	GPIOG5	GPIOG5	PWMB_3A	PWMA_FAULT3		
82	65	51	GPIOE4	GPIOE4	PWMA_2B	XB_IN2		
83	66	52	GPIOE5	GPIOE5	PWMA_2A	XB_IN3		
84	67	53	GPIOE6	GPIOE6	PWMA_3B	XB_IN4	PWMB_2B	
85	68	54	GPIOE7	GPIOE7	PWMA_3A	XB_IN5	PWMB_2A	
86	69	—	GPIOG6	GPIOG6	PWMA_FAULT4	PWMB_FAULT4	TB2	XB_OUT8
87	70	55	GPIOC14	GPIOC14	SDA0	XB_OUT4		
88	71	56	GPIOC15	GPIOC15	SCL0	XB_OUT5		
89	—	—	GPIOF12	GPIOF12	MISO1	PWMB_FAULT2		
90	—	—	GPIOF13	GPIOF13	MOSI1	PWMB_FAULT1		
91	—	—	GPIOF14	GPIOF14	SCLK1	PWMB_FAULT0		
92	72	—	GPIOG7	GPIOG7	PWMA_FAULT5	PWMB_FAULT5	XB_OUT9	
93	73	57	VCAP	VCAP				
94	74	58	GPIOF6	GPIOF6	TB2	PWMA_3X	PWMB_3X	XB_IN2
95	75	59	GPIOF7	GPIOF7	TB3	CMPC_O	SS1_B	XB_IN3
96	76	60	VDD	VDD				
97	77	61	VSS	VSS				
98	78	62	TDO	TDO	GPIOD1			
99	79	63	TMS	TMS	GPIOD3			
100	80	64	TDI	TDI	GPIOD0			

11.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

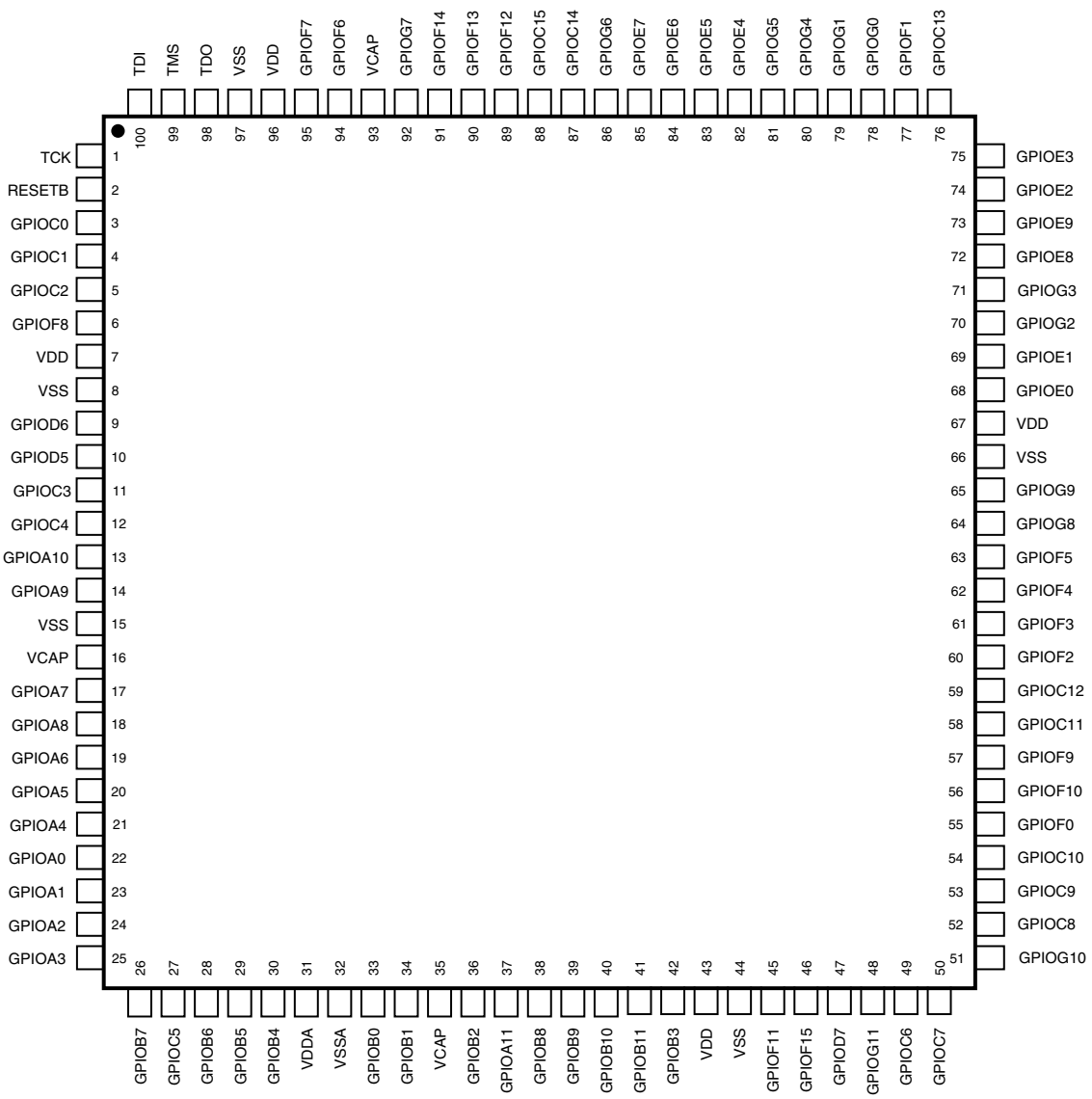


Figure 23. 100-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

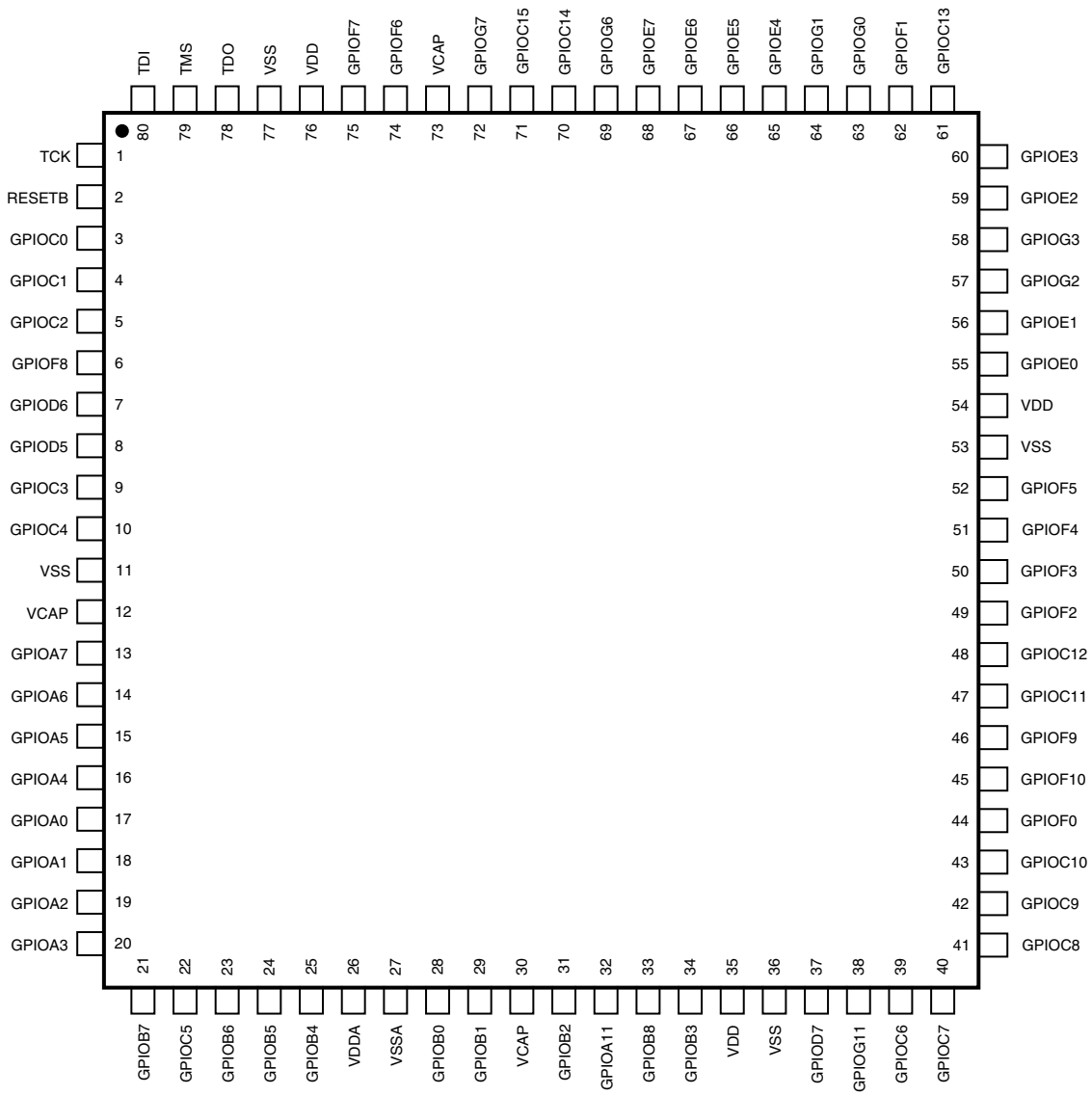


Figure 24. 80-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

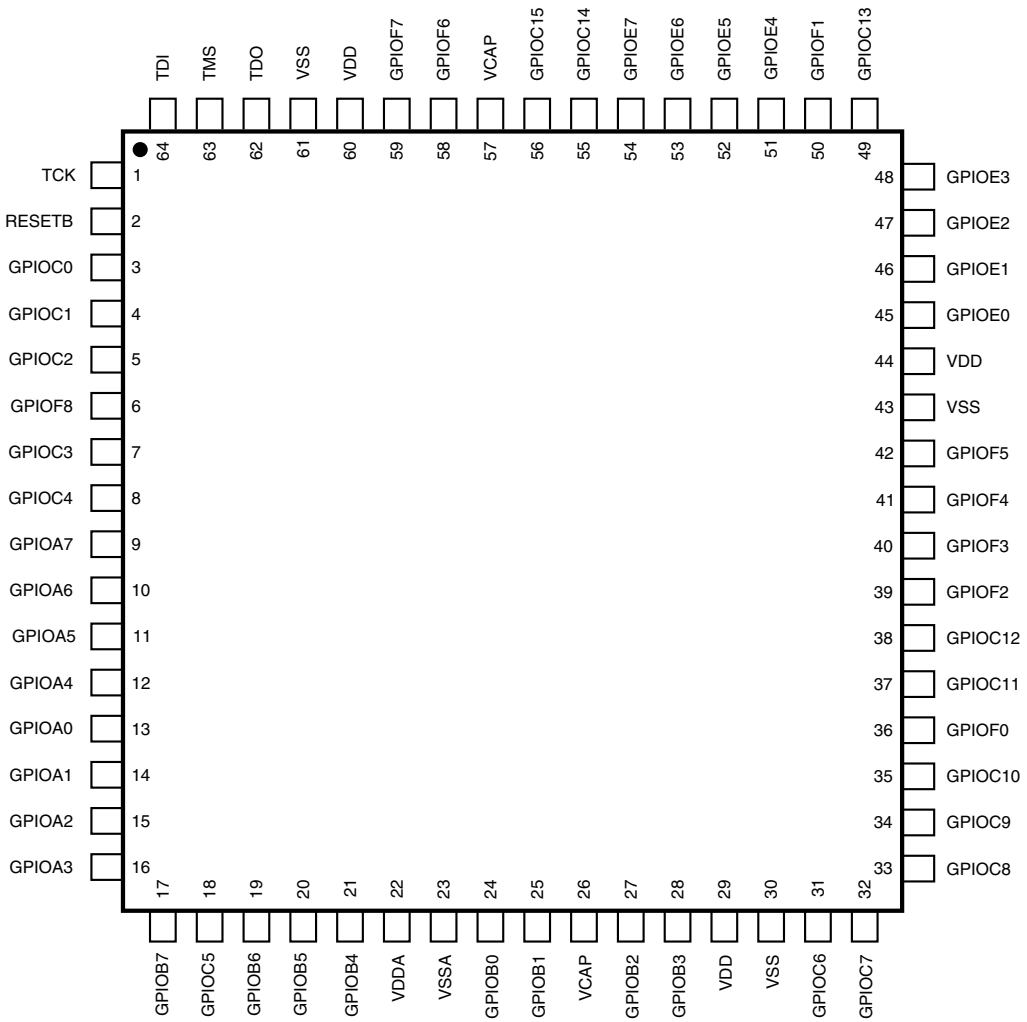


Figure 25. 64-pin LQFP

NOTE

The RESETB pin is a 3.3 V pin only.

12 Product Documentation

The documents listed in Table 36 are required for a complete description and proper design with the device. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, or online at http://www.freescale.com.

Table 36. Device Documentation

Topic	Description	Document Number
DSP56800E/DSP56800EX Reference Manual	Detailed description of the 56800EX family architecture, 32-bit digital signal controller core processor, and the instruction set	DSP56800ERM
MC56F847xx Reference Manual	Detailed functional description and programming model	MC56F847XXRM
Serial Bootloader User Guide	Detailed description of the Serial Bootloader in the DSC family of devices	
MC56F847xx Data Sheet	Electrical and timing specifications, pin descriptions, and package information (this document)	MC56F847XX
MC56F84xxx Errata	Details any chip issues that might be present	MC56F84XXX_0N27E

13 Revision History

The following table summarizes changes to this document since the release of the previous version.

Table 37. Revision History

Rev.	Date	Substantial Changes
3	08/2012	In various locations: Clarified that the RESETB pin is a 3.3 V pin only
		MC56F844x/5x/7x Product Family: Clarified that DAC table row applies to 12-bit DAC
		Voltage and current operating ratings: Added rows for RESET input voltage range and RESET output voltage range
		Voltage and current operating requirements: Added row for RESET voltage high, and added new final footnote
		Voltage and current operating behaviors: For Digital Input Current High, created separate sub-rows for Pin Groups 1 and 2
		Power mode transition operating behaviors: Updated row for RESET deassertion to First Address Fetch
		Power consumption operating behaviors: Replaced all TBD values, and updated Typical at 3.3 V I_{DDA} value for WAIT mode
		EMC radiated emissions operating behaviors: Removed this section
		Thermal attributes: Updated values for 100 LQFP
		JTAG Timing: Changed divider value of Max for TCK frequency of operation
		Relaxation Oscillator Timing: Replaced all TBDs, and removed Standby Mode specification for 8 MHz Frequency Variation
		Peripheral operating requirements and behaviors: Updated Flash timing specifications and added Flash high voltage current behaviors
		16-bit ADC electrical characteristics: Updated DNL information about Max value for 16-bit modes and 12-bit modes, and updated INL information about Max value for 16-bit modes
		Signal Multiplexing and Pin Assignments: Added note about GPIOC1, added JTAG signals to table and diagrams, and changed "SCK" signal names to "SCLK"

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Document Number: MC56F847XX
Rev. 3, 08/2012

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