

System Lens Driver for Digital Still Cameras / Single-lens Reflex Cameras



5ch System Lens Drivers for Digital Still Cameras

BD6370GUL, BD6758MWV, BD6758KN

No.09014EAT01

●Description

The BD6370GUL motor driver provides 3 Constant-Voltage Drive / Full-ON Drive H-bridge channels, 1 Constant-Voltage Drive / Linear Constant-Current Drive / Full-ON Drive H-bridge channel, and 1 Constant-Current Drive H-bridge channel, while the BD6758MWV and the BD6758KN provides 4 Full-ON Drive H-bridge channels and 1 Linear Constant-Current Drive H-bridge channel.

A Stepping motor can be used for auto focus and a DC motor for zoom and iris. ROHM offers both an advance type equipped with a D/A converter in all channels and a standard type, allowing selection of the ideal unit depending on the application.

●Features

- 1) Subminiature 24PIN Wafer-level CSP (Chip Size Package): 2.6 x 2.6 x 0.55mm³ (BD6370GUL)
- 2) Resemblance 6ch drive function (BD6370GUL)
- 3) Drive type selection (BD6370GUL)
- 4) Low ON-Resistance Power CMOS output:
All blocks (Const.-V/Full-ON Drive, Const.-V/Const.-C/Full-ON Drive, and Const.-Current Drive) with 1.4Ω Typ. (BD6370GUL)
Full-ON Drive block with 1.2Ω Typ. and Linear Constant-Current Drive block with 1.0Ω Typ. (BD6758MWV / KN)
- 5) Serial interface 3-line bus control input (BD6370GUL)
- 6) Built-in Constant-Voltage control 6-bit D/A converter and Constant-Current control 6-bit D/A converter resolution (BD6370GUL)
- 7) Built-in ±5% high-precision Constant-Voltage Driver (BD6370GUL)
- 8) Built-in ±3% high-precision Linear Constant-Current Driver
- 9) Constant-Voltage Drive block and Constant-Current Drive block features phase compensation capacitor-free design
- 10) 1.2V±3% high-precision reference voltage output (BD6758MWV / KN)
- 11) Drive mode switching function (BD6758MWV / KN)
- 12) UVLO (Under Voltage Lockout Protection) function
- 13) Built-in TSD (Thermal Shut Down) circuit
- 14) Standby current consumption: 0μA Typ.

●Absolute Maximum Ratings

| Parameter | Symbol | Limit | | | Unit |
|-----------------------------|--------|----------------------------|----------------------------|----------------------------|-------|
| | | BD6370GUL | BD6758MWV | BD6758KN | |
| Power supply voltage | VCC | -0.3 to +6.5 | 0 to +7.0 | 0 to +7.0 | V |
| Motor power supply voltage | VM | -0.3 to +6.5 | 0 to +7.0 | 0 to +7.0 | V |
| Control input voltage | VIN | -0.3 to VCC+0.3 | 0 to VCC | 0 to VCC | V |
| Power dissipation | Pd | 830 ^{※1} | 880 ^{※2} | 875 ^{※3} | mW |
| Operating temperature range | Topr | -25 to +85 | -25 to +85 | -25 to +85 | °C |
| Junction temperature | Tjmax | +150 | +150 | +150 | °C |
| Storage temperature range | Tstg | -55 to +150 | -55 to +150 | -55 to +150 | °C |
| H-bridge output current | Iout | -500 to +500 ^{※4} | -800 to +800 ^{※4} | -800 to +800 ^{※4} | mA/ch |

※1 Reduced by 6.64mW/°C over 25°C, when mounted on a glass epoxy board (50mm × 58mm × 1.75mm; 8layers).

※2 Reduced by 7.0mW/°C over 25°C, when mounted on a glass epoxy board (74.2mm × 74.2mm × 1.6mm).

※3 Reduced by 7.0mW/°C over 25°C, when mounted on a glass epoxy board (70mm × 70mm × 1.6mm).

※4 Must not exceed Pd, ASO, or Tjmax of 150°C.

● Operating Conditions (Ta=-25 to +85°C)

| Parameter | Symbol | Limit | | | Unit |
|------------------------------|--------|----------------------------|----------------------------|----------------------------|-------|
| | | BD6370GUL | BD6758MWV | BD6758KN | |
| Power supply voltage | VCC | 2.7 to 5.5 | 2.5 to 5.5 | 2.5 to 5.5 | V |
| Motor power supply voltage | VM | 2.7 to 5.5 | 2.5 to 5.5 | 2.5 to 5.5 | V |
| Control input voltage | VIN | 0 to VCC | 0 to VCC | 0 to VCC | V |
| Control input frequency | FIN | 100 ^{※5} | 100 ^{※5} | 100 ^{※5} | kHz |
| Serial clock input frequency | FSCLK | 10 ^{※5} | - | - | MHz |
| H-bridge output current | Iout | -400 to +400 ^{※6} | -500 to +500 ^{※6} | -500 to +500 ^{※6} | mA/ch |

※5 ON duty=50%

※6 Must not exceed Pd or ASO.

● Electrical Characteristics and Diagrams

1) BD6370GUL Electrical DC Characteristics (Unless otherwise specified, Ta=25°C, VCC=3.0V, VM=5.0V)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|---|--------|-------|-------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Overall | | | | | | |
| Circuit current (Standby mode) | ICCST | - | 0 | 3.0 | μA | PS=0V |
| Circuit current (Active mode) | ICC | - | 1.3 | 2.0 | mA | PS=3V with no control signal, and no load |
| Control input (IN=PS, INPUT1, 2, 34, 45, STROBE, SCLK, and SDATA) | | | | | | |
| High level input voltage | VINH | 2.0 | - | VCC | V | |
| Low level input voltage | VINL | 0 | - | 0.7 | V | |
| High level input current 1 | IINH1 | 15 | 30 | 60 | μA | VINH1 (PS, INPUT1, 2, 34, 45) =3V |
| High level input current 2 | IINH2 | 7.5 | 15 | 30 | μA | VINH2 (STROBE, SCLK, SDATA) =3V |
| Low level input current | IINL | -1 | 0 | - | μA | VINL=0V |
| UVLO | | | | | | |
| UVLO voltage | VUVLO | 1.6 | - | 2.4 | V | |
| Constant-Voltage Drive / Full-ON Drive block (ch1 to ch3) | | | | | | |
| Output ON-Resistance | RON | - | 1.40 | 1.75 | Ω | I _o =±400mA on high and low sides in total |
| Output high voltage 1 | VVOH1 | 1.35 | 1.50 | 1.65 | V | DACx=6'b01_0100, RL=20Ω |
| Output high voltage 2 | VVOH2 | 2.85 | 3.00 | 3.15 | V | DACx=6'b10_1000, RL=20Ω |
| Output high voltage 3 | VVOH3 | 4.49 | 4.725 | 4.96 | V | DACx=6'b11_1111, RL=20Ω |
| DAC resolution | DVRES | - | 6 | - | BITS | 75mV/LSB |
| Differential non-linear tolerance | DVDNL | -1 | - | 1 | LSB | |
| Integral non-linear tolerance | DVINL | -2 | - | 2 | LSB | |
| Min. voltage of DAC setting | DVRNG | 1.5 | - | - | V | DACx=6'b01_0100 |
| Constant-Voltage Drive / Constant-Current Drive / Full-ON Drive block (ch4) | | | | | | |
| Output ON-Resistance | RON | - | 1.40 | 1.75 | Ω | I _o =±400mA on high and low sides in total |
| Constant-Voltage Drive block in ch4 | | | | | | |
| Output high voltage 1 | VVOH1 | 1.35 | 1.50 | 1.65 | V | DACV4=6'b01_0100, RL=20Ω |
| Output high voltage 2 | VVOH2 | 2.85 | 3.00 | 3.15 | V | DACV4=6'b10_1000, RL=20Ω |
| Output high voltage 3 | VVOH3 | 4.49 | 4.725 | 4.96 | V | DACV4=6'b11_1111, RL=20Ω |
| DAC resolution | DVRES | - | 6 | - | BITS | 75mV/LSB |
| Differential non-linear tolerance | DVDNL | -1 | - | 1 | LSB | |
| Integral non-linear tolerance | DVINL | -2 | - | 2 | LSB | |
| Min. voltage of DAC setting | DVRNG | 1.5 | - | - | V | DACV4=6'b01_0100 |
| Constant-Current Drive block in ch4 | | | | | | |
| RNF voltage 1 | VIRNF1 | 40 | 50 | 60 | mV | DACI4=6'b00_1010, R _{RNF4} =0.5Ω, RL=10Ω |
| RNF voltage 2 | VIRNF2 | 94 | 99 | 104 | mV | DACI4=6'b01_0100, R _{RNF4} =0.5Ω, RL=10Ω |
| RNF voltage 3 | VIRNF3 | 178 | 198 | 218 | mV | DACI4=6'b10_1000, R _{RNF4} =0.5Ω, RL=10Ω |
| DAC resolution | DIRES | - | 6 | - | BITS | 5mV/LSB |
| Differential non-linear tolerance | DIDNL | -1 | - | 1 | LSB | |
| Integral non-linear tolerance | DIINL | -2 | - | 2 | LSB | |
| Min. voltage of DAC setting | DIRNG | 50 | - | - | mV | DACI4=6'b00_1010 |
| Constant-Current Drive block (ch5) | | | | | | |
| Output ON-Resistance | RON | - | 1.4 | 1.75 | Ω | I _o =±400mA on high and low sides in total |
| RNF voltage 1 | VIRNF1 | 38 | 48 | 58 | mV | DAC5=6'b00_1010, R _{RNF5} =0.5Ω, RL=10Ω |
| RNF voltage 2 | VIRNF2 | 91 | 96 | 101 | mV | DAC5=6'b01_0100, R _{RNF5} =0.5Ω, RL=10Ω |
| RNF voltage 3 | VIRNF3 | 172 | 192 | 212 | mV | DAC5=6'b10_1000, R _{RNF5} =0.5Ω, RL=10Ω |
| DAC resolution | DIRES | - | 6 | - | BITS | 5mV/LSB |
| Differential non-linear tolerance | DIDNL | -1 | - | 1 | LSB | |
| Integral non-linear tolerance | DIINL | -2 | - | 2 | LSB | |
| Min. voltage of DAC setting | DIRNG | 50 | - | - | mV | DAC5=6'b00_1010 |

2) BD6370GUL Electrical DC Characteristic Diagrams

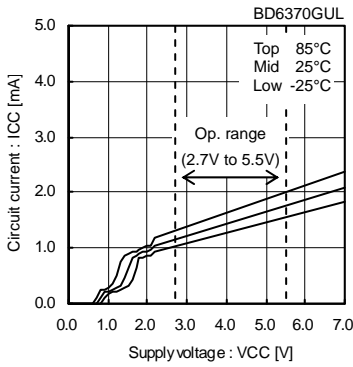


Fig.1 Circuit Current (Active mode)

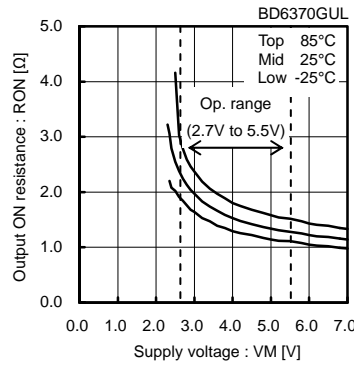


Fig.2 Output ON-Resistance (ch1 to ch3)

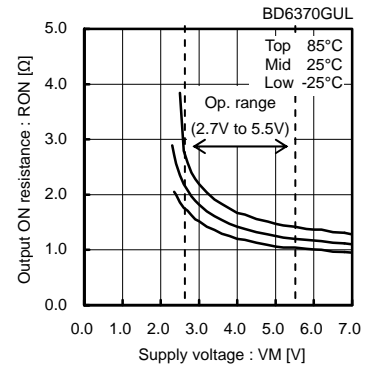


Fig.3 Output ON-Resistance (ch4 to ch5)

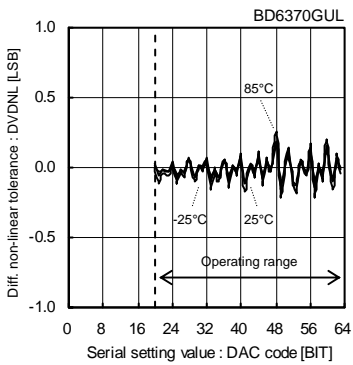


Fig.4 Differential Non-Linear Tolerance

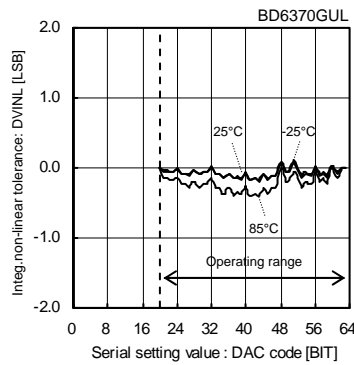


Fig.5 Integral Non-Linear Tolerance (Const.-Voltage drive block, $R_L=20\Omega$)

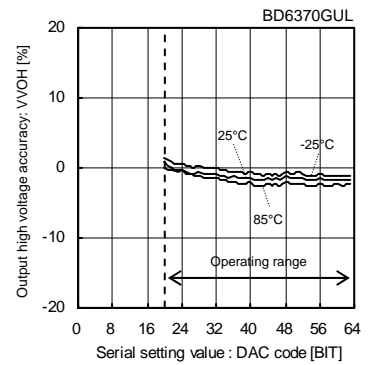


Fig.6 Output High Voltage Accuracy (Const.-Voltage drive block, $R_L=20\Omega$)

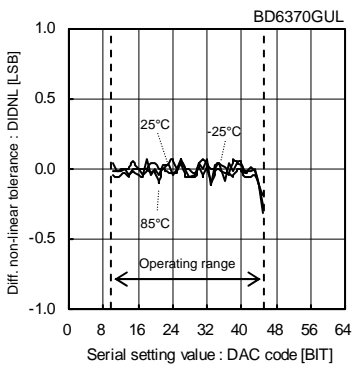


Fig.7 Differential Non-Linear Tolerance

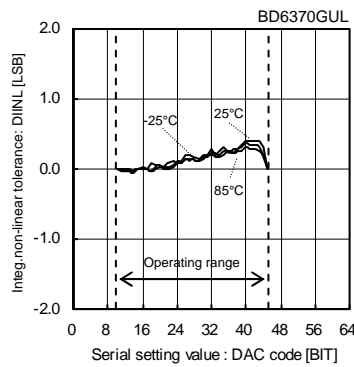


Fig.8 Integral Non-Linear Tolerance (Const.-Current drive block, $R_{RNFx}=0.5\Omega$, $R_L=10\Omega$)

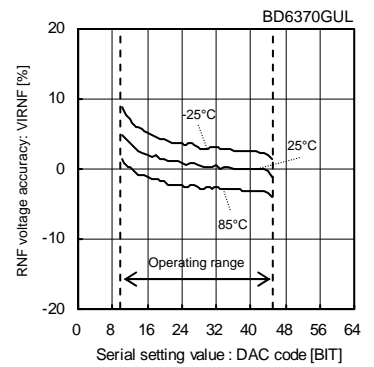


Fig.9 RNF Voltage Accuracy (Const.-Current drive block, $R_{RNFx}=0.5\Omega$, $R_L=10\Omega$)

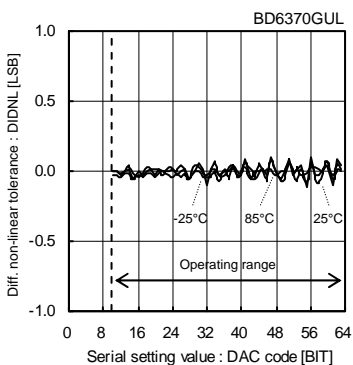


Fig.10 Differential Non-Linear Tolerance

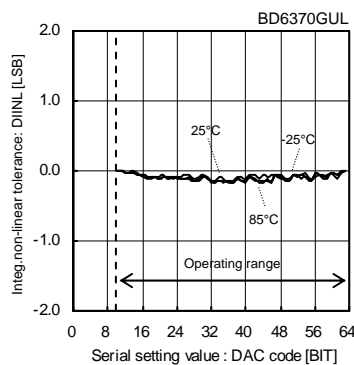


Fig.11 Integral Non-Linear Tolerance

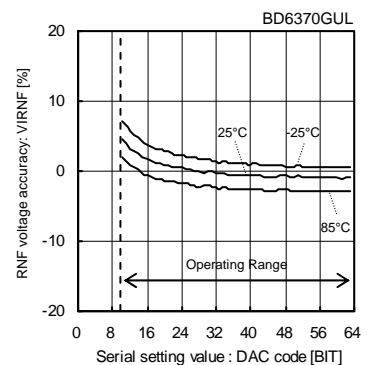


Fig.12 RNF Voltage Accuracy (Const.-Current drive block, $R_{RNFx}=1.0\Omega$, $R_L=10\Omega$)

3) BD6370GUL Electrical AC Characteristics (Unless otherwise specified, Ta=25°C, VCC=3.0V, VM=5.0V)

Constant-Voltage / Full-ON Type Drive blocks (ch1 to ch3)

| Parameter | Symbol | Information ^{※7} | | | Unit | Conditions |
|-----------------------------|--------|---------------------------|------|------|------|-------------------------|
| | | ch1 | ch2 | ch3 | | |
| Full-ON Drive Mode | | | | | | |
| Turn on time | ton | 1.11 | 1.04 | 1.10 | μs | DACx=6'b11_1111, RL=20Ω |
| Turn off time | toff | 0.06 | 0.06 | 0.06 | μs | |
| Rise time | tr | 1.64 | 1.42 | 1.50 | μs | |
| Fall time | tf | 0.01 | 0.01 | 0.01 | μs | |
| Constant-Voltage Drive Mode | | | | | | |
| Turn on time | ton | 1.26 | 1.23 | 1.22 | μs | DACx=6'b10_1000, RL=20Ω |
| Turn off time | toff | 0.04 | 0.04 | 0.04 | μs | |
| Rise time | tr | 1.31 | 1.35 | 1.30 | μs | |
| Fall time | tf | 0.02 | 0.02 | 0.02 | μs | |

Constant-Voltage / Constant-Current / Full-ON Type Drive block (ch4)

| Parameter | Symbol | Information ^{※7} | | | Unit | Conditions |
|-----------------------------|--------|---------------------------|------|---|------|--|
| | | - | ch4 | - | | |
| Full-ON Drive Mode | | | | | | |
| Turn on time | ton | - | 0.76 | - | μs | DACV4=6'b11_1111, DACI4=6'b11_1111, RL=20Ω |
| Turn off time | toff | - | 0.05 | - | μs | |
| Rise time | tr | - | 0.68 | - | μs | |
| Fall time | tf | - | 0.02 | - | μs | |
| Constant-Voltage Drive Mode | | | | | | |
| Turn on time | ton | - | 1.19 | - | μs | DACV4=6'b10_1000, DACI4=6'b11_1111, RL=20Ω |
| Turn off time | toff | - | 0.04 | - | μs | |
| Rise time | tr | - | 1.31 | - | μs | |
| Fall time | tf | - | 0.01 | - | μs | |
| Constant-Current Drive Mode | | | | | | |
| Turn on time | ton | - | 0.83 | - | μs | DACV4=6'b11_1111, DACI4=6'b10_1100 (I _O =400mA), R _{RNF4} =0.5Ω, RL=10Ω, R _{METAL4} =4mΩ, R _W =40mΩ |
| Turn off time | toff | - | 0.05 | - | μs | |
| Rise time | tr | - | 0.89 | - | μs | |
| Fall time | tf | - | 0.03 | - | μs | |
| Turn on time | ton | - | 0.69 | - | μs | DACV4=6'b11_1111, DACI4=6'b10_1010 (I _O =200mA), R _{RNF4} =1.0Ω, RL=10Ω, R _{METAL4} =4mΩ, R _W =40mΩ |
| Turn off time | toff | - | 0.04 | - | μs | |
| Rise time | tr | - | 0.29 | - | μs | |
| Fall time | tf | - | 0.03 | - | μs | |

Constant-Current Type Drive block (ch5)

| Parameter | Symbol | Information ^{※7} | | | Unit | Conditions |
|-----------------------------|--------|---------------------------|------|---|------|---|
| | | - | ch5 | - | | |
| Constant-Current Drive Mode | | | | | | |
| Turn on time | ton | - | 0.77 | - | μs | DAC5=6'b10_1101 (I _O =400mA), R _{RNF5} =0.5Ω, RL=10Ω, R _{METAL5} =22mΩ, R _W =40mΩ |
| Turn off time | toff | - | 0.04 | - | μs | |
| Rise time | tr | - | 0.47 | - | μs | |
| Fall time | tf | - | 0.04 | - | μs | |
| Turn on time | ton | - | 0.69 | - | μs | DAC5=6'b10_1010 (I _O =200mA), R _{RNF5} =1.0Ω, RL=10Ω, R _{METAL5} =22mΩ, R _W =40mΩ |
| Turn off time | toff | - | 0.04 | - | μs | |
| Rise time | tr | - | 0.24 | - | μs | |
| Fall time | tf | - | 0.02 | - | μs | |

※7 AC characteristics are reference values, then the performance of IC's characteristics is not guaranteed.

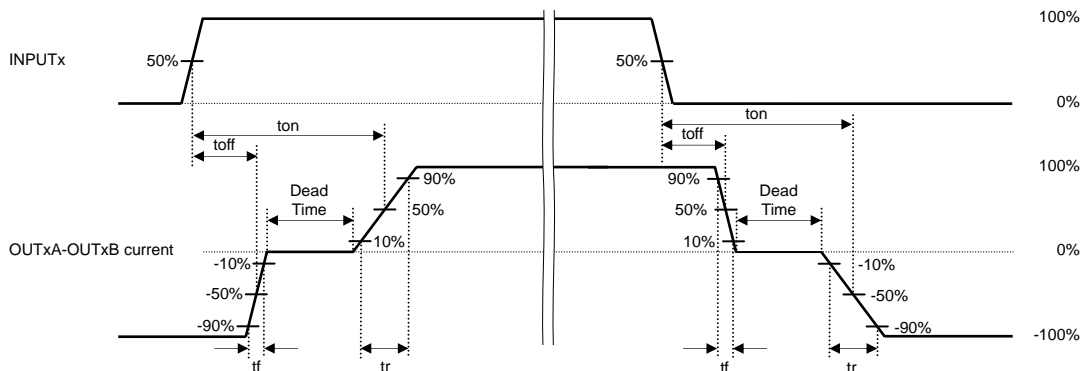


Fig.13 The Definition of I/O Switching Waveforms

4) BD6370GUL Electrical AC Characteristic Diagrams

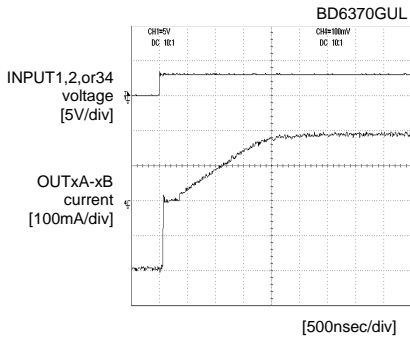


Fig.14 I/O AC Responses (ton, tr)
 ch1 to ch3 Full-ON Drive Mode
 DACx=6'b11_1111, RL=20Ω

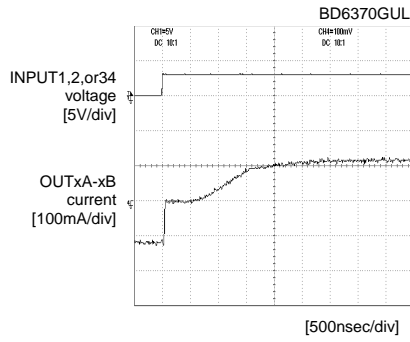


Fig.15 I/O AC Responses (ton, tr)
 ch1 to ch3 Constant-Voltage Drive Mode
 DACx=6'b10_1000, RL=20Ω

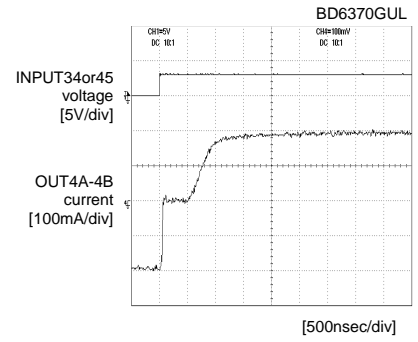


Fig.16 I/O AC Responses (ton, tr)
 ch4 Full-ON Drive Mode
 DACV4=DACI4=6'b11_1111, RL=20Ω

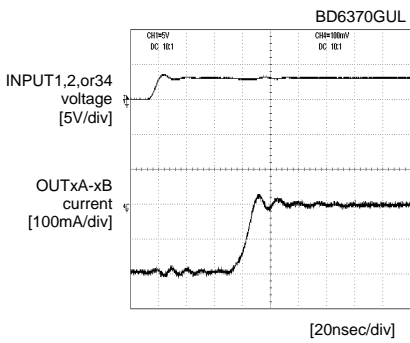


Fig.17 I/O AC Responses (toff, tf)
 ch1 to ch3 Full-ON Drive Mode
 DACx=6'b11_1111, RL=20Ω

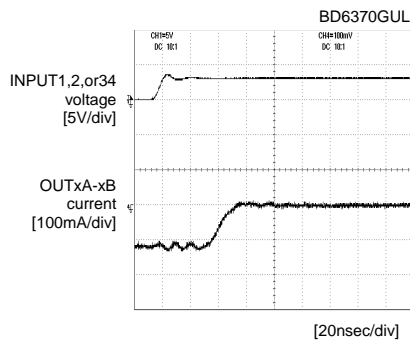


Fig.18 I/O AC Responses (toff, tf)
 ch1 to ch3 Constant-Voltage Drive Mode
 DACx=6'b10_1000, RL=20Ω

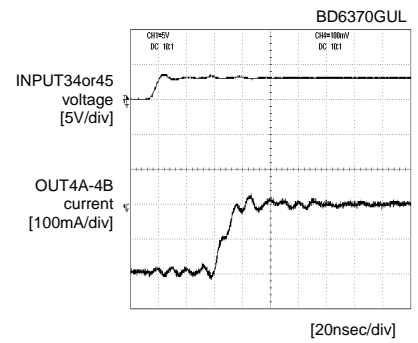


Fig.19 I/O AC Responses (toff, tf)
 ch4 Full-ON Drive Mode
 DACV4=DACI4=6'b11_1111, RL=20Ω

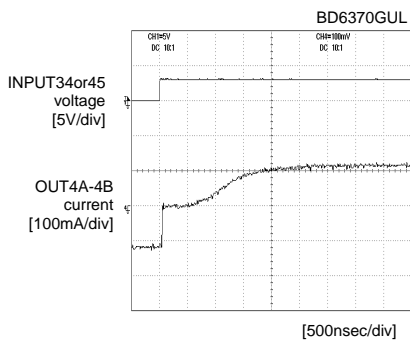


Fig.20 I/O AC Responses (ton, tr)
 ch4 Constant-Voltage Drive Mode
 DACV4=6'b10_1000, DACI4=6'b11_1111, RL=20Ω

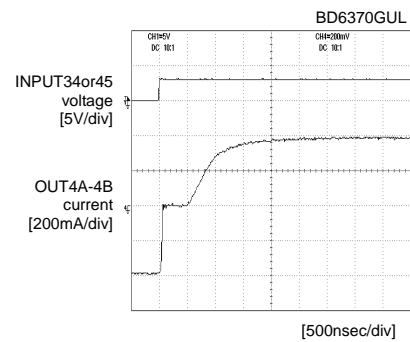


Fig.21 I/O AC Responses (ton, tr)
 ch4 Constant-Current Drive Mode
 DACV4=6'b11_1111, DACI4=6'b10_1100, RRNF4=0.5Ω, RL=10Ω

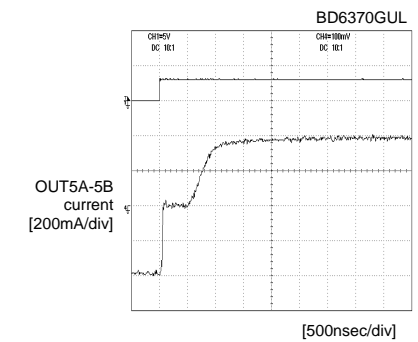


Fig.22 I/O AC Responses (ton, tr)
 ch5 Constant-Current Drive Mode
 DACV5=6'b10_1101, RRNF5=0.5Ω, RL=10Ω

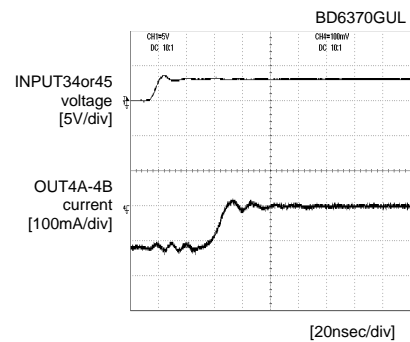


Fig.23 I/O AC Responses (toff, tf)
 ch4 Constant-Voltage Drive Mode
 DACV4=6'b10_1000, DACI4=6'b11_1111, RL=20Ω

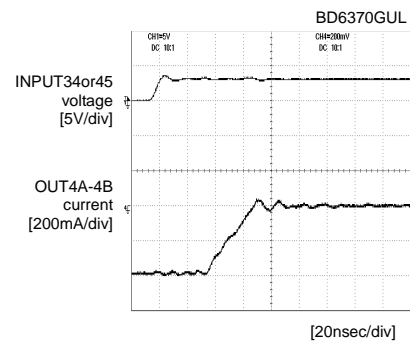


Fig.24 I/O AC Responses (toff, tf)
 ch4 Constant-Current Drive Mode
 DACV4=6'b11_1111, DACI4=6'b10_1100, RRNF4=0.5Ω, RL=10Ω

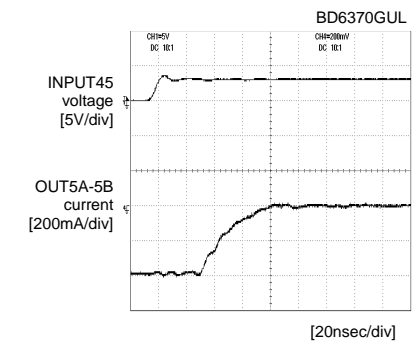


Fig.25 I/O AC Responses (toff, tf)
 ch5 Constant-Current Drive Mode
 DACV5=6'b10_1101, RRNF5=0.5Ω, RL=10Ω

AC characteristics are reference values, then the performance of IC's characteristics is not guaranteed.

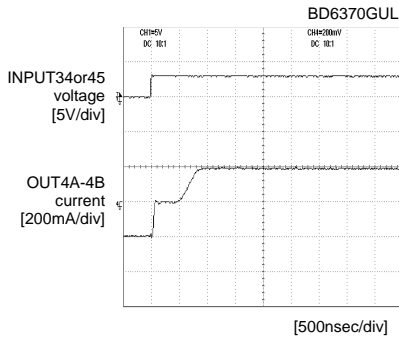


Fig.26 I/O AC Responses (ton, tr)
ch4 Constant-Current Drive Mode

DACV4=6'b11_1111, DACI4=6'b10_1010, $R_{RNF4}=1.0\Omega$, $R_L=10\Omega$

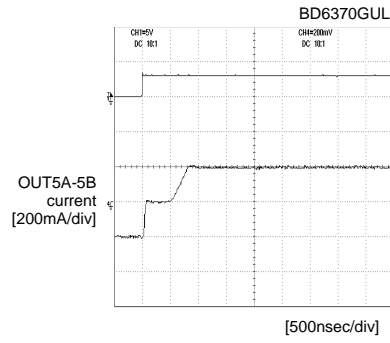


Fig.27 I/O AC Responses (ton, tr)
ch5 Constant-Current Drive Mode

DAC5=6'b10_1010, $R_{RNF5}=1.0\Omega$, $R_L=10\Omega$

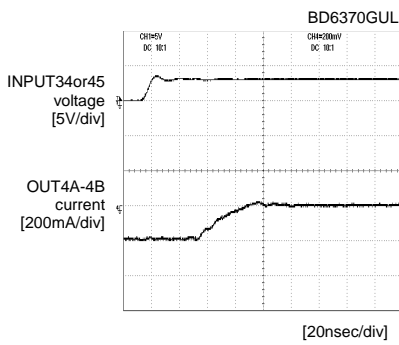


Fig.28 I/O AC Responses (toff, tf)
ch4 Constant-Current Drive Mode

DACV4=6'b11_1111, DACI4=6'b10_1010, $R_{RNF4}=1.0\Omega$, $R_L=10\Omega$

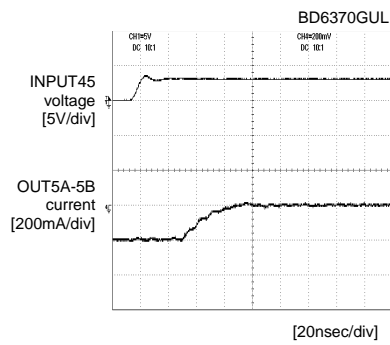


Fig.29 I/O AC Responses (toff, tf)
ch5 Constant-Current Drive Mode

DAC5=6'b10_1010, $R_{RNF5}=1.0\Omega$, $R_L=10\Omega$

AC characteristics are reference values, then the performance of IC's characteristics is not guaranteed.

5) BD6758MWV and BD6758KN Electrical Characteristics (Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{CC}=3.0\text{V}$, $V_M=5.0\text{V}$)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|--|--------|-------|------|------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Overall | | | | | | |
| Circuit current during standby operation | ICCST | - | 0 | 10 | μA | PS=0V |
| Circuit current | ICC | - | 1.4 | 2.5 | mA | PS=VCC with no signal |
| Control input (IN=PS, IN1A to 5B, SEL1 to 2, BRK1 to 2, EN1, and IN5) | | | | | | |
| High level input voltage | VINH | 2.0 | - | - | V | |
| Low level input voltage | VINL | - | - | 0.7 | V | |
| High level input current | IINH | 15 | 30 | 60 | μA | VINH=3V |
| Low level input current | IINL | -1 | 0 | - | μA | VINL=0V |
| Pull-down resistor | RIN | 50 | 100 | 200 | k Ω | |
| UVLO | | | | | | |
| UVLO voltage | VUVLO | 1.6 | - | 2.4 | V | |
| Full-ON Drive block (ch1 to ch4) | | | | | | |
| Output ON-Resistance | RON | - | 1.2 | 1.5 | Ω | $I_o=\pm 400\text{mA}$ on high and low sides in total |
| Linear Constant-Current Drive block (ch5) | | | | | | |
| Output ON-Resistance | RON | - | 1.0 | 1.25 | Ω | $I_o=\pm 400\text{mA}$ on high and low sides in total |
| VREF output voltage | VREF | 1.16 | 1.20 | 1.24 | V | $I_{out}=0\sim 1\text{mA}$ |
| Output limit voltage | VOL | 194 | 200 | 206 | mV | $R_{NF}=0.5\Omega$, $V_{LIM}=0.2\text{V}$ |

6) BD6758MWV and BD6758KN Electrical AC Characteristic Diagrams

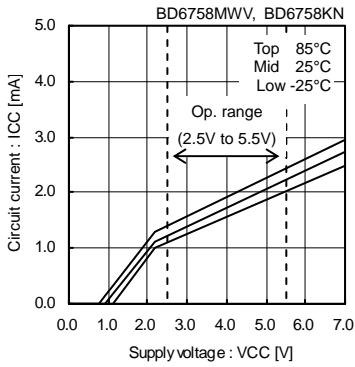


Fig.30 Circuit current

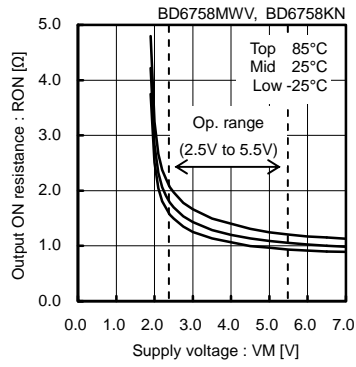


Fig.31 Output ON-Resistance (Full-ON Drive block)

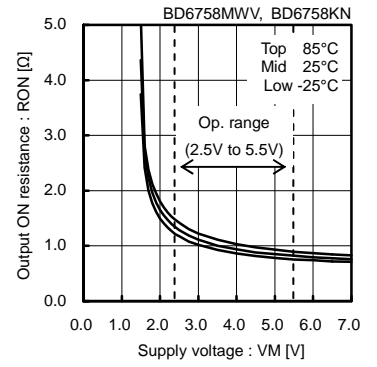


Fig.32 Output ON-Resistance (Linear Constant-Current Drive block)

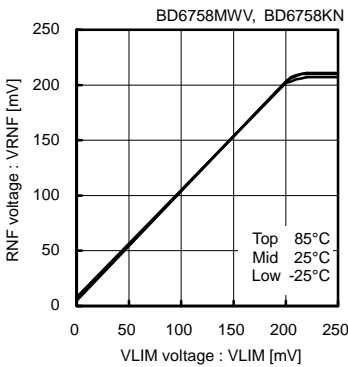


Fig.33 Output limit voltage (RNF=0.5Ω)

● Power Dissipation Reduction

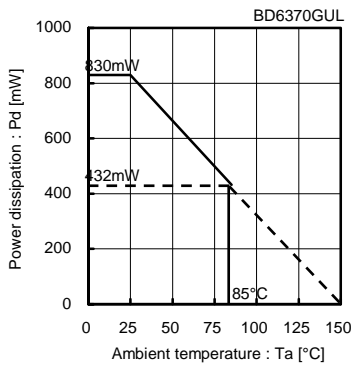


Fig.34 Power Dissipation Reduction

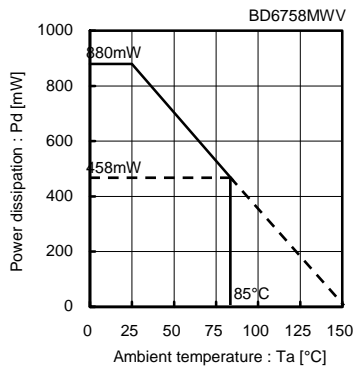


Fig.35 Power Dissipation Reduction

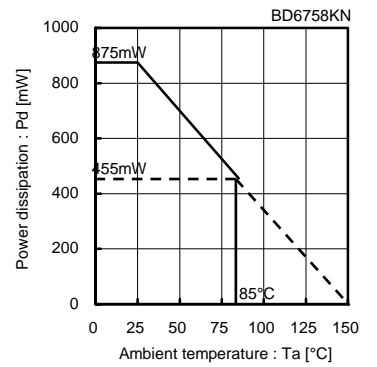


Fig.36 Power Dissipation Reduction

●Block Diagram, Pin Arrangement, and Pin Function

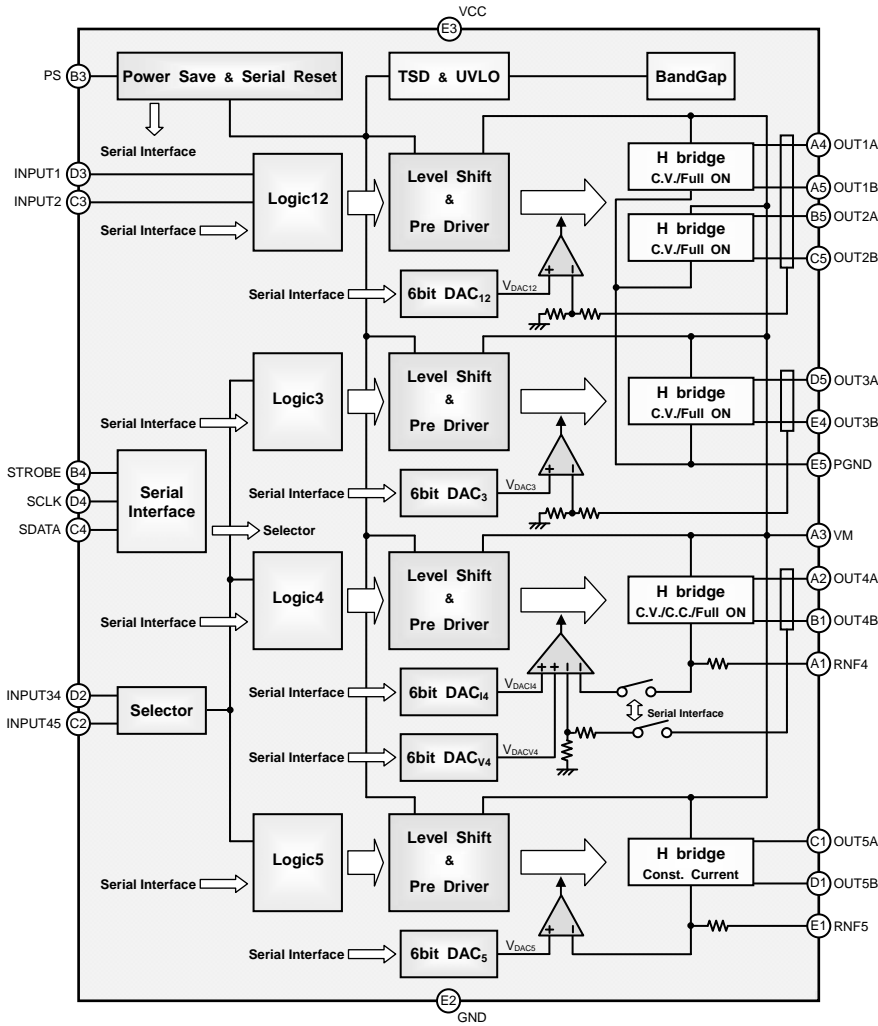


Fig.37 BD6370GUL Block Diagram

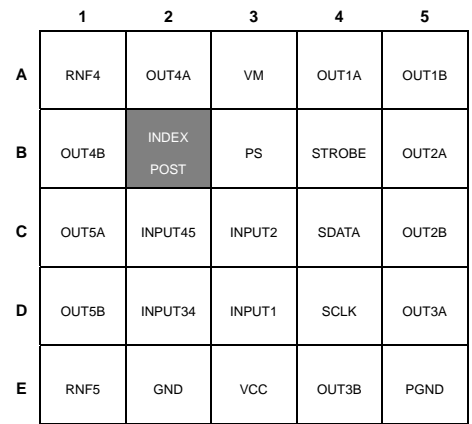


Fig.38 BD6370GUL Pin Arrangement (Top View) VCSP50L2 Package

BD6370GUL Pin Function Table

| No. | Pin Name | Function | No. | Pin Name | Function |
|-----|------------|--|-----|----------|--|
| A1 | RNF4 | Resistance connection pin for output current detection ch4 | D1 | OUT5B | H-bridge output pin ch5 B |
| A2 | OUT4A | H-bridge output pin ch4 A | D2 | INPUT34 | Control input pin ch3 or ch4 |
| A3 | VM | Motor power supply pin | D3 | INPUT1 | Control input pin ch1 |
| A4 | OUT1A | H-bridge output pin ch1 A | D4 | SCLK | Serial clock input pin |
| A5 | OUT1B | H-bridge output pin ch1 B | D5 | OUT3A | H-bridge output pin ch3 A |
| B1 | OUT4B | H-bridge output pin ch4 B | E1 | RNF5 | Resistance connection pin for output current detection ch5 |
| B2 | INDEX POST | - | E2 | GND | Ground pin |
| B3 | PS | Power-saving pin | E3 | VCC | Power supply pin |
| B4 | STROBE | Serial enable input pin | E4 | OUT3B | H-bridge output pin ch3 B |
| B5 | OUT2A | H-bridge output pin ch2 A | E5 | PGND | Motor ground pin ch1 to ch3 |
| C1 | OUT5A | H-bridge output pin ch5 A | | | |
| C2 | INPUT45 | Control input pin ch4 or ch5 | | | |
| C3 | INPUT2 | Control input pin ch2 | | | |
| C4 | SDATA | Serial data input pin | | | |
| C5 | OUT2B | H-bridge output pin ch2 B | | | |

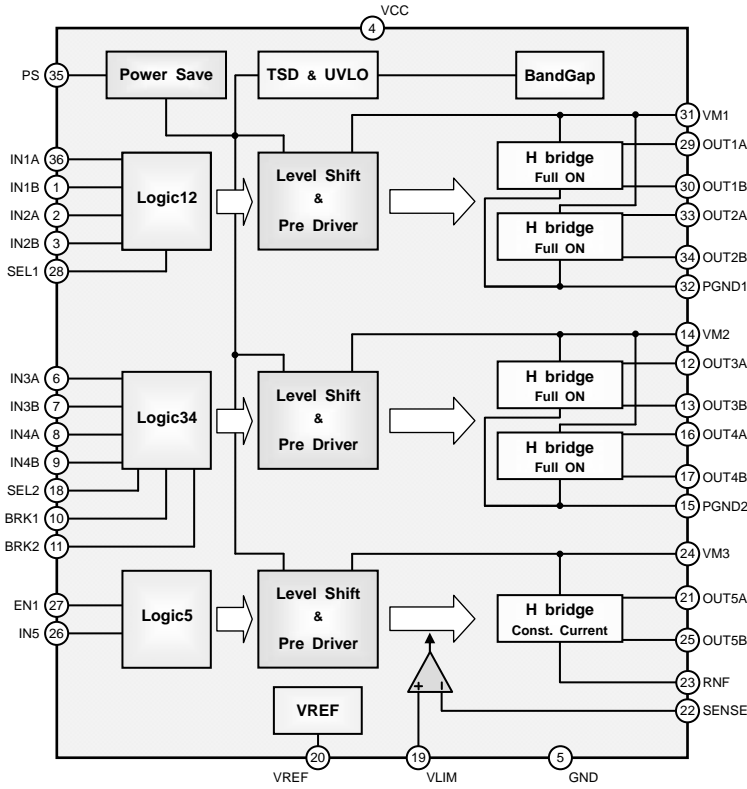


Fig.39 BD6758KN Block Diagram

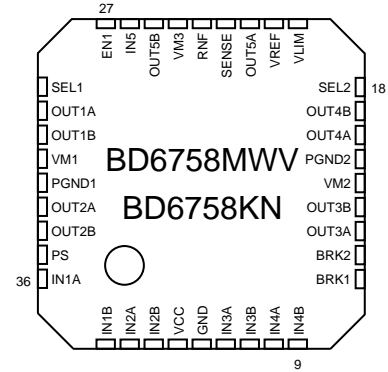


Fig.40 BD6758MWV / KN Pin Arrangement (Top View)
 MWV=UQFN036V5050 Package
 KN=VQFN36 Package

BD6758KN Pin Function Table

| No. | Pin Name | Function | No. | Pin Name | Function |
|-----|----------|--------------------------------------|-----|----------|--|
| 1 | IN1B | Control input pin ch1 B | 19 | VLIM | Output current setting pin ch5 |
| 2 | IN2A | Control input pin ch2 A | 20 | VREF | Reference voltage output pin |
| 3 | IN2B | Control input pin ch2 B | 21 | OUT5A | H-bridge output pin ch5 A |
| 4 | VCC | Power supply pin | 22 | SENSE | Output current detection ch5 |
| 5 | GND | Ground pin | 23 | RNF | Resistance connection pin for output current detection ch5 |
| 6 | IN3A | Control input pin ch3 A | 24 | VM3 | Motor power supply pin ch5 |
| 7 | IN3B | Control input pin ch3 B | 25 | OUT5B | H-bridge output pin ch5 B |
| 8 | IN4A | Control input pin ch4 A | 26 | IN5 | Control input pin ch5 INPUT |
| 9 | IN4B | Control input pin ch4 B | 27 | EN1 | Control input pin ch5 ENABLE |
| 10 | BRK1 | Control input pin ch3 BRAKE | 28 | SEL1 | Drive mode selection pin ch1 and ch2 |
| 11 | BRK2 | Control input pin ch4 BRAKE | 29 | OUT1A | H-bridge output pin ch1 A |
| 12 | OUT3A | H-bridge output pin ch3 A | 30 | OUT1B | H-bridge output pin ch1 B |
| 13 | OUT3B | H-bridge output pin ch3 B | 31 | VM1 | Motor power supply pin ch1 and ch2 |
| 14 | VM2 | Motor power supply pin ch3 and ch4 | 32 | PGND1 | Motor ground pin ch1 and ch2 |
| 15 | PGND2 | Motor ground pin ch3 and ch4 | 33 | OUT2A | H-bridge output pin ch2 A |
| 16 | OUT4A | H-bridge output pin ch4 A | 34 | OUT2B | H-bridge output pin ch2 B |
| 17 | OUT4B | H-bridge output pin ch4 B | 35 | PS | Power saving pin |
| 18 | SEL2 | Drive mode selection pin ch3 and ch4 | 36 | IN1A | Control input pin ch1 A |

●BD6370GUL Function Explanation

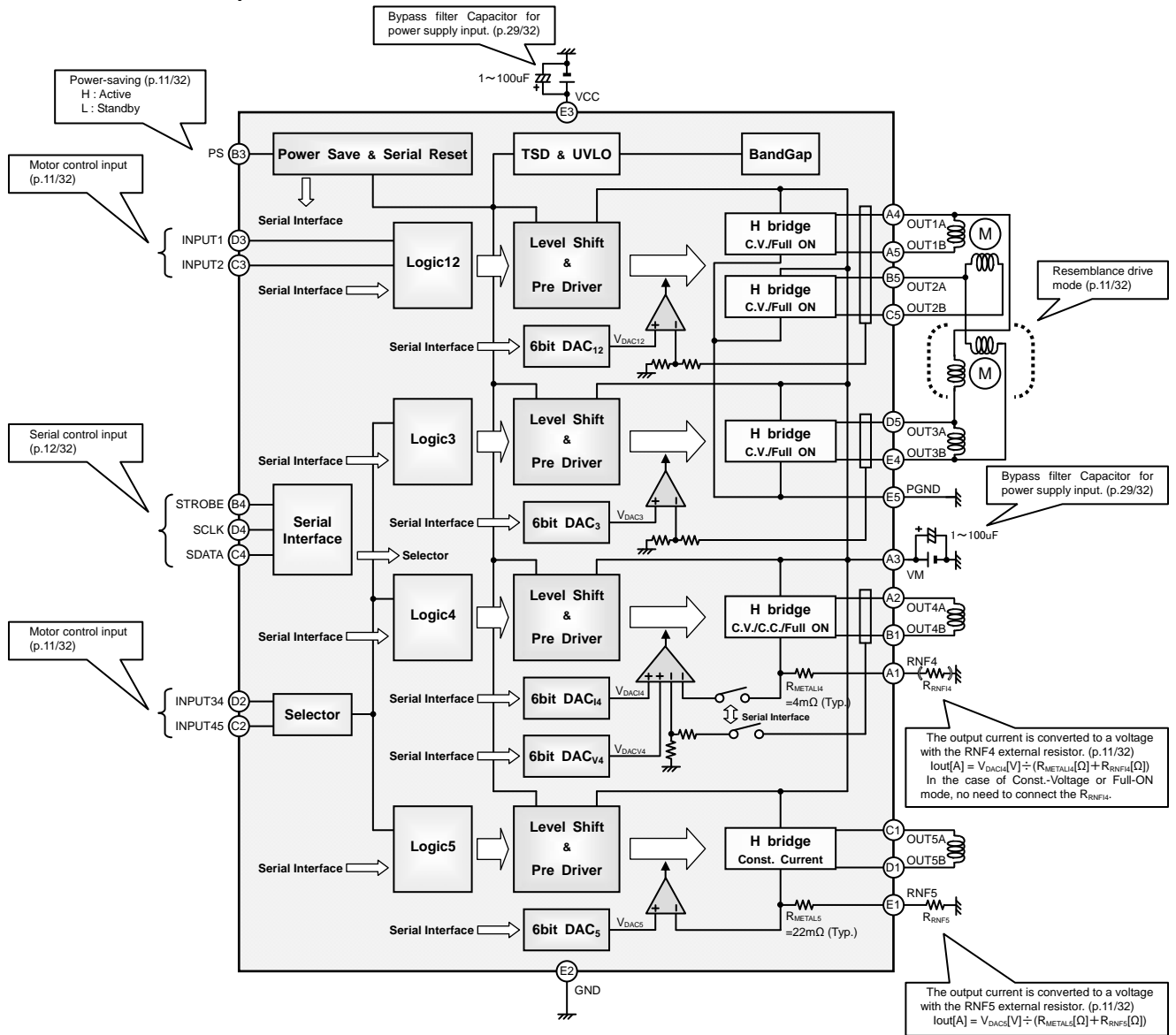


Fig.41 BD6370GUL Application Circuit Diagram

- 1) Power saving and Serial Reset (BD6370GUL; PS)
 - (1) Function Explanation p.11/32
- 2) Control Input (BD6370GUL; INPUTx)
 - (1) Function Explanation p.11/32
- 3) H-bridge (BD6370GUL; VM, OUTxA, OUTxB, and RNFx)
 - (1) Function Explanation p.11/32
 - (2) The D/A Converter Settings of Constant-Voltage, Constant-Current, and Full-ON Mode p.11/32
- 4) Serial Input (BD6370GUL; STROBE, SCLK, and SDATA)
 - (1) Function Explanation p.12/32
 - (2) Serial Register Bit Map p.12/32
- 5) Serial Register Data Bit Function (BD6370GUL)
 - (1) Address Bit [000] Function Explanation p.13/32 to p.14/32
 - (2) Address Bit [001] Function Explanation p.15/32
 - (3) Address Bit [010] Function Explanation p.16/32 to p.17/32
 - (4) Address Bit [011] Function Explanation p.18/32 to p.19/32
 - (5) Address Bit [100] Function Explanation p.20/32
- 6) I/O Truth Table (BD6370GUL) p.21/32 to p.23/32
- 7) The More Precise Constant-Current Settings (BD6370GUL) p.24/32 to p.23/32
- 8) Application Control Sequence (BD6370GUL)
 - (1) Stepping Motor drive controlled by 2 phases mode p.25/32 to p.26/32

1) Power-saving and Serial Reset (BD6370GUL; PS)

(1) Function Explanation

When Low-level voltage is applied to PS pin, the IC will be turned off internally and the circuit current will be 0 μ A (Typ.). During operating mode, PS pin should be High-level. (See the Electrical Characteristics; p.2/32)

Be cancelled power saving mode after turned on power supply VCC and VM, because of PS terminal combines power saving with serial reset function. If the case of power saving terminal always shorted power supply terminal, reset function may not be well, and it may cause the IC to malfunction. (See the Sequence of Serial Control Input; p.12/32)

2) Motor Control Input (BD6370GUL; INPUTx)

(1) Function Explanation

These pins are used to program and control the motor drive modes. So INPUTx switches CW or CCW, CW or Brake, and CCW or Brake, using serial function. (See the Electrical Characteristics; p.2/32 and I/O Truth Table; p.21/32 to p.23/32)

INPUT34 and INPUT45 pins drive ch3 or ch4, and ch4 or ch5, respectively. The driven channel is selected using serial function. (See the Driven Outputs for INPUT Terminal Table; p.14/32)

3) H-bridge (BD6370GUL; VM, OUTxA, OUTxB, and RNFx)

(1) Function Explanation

The H-bridge output transistors of BD6370GUL are Power CMOS Drivers. The total H-bridge ON-Resistance on the high and low sides varies with the VM voltage. The system must be designed so that the maximum H-bridge current for each channel is 500mA or below.

The 3 H-bridges of ch1 to ch3 can be driven as the resemblance 4-channels. For this reason, it is possible to drive the 2 Stepping Motors by ch1 to ch3 as long as the 2 motors don't move simultaneously. The selection of resemblance drive mode for ch1 to ch3 is set using serial function. (See the Driven Outputs for INPUT Terminal Table; p.14/32)

The 2 control input terminals of INPUT34 and INPUT45 drive the 3 H-bridges of ch3 to ch5. Use caution because it is impossible to drive all 3 H-bridges simultaneously.

(2) The D/A Converter Settings of Constant-Voltage, Constant-Current, and Full-ON Mode

The ch1 to ch3 enable Constant-Voltage or Full-ON Driving, and the ch4 enables Constant-Voltage, Constant-Current, or Full-ON Driving, while the ch5 is Constant-Current Driving.

In the case of Full-ON mode for ch1 to ch3, input serial data of each Constant-Voltage setting D/A Converter (DAC12 and DAC3) to be full bits high.

In the ch4, as it set Constant-Voltage mode, input serial data of Constant-Current setting D/A Converter (DACI4) to be full bits high. As it set Constant-Current mode, input serial data of Constant-Voltage setting D/A Converter (DACV4) to be full bits high, while as it set Full-ON mode, input serial data of both D/A Converters to be full bits high. In the settings of Constant-Voltage or Full-ON mode, no need to connect the external resistance for output current detection in RNF4 pin.

The selection of drive mode for ch1 to ch4 is set using serial function. (See the serial settings of the drive mode in each channel; p.13/32 and p.15/32)

(a) Constant-Voltage mode (ch1 to ch4)

Output high voltage; $V_{VOHx}[V] = 8 \times V_{DACx}[V]$ ($8 \times V_{DACx} \leq VM[V]$, $x = 1, 2, 3, \text{ and } 4$) $\dots\dots(1)$

$V_{VOHx}[V] = VM[V]$ ($8 \times V_{DACx} > VM[V]$, $x = 1, 2, 3, \text{ and } 4$) $\dots\dots(2)$

D/A Converter setting value; $8 \times V_{DACx}[V] = 1.5 \text{ to } 4.725$ ($DACx = 6'b01_0100 \text{ to } 6'b11_1111$, $x = 1, 2, 3, \text{ and } 4$)

In the ch4, set DACI4 = 6'b11_1111.

(b) Constant-Current mode (ch4 and ch5)

Output current; $I_{outx}[A] = V_{DACx}[V] \div (R_{METALx}[\Omega] + R_{RNFx}[\Omega])$ ($x = 4 \text{ and } 5$) $\dots\dots(3)$

D/A Converter setting value; $V_{DACx}[V] = 0.05 \text{ to } 0.315$ ($DACx = 6'b00_1010 \text{ to } 6'b11_1111$, $x = 4 \text{ and } 5$)

R_{METALx} ; metal impedance of BD6370GUL's inside (ch4; $R_{METAL4}[\Omega] = 0.004$ (Typ.), ch5; $R_{METAL5}[\Omega] = 0.022$ (Typ.))

R_{RNFx} ; Resistance to connect RNFx pin for output current detection

In the ch4, set DACV4 = 6'b11_1111.

(c) Full-ON mode (ch1 to ch4)

D/A Converter setting value; $DACx = 6'b11_1111$ ($x = 1, 2, 3, 4, \text{ and } 5$)

4) Serial Input (BD6370GUL; STROBE, SCLK, and SDATA)

(1) Function Explanation

The BD6370GUL provides a 3-line serial interface for setting output modes and D/A converters.

SDATA is sent to the internal shift register during the STROBE low interval at the SCLK rising edge. Shift register data (Bit[B] to Bit[0]) is written to the IC's internal 12-bit memory at the STROBE rising edge, according to the addresses stored in Bit[E], Bit[D], and Bit[C]. The serial data input order is Bit[E] to Bit[0].

In the case of the resemblance drive mode (MODE13=1 and/or MODE23=1), input the serial data to be the same condition of DAC12 and DAC3.

Be cancelled power saving mode after turned on power supply VCC and VM. Serial settings are reset when the PS pin changes to Low-level control voltage, because of PS terminal combines power saving with serial reset function. Serial settings are also reset when the UVLO or TSD circuit operates.

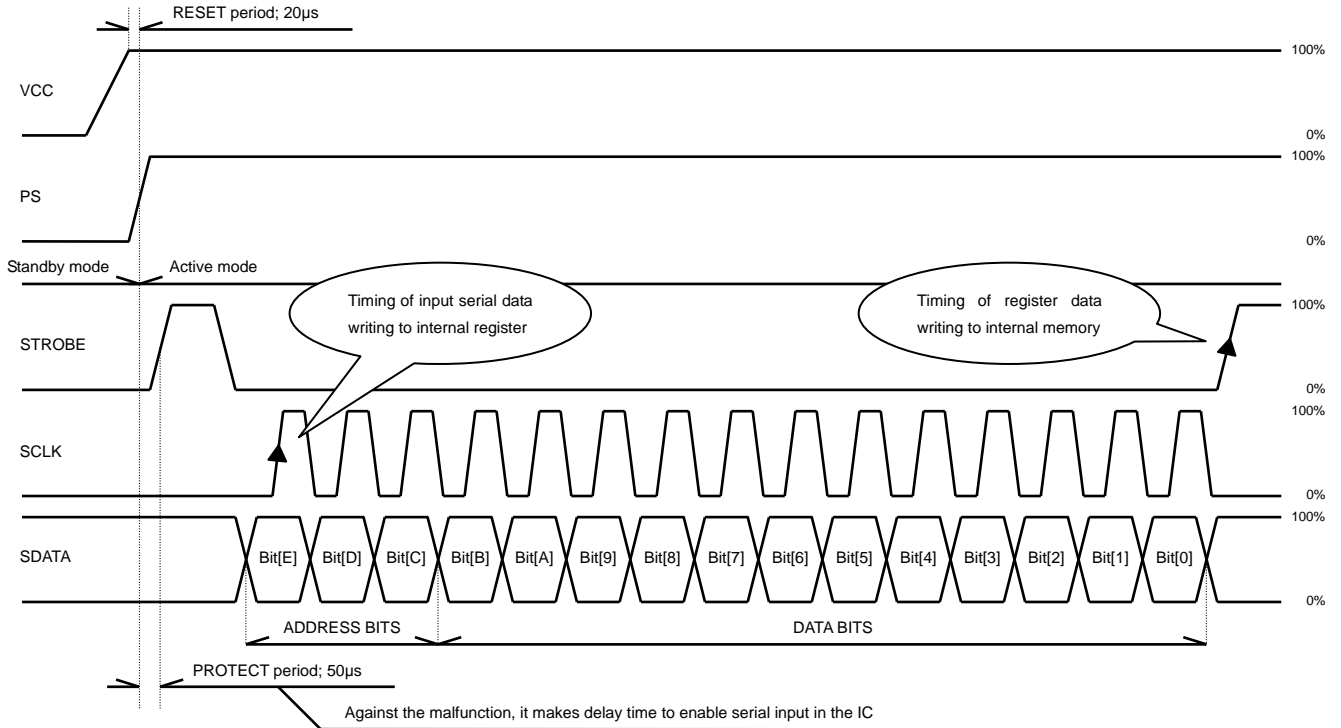


Fig.42 Sequence of Serial Control Input

(2) Serial Register Bit Map

Bit Map is consisted of 5 addresses and 60 data. It is the prohibited bit of MODExx input. Don't input the prohibited bit at all times. A low level should be input to the TEST bit at all times. A high signal may cause the IC to malfunction.

(a) The Prohibited Input of MODE Bit

(MODE45, MODE34, MODE23, MODE13) = (0, 0, 0, 1), (0, 0, 1, 0), (0, 0, 1, 1), (1, 0, 0, 1), (1, 0, 1, 0), (1, 0, 1, 1), (1, 1, 0, 0), (1, 1, 0, 1), (1, 1, 1, 0), (1, 1, 1, 1)

BD6370GUL Serial Register Bit Map

| No. | ADDRESS BIT | | | DATA BIT | | | | | | | | | | | |
|-----|-------------|--------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| | Bit[E] | Bit[D] | Bit[C] | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 00H | 0 | 0 | 0 | TEST | TEST | MODE45 | MODE34 | MODE23 | MODE13 | MODE3C | MODE3B | MODE3A | MODE12C | MODE12B | MODE12A |
| 01H | 0 | 0 | 1 | DAC12[5] | DAC12[4] | DAC12[3] | DAC12[2] | DAC12[1] | DAC12[0] | MODE5B | MODE5A | MODE4D | MODE4C | MODE4B | MODE4A |
| 02H | 0 | 1 | 0 | DAC5[5] | DAC5[4] | DAC5[3] | DAC5[2] | DAC5[1] | DAC5[0] | DAC3[5] | DAC3[4] | DAC3[3] | DAC3[2] | DAC3[1] | DAC3[0] |
| 03H | 0 | 1 | 1 | DACV4[5] | DACV4[4] | DACV4[3] | DACV4[2] | DACV4[1] | DACV4[0] | DACI4[5] | DACI4[4] | DACI4[3] | DACI4[2] | DACI4[1] | DACI4[0] |
| 04H | 1 | 0 | 0 | TEST | TEST | IN5B | IN5A | IN4B | IN4A | IN3B | IN3A | IN2B | IN2A | IN1B | IN1A |

BD6370GUL Serial Register Bit Function

| Bit Name | Function | Bit Name | Function |
|----------|---|----------|---|
| MODE13 | OUT1A-OUT3A resemblance drive select | MODExA | Control input mode select ch1 to ch5 (x=1 to 5) |
| MODE23 | OUT2A-OUT3B resemblance drive select | MODExB | Control input mode select ch1 to ch5 (x=1 to 5) |
| MODE34 | INPUT34 terminal select ch3 or ch4 | MODExC | Output drive select Constant-Voltage / Full-ON mode ch1 to ch3 (x=1 to 3) |
| MODE45 | INPUT45 terminal select ch4 or ch5 | | |
| INxA | Control input mode select ch1 to ch5 (x=1 to 5) | MODExC | Output drive select Constant-Voltage / |
| INxB | Control input mode select ch1 to ch5 (x=1 to 5) | MODExD | Constant-Current / Full-ON mode ch4 (x=4) |
| TEST | TEST BIT (Low level input fixed) | DACx[y] | 6Bit D/A Converter output select ch1 to ch5 (x=12 to 5, y=0 to 5) |

5) Serial Register Data Bit Function (BD6370GUL)

(1) ADDRESS BIT [000] Function Explanation

| No. | ADDRESS BIT | | | DATA BIT | | | | | | | | | | | |
|-----|-------------|--------|--------|----------|--------|--------|--------|--------|--------|--------|--------|--------|---------|---------|---------|
| | Bit[E] | Bit[D] | Bit[C] | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 00H | 0 | 0 | 0 | TEST | TEST | MODE45 | MODE34 | MODE23 | MODE13 | MODE3C | MODE3B | MODE3A | MODE12C | MODE12B | MODE12A |

(a) TEST; test bit for shipment inspection

A low signal should be input to the TEST bit at all times. A high signal may cause the IC to malfunction.

(b) MODE3C and MODE12C; output drive mode select for ch1, ch2, and ch3

| Bit[5] | Bit[2] | drive mode for OUTPUT terminal | | | Note |
|--------|---------|--------------------------------|------------------|------------------|----------------------|
| MODE3C | MODE12C | ch3 | ch2 | ch1 | |
| 0 | - | Full-ON | - | - | set DAC3=6'b11_1111 |
| 1 | - | Constant-Voltage | - | - | |
| - | 0 | - | Full-ON | Full-ON | set DAC12=6'b11_1111 |
| - | 1 | - | Constant-Voltage | Constant-Voltage | |

(c) MODE3B, MODE3A, MODE12B, and MODE12A; control input mode select for ch3, ch2, and ch1, respectively

Refer to I/O Truth Table (p.21/32 to p.22/32) for the detail logic of MODE3B, MODE3A, MODE12B, and MODE12A.

(d) MODE45, MODE34; input terminal select for ch3, ch4, and ch5, and MODE23, MODE13; resemblance drive select for ch1, ch2, and ch3

| Bit[9] | Bit[8] | Bit[7] | Bit[6] | driven outputs for INPUTx terminal | | | | Note | |
|--------|--------|--------|--------|------------------------------------|-------------|-------------|-------------|--|---------|
| MODE45 | MODE34 | MODE23 | MODE13 | INPUT45 | INPUT34 | INPUT2 | INPUT1 | output terminal of OPEN mode | Ref No. |
| 0 | 0 | 0 | 0 | OUT4A-OUT4B | OUT3A-OUT3B | OUT2A-OUT2B | OUT1A-OUT1B | OUT5A, OUT5B | 1 |
| 0 | 0 | 0 | 1 | OUT4A-OUT4B | OUT3B | OUT2A-OUT2B | OUT1A-OUT3A | OUT1B, OUT5A, OUT5B | - |
| 0 | 0 | 1 | 0 | OUT4A-OUT4B | OUT3A | OUT2A-OUT3B | OUT1A-OUT1B | OUT2B, OUT5A, OUT5B | - |
| 0 | 0 | 1 | 1 | OUT4A-OUT4B | don't care | OUT2A-OUT3B | OUT1A-OUT3A | OUT1B, OUT2B, OUT5A, OUT5B | - |
| 0 | 1 | 0 | 0 | OUT5A-OUT5B | OUT4A-OUT4B | OUT2A-OUT2B | OUT1A-OUT1B | OUT3A, OUT3B | 2 |
| 0 | 1 | 0 | 1 | OUT5A-OUT5B | OUT4A-OUT4B | OUT2A-OUT2B | OUT1A-OUT3A | OUT1B, OUT3B | 3 |
| 0 | 1 | 1 | 0 | OUT5A-OUT5B | OUT4A-OUT4B | OUT2A-OUT3B | OUT1A-OUT1B | OUT2B, OUT3A | 4 |
| 0 | 1 | 1 | 1 | OUT5A-OUT5B | OUT4A-OUT4B | OUT2A-OUT3B | OUT1A-OUT3A | OUT1B, OUT2B | 5 |
| 1 | 0 | 0 | 0 | OUT5A-OUT5B | OUT3A-OUT3B | OUT2A-OUT2B | OUT1A-OUT1B | OUT4A, OUT4B | 6 |
| 1 | 0 | 0 | 1 | OUT5A-OUT5B | OUT3B | OUT2A-OUT2B | OUT1A-OUT3A | OUT1B, OUT4A, OUT4B | - |
| 1 | 0 | 1 | 0 | OUT5A-OUT5B | OUT3A | OUT2A-OUT3B | OUT1A-OUT1B | OUT2B, OUT4A, OUT4B | - |
| 1 | 0 | 1 | 1 | OUT5A-OUT5B | don't care | OUT2A-OUT3B | OUT1A-OUT3A | OUT1B, OUT2B, OUT4A, OUT4B | - |
| 1 | 1 | 0 | 0 | don't care | don't care | OUT2A-OUT2B | OUT1A-OUT1B | OUT3A, OUT3B, OUT4A, OUT4B, OUT5A, OUT5B | - |
| 1 | 1 | 0 | 1 | don't care | don't care | OUT2A-OUT2B | OUT1A-OUT3A | OUT1B, OUT3B, OUT4A, OUT4B, OUT5A, OUT5B | - |
| 1 | 1 | 1 | 0 | don't care | don't care | OUT2A-OUT3B | OUT1A-OUT1B | OUT2B, OUT3A, OUT4A, OUT4B, OUT5A, OUT5B | - |
| 1 | 1 | 1 | 1 | don't care | don't care | OUT2A-OUT3B | OUT1A-OUT3A | OUT1B, OUT2B, OUT4A, OUT4B, OUT5A, OUT5B | - |

Gray lines are prohibition serial bit; don't input their bits at all times

ATTENTION in the case of resemblance drive mode (MODE23=1 and/or MODE13=1)

MODE3B, MODE3A, IN3B, and IN3A bits are "don't care". Because OUT1A-OUT3A is driven by MODE12B, MODE12A, IN1B, and IN1A bits, and INPUT1 terminal control. In the same condition, MODE12B, MODE12A, IN2B, and IN2A bits, and INPUT2 terminal drive OUT2A-OUT3B. And set the serial data as DAC12 = DAC3, if not, Output high voltage is different value between OUT1A and OUT3A, and/or OUT2A and OUT3B.

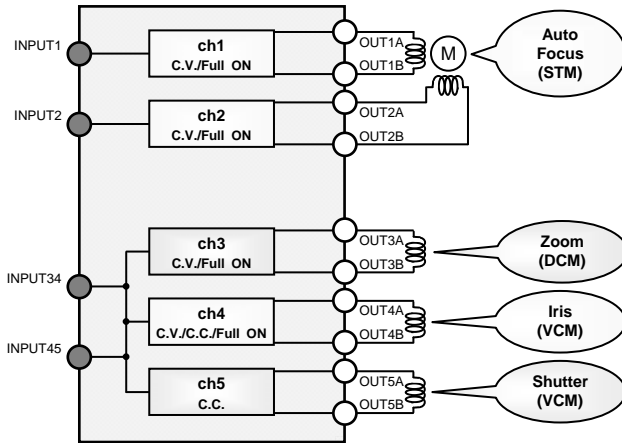


Fig.43 Example of Standard Model (ref No. 1, 2, and 6)

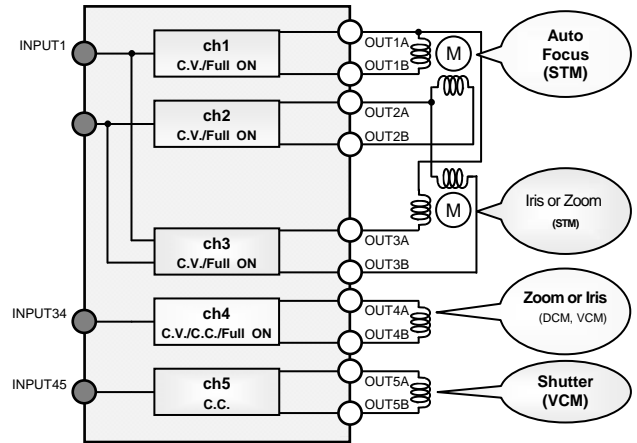


Fig.44 Example of High Performance Model (ref No.2 and 5)

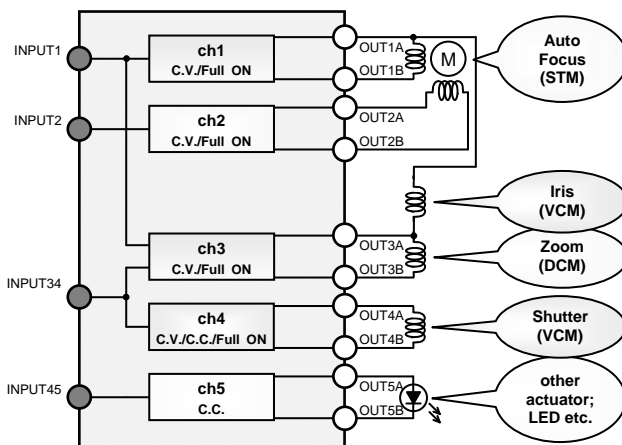


Fig.45 Example of Standard Model and 1 Actuator (ref No.3 and 6)

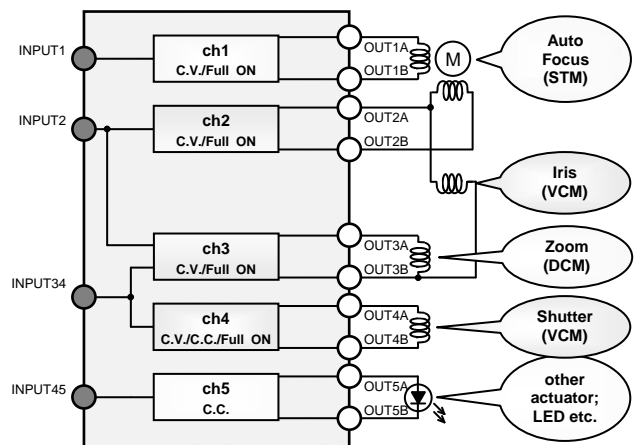


Fig.46 Example of Standard Model and 1 Actuator (ref No.4 and 6)

C.V.=Constant-Voltage drive mode, Full ON=Full-ON drive mode, and C.C.=Constant-Current drive mode
 STM=Stepping Motor, DCM=DC Motor, and VCM=Voice Coil Motor

Examples of Applications above are typical. BD6370GUL is not limited to these applications.

(2) ADDRESS BIT [001] Function Explanation

| No. | ADDRESS BIT | | | DATA BIT | | | | | | | | | | | |
|-----|-------------|--------|--------|----------|----------|----------|----------|----------|----------|--------|--------|--------|--------|--------|--------|
| | Bit[E] | Bit[D] | Bit[C] | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 01H | 0 | 0 | 1 | DAC12[5] | DAC12[4] | DAC12[3] | DAC12[2] | DAC12[1] | DAC12[0] | MODE5B | MODE5A | MODE4D | MODE4C | MODE4B | MODE4A |

(a) DAC12[5] to DAC12[0]; D/A Converter setting for output high voltage of Constant-Voltage mode in ch1 and ch2

| Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | DAC12 setting voltage; V_{DAC12} [V] | Output high voltage; V_{VOH} [V] |
|----------|----------|----------|----------|----------|----------|---|---------------------------------------|
| DAC12[5] | DAC12[4] | DAC12[3] | DAC12[2] | DAC12[1] | DAC12[0] | | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0.188 | 1.500 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0.197 | 1.575 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0.206 | 1.650 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.216 | 1.725 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.225 | 1.800 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.234 | 1.875 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.244 | 1.950 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.253 | 2.025 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.263 | 2.100 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.272 | 2.175 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.281 | 2.250 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.291 | 2.325 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0.300 | 2.400 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.309 | 2.475 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.319 | 2.550 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.328 | 2.625 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.338 | 2.700 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.347 | 2.775 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.356 | 2.850 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.366 | 2.925 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.375 | 3.000 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.384 | 3.075 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0.394 | 3.150 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0.403 | 3.225 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0.413 | 3.300 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0.422 | 3.375 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0.431 | 3.450 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0.441 | 3.525 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.450 | 3.600 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0.459 | 3.675 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0.469 | 3.750 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0.478 | 3.825 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0.488 | 3.900 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0.497 | 3.975 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0.506 | 4.050 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0.516 | 4.125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0.525 | 4.200 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0.534 | 4.275 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0.544 | 4.350 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0.553 | 4.425 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0.563 | 4.500 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.572 | 4.575 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.581 | 4.650 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.591 | 4.725 |

(b) MODE4D and MODE4C; output drive mode select for ch4

| Bit[3] MODE4D | Bit[2] MODE4C | drive mode for ch4 | Note |
|------------------|------------------|--------------------|---|
| 0 | 0 | Full-ON | set DACV4=DACI4=6'b11_1111, and RNF4 terminal to ground |
| 0 | 1 | Full-ON | set DACV4=DACI4=6'b11_1111, and RNF4 terminal to ground |
| 1 | 0 | Constant Voltage | set DACI4=6'b11_1111, and RNF4 terminal to ground |
| 1 | 1 | Constant Current | set DACV4=6'b11_1111, and RNF4 terminal with resistance to ground |

(c) MODE5B, MODE5A, MODE4B, and MODE4A; control input mode select for ch5 and ch4, respectively
Refer to I/O Truth Table (p.23/32) for the detail logic of MODE5B, MODE5A, MODE4B, and MODE4A.

(3) ADDRESS BIT [010] Function Explanation

| No. | ADDRESS BIT | | | DATA BIT | | | | | | | | | | | |
|-----|-------------|--------|--------|----------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| | Bit[E] | Bit[D] | Bit[C] | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 02H | 0 | 1 | 0 | DAC5[5] | DAC5[4] | DAC5[3] | DAC5[2] | DAC5[1] | DAC5[0] | DAC3[5] | DAC3[4] | DAC3[3] | DAC3[2] | DAC3[1] | DAC3[0] |

(a) DAC5[5] to DAC5[0]; D/A Converter setting for output current (DAC5 setting voltage) of Constant-Current mode in ch5
 As regards how to calculate the output current setting, refer to p.11/32 and p.24/32

| Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | DAC5 setting voltage; V _{DAC5} [mV] | R _{RNF5} =0.5Ω Output current [mA] | R _{RNF5} =1.0Ω Output current [mA] |
|---------|---------|---------|---------|---------|---------|--|---|---|
| DAC5[5] | DAC5[4] | DAC5[3] | DAC5[2] | DAC5[1] | DAC5[0] | | | |
| 0 | 0 | 1 | 0 | 1 | 0 | 50 | 96 | 49 |
| 0 | 0 | 1 | 0 | 1 | 1 | 55 | 105 | 54 |
| 0 | 0 | 1 | 1 | 0 | 0 | 60 | 115 | 59 |
| 0 | 0 | 1 | 1 | 0 | 1 | 65 | 125 | 64 |
| 0 | 0 | 1 | 1 | 1 | 0 | 70 | 134 | 68 |
| 0 | 0 | 1 | 1 | 1 | 1 | 75 | 144 | 73 |
| 0 | 1 | 0 | 0 | 0 | 0 | 80 | 153 | 78 |
| 0 | 1 | 0 | 0 | 0 | 1 | 85 | 163 | 83 |
| 0 | 1 | 0 | 0 | 1 | 0 | 90 | 172 | 88 |
| 0 | 1 | 0 | 0 | 1 | 1 | 95 | 182 | 93 |
| 0 | 1 | 0 | 1 | 0 | 0 | 100 | 192 | 98 |
| 0 | 1 | 0 | 1 | 0 | 1 | 105 | 201 | 103 |
| 0 | 1 | 0 | 1 | 1 | 0 | 110 | 211 | 108 |
| 0 | 1 | 0 | 1 | 1 | 1 | 115 | 220 | 113 |
| 0 | 1 | 1 | 0 | 0 | 0 | 120 | 230 | 117 |
| 0 | 1 | 1 | 0 | 0 | 1 | 125 | 239 | 122 |
| 0 | 1 | 1 | 0 | 1 | 0 | 130 | 249 | 127 |
| 0 | 1 | 1 | 0 | 1 | 1 | 135 | 259 | 132 |
| 0 | 1 | 1 | 1 | 0 | 0 | 140 | 268 | 137 |
| 0 | 1 | 1 | 1 | 0 | 1 | 145 | 278 | 142 |
| 0 | 1 | 1 | 1 | 1 | 0 | 150 | 287 | 147 |
| 0 | 1 | 1 | 1 | 1 | 1 | 155 | 297 | 152 |
| 1 | 0 | 0 | 0 | 0 | 0 | 160 | 307 | 157 |
| 1 | 0 | 0 | 0 | 0 | 1 | 165 | 316 | 161 |
| 1 | 0 | 0 | 0 | 1 | 0 | 170 | 326 | 166 |
| 1 | 0 | 0 | 0 | 1 | 1 | 175 | 336 | 171 |
| 1 | 0 | 0 | 1 | 0 | 0 | 180 | 345 | 176 |
| 1 | 0 | 0 | 1 | 0 | 1 | 185 | 355 | 181 |
| 1 | 0 | 0 | 1 | 1 | 0 | 190 | 364 | 186 |
| 1 | 0 | 0 | 1 | 1 | 1 | 195 | 374 | 191 |
| 1 | 0 | 1 | 0 | 0 | 0 | 200 | 383 | 196 |
| 1 | 0 | 1 | 0 | 0 | 1 | 205 | 393 | 201 |
| 1 | 0 | 1 | 0 | 1 | 0 | 210 | Over Operating Condition | 205 |
| 1 | 0 | 1 | 0 | 1 | 1 | 215 | | 210 |
| 1 | 0 | 1 | 1 | 0 | 0 | 220 | | 216 |
| 1 | 0 | 1 | 1 | 0 | 1 | 225 | | 220 |
| 1 | 0 | 1 | 1 | 1 | 0 | 230 | | 225 |
| 1 | 0 | 1 | 1 | 1 | 1 | 235 | | 230 |
| 1 | 1 | 0 | 0 | 0 | 0 | 240 | | 235 |
| 1 | 1 | 0 | 0 | 0 | 1 | 245 | | 240 |
| 1 | 1 | 0 | 0 | 1 | 0 | 250 | | 245 |
| 1 | 1 | 0 | 0 | 1 | 1 | 255 | | 250 |
| 1 | 1 | 0 | 1 | 0 | 0 | 260 | | 254 |
| 1 | 1 | 0 | 1 | 0 | 1 | 265 | | 259 |
| 1 | 1 | 0 | 1 | 1 | 0 | 270 | | 264 |
| 1 | 1 | 0 | 1 | 1 | 1 | 275 | | 269 |
| 1 | 1 | 1 | 0 | 0 | 0 | 280 | | 274 |
| 1 | 1 | 1 | 0 | 0 | 1 | 285 | | 279 |
| 1 | 1 | 1 | 0 | 1 | 0 | 290 | | 284 |
| 1 | 1 | 1 | 0 | 1 | 1 | 295 | | 289 |
| 1 | 1 | 1 | 1 | 0 | 0 | 300 | | 294 |
| 1 | 1 | 1 | 1 | 0 | 1 | 305 | | 298 |
| 1 | 1 | 1 | 1 | 1 | 0 | 310 | 303 | |
| 1 | 1 | 1 | 1 | 1 | 1 | 315 | 308 | |

(b) DAC3[5] to DAC3[0]; D/A Converter setting for output high voltage of Constant-Voltage mode in ch3

| Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] | DAC3 setting voltage; V_{DAC3} [V] | Output high voltage; V_{VOH} [V] |
|---------|---------|---------|---------|---------|---------|---|---------------------------------------|
| DAC3[5] | DAC3[4] | DAC3[3] | DAC3[2] | DAC3[1] | DAC3[0] | | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0.188 | 1.500 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0.197 | 1.575 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0.206 | 1.650 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.216 | 1.725 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.225 | 1.800 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.234 | 1.875 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.244 | 1.950 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.253 | 2.025 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.263 | 2.100 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.272 | 2.175 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.281 | 2.250 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.291 | 2.325 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0.300 | 2.400 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.309 | 2.475 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.319 | 2.550 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.328 | 2.625 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.338 | 2.700 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.347 | 2.775 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.356 | 2.850 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.366 | 2.925 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.375 | 3.000 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.384 | 3.075 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0.394 | 3.150 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0.403 | 3.225 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0.413 | 3.300 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0.422 | 3.375 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0.431 | 3.450 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0.441 | 3.525 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.450 | 3.600 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0.459 | 3.675 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0.469 | 3.750 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0.478 | 3.825 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0.488 | 3.900 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0.497 | 3.975 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0.506 | 4.050 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0.516 | 4.125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0.525 | 4.200 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0.534 | 4.275 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0.544 | 4.350 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0.553 | 4.425 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0.563 | 4.500 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.572 | 4.575 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.581 | 4.650 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.591 | 4.725 |

(4) ADDRESS BIT [011] Function Explanation

| No. | ADDRESS BIT | | | DATA BIT | | | | | | | | | | | |
|-----|-------------|--------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| | Bit[E] | Bit[D] | Bit[C] | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 03H | 0 | 1 | 1 | DACV4[5] | DACV4[4] | DACV4[3] | DACV4[2] | DACV4[1] | DACV4[0] | DACI4[5] | DACI4[4] | DACI4[3] | DACI4[2] | DACI4[1] | DACI4[0] |

(a) DACV4[5] to DACV4[0]; D/A Converter setting for output high voltage of Constant-Voltage mode in ch4

| Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | DACV4 setting voltage; V_{DACV4} [V] | Output high voltage; V_{VOH} [V] |
|----------|----------|----------|----------|----------|----------|---|---------------------------------------|
| DACV4[5] | DACV4[4] | DACV4[3] | DACV4[2] | DACV4[1] | DACV4[0] | | |
| 0 | 1 | 0 | 1 | 0 | 0 | 0.188 | 1.500 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0.197 | 1.575 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0.206 | 1.650 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0.216 | 1.725 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0.225 | 1.800 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0.234 | 1.875 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0.244 | 1.950 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0.253 | 2.025 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0.263 | 2.100 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0.272 | 2.175 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0.281 | 2.250 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0.291 | 2.325 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0.300 | 2.400 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.309 | 2.475 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0.319 | 2.550 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0.328 | 2.625 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0.338 | 2.700 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0.347 | 2.775 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0.356 | 2.850 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0.366 | 2.925 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0.375 | 3.000 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0.384 | 3.075 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0.394 | 3.150 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0.403 | 3.225 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0.413 | 3.300 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0.422 | 3.375 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0.431 | 3.450 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0.441 | 3.525 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0.450 | 3.600 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0.459 | 3.675 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0.469 | 3.750 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0.478 | 3.825 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0.488 | 3.900 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0.497 | 3.975 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0.506 | 4.050 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0.516 | 4.125 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0.525 | 4.200 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0.534 | 4.275 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0.544 | 4.350 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0.553 | 4.425 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0.563 | 4.500 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0.572 | 4.575 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0.581 | 4.650 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0.591 | 4.725 |

(b) DACI4[5] to DACI4[0]; D/A Converter setting for output current (DACI4 setting voltage) of Constant-Current mode in ch4
As regards how to calculate the output current setting, refer to p.11/32 and p.24/32

| Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] | DACI4 setting voltage; V_{DACI4} [mV] | $R_{RNFI4}=0.5\Omega$ Output current [mA] | $R_{RNFI4}=1.0\Omega$ Output current [mA] |
|----------|----------|----------|----------|----------|----------|--|--|--|
| DACI4[5] | DACI4[4] | DACI4[3] | DACI4[2] | DACI4[1] | DACI4[0] | | | |
| 0 | 0 | 1 | 0 | 1 | 0 | 50 | 99 | 50 |
| 0 | 0 | 1 | 0 | 1 | 1 | 55 | 109 | 55 |
| 0 | 0 | 1 | 1 | 0 | 0 | 60 | 119 | 60 |
| 0 | 0 | 1 | 1 | 0 | 1 | 65 | 129 | 65 |
| 0 | 0 | 1 | 1 | 1 | 0 | 70 | 139 | 70 |
| 0 | 0 | 1 | 1 | 1 | 1 | 75 | 149 | 75 |
| 0 | 1 | 0 | 0 | 0 | 0 | 80 | 159 | 80 |
| 0 | 1 | 0 | 0 | 0 | 1 | 85 | 169 | 85 |
| 0 | 1 | 0 | 0 | 1 | 0 | 90 | 179 | 90 |
| 0 | 1 | 0 | 0 | 1 | 1 | 95 | 188 | 95 |
| 0 | 1 | 0 | 1 | 0 | 0 | 100 | 198 | 100 |
| 0 | 1 | 0 | 1 | 0 | 1 | 105 | 208 | 105 |
| 0 | 1 | 0 | 1 | 1 | 0 | 110 | 218 | 110 |
| 0 | 1 | 0 | 1 | 1 | 1 | 115 | 228 | 115 |
| 0 | 1 | 1 | 0 | 0 | 0 | 120 | 238 | 120 |
| 0 | 1 | 1 | 0 | 0 | 1 | 125 | 248 | 125 |
| 0 | 1 | 1 | 0 | 1 | 0 | 130 | 258 | 129 |
| 0 | 1 | 1 | 0 | 1 | 1 | 135 | 268 | 134 |
| 0 | 1 | 1 | 1 | 0 | 0 | 140 | 278 | 139 |
| 0 | 1 | 1 | 1 | 0 | 1 | 145 | 288 | 144 |
| 0 | 1 | 1 | 1 | 1 | 0 | 150 | 298 | 149 |
| 0 | 1 | 1 | 1 | 1 | 1 | 155 | 308 | 154 |
| 1 | 0 | 0 | 0 | 0 | 0 | 160 | 317 | 159 |
| 1 | 0 | 0 | 0 | 0 | 1 | 165 | 327 | 164 |
| 1 | 0 | 0 | 0 | 1 | 0 | 170 | 337 | 169 |
| 1 | 0 | 0 | 0 | 1 | 1 | 175 | 347 | 174 |
| 1 | 0 | 0 | 1 | 0 | 0 | 180 | 357 | 179 |
| 1 | 0 | 0 | 1 | 0 | 1 | 185 | 367 | 184 |
| 1 | 0 | 0 | 1 | 1 | 0 | 190 | 377 | 189 |
| 1 | 0 | 0 | 1 | 1 | 1 | 195 | 387 | 194 |
| 1 | 0 | 1 | 0 | 0 | 0 | 200 | 397 | 199 |
| 1 | 0 | 1 | 0 | 0 | 1 | 205 | | 204 |
| 1 | 0 | 1 | 0 | 1 | 0 | 210 | | 209 |
| 1 | 0 | 1 | 0 | 1 | 1 | 215 | | 214 |
| 1 | 0 | 1 | 1 | 0 | 0 | 220 | | 219 |
| 1 | 0 | 1 | 1 | 0 | 1 | 225 | | 224 |
| 1 | 0 | 1 | 1 | 1 | 0 | 230 | | 229 |
| 1 | 0 | 1 | 1 | 1 | 1 | 235 | | 234 |
| 1 | 1 | 0 | 0 | 0 | 0 | 240 | | 239 |
| 1 | 1 | 0 | 0 | 0 | 1 | 245 | | 244 |
| 1 | 1 | 0 | 0 | 1 | 0 | 250 | | 249 |
| 1 | 1 | 0 | 0 | 1 | 1 | 255 | | 254 |
| 1 | 1 | 0 | 1 | 0 | 0 | 260 | Over Operating Condition | 259 |
| 1 | 1 | 0 | 1 | 0 | 1 | 265 | | 264 |
| 1 | 1 | 0 | 1 | 1 | 0 | 270 | | 269 |
| 1 | 1 | 0 | 1 | 1 | 1 | 275 | | 274 |
| 1 | 1 | 1 | 0 | 0 | 0 | 280 | | 279 |
| 1 | 1 | 1 | 0 | 0 | 1 | 285 | | 284 |
| 1 | 1 | 1 | 0 | 1 | 0 | 290 | | 289 |
| 1 | 1 | 1 | 0 | 1 | 1 | 295 | | 294 |
| 1 | 1 | 1 | 1 | 0 | 0 | 300 | | 299 |
| 1 | 1 | 1 | 1 | 0 | 1 | 305 | | 304 |
| 1 | 1 | 1 | 1 | 1 | 0 | 310 | | 309 |
| 1 | 1 | 1 | 1 | 1 | 1 | 315 | | 314 |

(5) ADDRESS BIT [100] Function Explanation

| No. | ADDRESS BIT | | | DATA BIT | | | | | | | | | | | |
|-----|-------------|--------|--------|----------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| | Bit[E] | Bit[D] | Bit[C] | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| 04H | 1 | 0 | 0 | TEST | TEST | IN5B | IN5A | IN4B | IN4A | IN3B | IN3A | IN2B | IN2A | IN1B | IN1A |

- (a) TEST; test bit for shipment inspection
 A low signal should be input to the TEST bit at all times. A high signal may cause the IC to malfunction.
- (b) IN5B to IN1A; control input mode select for ch1 to ch5, respectively
 Refer to I/O Truth Table (p.21/32 to p.23/32) for the detail logic of IN1A to IN5B.

6) I/O Truth Table (BD6370GUL)

(1) I/O truth table for ch1 and ch2, in the case of MODE13=0, MODE23=0 (x=1 or 2)

| Serial interface input bit | | | | Terminal | Output terminal | | MODE |
|--|---------|------|------|----------|-----------------|-------|-------|
| MODE12B | MODE12A | INxB | INxA | INPUTx | OUTxA | OUTxB | |
| PWM Drive Mode by INPUTx terminal | | | | | | | |
| 0 | 0 | 0 | 0 | X | Z | Z | OFF |
| 0 | 0 | 0 | 1 | L | L | L | Brake |
| 0 | 0 | 0 | 1 | H | H | L | CW |
| 0 | 0 | 1 | 0 | L | L | L | Brake |
| 0 | 0 | 1 | 0 | H | L | H | CCW |
| 0 | 0 | 1 | 1 | X | L | L | Brake |
| PWM Drive Mode by INPUTx terminal | | | | | | | |
| 0 | 1 | 0 | 0 | X | Z | Z | OFF |
| 0 | 1 | 0 | 1 | L | H | L | CW |
| 0 | 1 | 0 | 1 | H | L | L | Brake |
| 0 | 1 | 1 | 0 | L | L | H | CCW |
| 0 | 1 | 1 | 0 | H | L | L | Brake |
| 0 | 1 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUTx terminal | | | | | | | |
| 1 | 0 | X | 0 | X | Z | Z | OFF |
| 1 | 0 | 0 | 1 | L | L | H | CCW |
| 1 | 0 | 0 | 1 | H | H | L | CW |
| 1 | 0 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUTx terminal | | | | | | | |
| 1 | 1 | X | 0 | X | Z | Z | OFF |
| 1 | 1 | 0 | 1 | L | H | L | CW |
| 1 | 1 | 0 | 1 | H | L | H | CCW |
| 1 | 1 | 1 | 1 | X | L | L | Brake |

H; High level, L; Low level, Z; Hi impedance, X; Don't care

At CW, current flows from OUTxA to OUTxB. At CCW, current flows from OUTxB to OUTxA.

(2) I/O truth table for ch3, in the case of MODE34=0, MODE13=0, and MODE23=0

| Serial interface input bit | | | | Terminal | Output terminal | | MODE |
|---|--------|------|------|----------|-----------------|-------|-------|
| MODE3B | MODE3A | IN3B | IN3A | INPUT34 | OUT3A | OUT3B | |
| PWM Drive Mode by INPUT34 terminal | | | | | | | |
| 0 | 0 | 0 | 0 | X | Z | Z | OFF |
| 0 | 0 | 0 | 1 | L | L | L | Brake |
| 0 | 0 | 0 | 1 | H | H | L | CW |
| 0 | 0 | 1 | 0 | L | L | L | Brake |
| 0 | 0 | 1 | 0 | H | L | H | CCW |
| 0 | 0 | 1 | 1 | X | L | L | Brake |
| PWM Drive Mode by INPUT34 terminal | | | | | | | |
| 0 | 1 | 0 | 0 | X | Z | Z | OFF |
| 0 | 1 | 0 | 1 | L | H | L | CW |
| 0 | 1 | 0 | 1 | H | L | L | Brake |
| 0 | 1 | 1 | 0 | L | L | H | CCW |
| 0 | 1 | 1 | 0 | H | L | L | Brake |
| 0 | 1 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUT34 terminal | | | | | | | |
| 1 | 0 | X | 0 | X | Z | Z | OFF |
| 1 | 0 | 0 | 1 | L | L | H | CCW |
| 1 | 0 | 0 | 1 | H | H | L | CW |
| 1 | 0 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUT34 terminal | | | | | | | |
| 1 | 1 | X | 0 | X | Z | Z | OFF |
| 1 | 1 | 0 | 1 | L | H | L | CW |
| 1 | 1 | 0 | 1 | H | L | H | CCW |
| 1 | 1 | 1 | 1 | X | L | L | Brake |

H; High level, L; Low level, Z; Hi impedance, X; Don't care

At CW, current flows from OUT3A to OUT3B. At CCW, current flows from OUT3B to OUT3A.

(3) I/O truth table for ch1, ch3, in the case of MODE13=1 (OUT1A-OUT3A resemblance drive mode)

| Serial interface input bit | | | | Terminal INPUT1 | Output terminal | | MODE |
|--|---------|------|------|--------------------|-----------------|-------|-------|
| MODE12B | MODE12A | IN1B | IN1A | | OUT1A | OUT3A | |
| PWM Drive Mode by INPUT1 terminal | | | | | | | |
| 0 | 0 | 0 | 0 | X | Z | Z | OFF |
| 0 | 0 | 0 | 1 | L | L | L | Brake |
| 0 | 0 | 0 | 1 | H | H | L | CW |
| 0 | 0 | 1 | 0 | L | L | L | Brake |
| 0 | 0 | 1 | 0 | H | L | H | CCW |
| 0 | 0 | 1 | 1 | X | L | L | Brake |
| PWM Drive Mode by INPUT1 terminal | | | | | | | |
| 0 | 1 | 0 | 0 | X | Z | Z | OFF |
| 0 | 1 | 0 | 1 | L | H | L | CW |
| 0 | 1 | 0 | 1 | H | L | L | Brake |
| 0 | 1 | 1 | 0 | L | L | H | CCW |
| 0 | 1 | 1 | 0 | H | L | L | Brake |
| 0 | 1 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUT1 terminal | | | | | | | |
| 1 | 0 | X | 0 | X | Z | Z | OFF |
| 1 | 0 | 0 | 1 | L | L | H | CCW |
| 1 | 0 | 0 | 1 | H | H | L | CW |
| 1 | 0 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUT1 terminal | | | | | | | |
| 1 | 1 | X | 0 | X | Z | Z | OFF |
| 1 | 1 | 0 | 1 | L | H | L | CW |
| 1 | 1 | 0 | 1 | H | L | H | CCW |
| 1 | 1 | 1 | 1 | X | L | L | Brake |

H; High level, L; Low level, Z; Hi impedance, X; Don't care, OUT1B; Hi impedance
At CW, current flows from OUT1A to OUT3A. At CCW, current flows from OUT3A to OUT1A.

(4) I/O truth table for ch2, ch3, in the case of MODE23=1 (OUT2A-OUT3B resemblance drive mode)

| Serial interface input bit | | | | Terminal INPUT2 | Output terminal | | MODE |
|--|---------|------|------|--------------------|-----------------|-------|-------|
| MODE12B | MODE12A | IN2B | IN2A | | OUT2A | OUT3B | |
| PWM Drive Mode by INPUT2 terminal | | | | | | | |
| 0 | 0 | 0 | 0 | X | Z | Z | OFF |
| 0 | 0 | 0 | 1 | L | L | L | Brake |
| 0 | 0 | 0 | 1 | H | H | L | CW |
| 0 | 0 | 1 | 0 | L | L | L | Brake |
| 0 | 0 | 1 | 0 | H | L | H | CCW |
| 0 | 0 | 1 | 1 | X | L | L | Brake |
| PWM Drive Mode by INPUT2 terminal | | | | | | | |
| 0 | 1 | 0 | 0 | X | Z | Z | OFF |
| 0 | 1 | 0 | 1 | L | H | L | CW |
| 0 | 1 | 0 | 1 | H | L | L | Brake |
| 0 | 1 | 1 | 0 | L | L | H | CCW |
| 0 | 1 | 1 | 0 | H | L | L | Brake |
| 0 | 1 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUT2 terminal | | | | | | | |
| 1 | 0 | X | 0 | X | Z | Z | OFF |
| 1 | 0 | 0 | 1 | L | L | H | CCW |
| 1 | 0 | 0 | 1 | H | H | L | CW |
| 1 | 0 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUT2 terminal | | | | | | | |
| 1 | 1 | X | 0 | X | Z | Z | OFF |
| 1 | 1 | 0 | 1 | L | H | L | CW |
| 1 | 1 | 0 | 1 | H | L | H | CCW |
| 1 | 1 | 1 | 1 | X | L | L | Brake |

H; High level, L; Low level, Z; Hi impedance, X; Don't care, OUT2B; Hi impedance
At CW, current flows from OUT2A to OUT3B. At CCW, current flows from OUT3B to OUT2A.

ATTENTION in the case of resemblance drive mode (MODE23=1 and/or MODE13=1)

MODE3B, MODE3A, IN3B, and IN3A bits are "don't care". Because OUT1A-OUT3A is driven by MODE12B, MODE12A, IN1B, and IN1A bits, and INPUT1 terminal control. In the same condition, MODE12B, MODE12A, IN2B, and IN2A bits, and INPUT2 terminal drive OUT2A-OUT3B. And set the serial data as DAC12 = DAC3, if not, Output high voltage is different value between OUT1A and OUT3A, and/or OUT2A and OUT3B.

(5) I/O truth table for ch4, in the case of MODE45=0 (if MODE34=0, then x=45, else then x=34)

| Serial interface input bit | | | | Terminal | Output terminal | | MODE |
|--|--------|------|------|----------|-----------------|-------|-------|
| MODE4B | MODE4A | IN4B | IN4A | INPUTx | OUT4A | OUT4B | |
| PWM Drive Mode by INPUTx terminal | | | | | | | |
| 0 | 0 | 0 | 0 | X | Z | Z | OFF |
| 0 | 0 | 0 | 1 | L | L | L | Brake |
| 0 | 0 | 0 | 1 | H | H | L | CW |
| 0 | 0 | 1 | 0 | L | L | L | Brake |
| 0 | 0 | 1 | 0 | H | L | H | CCW |
| 0 | 0 | 1 | 1 | X | L | L | Brake |
| PWM Drive Mode by INPUTx terminal | | | | | | | |
| 0 | 1 | 0 | 0 | X | Z | Z | OFF |
| 0 | 1 | 0 | 1 | L | H | L | CW |
| 0 | 1 | 0 | 1 | H | L | L | Brake |
| 0 | 1 | 1 | 0 | L | L | H | CCW |
| 0 | 1 | 1 | 0 | H | L | L | Brake |
| 0 | 1 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUTx terminal | | | | | | | |
| 1 | 0 | X | 0 | X | Z | Z | OFF |
| 1 | 0 | 0 | 1 | L | L | H | CCW |
| 1 | 0 | 0 | 1 | H | H | L | CW |
| 1 | 0 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUTx terminal | | | | | | | |
| 1 | 1 | X | 0 | X | Z | Z | OFF |
| 1 | 1 | 0 | 1 | L | H | L | CW |
| 1 | 1 | 0 | 1 | H | L | H | CCW |
| 1 | 1 | 1 | 1 | X | L | L | Brake |

H; High level, L; Low level, Z; Hi impedance, X; Don't care

At CW, current flows from OUT4A to OUT4B. At CCW, current flows from OUT4B to OUT4A.

(6) I/O truth table for ch5, in the case of MODE45=1, MODE34=0 (or MODE45=0, MODE34=1)

| Serial interface input bit | | | | Terminal | Output terminal | | MODE |
|---|--------|------|------|----------|-----------------|-------|-------|
| MODE5B | MODE5A | IN5B | IN5A | INPUT45 | OUT5A | OUT5B | |
| PWM Drive Mode by INPUT45 terminal | | | | | | | |
| 0 | 0 | 0 | 0 | X | Z | Z | OFF |
| 0 | 0 | 0 | 1 | L | L | L | Brake |
| 0 | 0 | 0 | 1 | H | H | L | CW |
| 0 | 0 | 1 | 0 | L | L | L | Brake |
| 0 | 0 | 1 | 0 | H | L | H | CCW |
| 0 | 0 | 1 | 1 | X | L | L | Brake |
| PWM Drive Mode by INPUT45 terminal | | | | | | | |
| 0 | 1 | 0 | 0 | X | Z | Z | OFF |
| 0 | 1 | 0 | 1 | L | H | L | CW |
| 0 | 1 | 0 | 1 | H | L | L | Brake |
| 0 | 1 | 1 | 0 | L | L | H | CCW |
| 0 | 1 | 1 | 0 | H | L | L | Brake |
| 0 | 1 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUT45 terminal | | | | | | | |
| 1 | 0 | X | 0 | X | Z | Z | OFF |
| 1 | 0 | 0 | 1 | L | L | H | CCW |
| 1 | 0 | 0 | 1 | H | H | L | CW |
| 1 | 0 | 1 | 1 | X | L | L | Brake |
| CW / CCW Drive Mode by INPUT45 terminal | | | | | | | |
| 1 | 1 | X | 0 | X | Z | Z | OFF |
| 1 | 1 | 0 | 1 | L | H | L | CW |
| 1 | 1 | 0 | 1 | H | L | H | CCW |
| 1 | 1 | 1 | 1 | X | L | L | Brake |

H; High level, L; Low level, Z; Hi impedance, X; Don't care

At CW, current flows from OUT5A to OUT5B. At CCW, current flows from OUT5B to OUT5A.

7) The More Precise Constant-Current Settings (BD6370GUL)

Regarding Constant-Current Drive blocks (ch4 and ch5), there is the metal impedance of each RNF in BD6370GUL inside: 4mΩ (Typ.) and 22mΩ (Typ.), respectively. Then the metal impedances and the board patterning impedances of RNF4 and RNF5 lines considered, set each D/A Converter to drive the actuator in the more precise constant current.

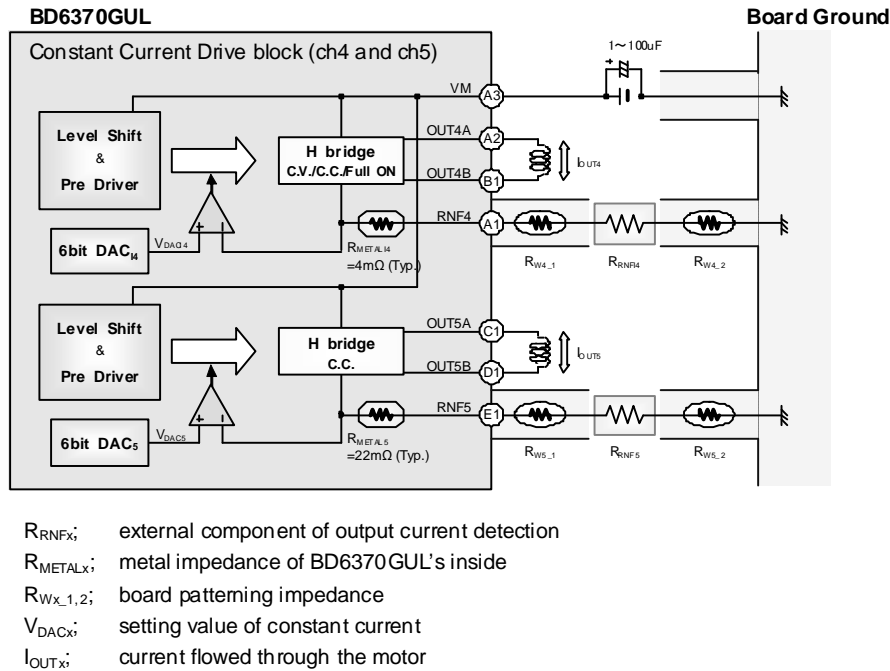


Fig.47 Metal Impedance and Board Patterning Impedance of Constant-Current block

The more correct D/A Converter settings of Constant-Current H-bridge (ch4 and ch5)

Output current value; $I_{OUTx}[A] = V_{DACx}[V] \div (R_{RNFx}[\Omega] + R_{METALx}[\Omega] + R_{Wx,1}[\Omega] + R_{Wx,2}[\Omega])$

(ex.) If there are $V_{DACx}=0.1[V]$, $R_{RNFx}=0.5[\Omega]$, and $R_{Wx,1} + R_{Wx,2}=0[\Omega]$ (the ideal patterning condition), then

Output current value (ch4); $I_{OUT4}[A] = 0.1[V] \div (0.5[\Omega] + 0.004[\Omega] + 0[\Omega]) = \mathbf{0.198}$

Output current value (ch5); $I_{OUT5}[A] = 0.1[V] \div (0.5[\Omega] + 0.022[\Omega] + 0[\Omega]) = \mathbf{0.191}$

Else if there are $V_{DACx}=0.1[V]$, $R_{RNFx}= 0.5[\Omega]$, and $R_{Wx,1} + R_{Wx,2}=\mathbf{0.05}[\Omega]$ (the more closely real patterning condition; the value is different to the patterning), then

Output current value (ch4); $I_{OUT4}[A] = 0.1[V] \div (0.5[\Omega] + 0.004[\Omega] + 0.05[\Omega]) = \mathbf{0.181}$

Output current value (ch5); $I_{OUT5}[A] = 0.1[V] \div (0.5[\Omega] + 0.022[\Omega] + 0.05[\Omega]) = \mathbf{0.175}$

8) Application control sequences (BD6370GUL)
 (1) Stepping Motor drive controlled by 2 phases mode

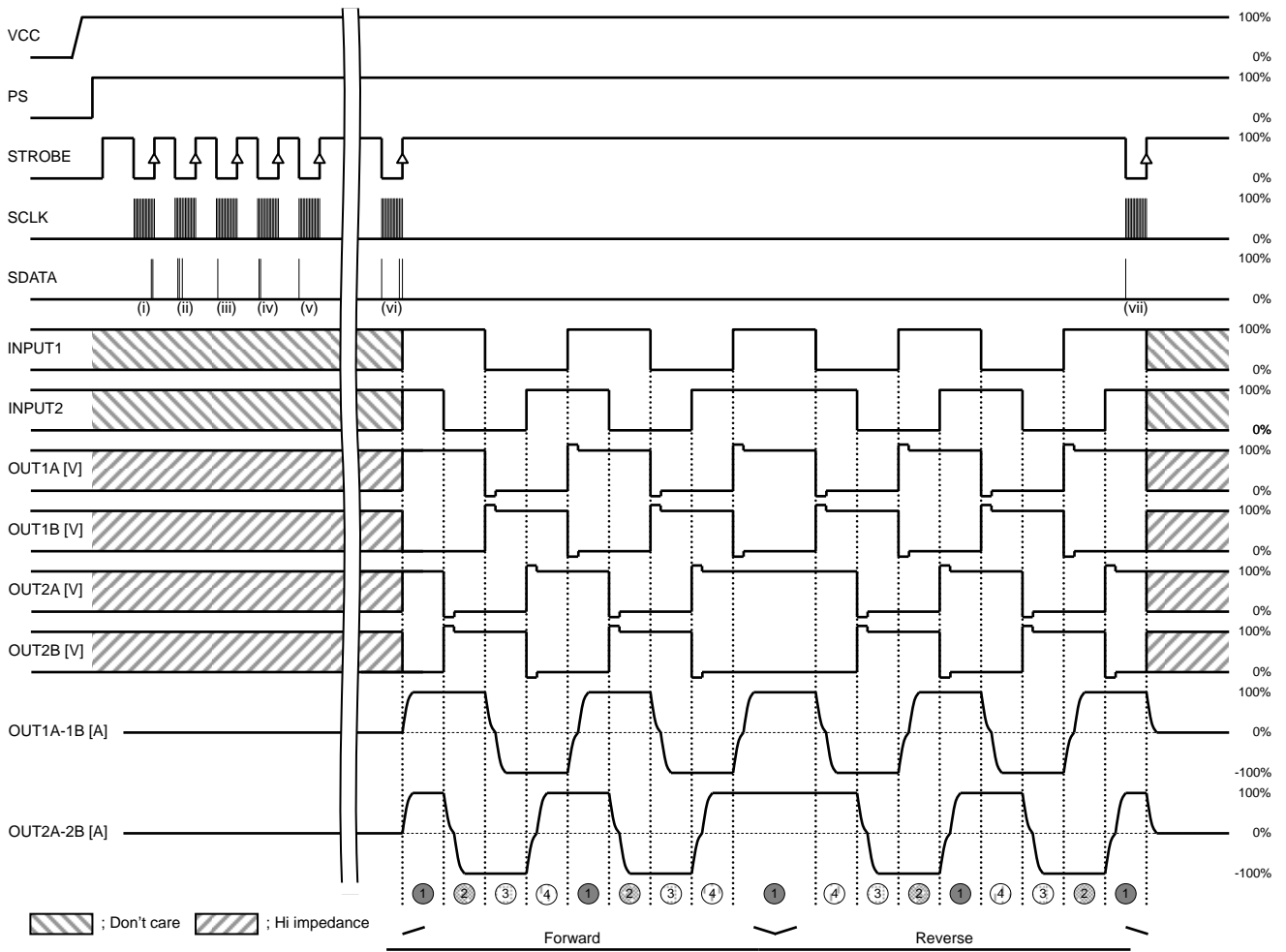


Fig.48 Timing Chart of Stepping Motor Drive

Sequence of Stepping Motor Drive

| Serial interface input bit | | | | | | Terminal | | Output terminal | | | | MODE | | |
|-------------------------------------|----------|------|------|------|------|----------|--------|-----------------|-------|-------|-------|------|-----|----------|
| MODE 12B | MODE 12A | IN2B | IN2A | IN1B | IN1A | INPUT1 | INPUT2 | OUT1A | OUT1B | OUT2A | OUT2B | ch1 | ch2 | Position |
| Control standby | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | X | X | Z | Z | Z | Z | | | |
| Start 2 phase mode driving | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 1 | 0 | 1 | H | H | H | L | H | L | CW | CW | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | H | L | H | L | L | H | CW | CCW | 2 |
| 1 | 0 | 0 | 1 | 0 | 1 | L | L | L | H | L | H | CCW | CCW | 3 |
| 1 | 0 | 0 | 1 | 0 | 1 | L | H | L | H | H | L | CCW | CW | 4 |
| 1 | 0 | 0 | 1 | 0 | 1 | H | H | H | L | H | L | CW | CW | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | H | H | H | L | H | L | CW | CW | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | L | H | L | H | H | L | CCW | CW | 4 |
| 1 | 0 | 0 | 1 | 0 | 1 | L | L | L | H | L | H | CCW | CCW | 3 |
| 1 | 0 | 0 | 1 | 0 | 1 | H | L | H | L | L | H | CW | CCW | 2 |
| 1 | 0 | 0 | 1 | 0 | 1 | H | H | H | L | H | L | CW | CW | 1 |
| End timing (control standby) | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 0 | 0 | 0 | X | X | Z | Z | Z | Z | | | |

H; High level, L; Low level, Z; Hi impedance, X; Don't care
 At CW, current flows from OUTxA to OUTxB. At CCW, current flows from OUTxB to OUTxA.
 At Forward; position up from "1" to "4". At Reverse; position down from "4" to "1".

In Fig.49, it shows minimum step angle, and the relation between size and direction of the current to motor.

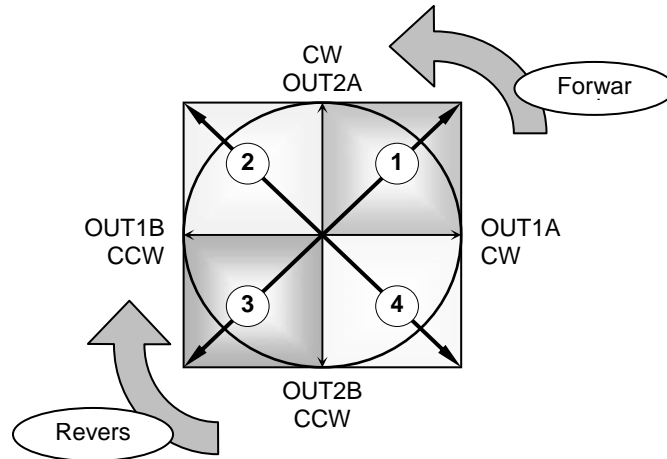


Fig.49 Torque Vector of 2 Phases Mode

Serial Control Input from Initial Set Up (i) to End Timing (vii)

| No. | ADDRESS BIT | | | DATA BIT | | | | | | | | | | | |
|---|-------------|--------|--------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| | Bit[E] | Bit[D] | Bit[C] | Bit[B] | Bit[A] | Bit[9] | Bit[8] | Bit[7] | Bit[6] | Bit[5] | Bit[4] | Bit[3] | Bit[2] | Bit[1] | Bit[0] |
| Initial set up | | | | | | | | | | | | | | | |
| (i) ADDRESS BIT [000]; set ch1 and ch2; Constant-Voltage drive mode | | | | | | | | | | | | | | | |
| 00H | 0 | 0 | 0 | TEST | TEST | MODE45 | MODE34 | MODE23 | MODE13 | MODE3C | MODE3B | MODE3A | MODE12C | MODE12B | MODE12A |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| (ii) ADDRESS BIT [001]; set Output high voltage=3.0V for ch1 and ch2 | | | | | | | | | | | | | | | |
| 01H | 0 | 0 | 1 | DAC12[5] | DAC12[4] | DAC12[3] | DAC12[2] | DAC12[1] | DAC12[0] | MODE5B | MODE5A | MODE4D | MODE4C | MODE4B | MODE4A |
| | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (iii) ADDRESS BIT [010]; in this case, don't care | | | | | | | | | | | | | | | |
| 02H | 0 | 1 | 0 | DAC5[5] | DAC5[4] | DAC5[3] | DAC5[2] | DAC5[1] | DAC5[0] | DAC3[5] | DAC3[4] | DAC3[3] | DAC3[2] | DAC3[1] | DAC3[0] |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (iv) ADDRESS BIT [011]; in this case, don't care | | | | | | | | | | | | | | | |
| 03H | 0 | 1 | 1 | DACV4[5] | DACV4[4] | DACV4[3] | DACV4[2] | DACV4[1] | DACV4[0] | DACI4[5] | DACI4[4] | DACI4[3] | DACI4[2] | DACI4[1] | DACI4[0] |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| (v) ADDRESS BIT [100]; set control standby mode | | | | | | | | | | | | | | | |
| 04H | 1 | 0 | 0 | TEST | TEST | IN5B | IN5A | IN4B | IN4A | IN3B | IN3A | IN2B | IN2A | IN1B | IN1A |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Start timing | | | | | | | | | | | | | | | |
| (vi) ADDRESS BIT [100] | | | | | | | | | | | | | | | |
| 04H | 1 | 0 | 0 | TEST | TEST | IN5B | IN5A | IN4B | IN4A | IN3B | IN3A | IN2B | IN2A | IN1B | IN1A |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| End timing | | | | | | | | | | | | | | | |
| (vii) ADDRESS BIT [100] | | | | | | | | | | | | | | | |
| 04H | 1 | 0 | 0 | TEST | TEST | IN5B | IN5A | IN4B | IN4A | IN3B | IN3A | IN2B | IN2A | IN1B | IN1A |
| | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The above Sequence is one example. BD6370GUL is not limited to this sequence.

●BD6758MWV and BD6758KN Function Explanation

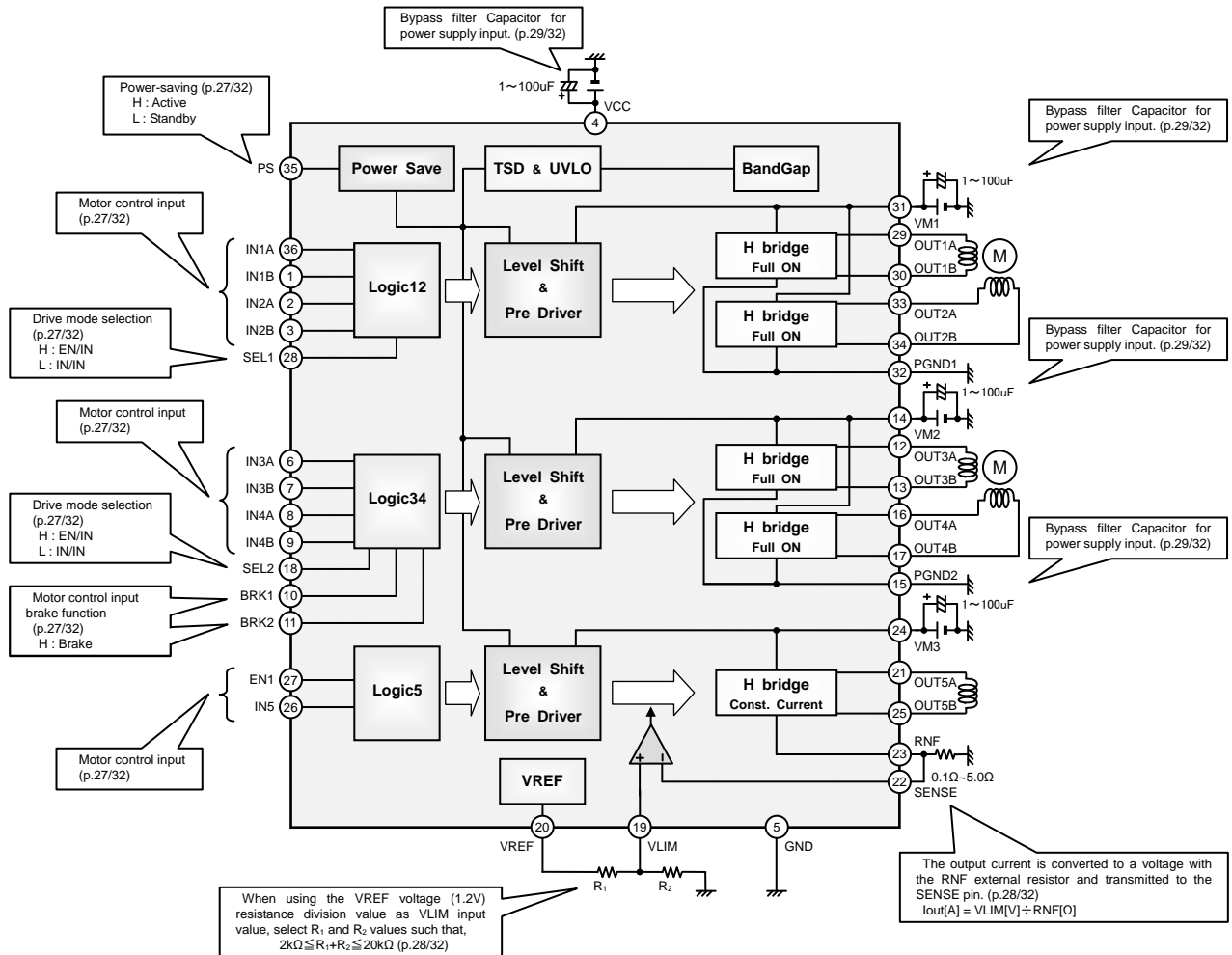


Fig.50 BD6758MWV / KN Application Circuit Diagram

1) Power-saving function (BD6758MWV / KN)

When Low-level voltage is applied to PS pin, the IC will be turned off internally and the circuit current will be 0μA (Typ.). During operating mode, PS pin should be High-level. (See the Electrical Characteristics; p.6/32)

2) Control input (BD6758MWV / KN)

(1) INxA, INxB, EN1 and IN5 pins

These pins are used to program and control the motor drive modes. (See the Electrical Characteristics; p.6/32 and I/O Truth Table; p.28/32)

(2) SELx pins

When the Low-level voltage is applied to the SEL pin, the I/O logic can be set to EN/IN mode. However, when the High-level voltage is applied, the I/O logic can be set to IN/IN mode. (See the Electrical Characteristics; p.6/32 and I/O Truth Table; p.28/32)

(3) BRKx pins

Applying the High-level voltage to the BRKx pin will set the brake mode. (See the Electrical Characteristics; p.6/32 and I/O Truth Table; p.28/32)

3) H-bridge (BD6758MWV / KN)

The 5-channel H-bridges can be controlled independently. For this reason, it is possible to drive the H-bridges simultaneously, as long as the package thermal tolerances are not exceeded.

The H-bridge output transistors of BD6758MWV and BD6758KN are Power CMOS Drivers. The total H-bridge ON-Resistance on the high and low sides varies with the VM voltage. The system must be designed so that the maximum H-bridge current for each channel is 800mA or below. (See the Operating Conditions; p.2/32)

4) Drive system of Linear Constant-Current H-bridge (BD6758MWV / KN: ch5)

BD6758MWV / KN (ch5) enable Linear Constant-Current Driving.

(1) Reference voltage output (with a tolerance of ±3%)

The VREF pin outputs 1.2V, based on the internal reference voltage. The output current of the Constant-Current Drive block is controllable by connecting external resistance to the VREF pin of the IC and applying a voltage divided by the resistor to the output current setting pins (VLIM pin). It is recommended to set the external resistance to 2kΩ or above in consideration of the current capacity of the VREF pin, and 20kΩ or below in order to minimize the fluctuation of the set value caused by the base current of the internal transistor of the IC.

(2) Output current detection and current settings

By connecting external resistor (0.1Ω to 5.0Ω) to the RNF pin of the IC, the motor drive current will be converted into voltage in order to be detected. The output current is kept constant by shorting the RNF and SENSE pins and comparing the voltage with the VLIM voltage. To perform output current settings more precisely, trim the external RNF resistance if needed, and supply a precise voltage externally to the VLIM pin of the IC. In that case, open the VREF pin.

$$\text{Output current value} = \frac{\text{VLIM[V]}}{\text{RNF}[\Omega]}$$

The output current is 400mA±3% if 0.2V is applied to the VLIM pin and a 0.5Ω resistor is connected externally to the RNF pin.

If the VLIM pin is shorted to the VCC pin (or the same voltage level as the VCC is applied) and the SENSE and RNF pins are shorted to the ground, this channel can be used as a Full-ON Drive H-bridge like the other four channels of BD6758KN.

5) I/O truth table (BD6758MWV / KN)

BD6758MWV / KN Full-ON Driver ch1 and ch2 I/O Truth Table

| Drive mode | INPUT | | | OUTPUT | | Output mode |
|------------|-------|------|------|--------|-------|-------------|
| | SEL1 | INxA | INxB | OUTxA | OUTxB | |
| EN/IN | L | H | X | Z | Z | Standby |
| | | L | L | H | L | CW |
| | | L | H | L | H | CCW |
| IN/IN | H | L | L | Z | Z | Standby |
| | | H | L | H | L | CW |
| | | L | H | L | H | CCW |
| | | H | H | L | L | Brake |

L: Low, H: High, X: Don't care, Z: High impedance

At CW, current flows from OUTA to OUTB. At CCW, current flows from OUTB to OUTA.

BD6758MWV / KN Full-ON Driver ch3 and ch4 I/O Truth Table

| Drive mode | INPUT | | | | OUTPUT | | Output mode |
|------------|-------|------|------|------|--------|-------|-------------|
| | SEL2 | INxA | INxB | BRKx | OUTxA | OUTxB | |
| EN/IN | L | H | X | X | Z | Z | Standby |
| | | L | L | L | H | L | CW |
| | | L | H | L | L | H | CCW |
| | | L | X | H | L | L | Brake |
| IN/IN | H | L | L | X | Z | Z | Standby |
| | | H | L | X | H | L | CW |
| | | L | H | X | L | H | CCW |
| | | H | H | X | L | L | Brake |

L: Low, H: High, X: Don't care, Z: High impedance

At CW, current flows from OUTA to OUTB. At CCW, current flows from OUTB to OUTA.

BD6758MWV / KN Linear Constant-Current Driver ch5 I/O Truth Table

| Drive mode | INPUT | | OUTPUT | | Output mode |
|------------|-------|-----|--------|-------|-------------|
| | EN1 | IN5 | OUT5A | OUT5B | |
| EN/IN | H | X | Z | Z | Standby |
| | L | L | H | L | CW |
| | L | H | L | H | CCW |

L: Low, H: High, X: Don't care, Z: High impedance

At CW, current flows from OUTA to OUTB. At CCW, current flows from OUTB to OUTA.

● I/O Circuit Diagram

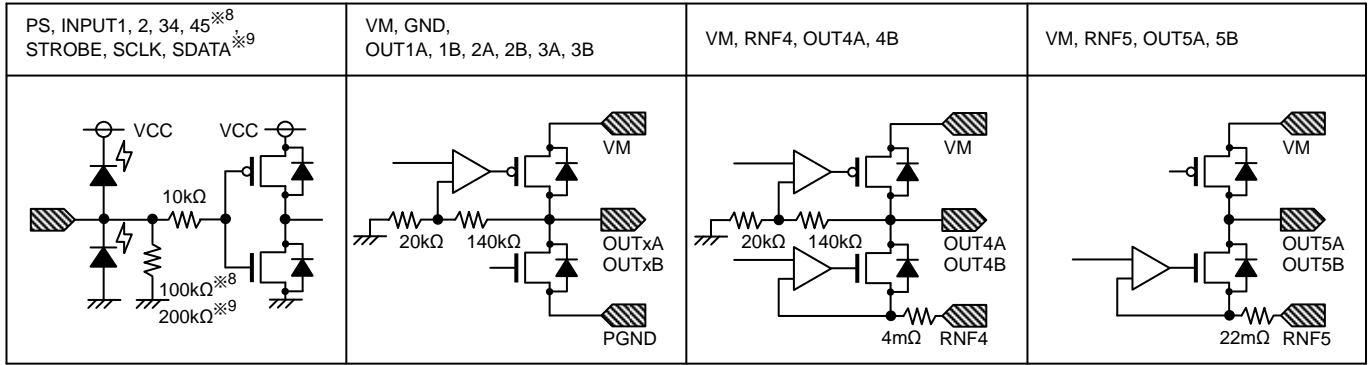


Fig.51 BD6370GUL I/O Circuit Diagram (Resistance values are typical ones)

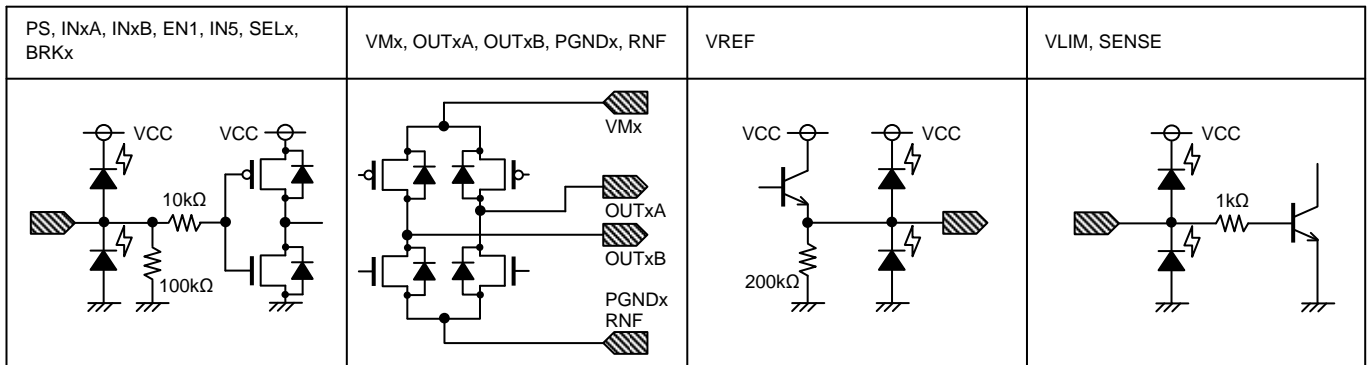


Fig.52 BD6758MWV / KN I/O Circuit Diagram (Resistance values are typical ones)

● Notes for use

- 1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.
- 2) Storage temperature range
As long as the IC is kept within this range, there should be no problems in the IC's performance. Conversely, extreme temperature changes may result in poor IC performance, even if the changes are within the above range.
- 3) Power supply pins and lines
None of the VM line for the H-bridges is internally connected to the VCC power supply line, which is only for the control logic or analog circuit. Therefore, the VM and VCC lines can be driven at different voltages. Although these lines can be connected to a common power supply, do not open the power supply pin but connect it to the power supply externally.
Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may lose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and ground pins.
For this IC with several power supplies and a part consists of the CMOS block, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays, and to the unstable internal logic, respectively. Therefore, give special consideration to power coupling capacitance, width of power and ground wirings, and routing of wiring.
- 4) Ground pins and lines
Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.
When using both small signal GND and large current MGND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.
The power supply and ground lines must be as short and thick as possible to reduce line impedance.
- 5) Thermal design
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

- 6) Pin short and wrong direction assembly of the device
Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.
- 7) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.
- 8) ASO
When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.
- 9) Thermal shutdown circuit
If the junction temperature (T_{jmax}) reaches 175°C, the TSD circuit will operate, and the coil output circuit of the motor will open. There is a temperature hysteresis of approximately 25°C (BD6373GW and BD6873KN Typ.) and 25°C (BD6753KV Typ.). The TSD circuit is designed only to shut off the IC in order to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. The performance of the IC's characteristics is not guaranteed and it is recommended that the device is replaced after the TSD is activated.
- 10) Serial data input
In the BD6370GUL, SDATA input string start with MSB first. A low level should be input to the TEST bit at all times. A high signal may cause the IC to malfunction. The serial settings are reset during standby mode operation and whenever the UVLO or TSD circuits are operating.
It is the prohibited bit of MODExx input. Don't input the prohibited bit at all times. (See the Serial Register Bit Map; p.12/32)
In the case of the resemblance drive mode (MODE13=1 and/or MODE23=1), MODE3B, MODE3A, IN3B, and IN3A bits are "don't care". Because OUT1A-OUT3A is driven by MODE12B, MODE12A, IN1B, and IN1A bits, and INPUT1 terminal control. In the same condition, MODE12B, MODE12A, IN2B, and IN2A bits, and INPUT2 terminal drive OUT2A-OUT3B. And set the serial data as DAC12 = DAC3, if not, Output high voltage is different value between OUT1A and OUT3A, and/or OUT2A and OUT3B. In the case of Full-ON mode for ch1 to ch3, input serial data of each Constant-Voltage setting D/A Converter (DAC12 and DAC3) to be full bits high.
In the ch4, as it set Constant-Voltage mode, input serial data of Constant-Current setting D/A Converter (DACI4) to be full bits high. As it set Constant-Current mode, input serial data of Constant-Voltage setting D/A Converter (DACV4) to be full bits high, while as it set Full-ON mode, input serial data of both D/A Converters to be full bits high. In the settings of Constant-Voltage or Full-ON mode, no need to connect the external resistance for output current detection in RNF4 pin.
- 11) Power saving terminal
Be cancelled power saving mode after turned on power supply VCC and VM, because of PS terminal combines power saving with serial reset function. If the case of power saving terminal always shorted power supply terminal, reset function may not be well, and it may cause the IC to malfunction.
- 12) Testing on application board
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.
- 13) Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics. When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.
- 14) Regarding input pin of the IC
This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
When GND > Pin A, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic diode and transistor.
Parasitic elements can occur inevitably in the structure of the IC. The operation of parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic elements operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

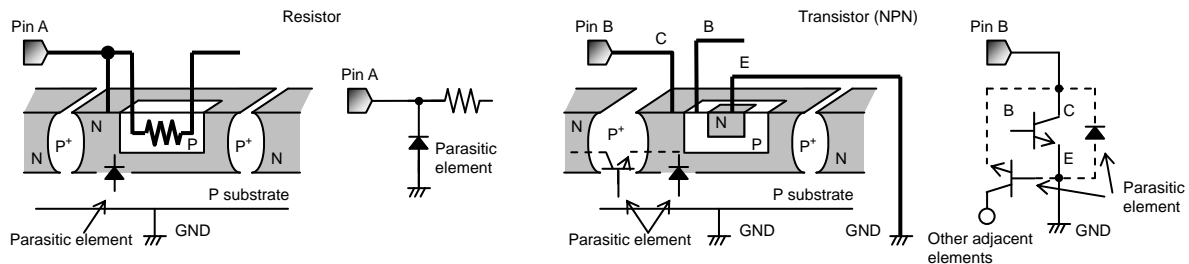


Fig.53 Example of Simple IC Architecture

● Ordering part number

| | |
|---|---|
| B | D |
|---|---|

| | | | |
|---|---|---|---|
| 6 | 3 | 7 | 0 |
|---|---|---|---|

| | | |
|---|---|---|
| G | U | L |
|---|---|---|

| | | |
|---|---|---|
| - | E | 2 |
|---|---|---|

Part No.

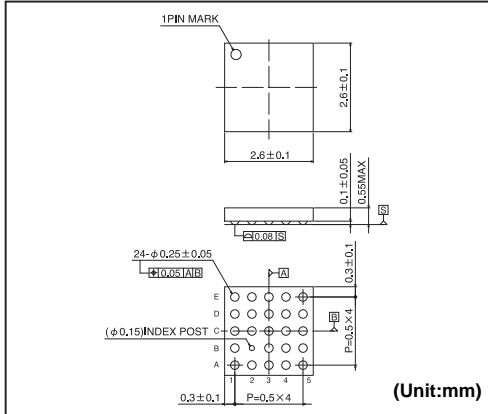
Part No.
 6370 :C.V./F.ON 3ch
 +C.V./C.C./F.ON 1ch
 +C.C. 1ch
 6758 :F.ON 4ch+C.C. 1ch

Package

GUL : VCSP50L2
 MWV : UQFN036V5050
 KN : VQFN36

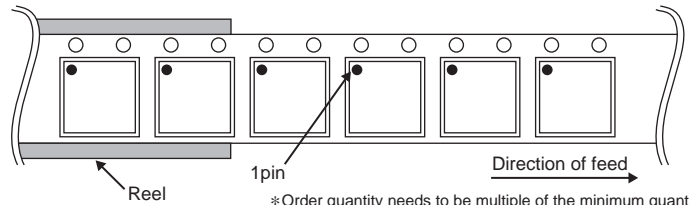
Packaging and forming specification
 E2: Embossed tape and reel

VCSP50L2 (BD6360GUL)

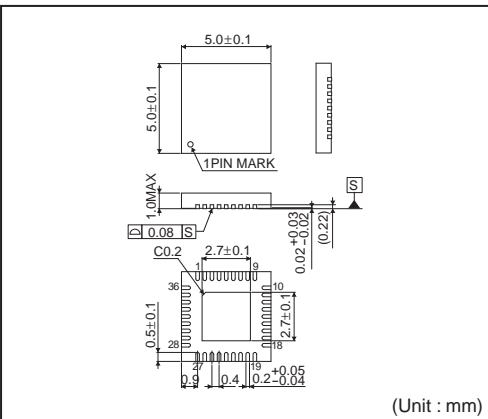


<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 3000pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |

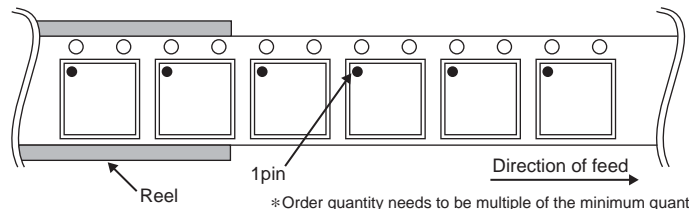


UQFN036V5050

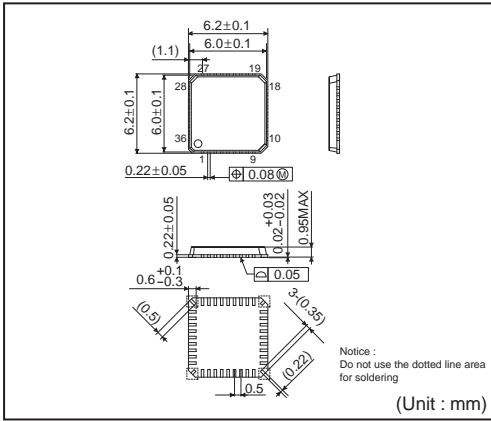


<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |

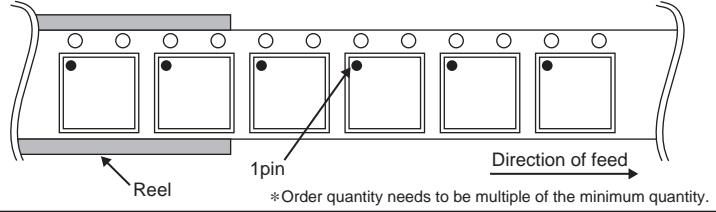


VQFN36



<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape (with dry pack) |
| Quantity | 2500pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



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| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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