

74AUP2G80

Low-power dual D-type flip-flop; positive-edge trigger

Rev. 10 — 19 November 2018

Product data sheet

1. General description

The 74AUP2G80 provides the dual positive-edge triggered D-type flip-flop. Information on the data input is transferred to the \bar{Q} output on the LOW-to-HIGH transition of the clock pulse. The input pin D must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 5 000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1 000 V
- Low static power consumption; $I_{CC} = 0.9 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G80DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G80GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm	SOT833-1
74AUP2G80GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm	SOT1089
74AUP2G80GM	-40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm	SOT902-2
74AUP2G80GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm	SOT1116
74AUP2G80GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AUP2G80DC	p80
74AUP2G80GT	p80
74AUP2G80GF	pT
74AUP2G80GM	p80
74AUP2G80GN	pT
74AUP2G80GS	pT

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

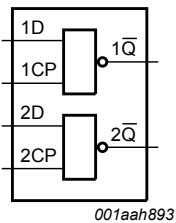


Fig. 1. Logic symbol

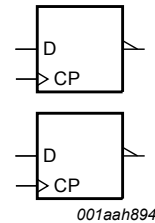


Fig. 2. IEC logic symbol

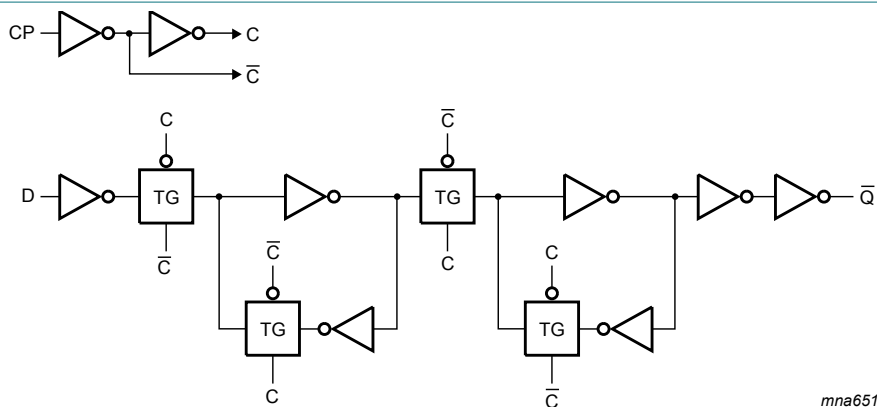
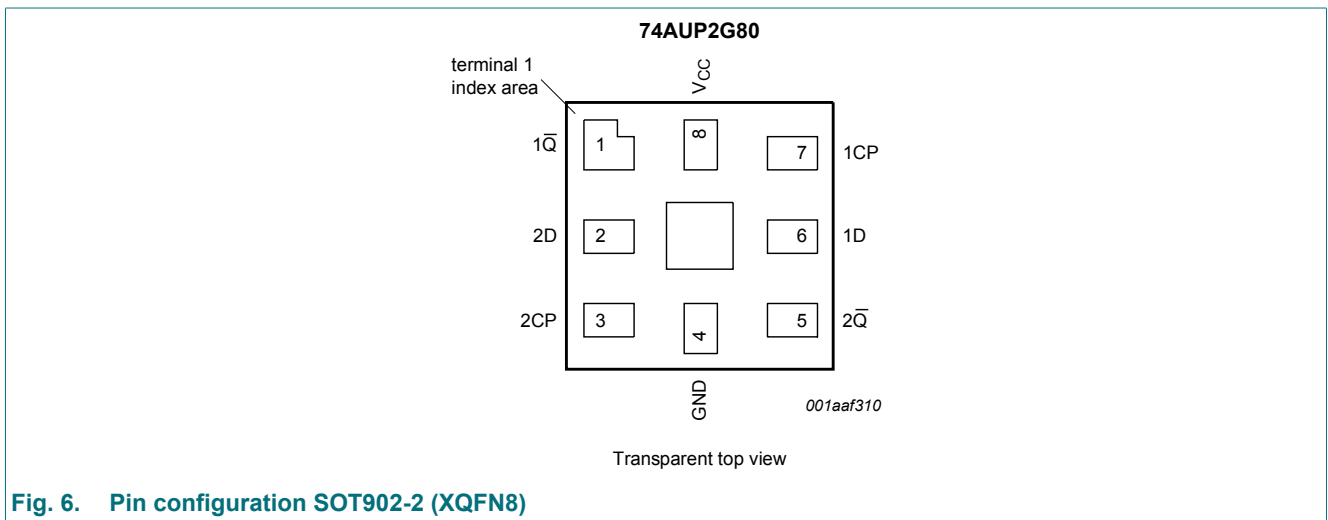
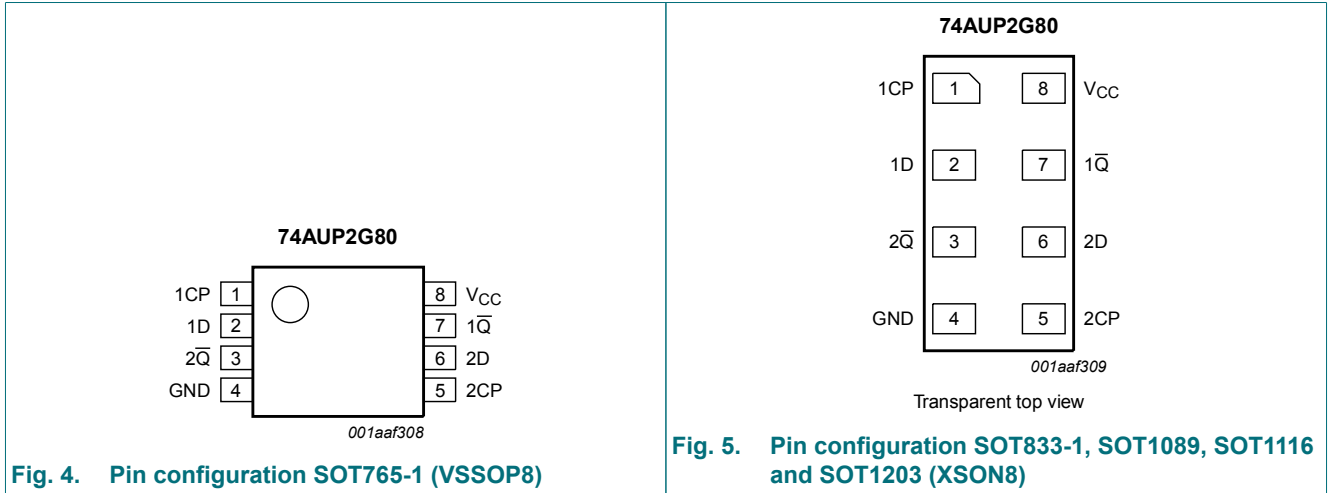


Fig. 3. Logic diagram (one flip-flop)

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT765-1, SOT833-1, SOT1089, SOT1116 and SOT1203	SOT902-2	
1CP, 2CP	1, 5	7, 3	clock input
1D, 2D	2, 6	6, 2	data input
GND	4	4	ground (0 V)
1Q̄, 2Q̄	7, 3	1, 5	data output
V _{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition; X = don't care;

q̄ = lower case letter indicates the state of referenced input, one setup time prior to the LOW-to-HIGH CP transition.

Input		Output
nCP	nD	nQ̄
↑	L	H
↑	H	L
L	X	q̄

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
V _O	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
I _O	output current	V _O = 0 V to V _{CC}	-	±20	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8 and XQFN8 packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		0.8	3.6	V
V _I	input voltage		0	3.6	V
V _O	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 0.8 V to 3.6 V	-	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.70 x V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65 x V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30 x V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35 x V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.75 x V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.11	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.32	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.72	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.30 x V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.1	µA
		V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.2	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.2	µA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.2	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.5	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V [1]	-	-	40	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.6	-	pF
C _O	output capacitance	V _O = GND; V _{CC} = 0 V	-	1.3	-	pF

Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.70 x V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65 x V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30 x V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35 x V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.70 x V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.03	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.30	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.67	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.30 x V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	µA
		V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.5	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.5	µA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.6	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.9	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V [2]	-	-	50	µA

Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.75 x V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.70 x V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25 x V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30 x V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.60 x V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33 x V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	µA
		V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	µA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	1.4	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V [2]	-	-	75	µA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

[2] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Fig. 9.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C				Unit
			Min	Typ[1]	Max	Min (85 °C)	Max (85 °C)	Min (125 °C)	Max (125 °C)	
C_L = 5 pF										
t _{pd}	propagation delay	nCP to nQ̄; see Fig. 7 [2]								
		V _{CC} = 0.8 V	-	20.9	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.9	6.0	12.9	2.6	14.3	2.6	15.7	ns
		V _{CC} = 1.4 V to 1.6 V	1.9	4.2	7.6	2.0	8.9	2.0	9.8	ns
		V _{CC} = 1.65 V to 1.95 V	1.7	3.4	5.9	1.6	7.0	1.6	7.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	2.6	4.3	1.2	5.6	1.2	6.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	2.2	3.6	1.0	4.4	1.0	4.8	ns
f _{max}	maximum frequency	nCP; see Fig. 8								
		V _{CC} = 0.8 V	-	53	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	203	-	170	-	170	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	347	-	310	-	300	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	435	-	400	-	390	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	550	-	490	-	480	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	619	-	550	-	510	-	MHz
C_L = 10 pF										
t _{pd}	propagation delay	nCP to nQ̄; see Fig. 7 [2]								
		V _{CC} = 0.8 V	-	24.6	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.3	6.9	14.9	3.0	16.5	3.0	18.2	ns
		V _{CC} = 1.4 V to 1.6 V	2.6	4.8	8.8	2.3	10.3	2.3	11.3	ns
		V _{CC} = 1.65 V to 1.95 V	2.3	3.9	6.8	2.0	8.1	2.0	8.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.9	3.1	5.1	1.7	6.3	1.7	6.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.8	2.7	4.4	1.4	4.9	1.4	5.4	ns
f _{max}	maximum frequency	nCP; see Fig. 8								
		V _{CC} = 0.8 V	-	52	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	192	-	150	-	150	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	324	-	280	-	230	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	421	-	310	-	250	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	486	-	370	-	360	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	550	-	410	-	360	-	MHz

Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C				Unit
			Min	Typ[1]	Max	Min (85 °C)	Max (85 °C)	Min (125 °C)	Max (125 °C)	
C_L = 15 pF										
t _{pd}	propagation delay	nCP to nQ; see Fig. 7 [2]								
		V _{CC} = 0.8 V	-	28.2	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.0	7.6	16.7	3.4	18.6	3.4	20.5	ns
		V _{CC} = 1.4 V to 1.6 V	3.0	5.3	9.8	2.6	11.5	2.6	12.7	ns
		V _{CC} = 1.65 V to 1.95 V	2.6	4.4	7.6	2.3	9.1	2.3	10.0	ns
		V _{CC} = 2.3 V to 2.7 V	2.2	3.5	5.7	2.0	6.9	2.0	7.6	ns
		V _{CC} = 3.0 V to 3.6 V	1.9	3.1	5.0	1.8	5.5	1.8	6.1	ns
f _{max}	maximum frequency	nCP; see Fig. 8								
		V _{CC} = 0.8 V	-	50	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	181	-	120	-	120	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	301	-	190	-	160	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	407	-	240	-	190	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	422	-	300	-	270	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	481	-	320	-	300	-	MHz
C_L = 30 pF										
t _{pd}	propagation delay	nCP to nQ; see Fig. 7 [2]								
		V _{CC} = 0.8 V	-	38.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.9	9.8	20.7	4.4	24.7	4.4	27.2	ns
		V _{CC} = 1.4 V to 1.6 V	4.0	6.8	12.7	3.5	15.0	3.5	16.5	ns
		V _{CC} = 1.65 V to 1.95 V	3.5	5.6	9.9	2.2	11.9	2.2	13.1	ns
		V _{CC} = 2.3 V to 2.7 V	3.1	4.5	7.5	2.8	9.3	2.8	10.2	ns
		V _{CC} = 3.0 V to 3.6 V	2.9	4.1	6.4	2.7	7.5	2.7	8.3	ns
f _{max}	maximum frequency	nCP; see Fig. 8								
		V _{CC} = 0.8 V	-	28	-	-	-	-	-	MHz
		V _{CC} = 1.1 V to 1.3 V	-	128	-	70	-	70	-	MHz
		V _{CC} = 1.4 V to 1.6 V	-	206	-	120	-	110	-	MHz
		V _{CC} = 1.65 V to 1.95 V	-	262	-	150	-	120	-	MHz
		V _{CC} = 2.3 V to 2.7 V	-	269	-	190	-	170	-	MHz
		V _{CC} = 3.0 V to 3.6 V	-	309	-	200	-	190	-	MHz

Low-power dual D-type flip-flop; positive-edge trigger

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +125 °C				Unit
			Min	Typ[1]	Max	Min (85 °C)	Max (85 °C)	Min (125 °C)	Max (125 °C)	
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
t _{su(H)}	set-up time HIGH	nD to nCP; see Fig. 8								
		V _{CC} = 0.8 V	-	2.5	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	0.5	-	2.3	-	2.3	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	0.3	-	1.2	-	1.2	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.3	-	0.8	-	0.8	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.2	-	0.6	-	0.6	-	ns
t _{su(L)}	set-up time LOW	nD to nCP; see Fig. 8								
		V _{CC} = 0.8 V	-	1.7	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	0.3	-	1.9	-	1.9	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	0.2	-	1.3	-	1.3	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.2	-	1.1	-	1.1	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.3	-	0.8	-	0.8	-	ns
t _h	hold time	nD to nCP; see Fig. 8								
		V _{CC} = 0.8 V	-	-2.1	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	-0.4	-	0.1	-	0.1	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	-0.3	-	0	-	0	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	-0.2	-	0	-	0	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	-0.2	-	0	-	0	-	ns
t _w	pulse width	nCP HIGH or LOW; see Fig. 8								
		V _{CC} = 0.8 V	-	5.2	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	-	1.0	-	3.0	-	3.0	-	ns
		V _{CC} = 1.4 V to 1.6 V	-	0.8	-	2.0	-	2.0	-	ns
		V _{CC} = 1.65 V to 1.95 V	-	0.6	-	2.0	-	2.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	-	0.5	-	2.0	-	2.0	-	ns
C _{PD}	power dissipation capacitance	f = 1 MHz; V _I = GND to V _{CC} [3]								
		V _{CC} = 0.8 V	-	1.8	-	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	1.8	-	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	1.9	-	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	2.0	-	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	2.4	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	2.9	-	-	-	-	pF	

[1] All typical values are measured at nominal V_{CC}.
 [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
 [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V; N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit

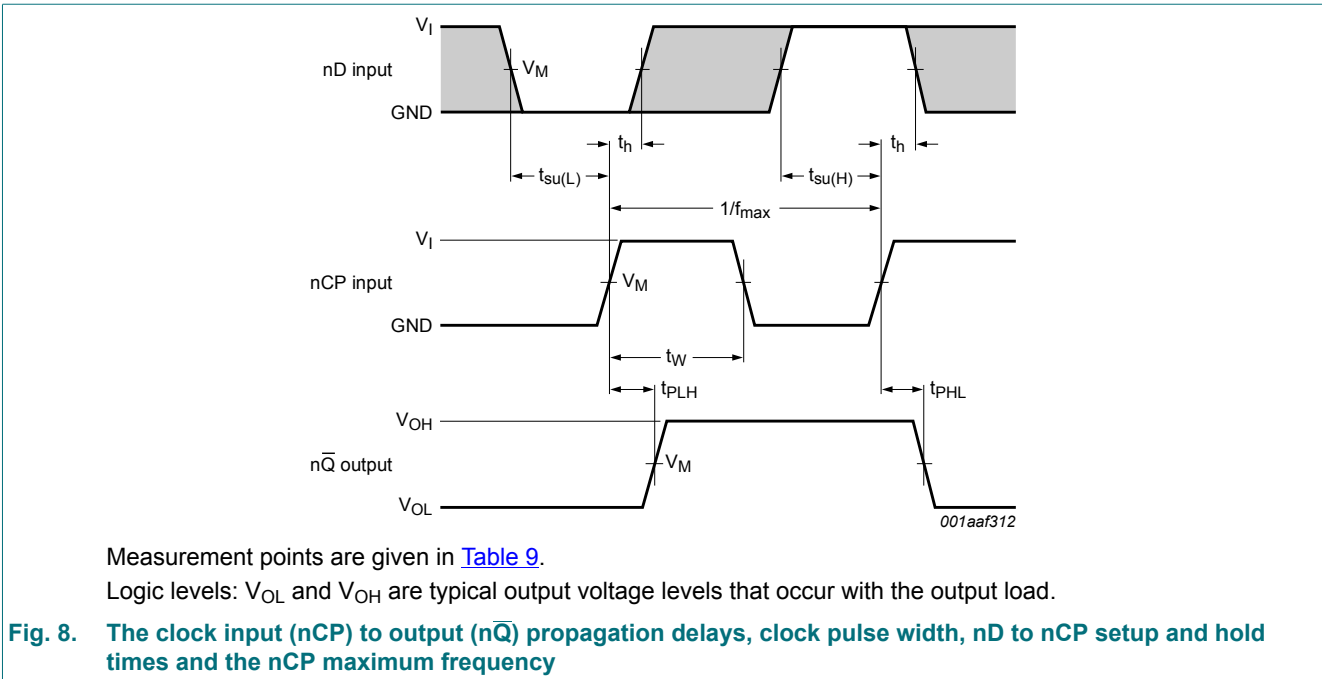
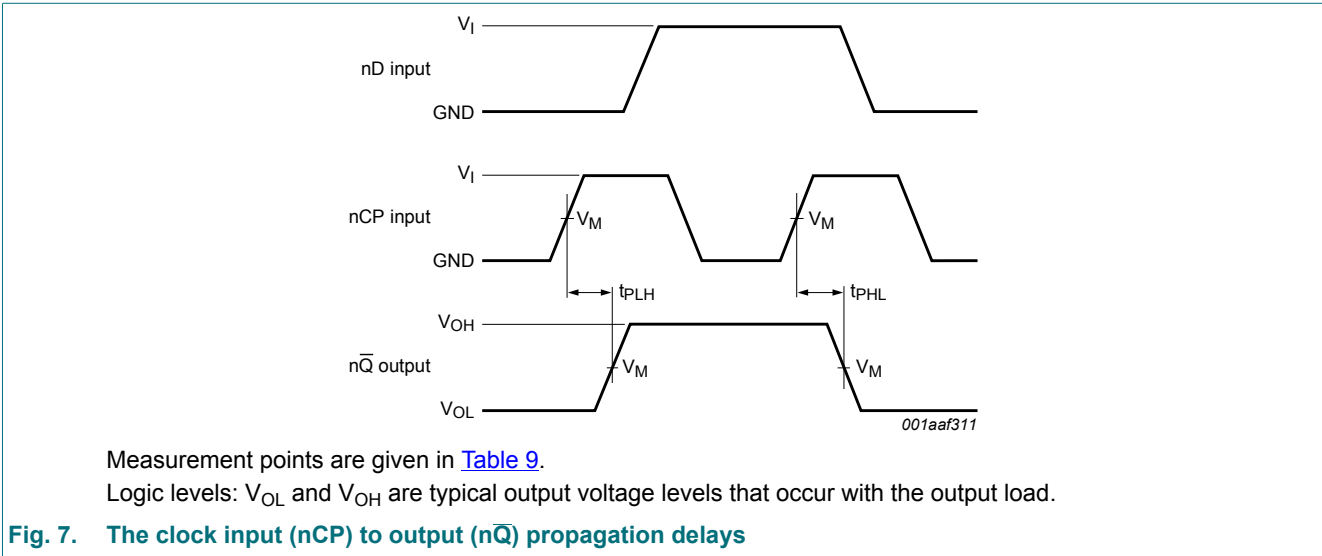


Table 9. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns

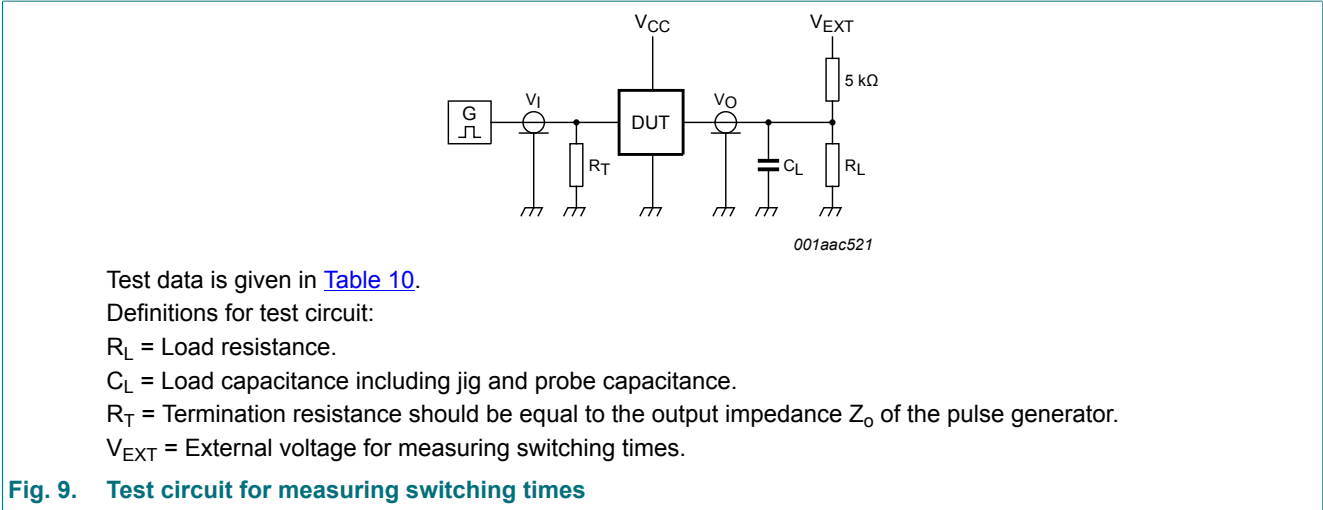


Fig. 9. Test circuit for measuring switching times

Table 10. Test data

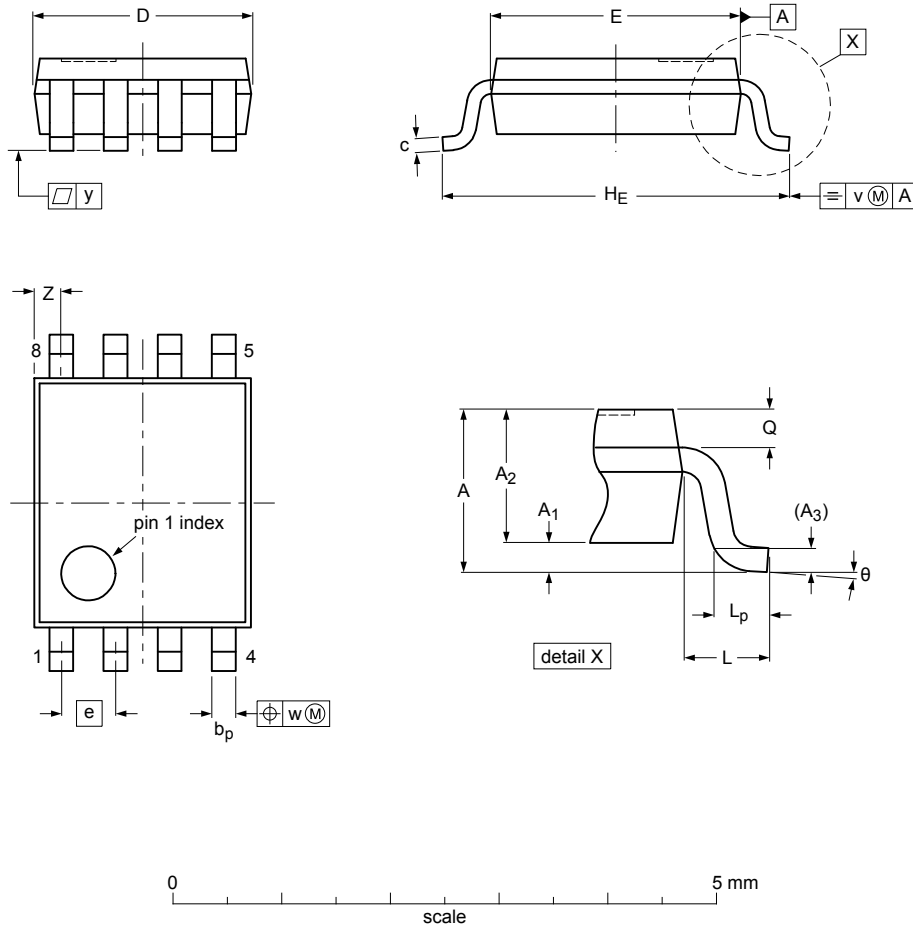
Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5 \text{ k}\Omega$
 For measuring propagation delays, setup and hold times and pulse width $R_L = 1 \text{ M}\Omega$.

12. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



Dimensions (mm are the original dimensions)

Unit	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
max	1	0.15	0.85		0.27	0.23	2.1	2.4	0.5	3.2	0.40	0.21		0.2	0.08	0.1	0.4	8°
nom				0.12							0.4							
min		0.00	0.60		0.17	0.08	1.9	2.2		3.0	0.15	0.19					0.1	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				07-06-02 16-05-31

Fig. 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max	A ₁ max	b	D	E	e	e ₁	L	L ₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

- Including plating thickness.
- Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	---	MO-252	---			-07-11-14- 07-12-07

Fig. 11. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089

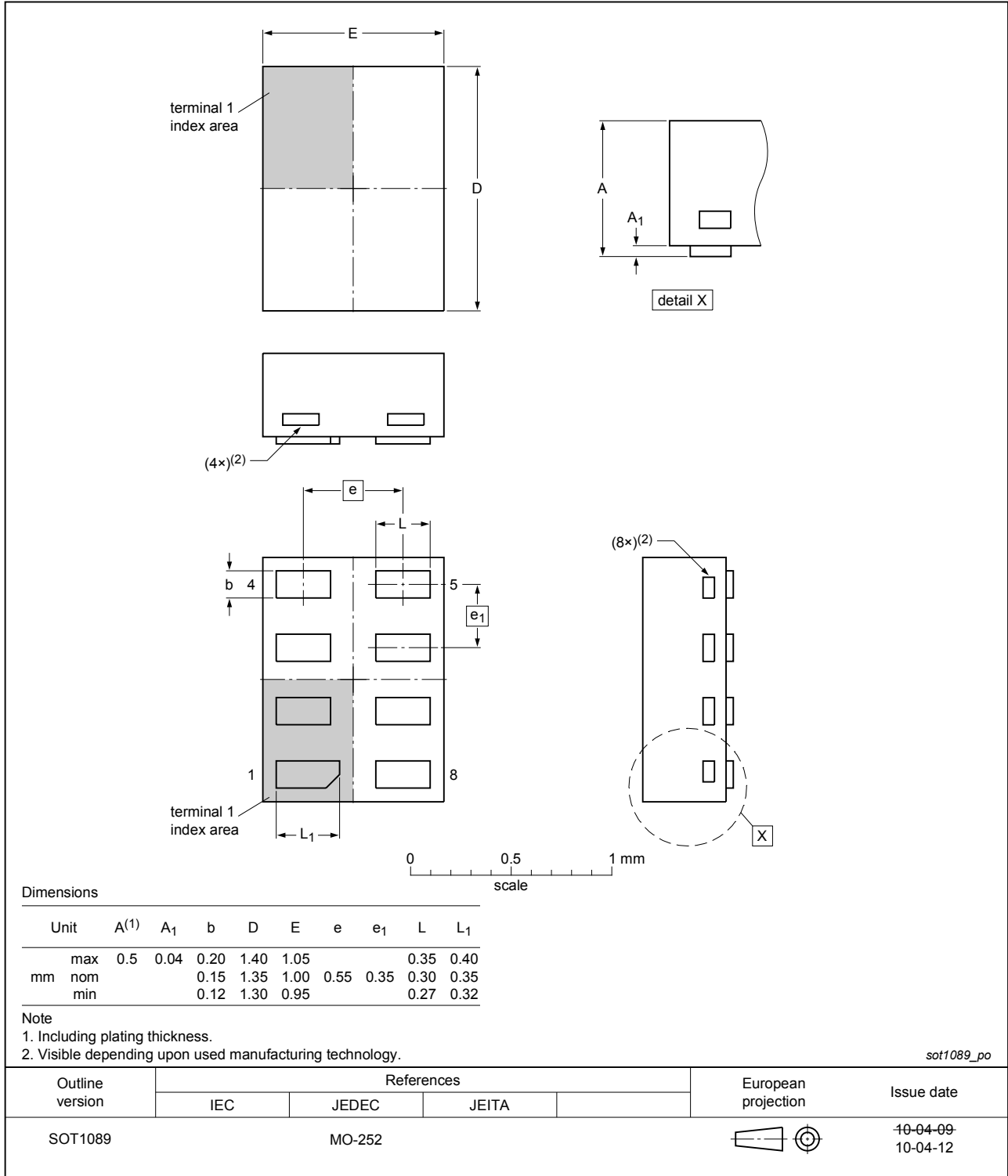
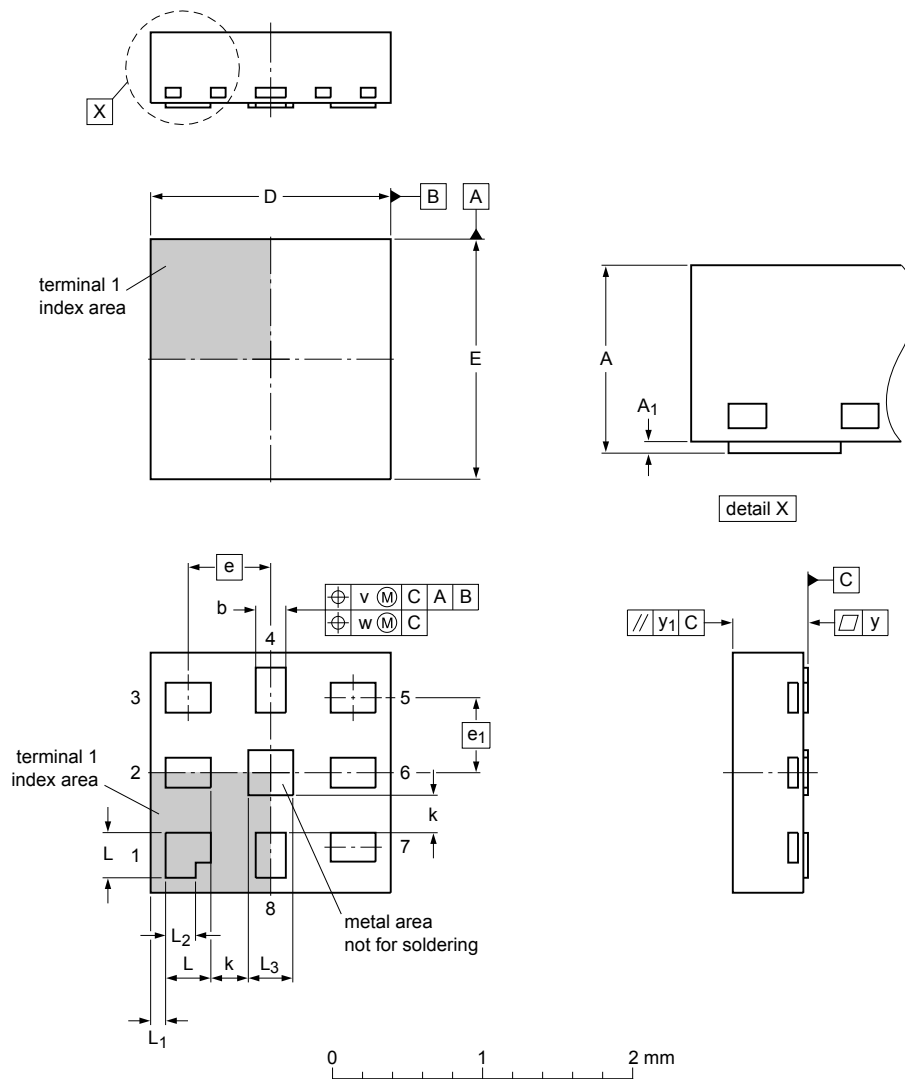


Fig. 12. Package outline SOT1089 (XSON8)

XQFN8: plastic, extremely thin quad flat package; no leads;
8 terminals; body 1.6 x 1.6 x 0.5 mm

SOT902-2



Dimensions

Unit ⁽¹⁾	A	A ₁	b	D	E	e	e ₁	k	L	L ₁	L ₂	L ₃	v	w	y	y ₁
max	0.5	0.05	0.25	1.65	1.65				0.35	0.15	0.25	0.35				
mm	nom		0.20	1.60	1.60	0.55	0.5		0.30	0.10	0.20	0.30	0.1	0.05	0.05	0.05
min		0.00	0.15	1.55	1.55			0.2	0.25	0.05	0.15	0.25				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

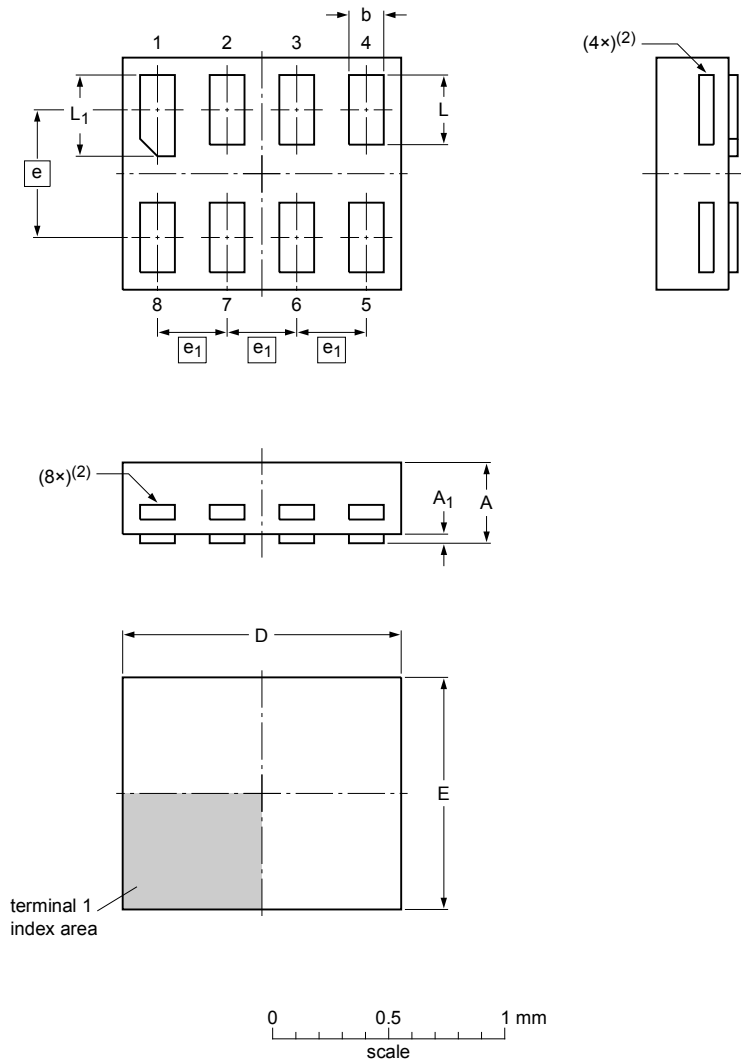
sot902-2_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT902-2	---	MO-255	---		16-07-14 16-11-08

Fig. 13. Package outline SOT902-2 (XQFN8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max 0.35	0.04	0.20	1.25	1.05			0.35	0.40
	nom		0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min		0.12	1.15	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

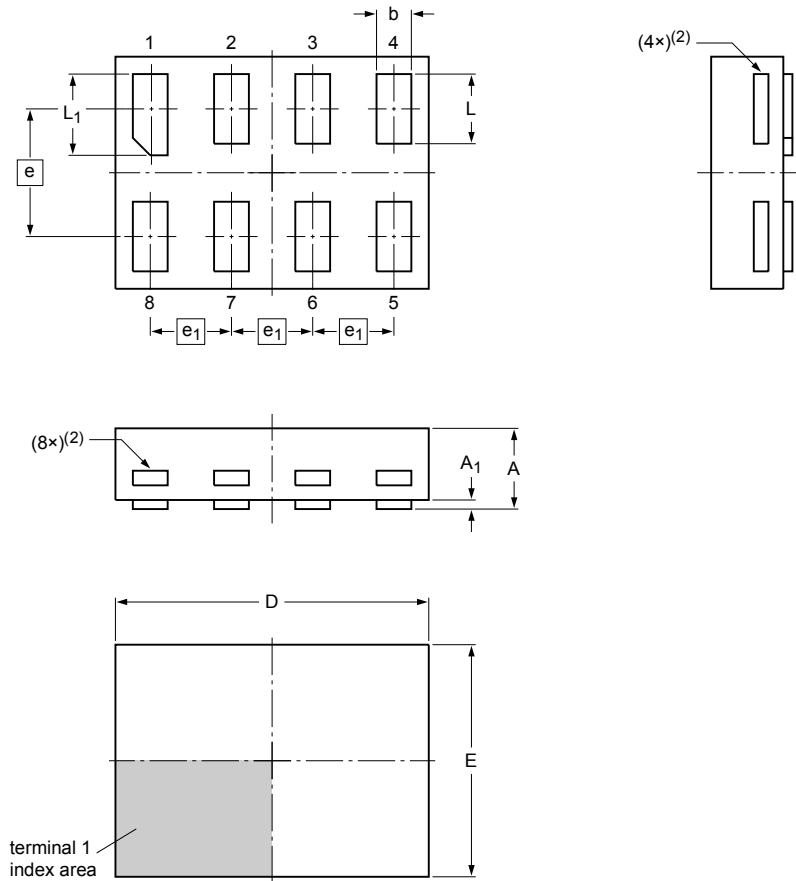
sot1116_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1116					10-04-02 10-04-07

Fig. 14. Package outline SOT1116 (XSON8)

**XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm**

SOT1203



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max 0.35	0.04	0.20	1.40	1.05			0.35	0.40
	nom		0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min		0.12	1.30	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						-10-04-02- 10-04-06

Fig. 15. Package outline SOT1203 (XSON8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G80 v.10	20181119	Product data sheet	-	74AUP2G80 v.9
Modifications:	<ul style="list-style-type: none"> Type number 74AUP2G80GD (SOT996-2/XSON8) removed. 			
74AUP2G80 v.9	20170818	Product data sheet	-	74AUP2G80 v.8
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74AUP2G80 v.8	20130121	Product data sheet	-	74AUP2G80 v.7
Modifications:	<ul style="list-style-type: none"> For type number 74AUP2G80GD XSON8U has changed to XSON8. 			
74AUP2G80 v.7	20120614	Product data sheet	-	74AUP2G80 v.6
74AUP2G80 v.6	20111207	Product data sheet	-	74AUP2G80 v.5
74AUP2G80 v.5	20101005	Product data sheet	-	74AUP2G80 v.4
74AUP2G80 v.4	20080602	Product data sheet	-	74AUP2G80 v.3
74AUP2G80 v.3	20080328	Product data sheet	-	74AUP2G80 v.2
74AUP2G80 v.2	20070801	Product data sheet	-	74AUP2G80 v.1
74AUP2G80 v.1	20060825	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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