

Silicon carbide Power MOSFET 1200 V, 45 A, 90 mΩ (typ., $T_J = 150\text{ }^\circ\text{C}$), in an HiP247™ long leads package

Datasheet - production data

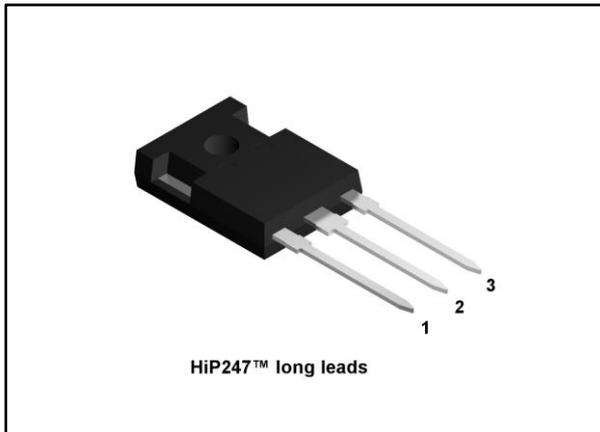
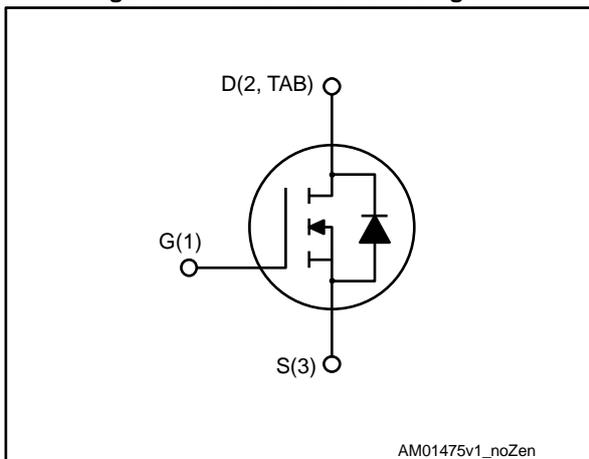


Figure 1: Internal schematic diagram



Features

- Very tight variation of on-resistance vs. temperature
- Very high operating junction temperature capability ($T_J = 200\text{ }^\circ\text{C}$)
- Very fast and robust intrinsic body diode
- Low capacitance

Applications

- Solar inverters, UPS
- Motor drives
- High voltage DC-DC converters
- Switch mode power supply

Description

This silicon carbide Power MOSFET is produced exploiting the advanced, innovative properties of wide bandgap materials. This results in unsurpassed on-resistance per unit area and very good switching performance almost independent of temperature. The outstanding thermal properties of the SiC material allow designers to use an industry-standard outline with significantly improved thermal capability. These features render the device perfectly suitable for high-efficiency and high power density applications.

Table 1: Device summary

Order code	Marking	Package	Packaging
SCTWA30N120	SCT30N120	HiP247™ long leads	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1200	V
V_{GS}	Gate-source voltage	-10 to 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$ (limited by die)	45	A
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$ (limited by package)	40	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	34	A
$I_{DM}^{(1)}$	Drain current (pulsed)	90	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	270	W
T_{stg}	Storage temperature range	-55 to 200	°C
T_j	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.65	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb	40	°C/W

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 1200\text{ V}$		1	25	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 1200\text{ V}$, $T_{\text{J}} = 200\text{ °C}$		50		μA
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = -10\text{ to }22\text{ V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 1\text{ mA}$	1.8	3.5		V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 20\text{ V}$, $I_{\text{D}} = 20\text{ A}$		80	100	m Ω
		$V_{\text{GS}} = 20\text{ V}$, $I_{\text{D}} = 20\text{ A}$ $T_{\text{J}} = 150\text{ °C}$		90		m Ω
		$V_{\text{GS}} = 20\text{ V}$, $I_{\text{D}} = 20\text{ A}$ $T_{\text{J}} = 200\text{ °C}$		100		m Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 400\text{ V}$, $f = 1\text{ MHz}$	-	1700	-	pF
C_{oss}	Output capacitance		-	130	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	5	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 800\text{ V}$, $I_{\text{D}} = 20\text{ A}$ $V_{\text{GS}} = 0\text{ to }20\text{ V}$	-	105	-	nC
Q_{gs}	Gate-source charge		-	16	-	nC
Q_{gd}	Gate-drain charge		-	40	-	nC

Table 6: Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
E_{on}	Turn-on switching energy	$V_{\text{DD}} = 800\text{ V}$, $I_{\text{D}} = 20\text{ A}$, $R_{\text{G}} = 6.8\text{ }\Omega$, $V_{\text{GS}} = -2\text{ to }20\text{ V}$	-	500	-	μJ
E_{off}	Turn-off switching energy		-	350	-	μJ
E_{on}	Turn-on switching energy	$V_{\text{DD}} = 800\text{ V}$, $I_{\text{D}} = 20\text{ A}$, $R_{\text{G}} = 6.8\text{ }\Omega$, $V_{\text{GS}} = -2\text{ to }20\text{ V}$ $T_{\text{J}} = 150\text{ °C}$	-	500	-	μJ
E_{off}	Turn-off switching energy		-	400	-	μJ

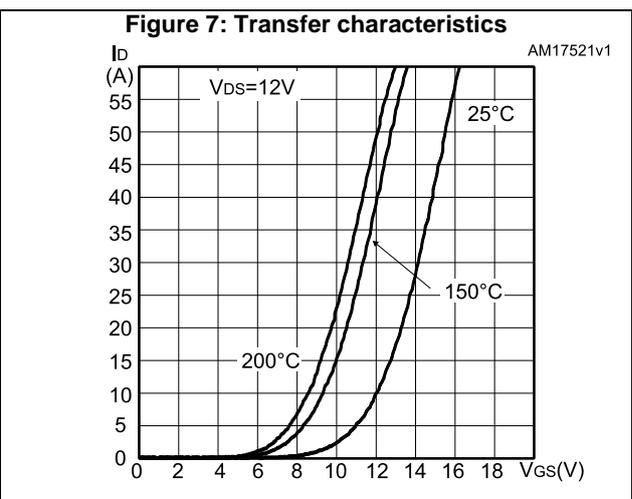
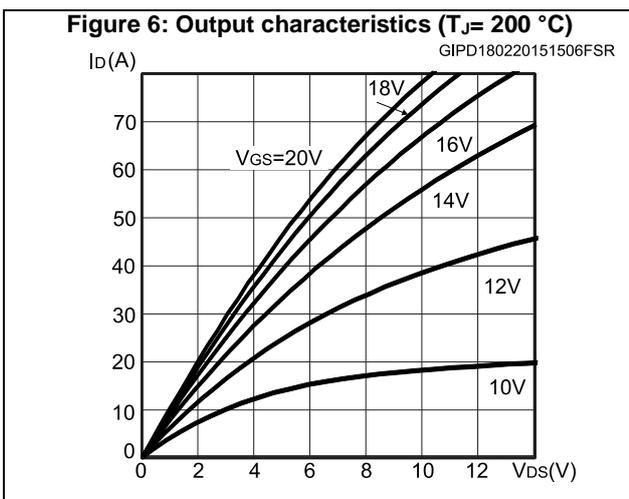
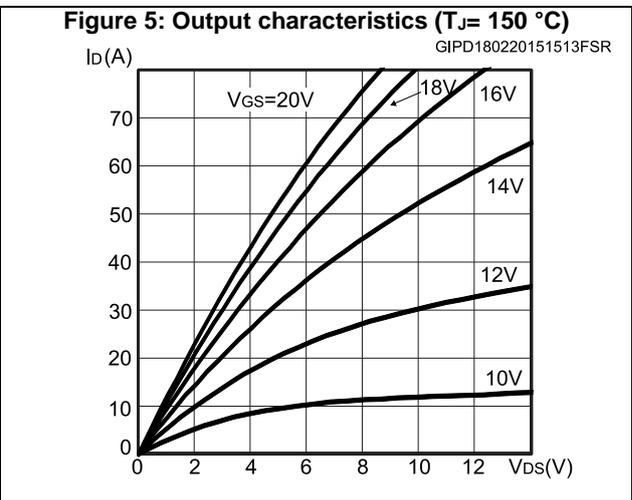
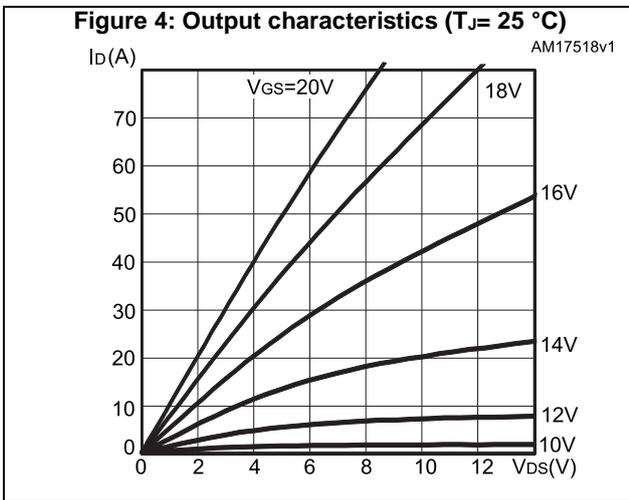
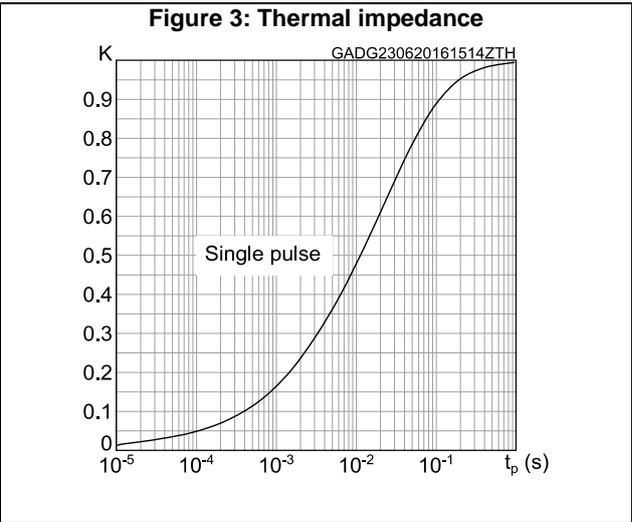
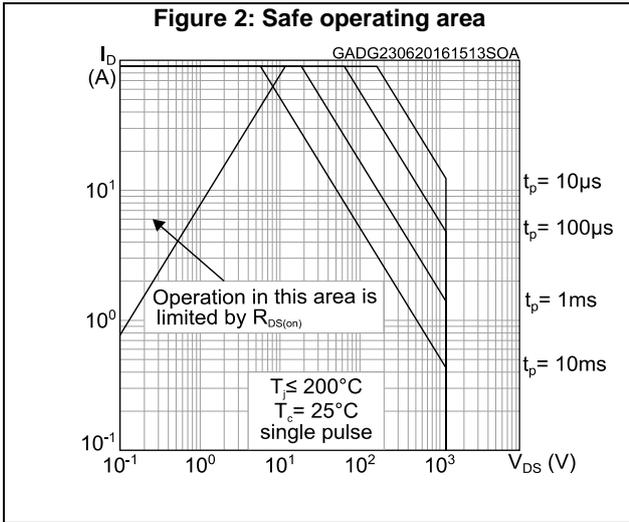
Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{\text{d(on)V}}$	Turn-on delay time	$V_{\text{DD}} = 800\text{ V}$, $I_{\text{D}} = 20\text{ A}$, $R_{\text{G}} = 0\text{ }\Omega$, $V_{\text{GS}} = 0\text{ to }20\text{ V}$	-	19	-	ns
$t_{\text{f(V)}}$	Fall time		-	28	-	ns
$t_{\text{d(off)V}}$	Turn-off-delay time		-	45	-	ns
$t_{\text{r(V)}}$	Rise time		-	20	-	ns

Table 8: Reverse SiC diode characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
V_{SD}	Diode forward voltage	$I_F = 10\text{ A}$, $V_{GS} = 0\text{ V}$	-	3.5	-	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 800\text{ V}$	-	140	-	ns
Q_{rr}	Reverse recovery charge		-	140	-	nC
I_{RRM}	Reverse recovery current		-	2	-	A

2.1 Electrical characteristics (curves)



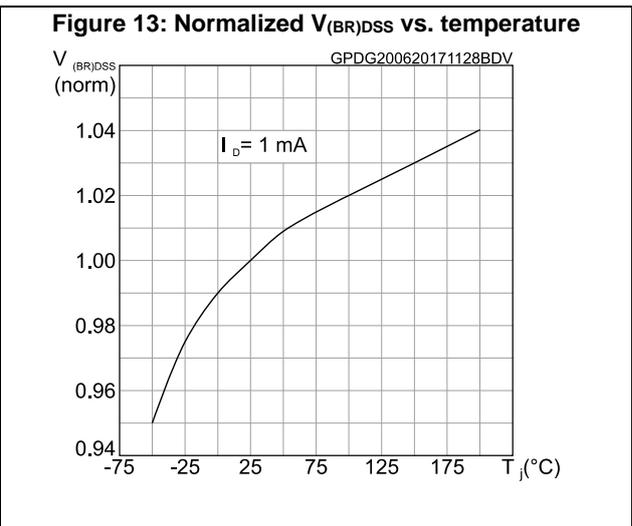
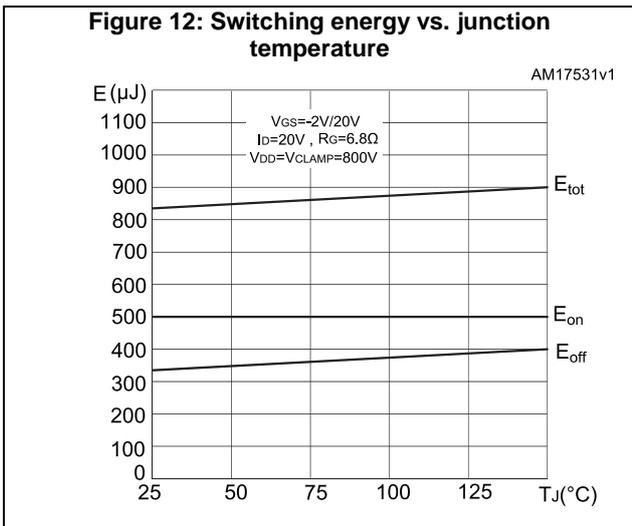
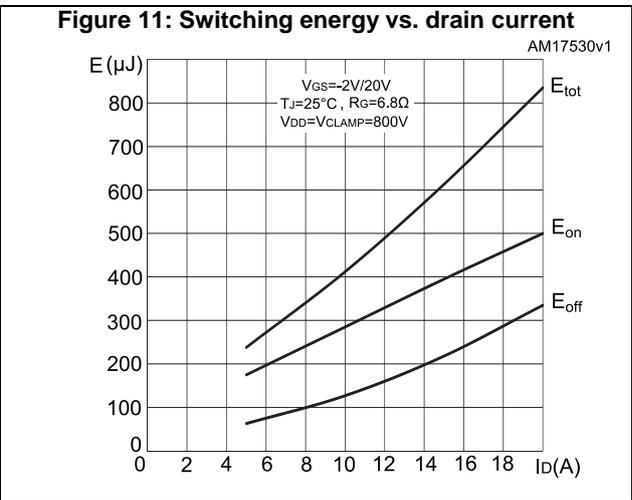
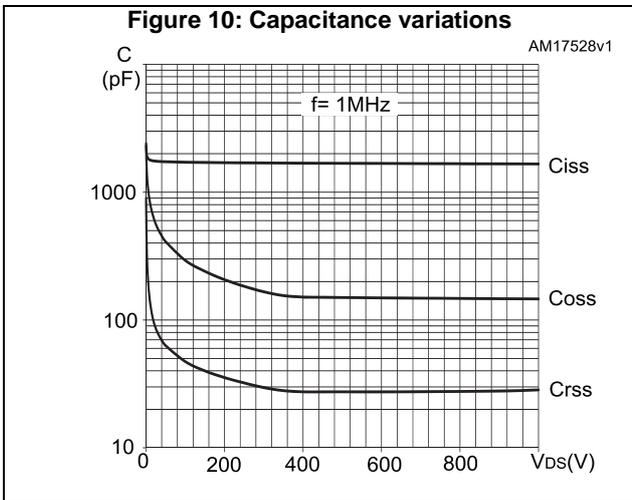
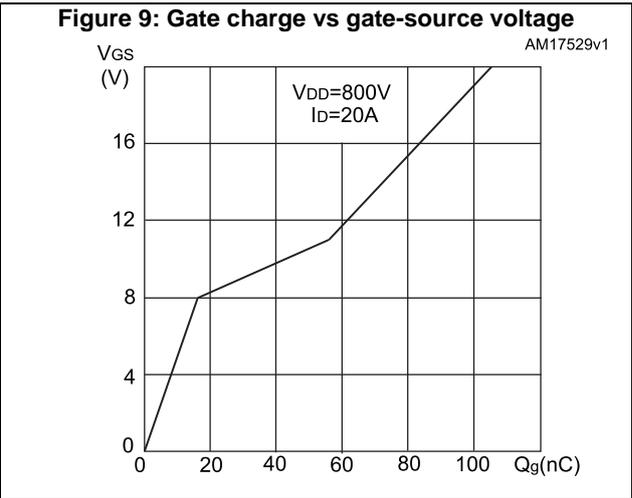
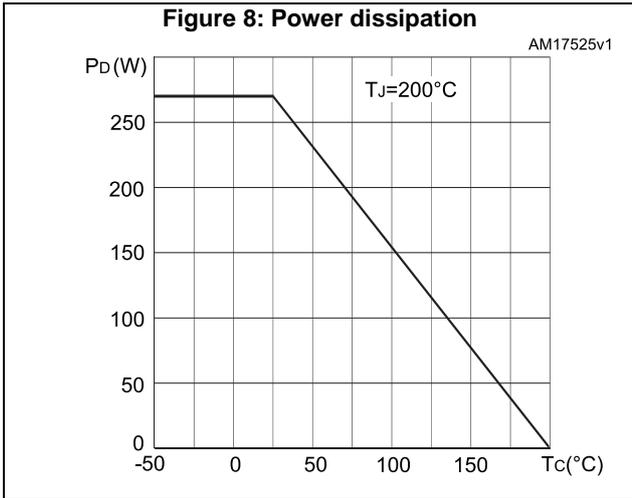


Figure 14: Normalized gate threshold voltage vs. temperature

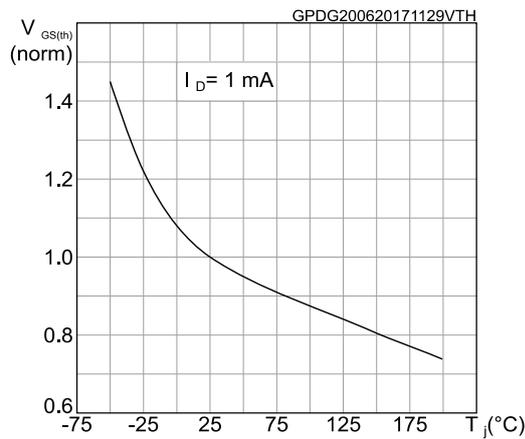


Figure 15: Normalized on-resistance vs. temperature

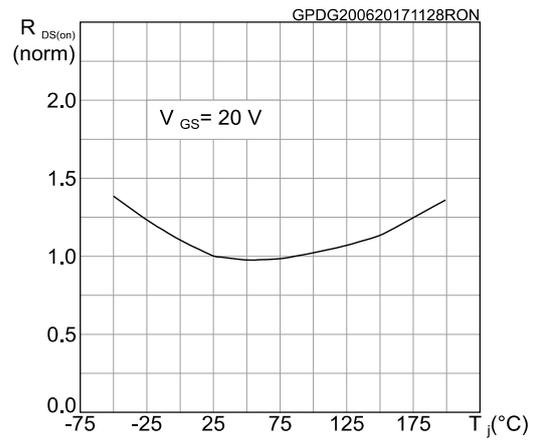


Figure 16: Body diode characteristics ($T_J = -50 \text{ }^\circ\text{C}$)

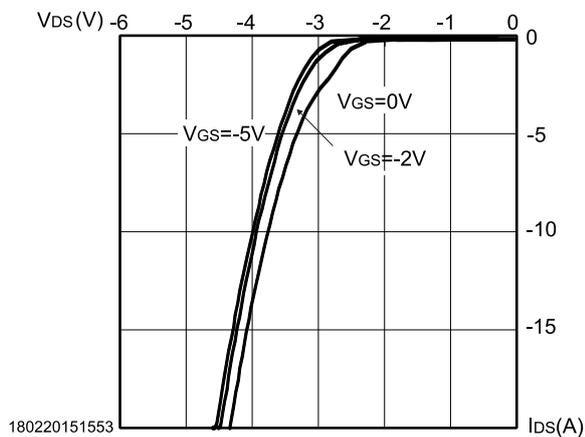


Figure 17: Body diode characteristics ($T_J = 25 \text{ }^\circ\text{C}$)

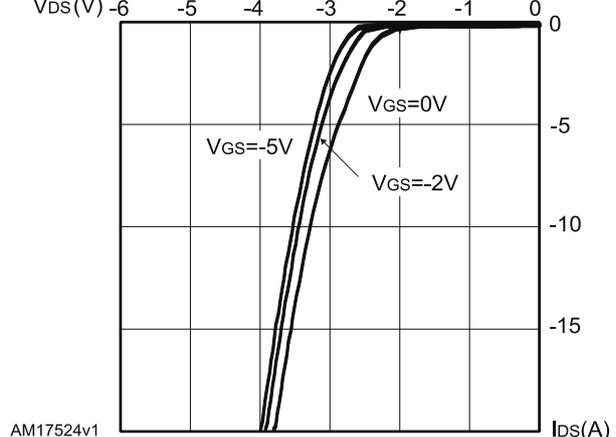


Figure 18: Body diode characteristics ($T_J = 150 \text{ }^\circ\text{C}$)

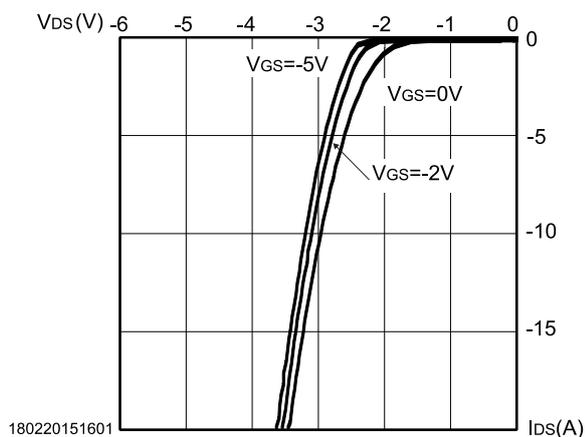


Figure 19: 3rd quadrant characteristics ($T_J = -50 \text{ }^\circ\text{C}$)

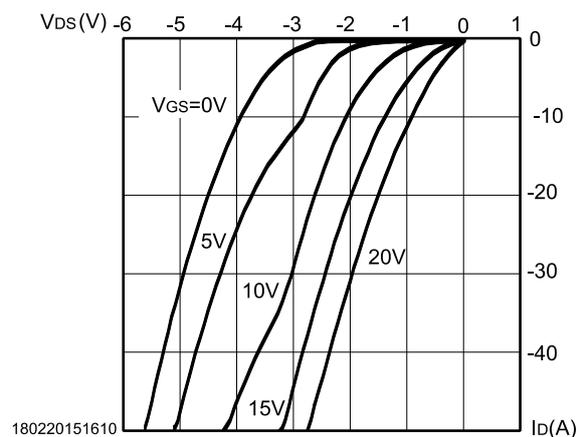


Figure 20: 3rd quadrant characteristics ($T_J = 25\text{ }^\circ\text{C}$)

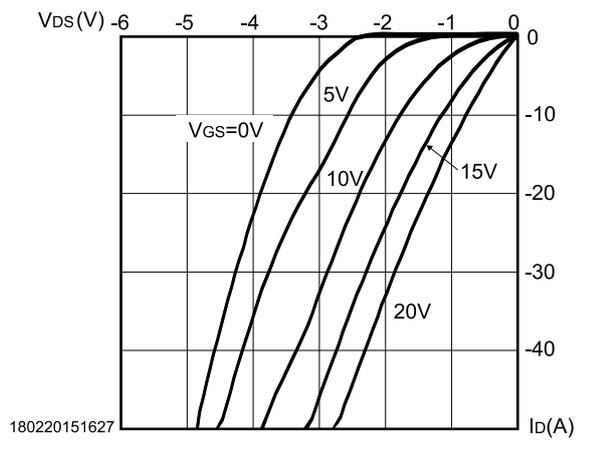
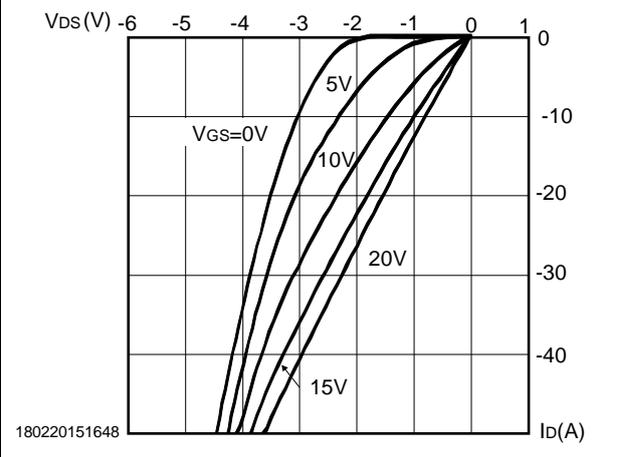


Figure 21: 3rd quadrant characteristics ($T_J = 150\text{ }^\circ\text{C}$)



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

3.1 HiP247 long leads package information

Figure 22: HiP247™ long leads package outline

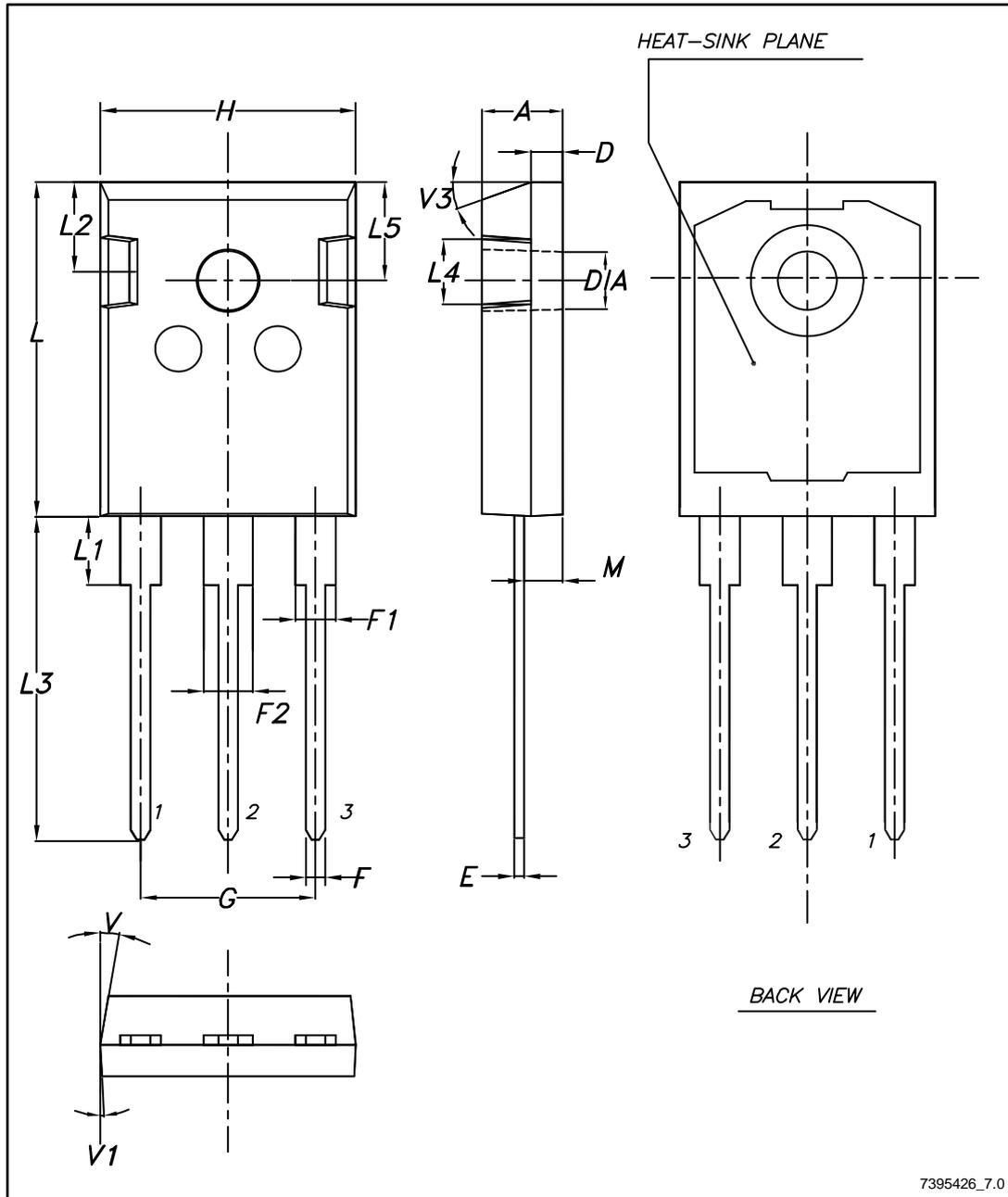


Table 9: HiP247™ long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90		5.15
D	1.85		2.10
E	0.55		0.67
F	1.07		1.32
F1	1.90		2.38
F2	2.87		3.38
G	10.90 BSC		
H	15.77		16.02
L	20.82		21.07
L1	4.16		4.47
L2	5.49		5.74
L3	20.05		20.30
L4	3.68		3.93
L5	6.04		6.29
M	2.25		2.55
V		10°	
V1		3°	
V3		20°	
DIA	3.55		3.66

4 Revision history

Table 10: Document revision history

Date	Revision	Changes
11-Jan-2016	1	First release.
19-Jun-2017	2	Updated title, features in cover page. Minor text edit in <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Updated <i>Figure 2: "Safe operating area"</i> , <i>Figure 3: "Thermal impedance"</i> , <i>Figure 13: "Normalized V(BR)DSS vs. temperature"</i> , <i>Figure 14: "Normalized gate threshold voltage vs. temperature"</i> and <i>Figure 15: "Normalized on-resistance vs. temperature"</i> . Document status promoted from preliminary to production data.

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