

## 1. General description

Planar passivated high commutation three quadrant triac in a SOT186A (TO-220F) "full pack" plastic package intended for use in circuits where high static and dynamic  $dV/dt$  and high  $dI/dt$  can occur. This "series BT" triac will commute the full RMS current at the maximum rated junction temperature ( $T_{j(max)} = 150\text{ °C}$ ) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

## 2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by  $dV/dt$
- High junction operating temperature capability
- High voltage capability
- Isolated mounting base package
- Least sensitive gate for highest noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only

## 3. Applications

- Applications subject to high temperature
- Heating controls
- High power motor control
- High power switching

## 4. Quick reference data

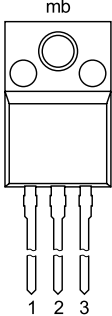
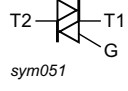
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage			-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 50\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>		-	-	20	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>		-	-	200	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$		-	-	220	A
$T_j$	junction temperature			-	-	150	°C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics</b>							
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	-	50	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	-	50	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	-	50	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>		-	-	60	mA
$V_T$	on-state voltage	$I_T = 24\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>		-	1.2	1.5	V
<b>Dynamic characteristics</b>							
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$ ; $T_j = 150\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit		1800	-	-	V/ $\mu\text{s}$
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}$ ; $T_j = 150\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 20\text{ A}$ ; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$ ; gate open circuit		25	-	-	A/ms
		$V_D = 400\text{ V}$ ; $T_j = 150\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 20\text{ A}$ ; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$ ; gate open circuit		65	-	-	A/ms

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

## 6. Ordering information

Table 3. Ordering information

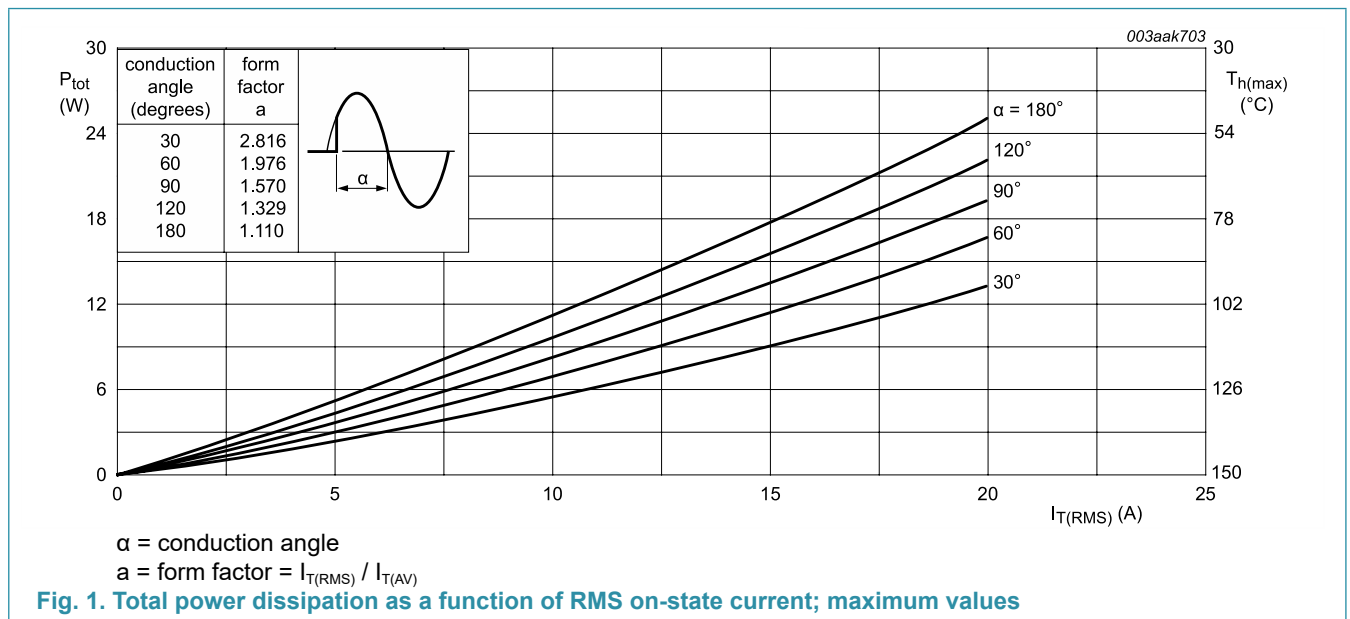
Type number	Package		
	Name	Description	Version
BTA420X-800BT	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{\text{DRM}}$	repetitive peak off-state voltage			-	800	V
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_h \leq 50\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>		-	20	A
$I_{\text{TSM}}$	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig 4</a> ; <a href="#">Fig 5</a>		-	200	A
		full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 16.7\text{ ms}$		-	220	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; sine-wave pulse		-	200	$\text{A}^2\text{s}$
$di_{\text{T}}/dt$	rate of rise of on-state current	$I_G = 100\text{ mA}$		-	100	$\text{A}/\mu\text{s}$
$I_{\text{GM}}$	peak gate current			-	2	A
$P_{\text{GM}}$	peak gate power			-	5	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period		-	0.5	W
$T_{\text{stg}}$	storage temperature			-40	150	$^{\circ}\text{C}$
$T_{\text{j}}$	junction temperature			-	150	$^{\circ}\text{C}$



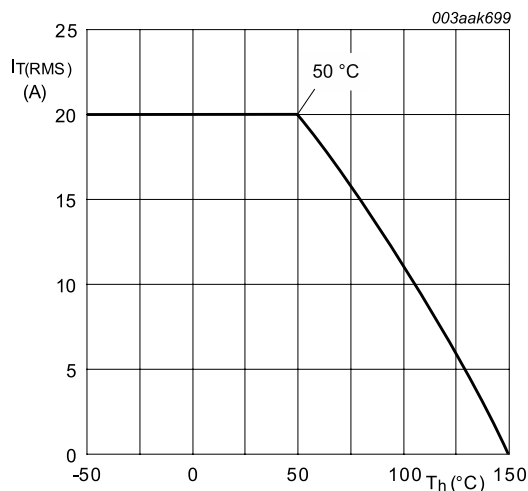
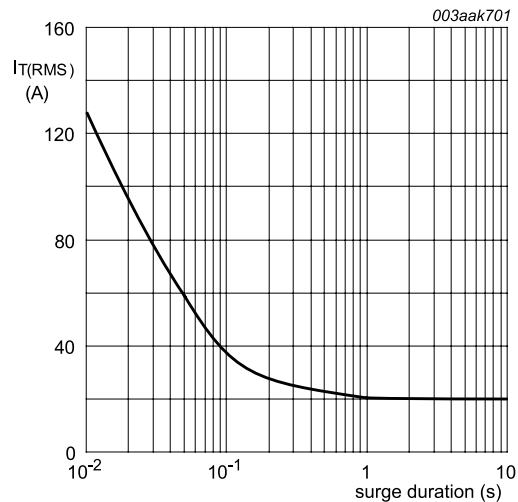
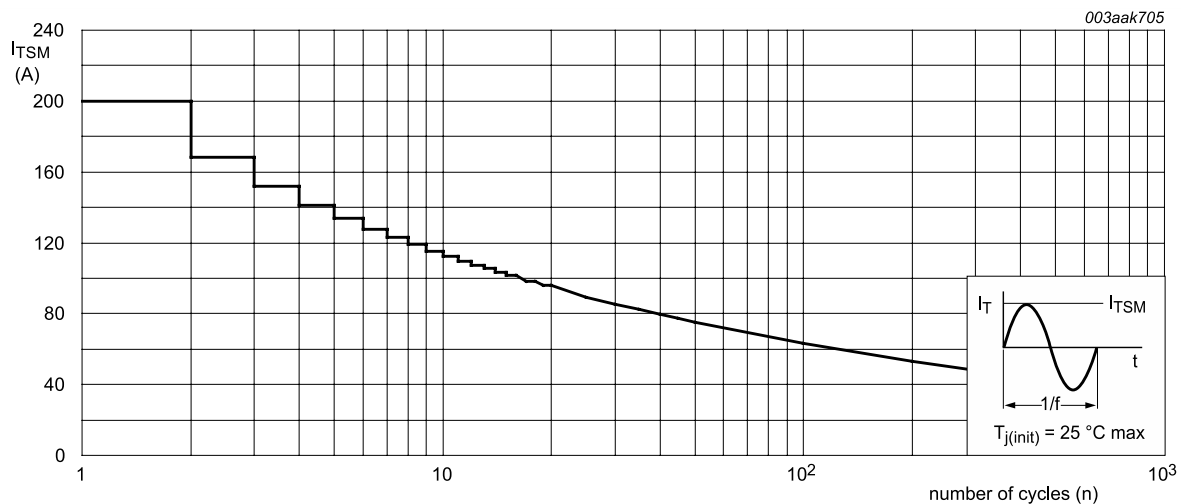


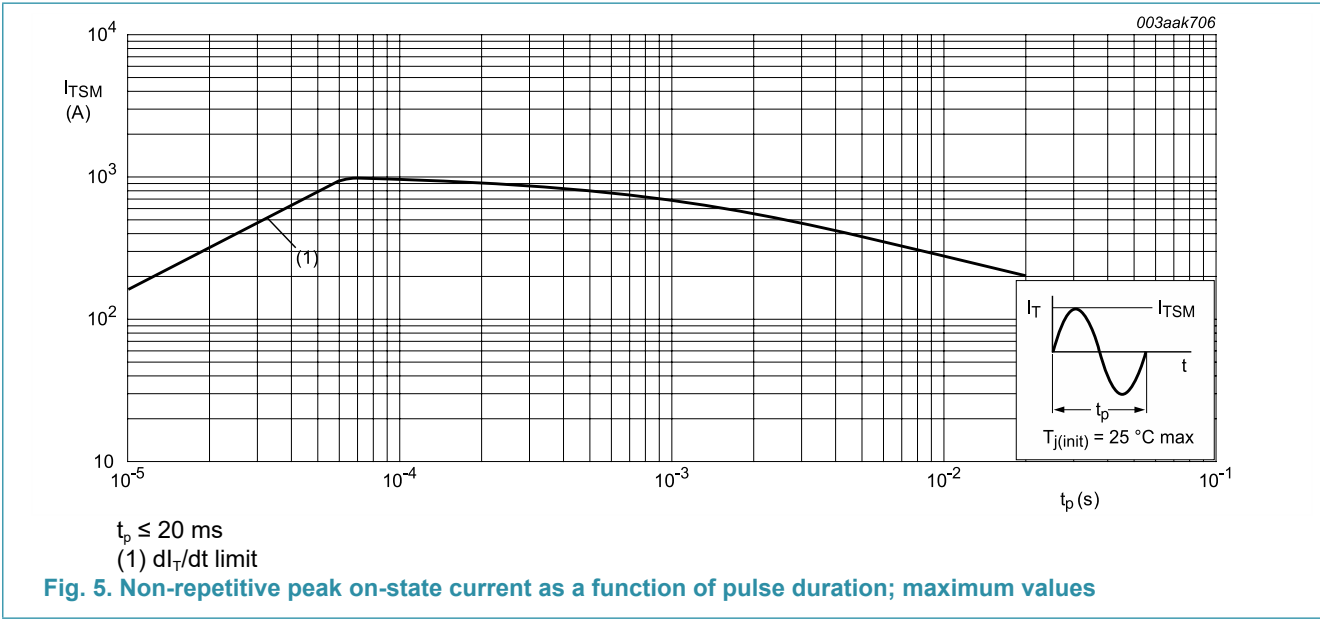
Fig. 2. RMS on-state current as a function of heatsink temperature; maximum values



$f = 50 \text{ Hz}; T_h = 50 \text{ °C}$   
Fig. 3. RMS on-state current as a function of surge duration; maximum values



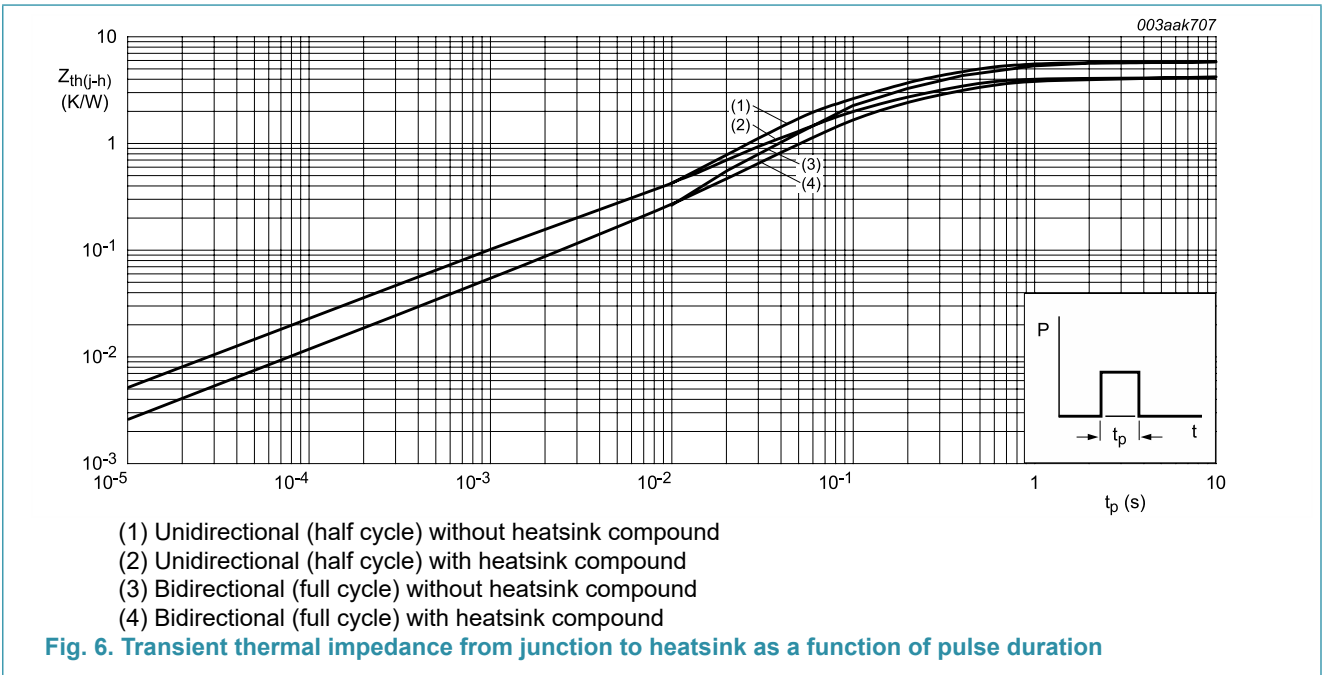
$f = 50 \text{ Hz}$   
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full cycle or half cycle; with heatsink compound; Fig. 6	-	-	4	K/W
		full cycle or half cycle; without heatsink compound; Fig. 6	-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W



9. Isolation characteristics

Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz $\leq f \leq$ 60 Hz; RH $\leq$ 65 %; $T_h = 25\text{ }^{\circ}\text{C}$	-	-	2500	V
$C_{isol}$	isolation capacitance	from main terminal 2 to external heatsink; $f = 1\text{ MHz}$ ; $T_h = 25\text{ }^{\circ}\text{C}$	-	10	-	pF

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Static characteristics</b>							
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	-	50	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	-	50	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>		-	-	50	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>		-	-	60	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>		-	-	90	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>		-	-	60	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>		-	-	60	mA
$V_T$	on-state voltage	$I_T = 24\text{ A}$ ; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>		-	1.2	1.5	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $T_J = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>		-	0.7	1	V
		$V_D = 400\text{ V}$ ; $T_J = 150\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>		0.2	0.4	-	V
$I_D$	off-state current	$V_D = 800\text{ V}$ ; $T_J = 150\text{ }^\circ\text{C}$		-	0.2	1	mA
<b>Dynamic characteristics</b>							
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$ ; $T_J = 150\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit		1800	-	-	V/ $\mu\text{s}$
$dI_{com}/dt$	rate of change of commutating current	$V_D = 400\text{ V}$ ; $T_J = 150\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 20\text{ A}$ ; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$ ; gate open circuit		25	-	-	A/ms
		$V_D = 400\text{ V}$ ; $T_J = 150\text{ }^\circ\text{C}$ ; $I_{T(RMS)} = 20\text{ A}$ ; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$ ; gate open circuit		65	-	-	A/ms

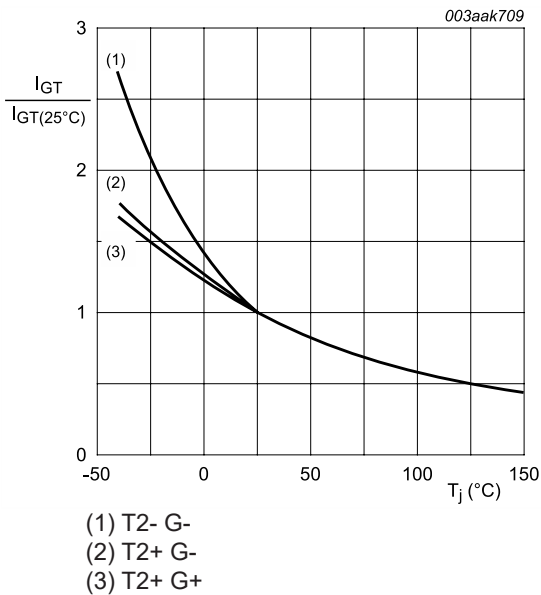


Fig. 7. Normalized gate trigger current as a function of junction temperature

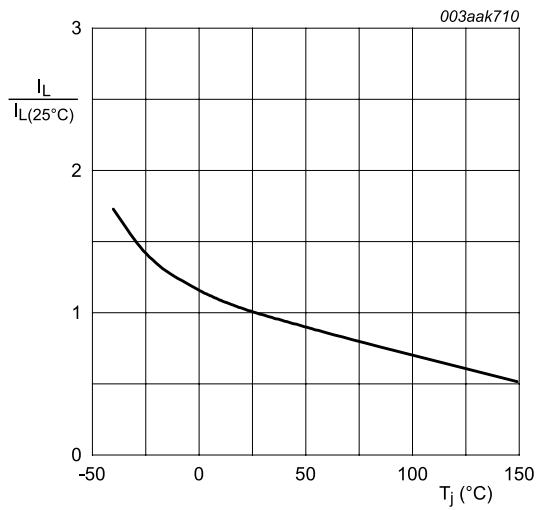


Fig. 8. Normalized latching current as a function of junction temperature

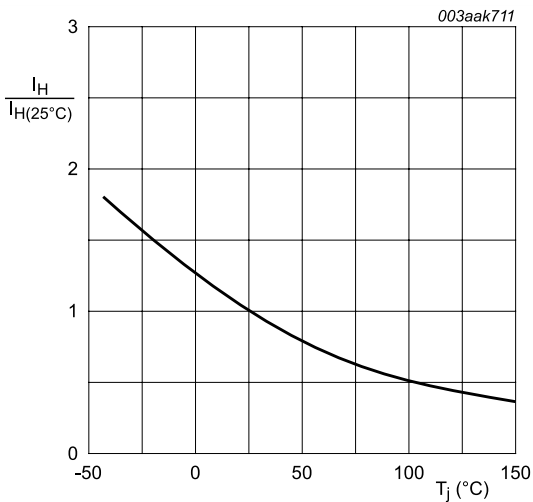


Fig. 9. Normalized holding current as a function of junction temperature

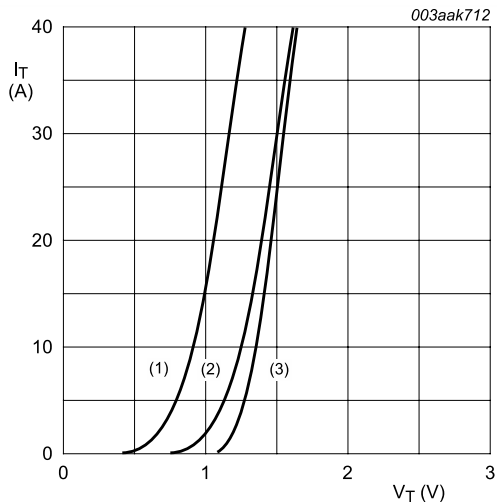


Fig. 10. On-state current as a function of on-state voltage



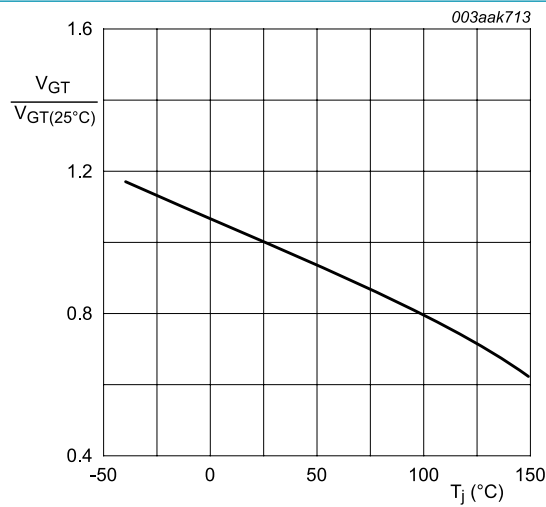
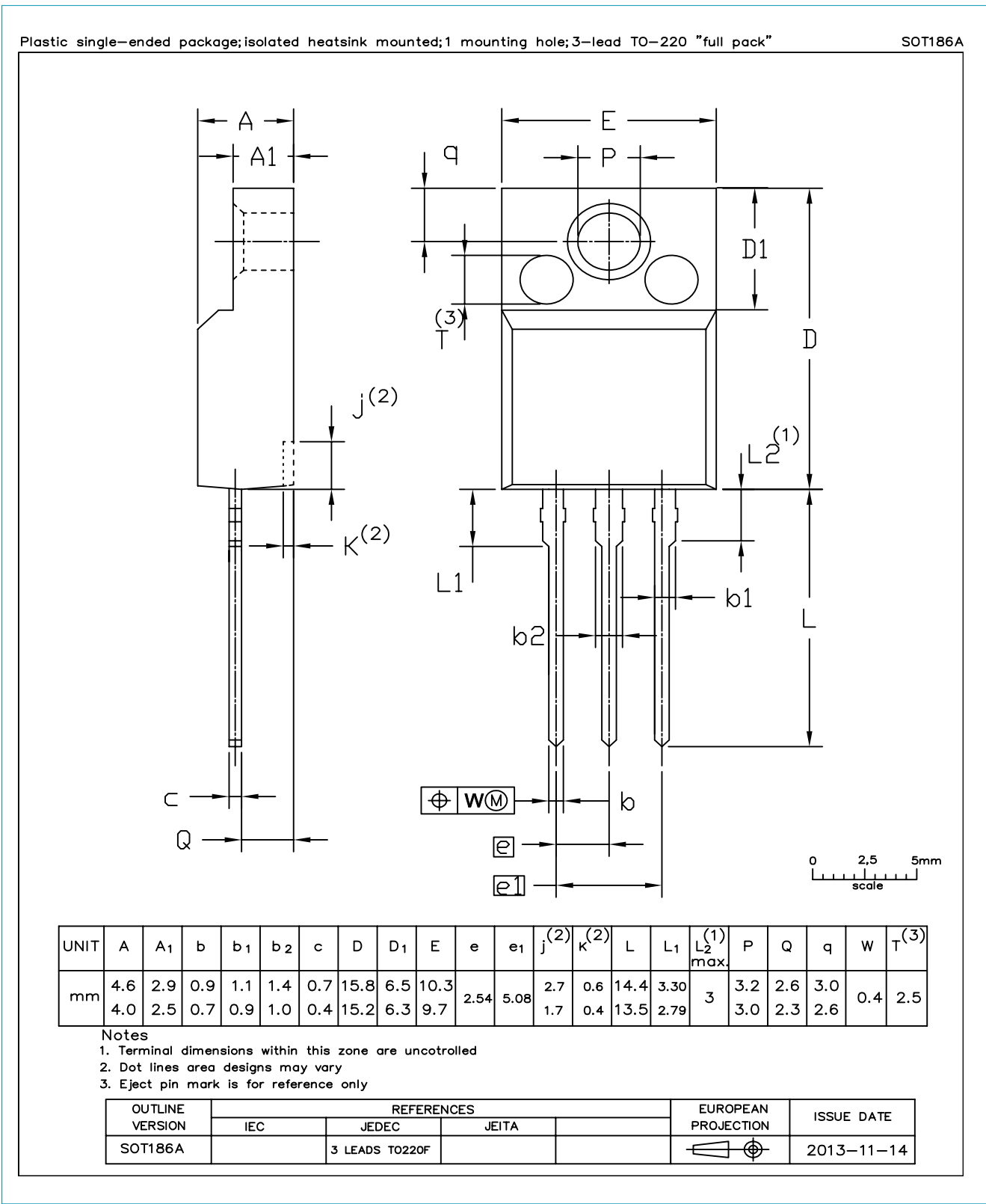


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline



## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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13. Contents

1. General description..... 1

2. Features and benefits ..... 1

3. Applications ..... 1

4. Quick reference data ..... 1

5. Pinning information..... 2

6. Ordering information..... 2

7. Limiting values ..... 3

8. Thermal characteristics ..... 6

9. Isolation characteristics ..... 6

10. Characteristics..... 7

11. Package outline ..... 10

12. Legal information ..... 11

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