EIGHT CHANNEL HD AUDIO CODEC 92HD73D1

PREMIUM WLP 3/4 COMPLIANT

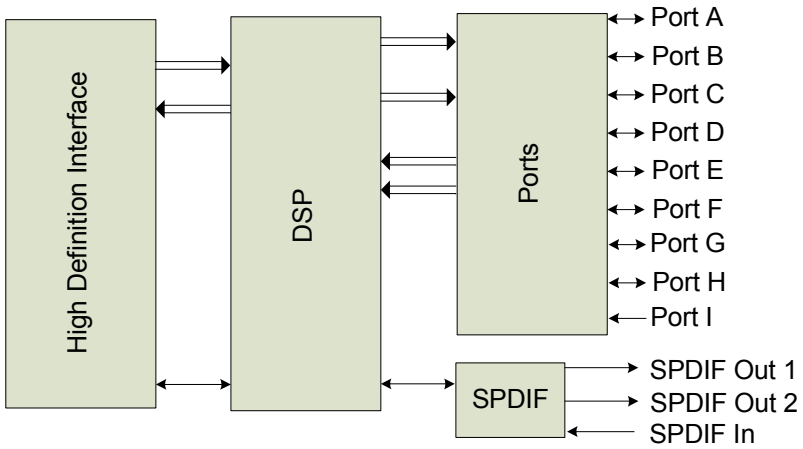
Description

The 92HD73D codec is a low power optimized, high fidelity, 8-channel audio codec compatible with Intel's High Definition (HD) Audio Interface. The 92HD73D codec provides stereo 24-bit resolution with sample rates up to 192kHz. Dual SPDIF provides connectivity to consumer electronic equipment that is WLP compliant. The 92HD73D provides high quality, HD Audio capability to multimedia notebook and desktop PC applications.

Features

- **8 Channels (4 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
  - Supports 7.1 audio
  - Supports full-duplex 5.1 audio and simultaneous VoIP
- **Microsoft WLP 3/4 premium logo compliant, as defined in WLP 3.09**
- **Optimized and flexible power management with pop/click mitigation**
- **2 independent S/PDIF Output converters for WLP compliant HDMI/SPDIF support.**
- **Support for 1.5V and 3.3V HDA signaling with runtime selection**
- **Digital microphone input (mono, stereo, or quad array)**
- **4 adjustable VREF Out pins for microphone bias**
- **High performance analog mixer**
- **9 stereo analog ports with presence detect capability**
- **Two-pin volume up/down control**
- **Digital and Analog PC Beep to all outputs**
- **Integrated headphone amps (3)**
- **Sample rates up to 192kHz**
- **+3.3 V, +4 V, +4.75 V and +5 V analog power supply options**
- **Package Options**
  - 48-pin QFP RoHS package
  - 48-pin QFP RoHS package INDUSTRIAL TEMP

Block Diagram



Software Support

- Intuitive graphical user interface that allows configurability and preference settings
- SKPI (Kernel Processing Interface)
  - Enables plug-ins that can operate globally on all audio streams of the system
- 12 band fully parametric equalizer (SKPI plug-in)
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- Dynamics Processing (SKPI plug-in)
  - Enables improved voice articulation
  - Compressor/limiter allows higher average noise level without resonances or damage to speakers.
- IDT Vista APO wrapper
  - Enables multiple APOs to be used with the IDT Driver
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- Dynamic Stream Switching
  - Improved multi-streaming user experience with less support calls
- Dolby PC Entertainment Experience Logo Program
  - Dolby Master Studio ™ (MS)
  - Dolby Home Theater™ (HT)
  - Dolby Sound Room™ (SR)
- Dolby Technologies
  - Dolby Headphone™, Dolby Virtual Speaker™
  - Dolby ProLogic II™, Dolby ProLogic IIx™
  - Dolby Digital Live™ (DDL)
- Maxx Player™ from Waves
- WOW™ and Tru Surround™ from SRS

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1. DESCRIPTION

1.1. Overview

The 92HD73D1 is a high fidelity, 8-channel audio codec compatible with the Intel High Definition (HD) Audio Interface. The 92HD73D1 codec provides high quality, HD Audio capability to desktop and multi-media notebook.

The 92HD73D1 is designed to meet or exceed premium logo requirements for Microsoft's Windows Logo Program (WLP) 3.09 and revisions 4 as indicated in WLP 3.09.

The 92HD73D1 provides stereo 24-bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. 92HD73D1 SPDIF outputs support sample rates of 192kHz, 176.4kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz. 92HD73D1 SPDIF input supports sample rates of 96kHz, 88.2kHz, 48kHz, and 44.1kHz. Additional sample rates are supported by the driver software.

The 92HD73D1 supports a wide range of desktop and consumer 8 channel configurations. The 2 independent SPDIF output interfaces provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. Simultaneous HDMI and SPDIF output is possible.

MIC inputs can be programmed with 0/10/20/30dB boost. For more advanced configurations, the 92HD73D1 has 8 General Purpose I/O (GPIO).

The port presence detect capabilities allow the codecs to detect when audio devices are connected to the codec. Load impedance sensing helps identify attached peripherals for easy set-up and a better user experience. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD73D1 operates with a 3.3V digital supply and either 3.3V, or 5V analog supply. It can also work with 1.5V and 3.3V HDA signaling; the correct signalling level is selected dynamically based on the power supply voltage on the DVDD-IO pin.

The 92HD73D1X is available in a 48-pin LQFP Environmental (ROHS) package.

The 92HD73D1T is available in a 48-pin LQFP Environmental (ROHS) INDUSTRIAL temperature package.

Additional products with the same features as the 92HD73D are the 10-channel 92HD73E and the 6-channel 92HD73C.

1.2. Orderable Part Numbers

92HD73D1X5PRGXyyX	8 channel, 5V, 48QFP
92HD73D1T5PRGIyyX	8 channel, 5V, 48QFP, i-temp

yy = silicon stepping/revision, contact sales for current data.
Add an "8" to the end for tape and reel delivery. Min/Mult order quantity 2ku.
Contact IDT if interested in 3.3V Analog version.

1.3. Block Diagram

Figure 1. 92HD73D1 Block Diagram

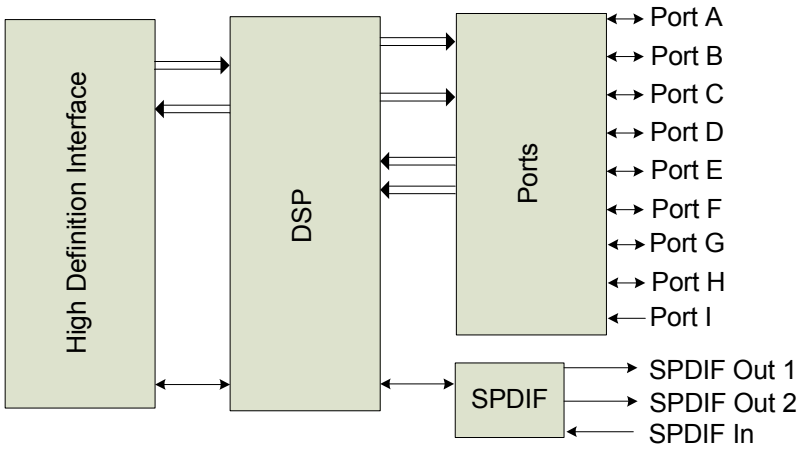
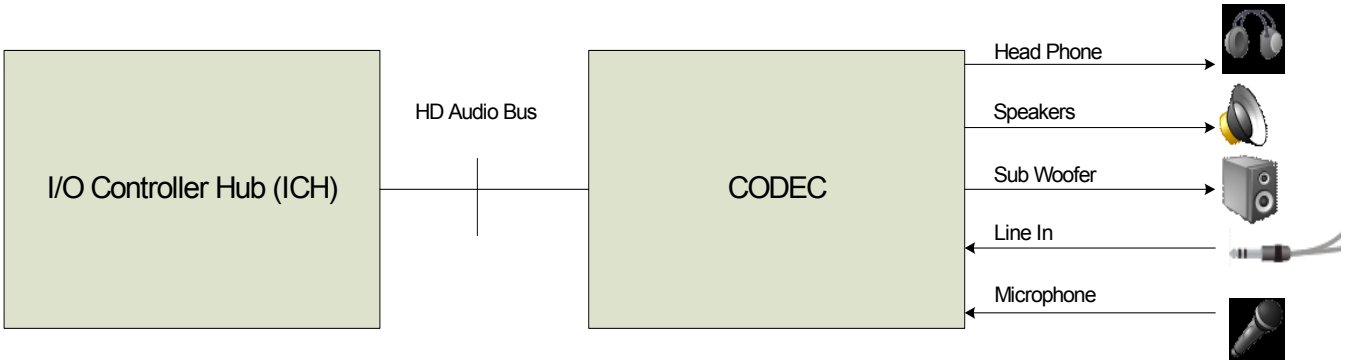


Figure 2. System Diagram



1.4. Detailed Description

1.4.1. Port Functionality

Multi-function (Input / output) ports allow for the highest possible flexibility. 8 bi-directional ports (3 headphone capable) support a wide variety of consumer desktop and mobile system use models.

Pins	Port	Input	Output	Headphone	Mic Bias (Vref pin)	Input boost amp[1]	CD (pseudo differential)
39/41	A	Yes	Yes	Yes	Yes	Yes	
21/22	B	Yes	Yes	Yes	Yes	Yes	
23/24	C	Yes	Yes		Yes	Yes	
35/36	D	Yes	Yes	Yes		Yes	
14/15	E	Yes	Yes		Yes	Yes	
16/17	F	Yes	Yes			Yes	
43/44	G	Yes	Yes			Yes	
45/46	H	Yes	Yes			Yes	
18/19/20	CD (Port I)	Yes					Yes
48	SPDIF_OUT0		Yes				
40	SPDIF_OUT1		Yes				
47	SPDIF_IN	Yes					
4 (CLK=2)	DMIC0	Yes				Yes	
30 (CLK=2)	DMIC1	Yes				Yes	

Table 1. Port Functionality

Note[1]: 40dB boost requires using the IDT driver. When the 40dB mic boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB MIC boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

1.4.2. Port Characteristics

Universal (Bi-directional) jacks are supported on all ports except the CD input. Ports A, B, and D are designed to drive a set of 32 ohm (nominal) headphones or a 10K (nominal) load with on board shunt resistance as low as 20K ohms (typical - used to maintain coupling CAP bias.) Line Level outputs are intended to drive an external 10K speaker load (nominal) and an on board shunt resistor of 20K-47K (nominal). However, applications may support load impedances of 5K ohms and above. Input ports are 47K (nominal) at the pin.

DAC full scale output and intended full scale input levels are 1V rms. Line output ports and Headphone output ports on 92HD73D1 may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing designs to use the 92HD73D1, ensure that there are no conflicts between the output ports on 92HD73D1 and existing circuitry.

AFG Power State	Input Enable	Output Enable	Mute	Port Behavior
D0-D2	1	1	-	Not allowed. Port becomes input.
	1	0	-	Active - port enabled as input
	0	1	0	Active - port enabled as output
	0	1	1	Mute - port enabled as output but drives silence
	0	0	-	Inactive - Port keeps coupling caps charged (same as mute.)
D3		-	-	Inactive (lower power) - Port keeps output coupling caps charged but consumes less power.

Table 2. Analog I/O Port Behavior

1.4.3. Jack Detect

Plugs inserted to a jack on Ports A, B, C, & D are detected using SENSE_A. Plugs inserted to a jack on Ports E, F, G, and H are detected using SENSE_B. The following table summarizes the proper resistor tolerances for different analog supply voltages.

SENSE_C, is different from SENSE_A and SENSE_B. Because SENSE_C only determines the presence of a plug for the CD port (port I), SENSE_C is a simple digital input pin referenced to the analog supply. An internal pull-up resistor is provided. No external resistors are needed (jack switch shorts to ground when a plug is inserted.) If external components are added, or if the pin is driven by a logic gate, care should be taken to ensure that the pin voltage is above 70% of AVDD when no plug is in the jack and less than 30% AVDD when a plug is inserted

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance SENSE_A (If port D used)	Resistor Tolerance SENSE_A (If port D is not used)	Resistor Tolerance SENSE_B (If port H used)	Resistor Tolerance SENSE_B (If port H is not used)
5V	1%	1%	1%	1%
4.75V	1%	1%	1%	1%
4V	0.50%	1%	0.50%	1%
3.3V	0.10%	1%	0.10%	1%

Table 3: SENSE Resistor Tolerance

See reference design for more information on Jack Detect implementation.

1.4.4. SPDIF Output

All SPDIF Outputs can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4KHz, and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

A second independant SPDIF Output is provided as an option for WLP compliant HDMI and SPDIF outputs. Its function is identical to the primary SPDIF output.

Note: Peak to peak jitter is currently limited to less than 4.5nS (half of the internal master clock cycle) which does not meet the IEC-60958-3 0.05UI requirement at 192KHz.

The two SPDIF ouput converters can not be aligned in phase with the DACs. Even when attached to the same stream, the two SPDIF output converters may be misaligned with respect to their frame boundaries.

SPDIF Outputs on pins 48 and 40 are outlined in tables below. Pin 47 behavior table resides in the EAPD section

AFG Power State	RESET#	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
D0	De-Asserted (High)	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down NA)
	De-Asserted (High)	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down NA)
	De-Asserted (High)	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut0 data (internal pull-down NA)
D1-D2	De-Asserted (High)	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	-	-	Active - Pin drives 0 (internal pull-down NA)
D3	De-Asserted (High)	-	-	-	Hi-Z (internal pull-down enabled)

Table 4. SPDIF OUT 0 (Pin 48) Behavior

AFG Power State	RESET#	GPIO 3 Enable	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
D0-D3	De-Asserted (High)	Enabled	-	-	-	Active - Pin reflects GPIO7 configuration (internal pull-up enabled)

Table 5. SPDIF OUT 1 (Pin 40) Behavior

AFG Power State	RESET#	GPIO 3 Enable	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0	De-Asserted (High)	Disabled	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut1 data (internal pull-down enabled)
D1-D2	De-Asserted (High)	Disabled	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	-	-	Active - Pin drives 0 (internal pull-down NA)
D3	De-Asserted (High)	Disabled	-	-	-	Hi-Z (internal pull-down enabled)

Table 5. SPDIF OUT 1 (Pin 40) Behavior

1.4.5. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz, 88.2 KHz or 96 KHz, and implements internal Jack Sensing.

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs. Advanced features such as record-slot-select and SPDIF_IN routing to the DAC allow for simultaneous record and play.

1.4.6. Analog Mixer

An analog mixer is available on the 92HD73D1. The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input. A master volume follows mixing and provides gain from -46.5dB to 0dB in 1.5dB steps.

The following inputs are available:

- CD
- Analog PC_Beep
- Inport0_Mux
- Inport1_Mux
- Inport2_Mux
- Inport3_mux

1.4.7. Input Multiplexers

92HD73D1 implements 4 port input multiplexers. These multiplexers allow a preselection of one of four possible inputs:

Inport0_Mux	Inport1_Mux	Inport2_Mux	Inport3_mux
Port A	Port A	Port B	DAC 0
Port B	Port E	Port C	DAC 1
Port D	Port G	Port G	DAC 2
Port F	Port H	Port H	DAC 3

Table 6. Input Multiplexers

1.4.8. ADC Multiplexers

92HD73D1 implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function (0 to +22.5dB gain in 1.5dB steps) as an output amp and allow a preselection of one of 12 possible inputs:

- DMIC 0
- DMIC 1
- Mixer output
- CD input
- Ports A - H

1.4.9. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG) and all converter widgets support the power state verb F05/705 (as well as the pin widget associated with pin 47.) Converter widgets are active in D0 and inactive in D1-D3.

The following table describes what functionality is active in each power state supported by the AFG.

Function	D0	D1[1]	D2	D3	vendor specific
SPDIF Outputs	On	Off	Off	Off	-
SPDIF Inputs	On	Off	Off	Off	-
Digital Microphone inputs	On	Off	Off	Off	-
DAC	On	Off	Off	Off	-
D2S	On	Off	Off	Off	-
ADC	On	Off	Off	Off	-
ADC Volume Control	On	Off	Off	Off	-
Ref ADC	On	Off	Off	Off	-
Analog Clocks	On	Off	Off	Off	-
GPIO pins	On	On	On	On	-
VrefOut Pins	On	On	Off	Off	-

Table 7. Function state vs. AFG power state

Function	D0	D1[1]	D2	D3	vendor specific
Input Boost	On	On	Off	Off	-
Analog mixer	On	On	Off	Off	-
Mixer Volumes	On	On	Off	Off	
Analog PC_Beep	On	On	Off	Off	
Digital PC_Beep	On	On	On	On	-
Lo Amp	On	On	On	Low Drive[2]	Programmable
HP Amps	On	On	On	Low Drive[2]	Programmable
VAG amp	On	On	On	Low Drive[3]	Programmable
Port Sense	On	On	On	On[4]	Programmable
Reference Bias generator	On	On	On	On	Programmable[5]
Reference Bandgap core	On	On	On	On	Programmable[5]
HD Audio-Link	On	On	On	On[6]	-

Table 7. Function state vs. AFG power state

1.No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2.VAG is kept active when ports are disabled or in D2/D3. Ports may be powered down using vendor specific verbs.
3.VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
4. BITCLK must be active and both AVDD and DVDD must be available for Port Sense to operate.
5.Vendor specific bit for Ref Top controls VAG generator, Bandgap Reference, and Reference bias generator. Place part into D3 and power down all ports (using vendor specific verbs) before powering down Ref Top.
6.Obviously not active if BITCLK is not running (Controller in D3).

1.4.9.1. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

1.4.9.2. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active.

1.4.9.3. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state.

1.4.9.4. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still very fast to meet Intel low power goals.

The traditional use for D3 was as a transitional state before power was removed (D3 cold) before the system entered into standby, hibernate, or shut-down. To conserve power, Intel now promotes using D3 whenever there are no active streams or other activity that requires the part to consume full power. The system remains in S0 during this time. When a stream request or user activity requires

the CODEC to become active, the driver will immediately transition the CODEC from D3 to D0. To enable this use model, the CODEC must resume within 10mS and not pop.

The default power state for the Audio Function Group after reset is D3-default

1.4.9.5. AFG D3 and vendor specific verbs

The programmable values, exposed via vendor-specific settings, are under the IDT Device Driver control for further power reduction.

1.4.10. Low-voltage HDA Signaling

The 92HD73D1 is compatible with either 1.5V or 3.3V HDA bus signaling; the voltage selection is done dynamically based on the input voltage of DVDD_IO.

When in 1.5V mode, the 92HD73D1 can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

1.4.11. Multi-channel capture

The capability to assign multiple ADC “Input Converters” to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported and is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones. However, the SPDIF input can not be used with an ADC to create a 4-channel stream. SPDIF_In only supports stereo capture.

The ADC Converters can be associated with a single stream as long as the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries” table.

An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2&3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

ADC1 CnvtrID	(NID = 0x08)	
	[3:0]	Ch = 2
ADC0 CnvtrID	(NID = 0x07)	
	[3:0]	Ch = 0

Table 8: Example channel mapping

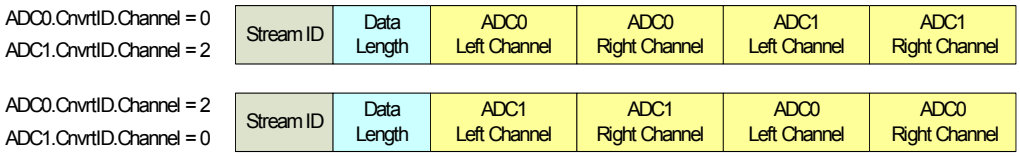


Figure 3. Multi-channel capture

The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

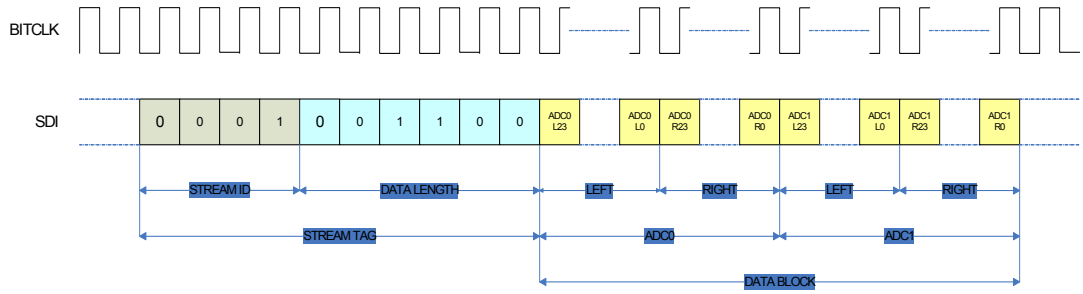


Figure 4. Multi-channel timing diagram

ADC[1:0] Cnvtr	Bit Number	Sub Field Name	Description
	[15]	StrmType	Stream Type (TYPE): 0: PCM 1: Non-PCM (not supported)
	[14]	FrmtSmplRate	Sample Base Rate 0= 48kHz 1=44.1KHz
	[13:11]	SmplRateMultp	Sample Base Rate Multiple 000=48kHz/44.1kHz or less 001= x2 010= x3 (not supported) 011= x4 100-111= Reserved

Table 9: Multi-Converter Stream Critical Entries.

	[10:8]	SmplRateDiv	Sample Base Rate Divisor 000= Divide by 1 001= Divide by 2 (not supported) 010= Divide by 3 (not supported) 011= Divide by 4 (not supported) 100= Divide by 5 (not supported) 101= Divide by 6 (not supported) 110= Divide by 7 (not supported) 111= Divide by 8 (not supported)
	[6:4]	BitsPerSmpl	Bits per Sample 000= 8 bits (not supported) 001= 16 bits 010= 20 bits 011= 24 bits 100-111= Reserved
	[3:0]	NmbrChan	Number of Channels Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link. 0000=1 channel (not supported) 0001 = 2 channels … 1111= 16 channels.
ADC[1:0] CnvtrID	**Bit Number**	**Sub Field Name**	**Description**
	[7:4]	Strm	Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused.
	[3:0]	Ch	Integer representing lowest channel used by converter. 0 and 2 are valid Entries If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2.

Table 9: Multi-Converter Stream Critical Entries.

1.4.12. EAPD

The EAPD pin (pin 47) also supports SPDIF_In and GPIO functions. The pin defaults to EAPD after power on reset and will remain in EAPD mode until either GPIO is enabled for pin 47 or the port I/O is enabled to support SPDIF. Although named External Amplifier Power Down (EAPD) by the HD Audio specification, this pin operates as an external amplifier power up signal. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up, and a 0 causes it to power down. When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value may remain 1. The default state of this pin is 0 (driving low) and a Pull-down prevents the line from floating high when the part is in reset.

AFG Power State	RESET#	GPIO Enable	Input Enable	EAPD Power State	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
D0	De-Asserted (High)	Enabled	-	-	Active - Pin reflects GPIO0 configuration (internal pull-up enabled)
	De-Asserted (High)	Disabled	Enabled	-	Active - Pin is SPDIF_In
	De-Asserted (High)	Disabled	Disabled	D0-D1	Active - Pin drives the value of the EAPD bit (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D2-D3	Hi-Z (internal pull-down enabled)
D1	De-Asserted (High)	Disabled	Enabled	-	Inactive - Pin configured as input, but SPDIF_In idle.
	De-Asserted (High)	Disabled	Disabled	D0-D1	Active - Pin drives the value of the EAPD bit (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D2-D3	Hi-Z (internal pull-down enabled)
D2	De-Asserted (High)	Disabled	-	D0-D3	Hi-Z (internal pull-down enabled)
D3	De-Asserted (High)	Disabled	-	D0-D3	Hi-Z (internal pull-down enabled)

Table 10. EAPD Behavior

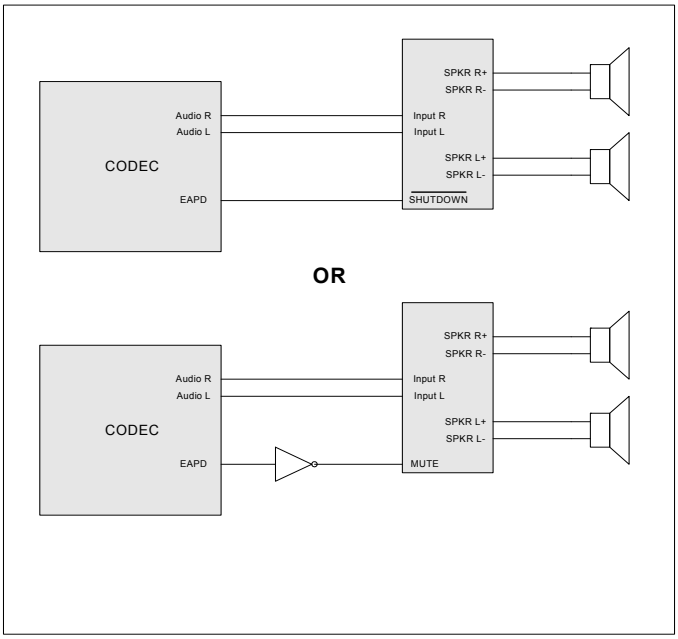


Figure 5. EAPD

1.4.13. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0, DMIC1, and DMIC_CLK 3-pin interface. The DMIC0 and DMIC1 signals are inputs that carry individual channels of digital Mic data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the 24Mhz internal clock. The default frequency is 2.352Mhz.

The two DMIC data inputs are reported as two stereo input pin widgets that incorporate a boost amplifier. The pin widgets are shown connected to the ADCs through the same multiplexors as the analog ports. Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

92HD73D1 supports the following digital microphone configurations:

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones
1	Single Edge	0, or 1	Available on either DMIC_0 or DMIC_1 Both ADC Channels produce data, may be in phase or out by 1/2 DMIC_CLK period depending upon external configuration and timing
2	Double Edge on either DMIC_0 or 1 OR Single Edge on DMIC_0 and 1	0, or 1	Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. If both DMIC_0 and DMIC_1 are used to support 2 digital microphones, 2 separate ADC units will be used, however, this configuration is not recommended since it consumes two stereo ADC resources.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0, or 1	Requires both DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration
4	Double Edge	0, or 1	Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration

Table 11. Valid Digital Mic Configurations

Power State	DMIC Widget Enabled	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D1-D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down

Table 12. DMIC_CLK and DMIC_0,1 Operation During Power States

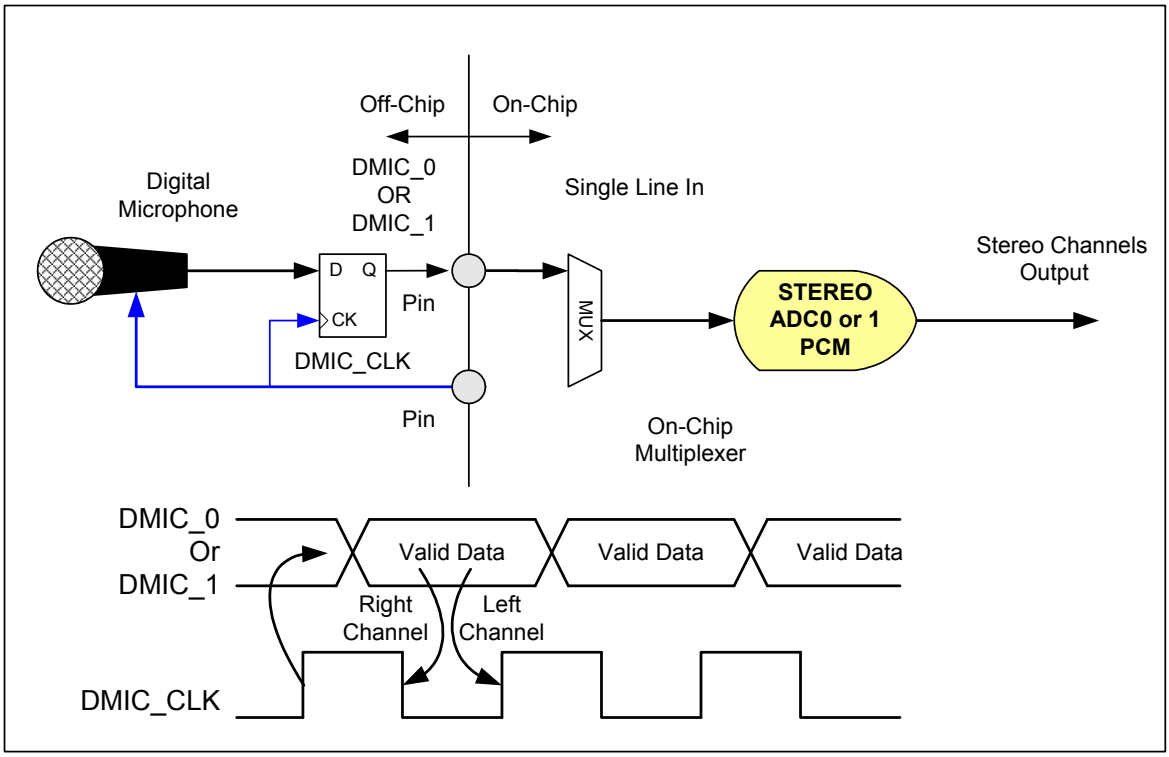


Figure 6: Mono Digital Microphone (data is ported to both left and right channels

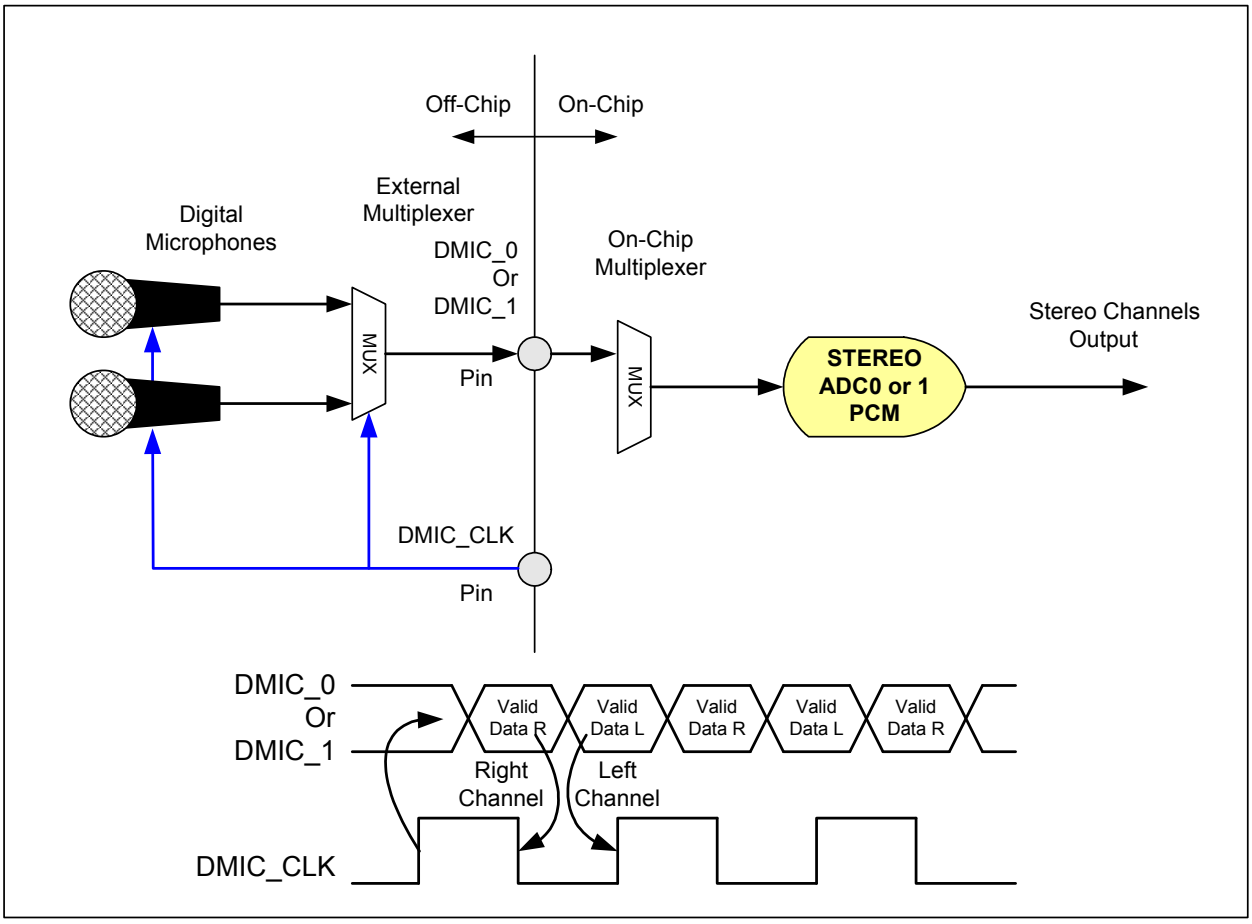


Figure 7: Stereo Digital Microphone Configuration

Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

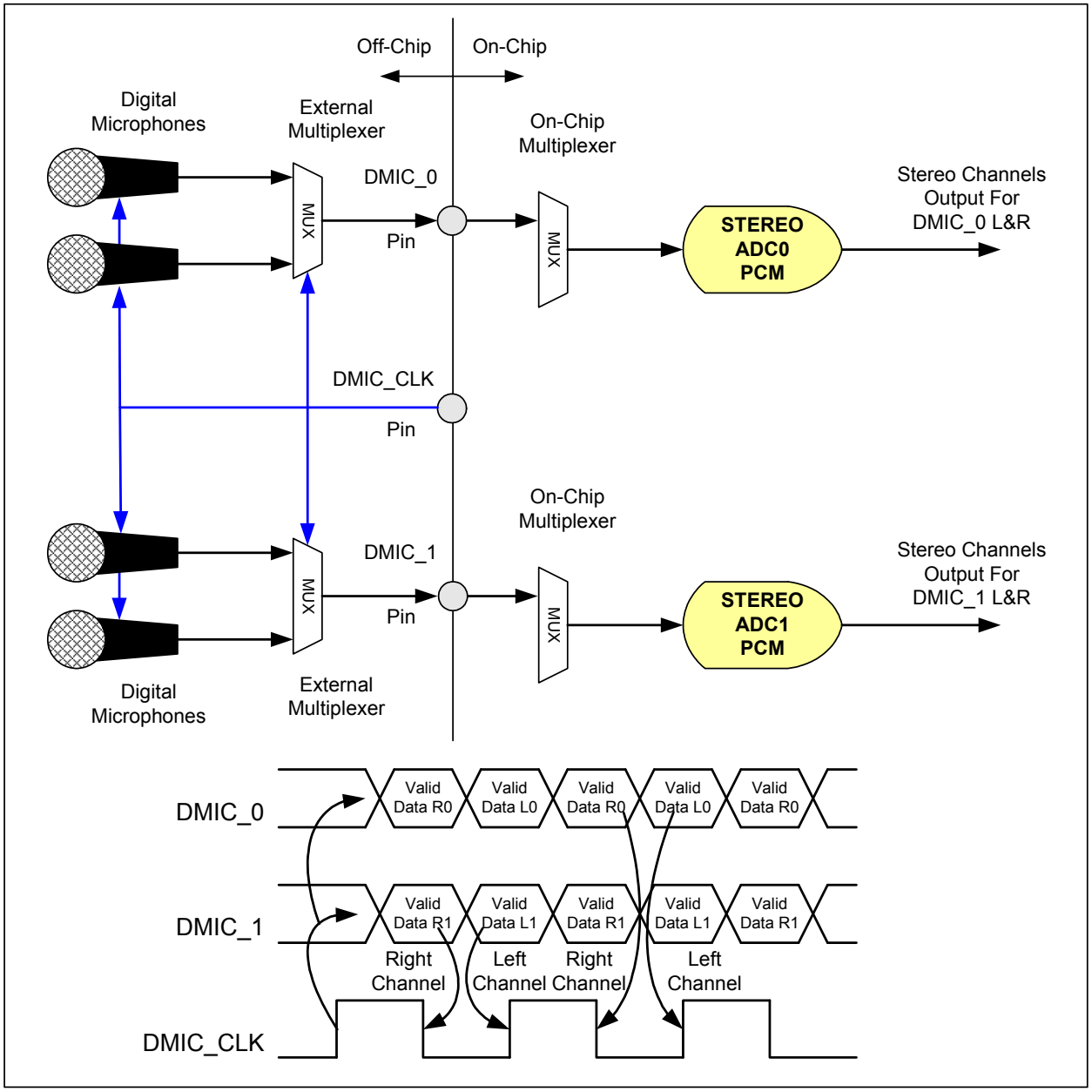


Figure 8: Quad Digital Microphone Configuration

Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

1.4.14. PC-Beep

92HD73D1 supports both analog and digital PC_Beep functions.

1.4.14.1. Analog PC-Beep

92HD73D1 does not support automatic routing of the PC_Beep pin to all outputs when the link is in reset. Analog PC-Beep may be supported during Link Reset if the mixer is manually configured for pass-thru. Otherwise, Reset# must be high and Bit_Clk active.

The default values for the vendor specific verb (7EE/FEE in AFG) associated with Analog PC-Beep are:

- Enable = 0h (Analog PC-Beep disabled - mute)
- volume = 3h (0dB)

Analog PC-Beep is supported in D3, but may be attenuated or distorted depending on the load-impedance on the port. Line outputs can drive 10K ohm loads in D3 at 1Vrms, but will be current limited when driving lower impedance loads. Enabling or disabling analog PC-Beep may cause a click or pop sound.

1.4.14.2. Digital PC-Beep

This block uses an 8-bit divider value to generate the PC beep from the 48kHz Azalia sync pulse. The digital PC_Beep block generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). Other audio sources are disabled when digital PC_Beep is active.

It should be noted that digital PC Beep is disabled if the divider = 00h.

1.4.15. Headphone Drivers

This product implements a +3dBV output option on headphone capable ports. (HP output and line output levels are defined as 1Vrms at this time with an option to enable +3dBV FSOV using a vendor specific verb.) The Microsoft Windows Logo Program allows up to the equivalent of 100ohms in series. However, an output level of +3dBV at the pin is required to support 300mV at the jack with a 32ohm load and 1V with a 320 ohm load. Microsoft allows device and system manufactures to limit output voltages to address EU safety requirements. (WLP 3.09 - please refer to the latest Windows Logo Program requirements from Microsoft.) 92HD73D1, however, requires external components (series resistors) to limit the output voltage to 150mV with a 32 ohm load or secure software limiting by restricting DAC and mixer gain ranges.

Although 3 Headphone amplifiers are present, only two may be used simultaneously.

Performance will degrade when driving more than one set of headphones. Only one set of headphones (32 ohm nominal) may be connected to a headphone capable port.

1.4.16. GPIO

1.4.16.1. GPIO Pin mapping and shared functions.

GPIO #	Pin	Supply	SPDIF In	SPDIF Out	GPI/O	GPI	GPO	VrefOut	DMIC	VOL	Pull Up	Pull Down
0	47	DVDD	YES		YES						50K (GPIO)	50K[1] (SPDIF/EAPD)
1	2	DVDD			YES				CLK	YES	50K (GPIO/VOL)	50K (DMIC)
2	4	DVDD			YES				IN	YES	50K (GPIO/VOL)	50K (DMIC)
3	40	AVDD		YES	YES						50K (GPIO)	50K[1] (SPDIF)
4	29	AVDD			YES			YES				
5	30	AVDD			YES				IN		50K[1]	50K (DMIC)
6	31	AVDD			YES			YES				
7	37	AVDD			YES			YES				

Table 13. GPIO Pin mapping

1.Default condition.

1.4.16.2. Volume/Digital Microphone/GPIO Selection

There are 3 functions available on pins 2 and 4. To determine which function is actually enabled on the 2 pins, the order of precedence is followed:

1. If the GPIOs are enabled, they override both Volume Control and Digital Mics
2. If the GPIOs are not enabled through the AFG, then at reset, the Volume control is enabled with the weak pull-up.
3. If BIOS or other software application enables either Digital Microphones inputs through the Configuration Default Register, the Volume is disconnected and the pull-ups are disconnected with the weak pull-downs enabled.

1.4.16.3. VRefOut/GPIO Selection

Two functions are available on pins 29, 31, and 37. To determine which function is actually enabled, the order of precedence is followed:

1. If the GPIOx function is enabled, it overrides VRefOut-X
2. If the GPIO function is not enabled through the AFG, then the VrefOut function is enabled and in its default state.
3. If using a VrefOut pin as GPIO, make sure to incorporate a 10K ohm external pull-up to AVDD to prevent the pin from floating in GPI mode and to allow proper operation in open-drain GPO mode.

1.4.17. External Volume Control

92HD73D1 incorporates a 2-pin volume control interface. Volume up, down, and mute functions are easily implemented using 2 push-button switches. The CODEC provides internal pull-up resistors simplifying external CODEC circuitry. Also, repeat and direct modes of operation add flexibility to the interface. The typical usage model is for front panel master volume buttons on an entertainment PC, or case mounted hardware volume control for mobile platforms.

1.4.17.1. Theory of Operation

The codec monitors the volume up/down inputs for a change of state from high to low, and waits for the inputs to settle. If the inputs have not settled by the end of the de-bounce period, then the value at the end of the period is used. A 0 (low voltage) on the Down pin will decrement the volume register, while a 0 on the Up pin will increment the volume register. If both inputs are 0 at the same time, then the volume register will be set to its lowest value (mute). Pressing Up, Down, or both buttons at the same time when the volume control interface is in mute mode, will cause the part to un-mute.

The de-bounce / repeat rate is selectable from 2.5Hz to 20Hz in 2.5Hz increments using the Volume Knob VCSR0 verb (FE0) Rate bits (bits 2:0). This value is used for both de-bounce and repeat rates. The de-bounce period is the time that the CODEC waits for the inputs to settle, and the repeat rate is the rate at which the CODEC will increment/decrement the volume if a volume button is pushed and held. When a falling edge is detected on either one of the volume control pins, the codec will wait for (1/Rate) seconds for the input to settle. If the Continuous bit is set in the Volume Knob VCSR0 verb (bit 3), then the codec will wait for the de-bounce period to expire then repeatedly increment or decrement the volume register at the rate specified in the Rate bits until the button is released.

1.4.17.2. Modes of Operation

- DIRECT MODE

In Direct mode, the Volume Knob widget directly controls the volume of all of the DACs in the part. The volume in the Volume Knob widget acts as the master volume and limits the maximum volume for each of the DAC amplifiers. The amp gain for each of the DACs can also be adjusted using the DAC amplifiers. However, the actual gain for an individual DAC will be the sum of the Volume Knob volume and the DAC amplifier volume. For example, if the DAC amplifier gain is set to 0x7F (0dB) and the Volume Knob volume is set to 0x3F (-48dB) the resulting gain would be -48dB. If the combination of gains is less than -95.25dB (the equivalent to a value of 0x0 for the DAC or Volume Knob volume settings) then the actual gain will be -95.25dB. For example, if the Volume Knob is set to 0x3F (-48dB) and the DAC amplifier volume is set to 0x1F (-72dB) then the DAC volume will be set to -95.25dB.

Direct mode is enabled by setting bit 7 in the Volume Knob Cntrl verb (F0F). The volume is reflected in the Volume Knob Cntrl bits 6:0 and the step size is 0.75dB. In direct mode, software can read or write the volume in the Volume Knob widget.

- INDIRECT MODE

In indirect mode, the Volume Knob widget does not directly control the DAC amplifier gains. An event on the volume Up/Down pins will increment/decrement the value in the Volume Knob Cntrl verb (F0F) volume bits (bits 6:0) just as in Direct mode. However, instead of adjusting the DAC amplifier gain, an unsolicited response is generated (if enabled) and the control software must read

the volume in the Volume Knob widget and take appropriate action. Indirect mode is particularly useful when it is undesirable to control all of the DAC amplifier volumes at the same time, or when implementing ADC volume control.

In indirect mode, there are only 128 volume levels in the Volume Knob Cntrl volume bits, the value will not go beyond the lower and upper limits (0x0 or 0x7F), and an unsolicited response will be generated if an input event tries to go beyond these limits. Therefore, it is the responsibility of the controlling software to monitor the volume in the Volume Knob Widget and take appropriate action.

Indirect mode is enabled by clearing bit 7 in the Volume Knob Cntrl verb (F0F). The volume is reflected in the Volume Knob Cntrl bits 6:0 and the step size is 0.75dB. In direct mode, software can read or write the volume in the Volume Knob widget.

1.4.17.3. Hardware Implementation

The Volume Knob interface is comprised of two input pins, CODEC pins 2 and 4. Both pins have internal pull-up resistors, so only two push button switches are required for most implementations. Typically, a series resistor and shunt capacitor are used to help reduce noise and prevent damage from ESD and other potential faults. An example circuit is shown below in below.

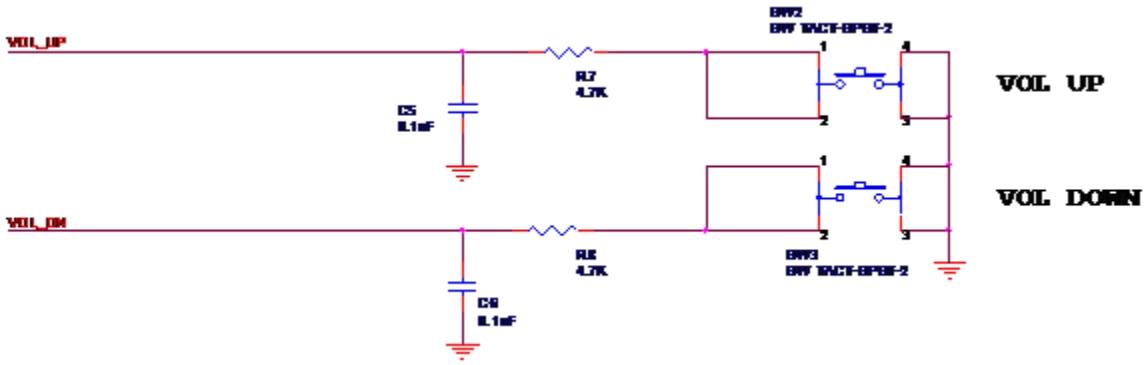


Figure 9: External Volume Control Circuit

2. CHARACTERISTICS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 92HD73D1. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 14. Electrical Specification: Maximum Ratings

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0 ^{o}C to +70 ^{o}C -40 ^{o}C to +85 ^{o}C (Industrial Temp)
Storage temperature		-55 ^{o}C to +125 ^{o}C
Soldering temperature		Soldering temperature information for all available in the package section of this datasheet.

2.1.2. Recommended Operating Conditions

Table 15. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: With Supply Override Enable Bit set to force 5 V operation.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 4.5 V	4.51	4.75	4.99	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} Commercial			+90	°C
	T_{case} Industrial			+110	°C

ESD: The 92HD73D1 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the 92HD73D1 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.2. 92HD73D1 5V, 4.75V, and 3.3V Analog Performance Characteristics

(Tambient = 25 ºC, AVdd = Supply ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 20Hz to 20KHz swept sinusoidal input; Sample Frequency = 48 kHz; 0 dB = 1 VRMS, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Digital to Analog Converters						
Resolution		All		24		Bits
Dynamic Range[1]: PCM to All Analog Outputs	-60dB FS signal level	5V 4.75V 3.3V	90 90 85	94 94 88		dB
SNR[2] - DAC to All Line-Out Ports	Analog Mixer Disabled, PCM data	5V 4.75V 3.3V	90 90 85	97 97 88		dB
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Disabled, 0dB FS Signal, PCM data	5V 4.75V 3.3V	80 80 80	83 83 83		dBr
THD+N[3] - DAC to All Line-Out Ports	Analog Mixer Disabled,-1dB FS Signal, PCM data	5V 4.75V 3.3V	80 80 80	83 83 83		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 10KΩ load, PCM data	5V 4.75V 3.3V	90 90 85	97 97 88		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, 0dB FS Signal, 10KΩ load, PCM data	5V 4.75V 3.3V	80 80 80	83 83 83		dBr
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, -1dB FS Signal, 10KΩ load, PCM data	5V 4.75V 3.3V	80 80 80	83 83 83		dBr
SNR[2] - DAC to All Headphone Ports	Analog Mixer Disabled, 32Ω load, PCM data	5V 4.75V 3.3V	90 90 85	97 97 88		dB
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, 0dB FS Signal, 32Ω load, PCM data	5V 4.75V 3.3V	65 65 65	70 70 70		dBr
THD+N[3] - DAC to All Headphone Ports	Analog Mixer Disabled, -1dB FS Signal, 32Ω load, PCM data	5V 4.75V 3.3V	65 65 65	70 70 70		dBr

Table 16. 92HD73D1 5V, 4.75V, and 3.3V Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Any Analog Input (ADC) to DAC Crosstalk	10KHz Signal Frequency. 0dBV signal applied to ADC, DACs idle, ports enabled as output.	All	-	-80	-	dB
Any Analog Input (ADC) to DAC Crosstalk	1KHz Signal Frequency see above	All	-	-85	-	dB
DAC L/R crosstalk	DAC to LO or HP 20-15KHz into 10KΩ load	All	65	70		dB
DAC L/R crosstalk	DAC to HP 20-15KHz into 32Ω load	All	65	70		dB
Gain Error	Analog Mixer Disabled	All			0.5	dB
Interchannel Gain Mismatch	Analog Mixer Disabled	All			0.5	dB
D/A Digital Filter Pass Band[4]		All	20	-	21,000	Hz
D/A Digital Filter Transition Band		All	21,000	-	31,000	Hz
D/A Digital Filter Stop Band		All	31,000	-	-	Hz
D/A Digital Filter Stop Band Rejection[5]		All	-100	-	-	dB
D/A Out-of-Band Rejection[6]		All	-55	-	-	dB
Group Delay (48KHz sample rate)		All	-	-	1	ms
Attenuation, Gain Step Size DIGITAL		All	-	0.75	-	dB
DAC Offset Voltage		All	-	10	20	mV
Deviation from Linear Phase		All	-	1	10	deg.
Analog Outputs						
Full Scale All Line-Outs	DAC PCM Data	5V 4.75V 3.3V	1.00 1.00 0.707	1.07 1.07 0.758	-	Vrms
Full Scale All Line-Outs	DAC PCM Data	5V 4.75V 3.3V	2.83 2.83 2.00	3.03 3.03 2.14	-	Vp-p
All Headphone Capable Outputs	32Ω load	5V 4.75V 3.3V	40 40 31	60 60 42	-	mW (peak)
Amplifier output impedance	Line Outputs Headphone Outputs	All		150 0.1		Ohms
Analog inputs						
Full Scale Input Voltage	0dB Boost @4.75V (input voltage required for 0dB FS output)	5V 4.75V 3.3V	1.05	1.10	-	Vrms
All Analog Inputs with boost	10dB Boost	5V 4.75V 3.3V	0.31	-	-	Vrms

Table 16. 92HD73D1 5V, 4.75V, and 3.3V Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
All Analog Inputs with boost	20dB Boost	5V 4.75V 3.3V	0.10	-	-	Vrms
All Analog Inputs with boost	30dB Boost	5V 4.75V 3.3V	0.03	-	-	Vrms
Input Impedance		All	-	50	-	KΩ
Input Capacitance		All	-	15	-	pF
Analog Mixer						
SNR[2] - All Line-Inputs or DACs to A, B, and D headphone capable outputs	Analog Mixer Enabled, 10KΩ load. DAC playing silence, line inputs driven by ATE. Gain set to 0dB	5V 4.75V 3.3V	85 85 85	90 90 90		dB
THD+N[3] - All Line-Inputs or DACs to A, B, and D headphone capable outputs	Analog Mixer Enabled, 0dB FS Signal, 10KΩ load	5V 4.75V 3.3V	70 70 70	75 75 75		dBr
SNR[2] - All Line-Inputs or DACs to A, B, and D headphone capable outputs	Analog Mixer Enabled, 32Ω load. DAC playing silence, Line inputs driven by ATE.	5V 4.75V 3.3V	85 85 85	90 90 90		dB
THD+N[3] - All Line-Inputs or DACs to A, B, and D headphone capable outputs	Analog Mixer Enabled, 0dB FS Signal, 32Ω load	5V 4.75V 3.3V	60 60 60	70 70 70		dBr
SNR[2] - DAC to All Line-Out Ports (C, E, F, G, and H)	Analog Mixer Enabled, DACs playing silence, line inputs driven by ATE. Gain set to 0dB	5V 4.75V 3.3V	85 85 85	90 90 90		dB
THD+N[3] - DAC to All Line-Out Ports (C, E, F, G, and H)	Analog Mixer Enabled, 0dB FS Signal, , 10KΩ load	5V 4.75V 3.3V	70 70 70	75 75 75		dBr
Attenuation, Gain Step Size ANALOG		All	-	1.5	-	dB
Gain Drift[7]		All	-	100	-	ppm/ºC
Analog to Digital Converter						
Resolution		All		24		Bits
Dynamic Range[1], All Analog Inputs to A/D	High Pass Filer Enabled, -60dB FS, No boost	5V 4.75V 3.3V	86 86 83	90 90 85		dB
SNR[2]- All Analog Inputs to A/D	High Pass Filter enabled	5V 4.75V 3.3V	86 86 83	90 90 85		dB
THD+N[3] All Analog Inputs to A/D	High Pass Filter enabled, -1dB FS signal level	5V 4.75V 3.3V	75 75 65	85 85 75		dBr
THD+N[3] All Analog Inputs to A/D	High Pass Filter enabled, -3dB FS signal level	5V 4.75V 3.3V	75 75 65	85 85 75		dBr

Table 16. 92HD73D1 5V, 4.75V, and 3.3V Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Analog Frequency Response[8]		All	10	-	30,000	Hz
A/D Digital Filter Pass Band[4]		All	20	-	21,000	Hz
A/D Digital Filter Transition Band		All	21,000	-	31,000	Hz
A/D Digital Filter Stop Band		All	31,000	-	-	Hz
A/D Digital Filter Stop Band Rejection[5]		All	-100	-90	-	dB
Group Delay	48 KHz sample rate	All	-	-	1	ms
Any unselected analog Input to ADC Crosstalk	10KHz Signal Frequency	All	-65	-80	-	dB
Any unselected analog Input to ADC Crosstalk	1KHz Signal Frequency	All	-65	-85	-	dB
ADC L/R crosstalk	Any selected input to ADC 20-15Khz	All	-65			dB
DAC to ADC crosstalk	DAC output 0dBFS. All outputs loaded. Input to ADC open. 20-15Khz	All	-55			dB
Spurious Tone Rejection[9]		All	-	-100	-	dB
Attenuation, Gain Step Size (analog)		All	-	1.5	-	dB
Gain Drift		All	-	100	-	ppm/ºC
Interchannel Gain Mismatch ADC		All	-	-	0.5	dB
Power Supply						
Power Supply Rejection Ratio	10kHz	All	-	-60	-	dB
Power Supply Rejection Ratio	1kHz	All	-	-70	-	dB
D0 (7.1 Playback)[10]	Single 7.1 stream. No ADC or SPDIF					
Didd	3.3V			68		mA
Aidd	5.0V, 4.75V, & 3.3V			50		mA
D0 (Stereo Playback)[10]	Single 2 channel stream. No ADC or SPDIF					
Didd	3.3V			38		mA
Aidd	5.0V, 4.75V, & 3.3V			37		mA
D0 (idle)[10]	All converters enabled but no streams playing					
Didd	3.3V			55		mA
Aidd	5.0V, 4.75V, & 3.3V			72		mA
D1[10]	Analog mixer active, all converters and ports off					
D1 Didd	3.3V			14		mA
D1 Aidd	5.0V, 4.75V, & 3.3V			35		mA
D2[10]	All converters, ports and mixer off					

Table 16. 92HD73D1 5V, 4.75V, and 3.3V Analog Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
D2 Didd	3.3V			14		mA
D2 Aidd	5.0V, 4.75V, & 3.3V			28		mA
D3[10]	Anti-pop enabled					
D3 Didd	3.3V			3		mA
D3 Aidd	5.0V, 4.75V, & 3.3V			14		mA
Differential Power[10]	Per converter power consumption					
One Stereo ADC Didd	3.3V			11		mA
One Stereo ADC Aidd	5.0V, 4.75V, & 3.3V			3		mA
One Stereo DAC Didd	3.3V			10		mA
One Stereo DAC Aidd	5.0V, 4.75V, & 3.3V			4		mA
Voltage Reference Outputs						
VREFOut[10]		All	-	0.5 X AVdd	-	V
VREFILT (VAG)		All		0.45 X AVdd		V
Phased Locked Loop						
PLL lock time		All		96	200	usec
PLL (or HD Audio Bit CLK) 24MHz clock jitter		All		150	500	psec
ESD / Latchup						
Latch-up	As described in JESD78A Class II	All		70		degC
ESD - Human Body Model	As described in JESD22-A114-B	All	2K	3K		V
Charged Device Model	As described in JESD22-C101	All	500	1K		V

Table 16. 92HD73D1 5V, 4.75V, and 3.3V Analog Performance Characteristics

1.Dynamic Range is the ratio of the full scale signal to the noise output with a -60dBFS signal as defined in AES17 as SNR in the presence of signal and outlined in AES6id, measured “A weighted” over 20 Hz to 20 kHz bandwidth

2.Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).

3.THD+N ratio as defined in AES17 and outlined in AES6id,non-weighted, over 20 Hz to 20 kHz bandwidth.Results at the jack are dependent on external components and will likely be 1 - 2dB worse.

4.Peak-to-Peak Ripple over Passband meets ± 0.125dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.

5.Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.

6.The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

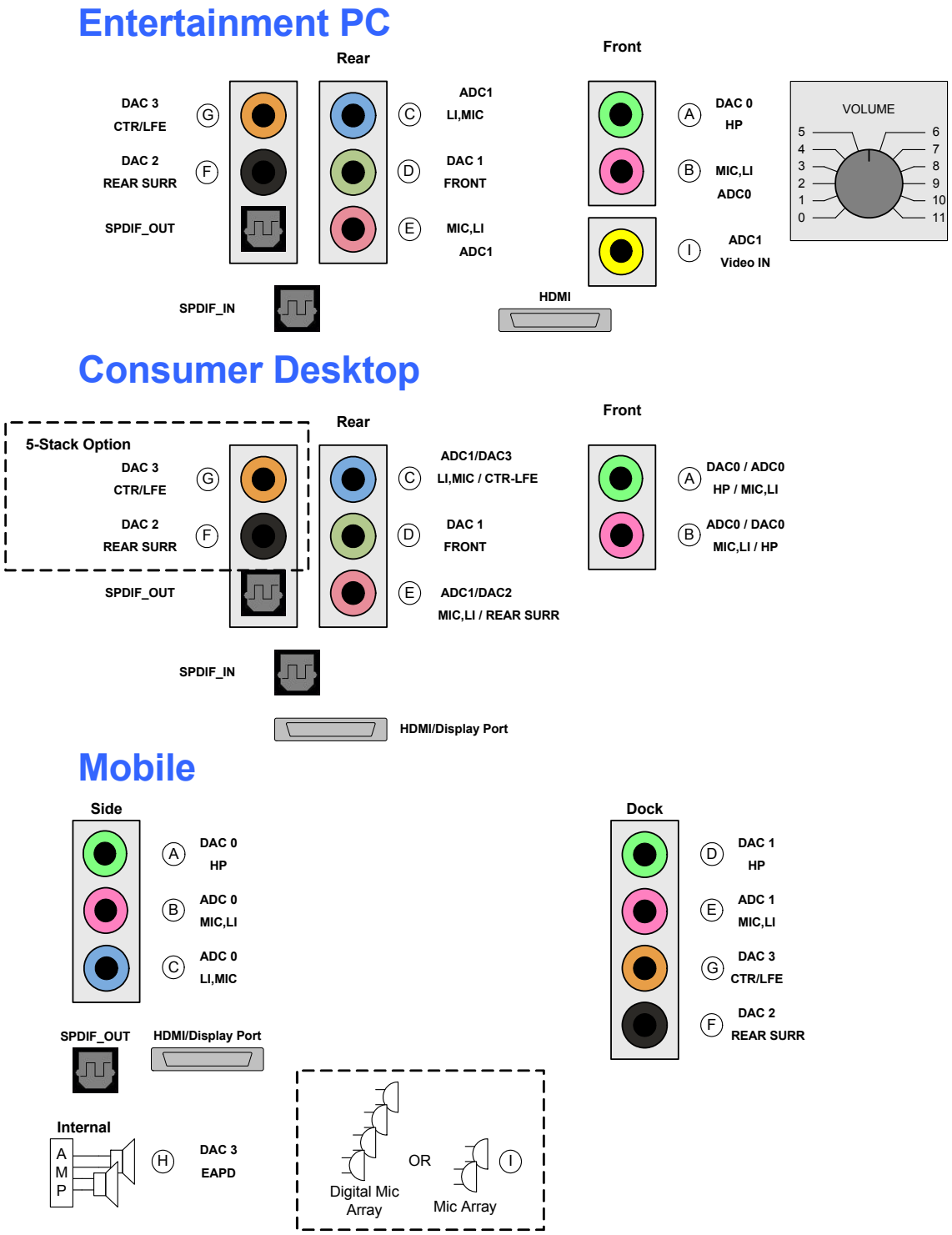
7.Gain drift is the change in analog volume control gain for each step across the supported 0 ^{o}C TO 70 ^{o}C temperature range referenced to the 25 ^{o}C gain value and specified in ppm per ^{o}C

8.± 1dB limits for Line Output & 0 dB gain, at -20dBV

9.Spurious tone rejection is tested with ADC dither enabled and compared to ADC performance without dither.

10.Can be set to 0.5 or 0.8 AVdd.

3. PORT CONFIGURATIONS



4 or 5 stereo DACs / 2 stereo ADCs, 8 ports UJ. 9 stereo ports total. Two SPDIF outputs. 3 HEADPHONE PORTS
DAC output can be mixed with inputs for record or playback.

Figure 10. Port Configuration

4. FUNCTIONAL BLOCK DIAGRAMS

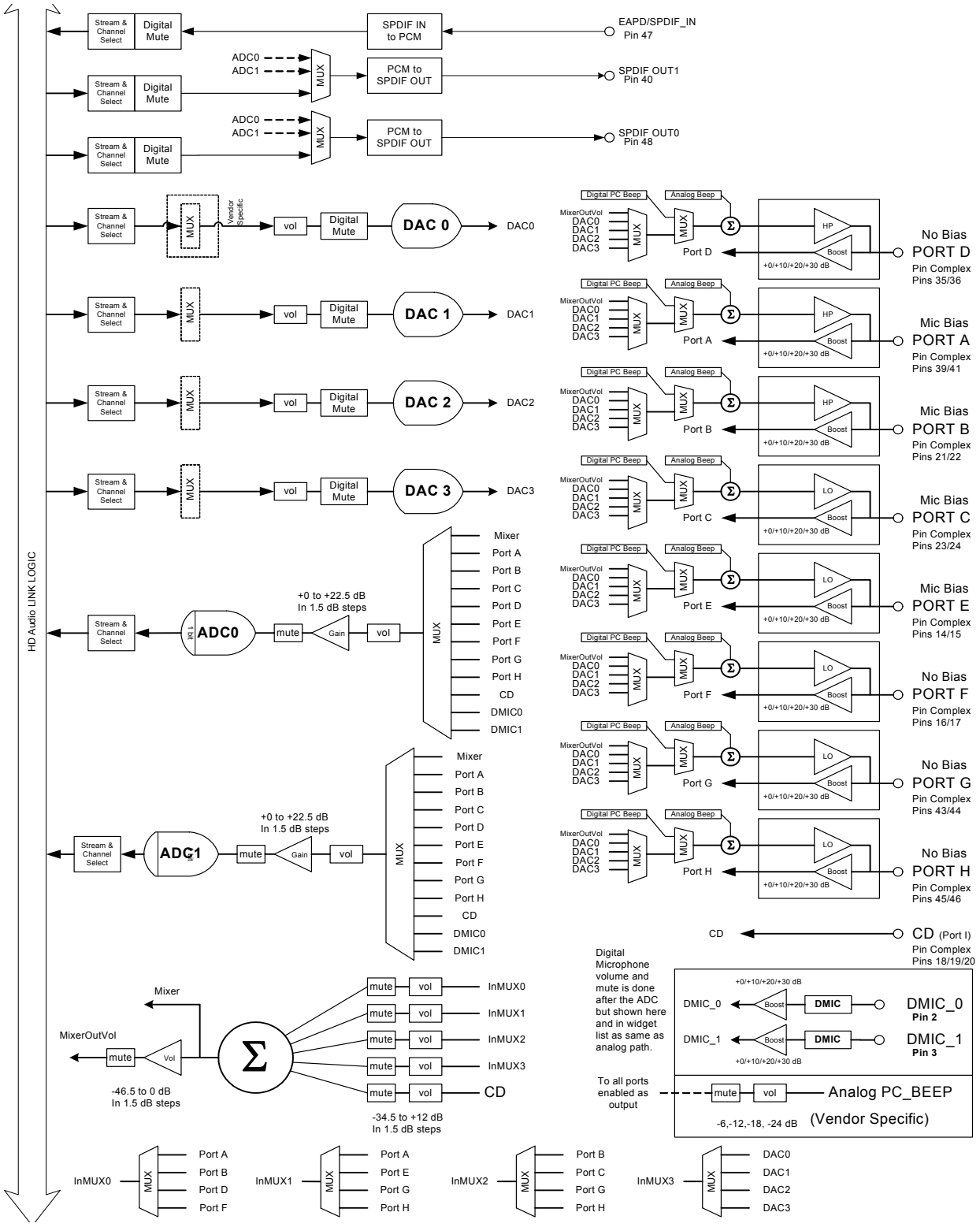


Figure 11. Functional Block Diagram

5. WIDGET INFORMATION AND SUPPORTED COMMAND VERBS

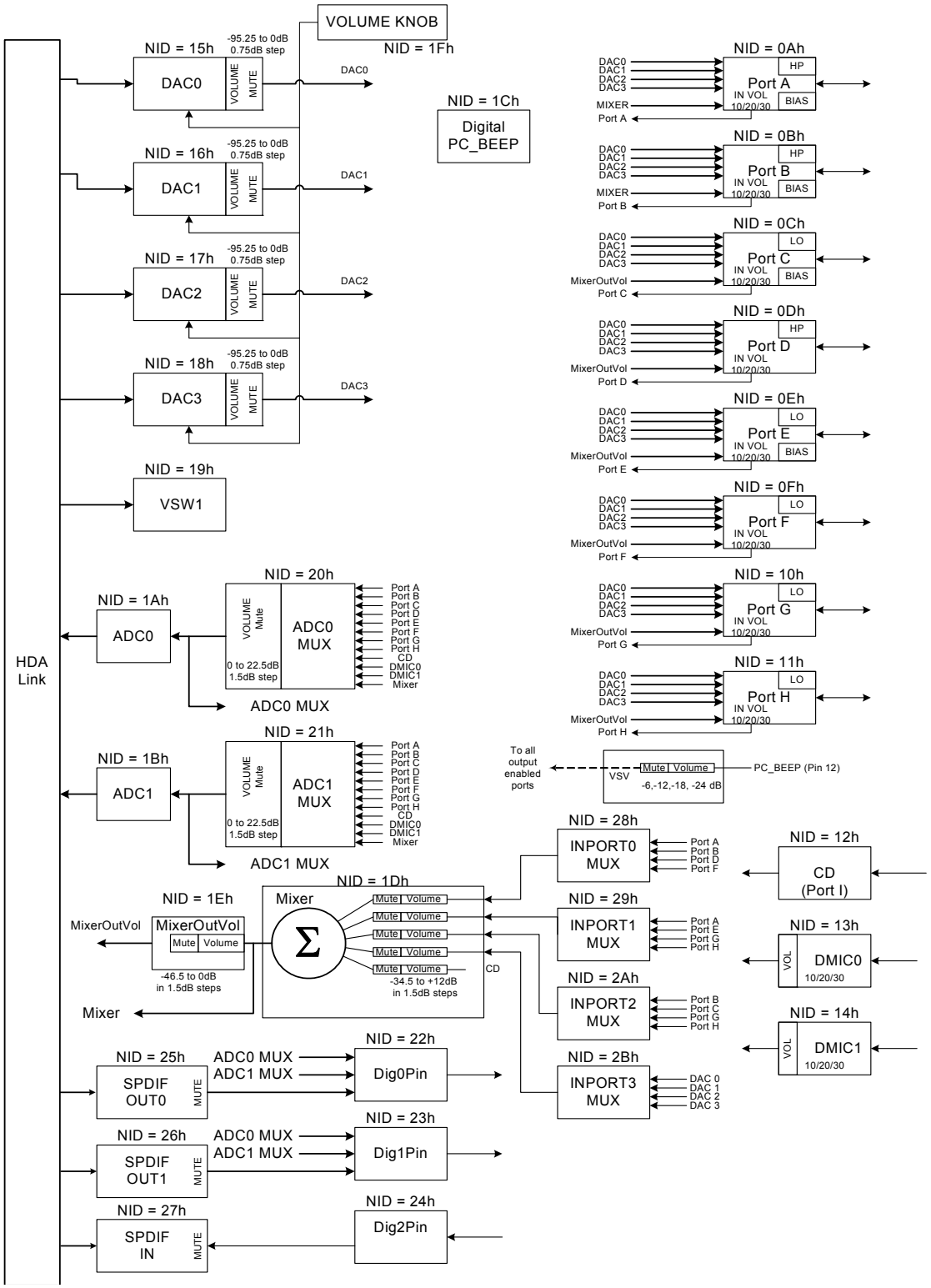


Figure 12. Widget Diagram

5.1. Widget List

ID	Widget Name	Description
00h	Root	Root Node
01h	AFG	Audio Function Group
0Ah	Port A	Port A Pin Widget (Configurable as HP, Line Out, Line In, Mic)
0Bh	Port B	Port B Pin Widget (Configurable as HP, Line Out, Line In, Mic)
0Ch	Port C	Port C Pin Widget (Configurable as Line In, Mic, Line Out)
0Dh	Port D	Port D Pin Widget (Configurable as HP, Line Out, Line In, Mic)
0Eh	Port E	Port E Pin Widget (Configurable as Line In, Mic, Line Out)
0Fh	Port F	Port F Pin Widget (Configurable as Line In, Mic, Line Out)
10h	Port G	Port G Pin Widget (Configurable as Line In, Mic, Line Out)
11h	Port H	Port H Pin Widget (Configurable as Line In, Mic, Line Out)
12h	CD (Port I)	CD Pin Widget (Configurable as Line In)
13h	DigMic0	Digital Microphone 0 Pin Widget
14h	DigMic1	Digital Microphone 1 Pin Widget
15h	DAC0	Stereo Output Converter to DAC
16h	DAC1	Stereo Output Converter to DAC
17h	DAC2	Stereo Output Converter to DAC
18h	DAC3	Stereo Output Converter to DAC (or Vendor Specific Widget)
19h	RSVD	Reserved
1Ah	ADC0	Stereo Input Converter to ADC
1Bh	ADC1	Stereo Input Converter to ADC
1Ch	PCBeep	Digital PC Beep
1Dh	Mixer	Mixer (Input Ports, DACs, Analog PC_Beep)
1Eh	MixerOutVol	Mixer Out Volume
1Fh	VolumeKnob	External Volume Control
20h	ADC0Mux	ADC0 Mux with volume and mute
21h	ADC1Mux	ADC1 Mux with volume and mute
22h	Dig0Pin	Digital Output Pin (pin48)
23h	Dig1Pin	Secondary Digital Output Pin (pin 40)
24h	Dig2Pin	EAPD and Digital Input Pin (Pin 47)
25h	SPDIFOut0	Stereo Output for SPDIF_Out
26h	SPDIFOut1	Second Stereo Output for SPDIF_Out
27h	SPDIFIn	Stereo converter widget for SPDIF_In

Table 17. High Definition Audio Widget

ID	Widget Name	Description
28h	InPort0Mux	Input port pre-select for mixer
29h	InPort1Mux	input port pre-select for mixer
2Ah	InPort2Mux	input port pre-select for mixer
2Bh	InPort3Mux	input port pre-select for mixer

Table 17. High Definition Audio Widget

5.2. Pin Configuration Default Register Settings

The configuration default registers are 32-bit registers required for each pin widget. These registers are normally used by the CODEC driver to determine the configuration of jacks and devices attached to the CODEC. When the CODEC is powered on, these registers are loaded with the default values provided by IDT for typical system usage, and are loaded in a way that is compatible with the Microsoft Universal Audio Architecture (UAA) driver. The values can be overridden by IDT customers according to their system configuration. Table 18 shows the Pin Widget Configuration Default settings

The settings reflect the Consumer Desktop use model with:

•Independent Front Headphone and Microphone for real time communication

•7.1 audio output at the rear

•Rear Microphone and Line Input jacks

•Optical SPDIF input and output jacks at the rear

•HDMI

•Digital Microphones are connected as a 4-mic array (Volume Knob Widget is visible, but inactive)

•Analog CD input is connected to an internal ATAPI connector.

.

Pin Name	Port	Location	Device	Connection	Color	Misc	Assoc.	Seq
PortAPin	Connect to Jack 00b	Mainboard Front 2h	HP Out 2h	1/8 inch Jack 1h	Green 4h	Jack Detect Override=0	3h	0h
PortBPin	Connect to Jack 00b	Mainboard Front 2h	Mic In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override=0	4h	0h
PortCPin	Connect to Jack 00b	Mainboard Rear 1h	Mic In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override=0	2h	0h
PortDPin	Connect to Jack 00b	Mainboard Rear 1h	Line Out 0h	1/8 inch Jack 1h	Green 4h	Jack Detect Override=0	1h	0h
PortEPin	Connect to Jack 00b	Mainboard Rear 1h	Line In 8h	1/8 inch Jack 1h	Blue 3h	Jack Detect Override=0	2h	Eh
PortFPin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
MonoOutPin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h

Table 18. Pin Configuration Default Settings

Pin Name	Port	Location	Device	Connection	Color	Misc	Assoc.	Seq
DigOutPin0	Connect to Jack 00b	Mainboard Rear 000001b	SPDIF Out 4h	optical 5h	Gray 2h	Jack Detect Override=0	5h	0h
DigOutPin1	Connect to Jack 10b	Internal 011000b	Digital Other Out 5h	Other Digital 6h	Unknown 0h	Jack Detect Override=0	6h	0h
DigOutPin2	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
DigMic0Pin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
DigMic1Pin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
Analog PC_BEEP Pin	Not Connected 01b	NA 000000b	Other Fh	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h

Table 18. Pin Configuration Default Settings

6. WIDGET INFORMATION

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:16]	BITS [15:0]
Reserved	CODEC Address	NID	Verb ID (4-bit)	Payload Data (16-bit)

Table 19. Command Format for Verb with 4-bit Identifier

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:8]	BITS [7:0]
Reserved	CODEC Address	NID	Verb ID (12-bit)	Payload Data (8-bit)

Table 20. Command Format for Verb with 12-bit Identifier

There are two types of responses: Solicited and Unsolicited. Solicited responses are provided as a direct response to an issued command and will be provided in the frame immediately following the command. Unsolicited responses are provided by the CODEC independent of any command. Unsolicited responses are the result of CODEC events such as a jack insertion detection. The formats for Solicited Responses and Unsolicited Responses are shown in the tables below. The “Tag” field in bits [31:28] of the Unsolicited Response identify the event.

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:0]
Valid (Valid = 1)	UnSol = 0	Reserved	Response

Table 21. Solicited Response Format

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:28]	BITS [27:0]
Valid (Valid = 1)	UnSol = 1	Reserved	Tag	Response

Table 22. Unsolicited Response Format

6.1. Root Node (NID = 00)

)

6.1.1. Root VendorID

	Verb ID	Payload	Response
Get	F00	00	See bitfield table.

6.1.1.1. Root VendorID

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Vendor	R	111D	Vendor ID.
[15.:8]	DeviceFix	R	76	Device ID 7674h
[7.:0]	DeviceProg	R	74	Device ID 7674h

6.1.2. Root RevID

	Verb ID	Payload	Response
Get	F00	02	See bitfield table.

6.1.2.1. Root RevID

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd	R	00	Reserved.
[23.:20]	Major	R	1	Compliant HDAudio spec major revision.
[19.:16]	Minor	R	0	Compliant HDAudio spec minor revision
[15.:12]	RevisionFix	R	0	Vendors rev number for this device.
[11.:8]	RevisionProg	R	1	Vendors rev number for this device.
[7.:4]	SteppingFix	R	0	Vendor RevID.
[3.:0]	SteppingProg	R	1	Vendor RevID.

6.1.2.2. Root NodeInfo

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:16]	StartNID	R	01	Starting node number (NID) of first function group
[15.:8]	Rsvd1	R	00	Reserved.
[7.:0]	TotalNodes	R	01	Total number of nodes

6.2. AFG Node (NID = 01

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6.2.1. AFG Reset

	Verb ID	Payload	Response
Get			See bitfield table.

6.2.1.1. AFG Reset

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd1	R	000000	Reserved.
[7.:0]	Execute	W	00	Function Reset.

6.2.2. AFG NodeInfo

	Verb ID	Payload	Response
Get	F00	04	See bitfield table.

6.2.2.1. AFG NodeInfo

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:16]	StartNID	R	0A	Starting node number for function group subordinate nodes.
[15.:8]	Rsvd1	R	00	Reserved.
[7.:0]	TotalNodes	R	22	Total number of nodes.

6.2.3. AFG FGType

	Verb ID	Payload	Response
Get	F00	05	See bitfield table.

6.2.3.1. AFG FGType

Bit	Bitfield Name	RW	Reset	Description
[31.:9]	Rsvd	R	000000	Reserved.
[8]	UnSol	R	1	Unsolicited response supported: 1 = yes 0 = no.
[7.:0]	NodeType	R	1	Function group type: 00h = Reserved; 01h = Audio Function Group; 02h = Vendor Defined Modem Function Group; 03h-7Fh = Reserved; 80h-FFh = Vendor Defined Function Group

6.2.4. AFG AFGCap

	Verb ID	Payload	Response
Get	F00	08	See bitfield table.

6.2.4.1. AFG AFGCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd3	R	00	Reserved.
[16]	BeepGen	R	1	Beep generator present: 1 = yes 0 = no.
[15.:12]	Rsvd2	R	0	Reserved.
[11.:8]	InputDelay	R	D	Typical latency in frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link.
[7.:4]	Rsvd1	R	0	Reserved.
[3.:0]	OutputDelay	R	D	Typical latency in frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin.

6.2.5. AFG PCMCap

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

6.2.5.1. AFG PCMCap

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	000	Reserved.
[20]	B32	R	0	32 bit audio format support: 1 = yes 0 = no.
[19]	B24	R	1	24 bit audio format support: 1 = yes 0 = no.
[18]	B20	R	1	20 bit audio format support: 1 = yes 0 = no.
[17]	B16	R	1	16 bit audio format support: 1 = yes 0 = no.
[16]	B8	R	0	8 bit audio format support: 1 = yes 0 = no.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	R12	R	0	384kHz rate support: 1 = yes 0 = no.
[10]	R11	R	1	192kHz rate support: 1 = yes 0 = no.
[9]	R10	R	1	176.4kHz rate support: 1 = yes 0 = no.
[8]	R9	R	1	96kHz rate support: 1 = yes 0 = no.
[7]	R8	R	1	88.2kHz rate support: 1 = yes 0 = no.
[6]	R7	R	1	48kHz rate support: 1 = yes 0 = no.
[5]	R6	R	1	44.1kHz rate support: 1 = yes 0 = no.
[4]	R5	R	0	32kHz rate support: 1 = yes 0 = no.
[3]	R4	R	0	22.05kHz rate support: 1 = yes 0 = no.
[2]	R3	R	0	16kHz rate support: 1 = yes 0 = no.

6.2.5.1. AFG PCMCap

Bit	Bitfield Name	RW	Reset	Description
[1]	R2	R	0	11.025kHz rate support: 1 = yes 0 = no.
[0]	R1	R	0	8kHz rate support: 1 = yes 0 = no.

6.2.6. AFG StreamCap

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

6.2.6.1. AFG StreamCap

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	00000000	Reserved.
[2]	AC3	R	0	AC-3 formatted data support: 1 = yes 0 = no.
[1]	Float32	R	0	Float32 formatted data support: 1 = yes 0 = no.
[0]	PCM	R	1	PCM-formatted data support: 1 = yes 0 = no.

6.2.7. AFG InAmpCap

	Verb ID	Payload	Response
Get	F00	0D	See bitfield table.

6.2.7.1. AFG InAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	27	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.

6.2.7.1. AFG InAmpCap

Bit	Bitfield Name	RW	Reset	Description
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	03	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

6.2.8. AFG PwrStateCap

	Verb ID	Payload	Response
Get	F00	0F	See bitfield table.

6.2.8.1. AFG PwrStateCap

Bit	Bitfield Name	RW	Reset	Description
[31.:4]	Rsvd	R	0000000	Reserved.
[3]	D3Sup	R	1	D3 power state support: 1 = yes 0 = no.
[2]	D2Sup	R	1	D2 power state support: 1 = yes 0 = no.
[1]	D1Sup	R	1	D1 power state support: 1 = yes 0 = no.
[0]	D0Sup	R	1	D0 power state support: 1 = yes 0 = no.

6.2.9. AFG GPIOCnt

	Verb ID	Payload	Response
Get	F00	11	See bitfield table.

6.2.9.1. AFG GPIOCnt

Bit	Bitfield Name	RW	Reset	Description
[31]	GPIWake	R	1	Wake capability. Assuming the Wake Enable Mask controls are enabled GPIOs configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin.
[30]	GPIUnsol	R	1	GPIO unsolicited response support: 1 = yes 0 = no.
[29.:24]	Rsvd	R	00	Reserved.
[23.:16]	NumGPIs	R	00	Number of GPI pins supported by function group.
[15.:8]	NumGPOs	R	00	Number of GPO pins supported by function group.
[7.:0]	NumGPIOs	R	08	Number of GPIO pins supported by function group.

6.2.10. AFG OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

6.2.10.1. AFG OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	02	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.

6.2.10.1. AFG OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[14.:8]	NumSteps	R	7F	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	7F	Indicates which step is 0dB

6.2.11. AFG PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

6.2.11.1. AFG PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

6.2.12. AFG UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.2.12.1. AFG UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.

6.2.12.1. AFG UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.2.13. AFG GPIO

	Verb ID	Payload	Response
Get	F15	00	See bitfield table.

6.2.13.1. AFG GPIO

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Data7	RW	0	Data for GPIO7. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[6]	Data6	RW	0	Data for GPIO6. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[5]	Data5	RW	0	Data for GPIO5. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[4]	Data4	RW	0	Data for GPIO4. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22

6.2.13.1. AFG GPIO

Bit	Bitfield Name	RW	Reset	Description
[3]	Data3	RW	0	Data for GPIO3. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[2]	Data2	RW	0	Data for GPIO2. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[1]	Data1	RW	0	Data for GPIO1. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22
[0]	Data0	RW	0	Data for GPIO0. If this GPIO bit is configured as Sticky (edge-sensitive) input it can be cleared by writing "0". For details of read back value refer to HD Audio spec. section 7.3.3.22

6.2.14. AFG GPIOEn

	Verb ID	Payload	Response
Get	F16	00	See bitfield table.

6.2.14.1. AFG GPIOEn

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mask7	RW	0	Enable for GPIO7: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[6]	Mask6	RW	0	Enable for GPIO6: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control

6.2.14.1. AFG GPIOEn

Bit	Bitfield Name	RW	Reset	Description
[5]	Mask5	RW	0	Enable for GPIO5: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[4]	Mask4	RW	0	Enable for GPIO4: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[3]	Mask3	RW	0	Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[2]	Mask2	RW	0	Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[1]	Mask1	RW	0	Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[0]	Mask0	RW	0	Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control

6.2.15. AFG GPIODir

	Verb ID	Payload	Response
Get	F17	00	See bitfield table.

6.2.15.1. AFG GPIODir

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Control7	RW	0	Direction control for GPIO7: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[6]	Control6	RW	0	Direction control for GPIO6: 0 = GPIO is configured as input; 1 = GPIO is configured as output

6.2.15.1. AFG GPIODir

Bit	Bitfield Name	RW	Reset	Description
[5]	Control5	RW	0	Direction control for GPIO5: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[4]	Control4	RW	0	Direction control for GPIO4: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[3]	Control3	RW	0	Direction control for GPIO3: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[2]	Control2	RW	0	Direction control for GPIO2: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[1]	Control1	RW	0	Direction control for GPIO1: 0 = GPIO is configured as input; 1 = GPIO is configured as output
[0]	Control0	RW	0	Direction control for GPIO0: 0 = GPIO is configured as input; 1 = GPIO is configured as output

6.2.16. AFG GPIOWakeEn

	Verb ID	Payload	Response
Get	F18	00	See bitfield table.

6.2.16.1. AFG GPIOWakeEn

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	W7	RW	0	Wake enable for GPIO7: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.

6.2.16.1. AFG GPIOWakeEn

Bit	Bitfield Name	RW	Reset	Description
[6]	W6	RW	0	Wake enable for GPIO6: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[5]	W5	RW	0	Wake enable for GPIO5: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[4]	W4	RW	0	Wake enable for GPIO4: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[3]	W3	RW	0	Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[2]	W2	RW	0	Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[1]	W1	RW	0	Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.
[0]	W0	RW	0	Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted) a wake-up event will trigger a Status Change Request event on the link.

6.2.17. AFG GPIOUnsol

	Verb ID	Payload	Response
Get	F19	00	See bitfield table.

6.2.17.1. AFG GPIOUnsol

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	EnMask7	RW	0	Unsolicited enable mask for GPIO7. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[6]	EnMask6	RW	0	Unsolicited enable mask for GPIO6. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[5]	EnMask5	RW	0	Unsolicited enable mask for GPIO5. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[4]	EnMask4	RW	0	Unsolicited enable mask for GPIO4. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[3]	EnMask3	RW	0	Unsolicited enable mask for GPIO3. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.

6.2.17.1. AFG GPIOUnsol

Bit	Bitfield Name	RW	Reset	Description
[2]	EnMask2	RW	0	Unsolicited enable mask for GPIO2. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO2 is configured as input and changes state.
[1]	EnMask1	RW	0	Unsolicited enable mask for GPIO1. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO1 is configured as input and changes state.
[0]	EnMask0	RW	0	Unsolicited enable mask for GPIO0. If set and the Unsolicited Response control for this widget has been enabled an unsolicited response will be sent when GPIO0 is configured as input and changes state.

6.2.18. AFG GPIOSticky

	Verb ID	Payload	Response
Get	F1A	00	See bitfield table.

6.2.18.1. AFG GPIOSticky

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mask7	RW	0	GPIO7 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[6]	Mask6	RW	0	GPIO6 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).

6.2.18.1. AFG GPIOSticky

Bit	Bitfield Name	RW	Reset	Description
[5]	Mask5	RW	0	GPIO5 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[4]	Mask4	RW	0	GPIO4 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[3]	Mask3	RW	0	GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[2]	Mask2	RW	0	GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[1]	Mask1	RW	0	GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).
[0]	Mask0	RW	0	GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive).

6.2.19. AFG SubID

	Verb ID	Payload	Response
Get	F20	00	See bitfield table.

6.2.19.1. AFG SubID

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Subsys3	RW	00	Subsystem ID (byte 3)
[23.:16]	Subsys2	RW	00	Subsystem ID (byte 2)
[15.:8]	Subsys1	RW	01	Subsystem ID (byte 1)
[7.:0]	Assembly	RW	00	Assembly ID (Not applicable to codec vendors).

6.2.20. AFG GPIOPIrty

	Verb ID	Payload	Response
Get	F70	00	See bitfield table.

6.2.20.1. AFG GPIOPIrty

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	GP7	RW	1	GPIO7 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[6]	GP6	RW	1	GPIO6 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[5]	GP5	RW	1	GPIO5 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[4]	GP4	RW	1	GPIO4 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[3]	GP3	RW	1	GPIO3 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[2]	GP2	RW	1	GPIO2 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected

6.2.20.1. AFG GPIOPlrty

Bit	Bitfield Name	RW	Reset	Description
[1]	GP1	RW	1	GPIO1 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected
[0]	GP0	RW	1	GPIO0 Polarity: If configured as output or non-sticky input: 0 = inverting; 1 = non-inverting. If configured as sticky input: 0 = falling edges will be detected; 1 = rising edges will be detected

6.2.21. AFG GPIODrive

	Verb ID	Payload	Response
Get	F71	00	See bitfield table.

6.2.21.1. AFG GPIODrive

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	OD7	RW	0	GPIO7 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[6]	OD6	RW	0	GPIO6 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[5]	OD5	RW	0	GPIO5 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[4]	OD4	RW	0	GPIO4 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[3]	OD3	RW	0	GPIO3 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).

6.2.21.1. AFG GPIODrive

Bit	Bitfield Name	RW	Reset	Description
[2]	OD2	RW	0	GPIO2 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[1]	OD1	RW	0	GPIO1 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0 float for 1).
[0]	OD0	RW	0	GPIO0 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open-drain (drive 0 float for 1).

6.2.22. AFG DMic

	Verb ID	Payload	Response
Get	F78	00	See bitfield table.

6.2.22.1. AFG DMic

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd	R	0000000	Reserved.
[5]	Mono1	RW	0	DMic1 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel).
[4]	Mono0	RW	0	DMic0 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel).
[3.:2]	PhAdj	RW	0	Selects what phase of the DMic clock the data should be latched: 0h = left data rising edge/right data falling edge; 1h = left data center of high/right data center of low; 2h = left data falling edge/right data rising edge; 3h = left data center of low/right data center of high
[1.:0]	Rate	RW	2	Selects the DMic clock rate: 0h = 4.704MHz; 1h = 3.528MHz; 2h = 2.352MHz; 3h = 1.176MHz.

6.2.23. AFG AnaBeep

	Verb ID	Payload	Response
Get	FEE	00	See bitfield table.

6.2.23.1. AFG AnaBeep

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	0000000	Reserved.
[2:1]	Gain	RW	3	Analog PCBeep Gain 0h=-18dB 1h=-12dB 2h=-6dB 3h=0dB
[0]	Enable	RW	0	Analog PCBeep enable 1=Analog PC Beep enabled 0=disabled

6.3. Port A Node (NID = 0A)

6.3.1. PortA WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.3.1.1. PortA WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

6.3.1.1. PortA WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.3.2. PortA PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.3.2.1. PortA PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	1	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

6.3.3. PortA ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.3.3.1. PortA ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.3.4. PortA ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.3.4.1. PortA ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	1E	InputMixer Summing widget (0x1E)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[14.:8]	ConL1	R	19	DAC1 Converter widget (0x19)
[7.:0]	ConL0	R	15	DAC0 Converter widget (0x15)

6.3.5. PortA ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.3.5.1. PortA ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.3.6. PortA PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.3.6.1. PortA PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	HPhnEn	RW	0	Headphone amp enable: 1 = enabled 0 = disabled.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[4.:3]	Rsvd1	R	0	Reserved.
[2.:0]	VRefEn	RW	0	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z, 001b= 50% 010b= GND, 011b= Reserved 100b= 80%, 101b= 100% 110b= Reserved, 111b= Reserved

6.3.7. PortA UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.3.7.1. PortA UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.3.8. PortA ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.3.8.1. PortA ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:1]	Impedence	R	3FFFFFFF	Impedance Sense Value (Bits 30:1): Measured impedence of the widget. An all ones value indicates an invalid sense reading
[0]	Execute	RW	1	Impedance Sense Value (Bit 0)/Trigger: Read = Impedance value bit 0 Write 0 = Impedance sense occurs using left channel Write 1 = Impedance sense occurs using right channel

6.3.9. PortA InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.3.9.1. PortA InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	00000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.3.10. PortA InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.3.10.1. PortA InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	00000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.3.11. PortA ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.3.11.1. PortA ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	02	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	2	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	Connection Type	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	4	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	3	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

6.4. PortB Node (NID = 0B)

6.4.1. PortB WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.4.1.1. PortB WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

6.4.1.1. PortB WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.4.2. PortB PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.4.2.1. PortB PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	17	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	1	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.

6.4.2.1. PortB PinCap

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	1	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	1	Impedance sense support: 1 = yes 0 = no.

6.4.3. PortB ConLstEntry0

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.4.3.1. PortB ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.4.4. PortB ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.4.4.1. PortB ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	1E	MixerOutVol Selector widget (0x1E)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[14.:8]	ConL1	R	18	DAC3 Converter widget (0x18)
[7.:0]	ConL0	R	15	DAC0 Converter widget (0x15)

6.4.5. PortB ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.4.5.1. PortB ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.4.6. PortB PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.4.6.1. PortB PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	0000000	Reserved.
[7]	HPhnEn	RW	0	Headphone amp enable: 1 = enabled, 0 = disabled.
[6]	OutEn	RW	0	Output enable: 1 = enabled, 0 = disabled.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:3]	Rsvd1	R	0	Reserved.
[2.:0]	VRefEn	RW	0	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z; 001b= 50%; 010b= GND; 011b= Reserved; 100b= 80%; 101b= 100%; 110b= Reserved; 111b= Reserved

6.4.7. PortB UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.4.7.1. PortB UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.4.8. PortB ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.4.8.1. PortB ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:1]	Impedence	R	3FFFFFFF	Impedance Sense Value (Bits 30:1): Measured impedence of the widget. An all ones value indicates an invalid sense reading
[0]	Execute	RW	1	Impedance Sense Value (Bit 0)/Trigger: Read = Impedance value bit 0 Write 0 = Impedance sense occurs using left channel Write 1 = Impedance sense occurs using right channel

6.4.9. PortB InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.4.9.1. PortB InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.4.10. PortD InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.4.10.1. PortD InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.4.11. PortB ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.4.11.1. PortB ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	02	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved

6.4.11.1. PortB ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[23.:20]	Device	RW	A	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	9	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	4	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

6.5. Port C Node (NID = 0C)

6.5.1. PortC WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.5.1.1. PortC WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.5.2. PortC PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.5.2.1. PortC PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	17	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	1	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	1	Impedance sense support: 1 = yes 0 = no.

6.5.3. PortC ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.5.3.1. PortC ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.5.4. PortC ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.5.4.1. PortC ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	17	InputMixer Summing widget (0x1E)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[14.:8]	ConL1	R	18	DAC3 Converter widget (0x18)
[7.:0]	ConL0	R	15	DAC0 Converter widget (0x15)

6.5.5. PortC ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.5.5.1. PortC ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.5.6. PortC PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.5.6.1. PortC PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:3]	Rsvd1	R	0	Reserved.
[2.:0]	VRefEn	RW	0	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z; 001b= 50%; 010b= GND; 011b= Reserved; 100b= 80%; 101b= 100%; 110b= Reserved; 111b= Reserved

6.5.7. PortC UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.5.7.1. PortC UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.5.8. PortC ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.5.8.1. PortC ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.

6.5.8.1. PortC ChSense

Bit	Bitfield Name	RW	Reset	Description
[30.:1]	Impedence	R	3FFFFFFF	Impedance Sense Value (Bits 30:1): Measured impedence of the widget. An all ones value indicates an invalid sense reading
[0]	Execute	RW	1	Impedance Sense Value (Bit 0)/Trigger: Read = Impedance value bit 0 Write 0 = Impedance sense occurs using left channel Write 1 = Impedance sense occurs using right channel

6.5.9. PortC InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.5.9.1. PortC InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	00000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.5.10. PortC InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.5.10.1. PortC InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	00000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.5.11. PortC ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.5.11.1. PortC ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	1	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved

6.5.11.1. PortC ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[23.:20]	Device	RW	8	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	3	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	2	Default assocation.
[3.:0]	Sequence	RW	1	Sequence.

6.6. Port D Node (NID = 0D)

6.6.1. PortD WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.6.1.1. PortD WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.6.2. PortD PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.6.2.1. PortD PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	1	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

6.6.3. PortD ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.6.3.1. PortD ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.6.4. PortD ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.6.4.1. PortD ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	1E	MixerOutVol Summing widget (0x1E)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[15.:8]	ConL1	R	18	DAC3 Converter widget (0x18)
[7.:0]	ConL0	R	15	DAC0 Converter widget (0x15)

6.6.5. PortD ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.6.5.1. PortD ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.6.6. PortD PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.6.6.1. PortD PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	HPhnEn	RW	0	Headphone amp enable: 1 = enabled, 0 = disabled.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:0]	Rsvd1	R	0	Reserved.

6.6.7. PortD UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.6.7.1. PortD UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.6.8. PortD ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.6.8.1. PortD ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.

6.6.8.1. PortD ChSense

Bit	Bitfield Name	RW	Reset	Description
[30.:1]	Impedence	R	3FFFFFFFh	Impedance Sense Value (Bits 30:1): Measured impedence of the widget. An all ones value indicates an invalid sense reading
[0]	Execute	RW	1	Impedance Sense Value (Bit 0)/Trigger: Read = Impedance value bit 0 Write 0 = Impedance sense occurs using left channel Write 1 = Impedance sense occurs using right channel

6.6.9. PortD InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.6.9.1. PortD InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.6.10. PortD InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.6.10.1. PortD InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.6.11. PortD ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.6.11.1. PortD ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	1	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	0	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other

6.6.11.1. PortD ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	4	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	1	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

6.7. PortE Node (NID = 0E)

6.7.1. PortE WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.7.1.1. PortE WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

6.7.1.1. PortE WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.7.2. PortE PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.7.2.1. PortE PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	17	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	1	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

6.7.3. PortE ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.7.3.1. PortE ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.7.4. PortE ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.7.4.1. PortE ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	1E	MixerOutVol Summing widget (0x1E)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[15.:8]	ConL1	R	18	DAC3 Converter widget (0x18)
[7.:0]	ConL0	R	15	DAC0 Converter widget (0x15)

6.7.5. PortE ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.7.5.1. PortE ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.7.6. PortE PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.7.6.1. PortE PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:3]	Rsvd1	R	0	Reserved.
[2.:0]	VRefEn	RW	0	Vref selection (See VrefCntrl field of PinCap parameter for supported selections): 000b= HI-Z; 001b= 50%; 010b= GND; 011b= Reserved; 100b= 80%; 101b= 100%; 110b= Reserved; 111b= Reserved

6.7.7. PortE UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.7.7.1. PortE UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.7.8. PortE ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.7.8.1. PortD ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:1]	Impedence	R	3FFFFFFFh	Impedance Sense Value (Bits 30:1): Measured impedence of the widget. An all ones value indicates an invalid sense reading
[0]	Execute	RW	1	Impedance Sense Value (Bit 0)/Trigger: Read = Impedance value bit 0 Write 0 = Impedance sense occurs using left channel Write 1 = Impedance sense occurs using right channel

6.7.9. PortE InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.7.9.1. PortE InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.7.10. PortE InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.7.10.1. PortE InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.7.11. PortE ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.7.11.1. PortE ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	1	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	A	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	9	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	2	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

6.8. PortF Node (NID = 0F)

6.8.1. PortF WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.8.1.1. PortF WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

6.8.1.1. PortF WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.8.2. PortF PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.8.2.1. PortF PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.

6.8.2.1. PortF PinCap

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	1	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	1	Impedance sense support: 1 = yes 0 = no.

6.8.3. PortF ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.8.3.1. PortF ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.8.4. PortF ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.8.4.1. PortF ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	17	InputMixer Summing widget (0x17)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[14.:8]	ConL1	R	11	DAC1 Converter widget (0x11)
[7.:0]	ConL0	R	10	DAC0 Converter widget (0x10)

6.8.5. PortF ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.8.5.1. PortF ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.8.6. PortF PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.8.6.1. PortF PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5]	InEn	RW	0	input enable: 1 = enabled 0 = disabled.
[4.:0]	Rsvd1	R	0	Reserved.

6.8.7. PortF UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.8.7.1. PortF UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.8.8. PortF ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.8.8.1. PortF ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:1]	Impedence	R	3FFFFFFFh	Impedance Sense Value (Bits 30:1): Measured impedence of the widget. An all ones value indicates an invalid sense reading
[0]	Execute	RW	1	Impedance Sense Value (Bit 0)/Trigger: Read = Impedance value bit 0 Write 0 = Impedance sense occurs using left channel Write 1 = Impedance sense occurs using right channel

6.8.9. PortF InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.8.9.1. PortF InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.8.10. PortF InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.8.10.1. PortF InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.9. PortG Node (NID = 10)

6.9.1. PortG WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.9.1.1. PortG WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.

6.9.1.1. PortG WCap

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.9.2. PortG PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.9.2.1. PortG PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.

6.9.2.1. PortG PinCap

Bit	Bitfield Name	RW	Reset	Description
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	1	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	1	Impedance sense support: 1 = yes 0 = no.

6.9.3. PortG ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.9.3.1. PortG ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.9.4. PortG ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.9.4.1. PortG ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	1E	MixerOutVol Selector widget (0x1E)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[14.:8]	ConL1	R	18	DAC3 Converter widget (0x18)
[7.:0]	ConL0	R	15	DAC0 Converter widget (0x15)

6.9.5. PortG ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.9.5.1. PortG ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.9.6. PortG PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.9.6.1. PortG PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5]	InEn	RW	0	input enable: 1 = enabled 0 = disabled.
[4.:0]	Rsvd1	R	0	Reserved.

6.9.7. PortG UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.9.7.1. PortG UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.9.8. PortG ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.9.8.1. PortG ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:1]	Impedence	R	3FFFFFFFh	Impedance Sense Value (Bits 30:1): Measured impedence of the widget. An all ones value indicates an invalid sense reading
[0]	Execute	RW	1	Impedance Sense Value (Bit 0)/Trigger: Read = Impedance value bit 0 Write 0 = Impedance sense occurs using left channel Write 1 = Impedance sense occurs using right channel

6.9.9. PortG InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.9.9.1. PortG InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.9.10. PortG InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.9.10.1. PortG InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.9.11. PortG ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.9.11.1. PortG ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	01	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	0	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	6	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other

6.9.11.1. PortG ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	1	Default assocation.
[3.:0]	Sequence	RW	1	Sequence.

6.10. PortH Node (NID = 11)

6.10.1. PortH WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.10.1.1. PortH WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.

6.10.1.1. PortH WCap

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.10.2. PortH PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.10.2.1. PortH PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.

6.10.2.1. PortH PinCap

Bit	Bitfield Name	RW	Reset	Description
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	1	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	1	Impedance sense support: 1 = yes 0 = no.

6.10.3. PortH ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.10.3.1. PortH ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.10.4. PortH ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.10.4.1. PortH ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	1Eh	MixerOutVol Selector widget (0x1E)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[14.:8]	ConL1	R	18	DAC3 Converter widget (0x18)
[7.:0]	ConL0	R	15	DAC0 Converter widget (0x15)

6.10.5. PortH ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.10.5.1. PortH ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.10.6. PortH PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.10.6.1. PortH PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5]	InEn	RW	0	input enable: 1 = enabled 0 = disabled.
[4.:0]	Rsvd1	R	0	Reserved.

6.10.7. PortH UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.10.7.1. PortH UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.10.8. PortH ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.10.8.1. PortH ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:1]	Impedence	R	3FFFFFFFh	Impedance Sense Value (Bits 30:1): Measured impedence of the widget. An all ones value indicates an invalid sense reading
[0]	Execute	RW	1	Impedance Sense Value (Bit 0)/Trigger: Read = Impedance value bit 0 Write 0 = Impedance sense occurs using left channel Write 1 = Impedance sense occurs using right channel

6.10.9. PortH InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.10.9.1. PortH InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.10.10. PortH InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.10.10.1. PortH InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.10.11. PortH ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.10.11.1. PortH ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	01	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	0	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	1	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	2	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other

6.10.11.1. PortH ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	1	Default assocation.
[3.:0]	Sequence	RW	4	Sequence.

6.11. PortI Node (NID = 12)

6.11.1. PortI WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.11.1.1. PortI WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.

6.11.1.1. PortI WCap

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	1	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.11.2. PortI PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.11.2.1. PortI PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.

6.11.2.1. PortI PinCap

Bit	Bitfield Name	RW	Reset	Description
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	1	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	1	Impedance sense support: 1 = yes 0 = no.

6.11.3. PortI PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.11.3.1. PortI PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	000000	Reserved.
[5]	InEn	RW	0	input enable: 1 = enabled 0 = disabled.
[4.:0]	Rsvd1	R	0	Reserved.

6.11.4. PortI UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.11.4.1. PortI UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.11.5. PortI ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.11.5.1. PortI ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:0]	Rsvd	R	00000000	Reserved

6.11.6. PortI ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.11.6.1. PortH ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	2	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	19	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	3	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	3	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	1	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	2	Default assocation.
[3.:0]	Sequence	RW	E	Sequence.

6.12. DMic0 Node (NID = 13)

6.12.1. DMic0 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.12.1.1. DMic0 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

6.12.1.1. DMic0 WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.12.2. DMic0 PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.12.2.1. DMic0 PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VRefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	0	Output support: 1 = yes 0 = no.
[3]	HPhnDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.

6.12.2.1. DMic0 PinCap

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

6.12.3. DMic0 PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.12.3.1. DMic0 PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:0]	Rsvd1	R	00	Reserved.

6.12.4. DMic0 InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.12.4.1. DMic0 InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.12.5. DMic0 InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.12.5.1. DMic0 InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.12.6. DMic0 ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.12.6.1. DMic0 ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	2	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	10	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved

6.12.6.1. DMic0 ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[23.:20]	Device	RW	A	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	3	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	7	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

6.13. DMic1 Node (NID = 14)

6.13.1. DMic1 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.13.1.1. DMic1 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.13.2. DMic1 PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.13.2.1. DMic1 PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VRefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	0	Output support: 1 = yes 0 = no.
[3]	HPhnDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

6.13.3. DMic1 PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.13.3.1. DMic1 PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5]	InEn	RW	0	Input enable: 1 = enabled 0 = disabled.
[4.:0]	Rsvd1	R	00	Reserved.

6.13.4. DMic1 InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.13.4.1. DMic1 InAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.13.5. DMic1 InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.13.5.1. DMic1 InAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd1	R	000000	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.13.6. DMic1 ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.13.6.1. DMic1 ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	2	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	10	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	A	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other

6.13.6.1. DMic1 ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	ConnectionType	RW	3	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	7	Default assocation.
[3.:0]	Sequence	RW	E	Sequence.

6.14. DAC0 Node (NID = 15)

6.14.1. DAC0 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.14.1.1. DAC0 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

6.14.1.1. DAC0 WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.14.2. DAC0 Cnvtr

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.

6.14.2.1. DAC0 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

6.14.3. DAC0 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.14.3.1. DAC0 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.14.4. DAC0 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

6.14.4.1. DAC0 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.14.5. DAC0 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

6.14.5.1. DAC0 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

6.14.6. DAC0 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

6.14.6.1. DAC0 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

6.14.7. DAC0 LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

6.14.7.1. DAC0 LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

6.15. DAC1 Node (NID = 16)

6.15.1. DAC1 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.15.1.1. DAC1 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).

6.15.1.1. DAC1 WCap

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.15.2. DAC1 Cnvtr

	Verb ID	Payload	Response
Get	A00	00	See bitfield table.

6.15.2.1. DAC1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.

6.15.2.1. DAC1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

6.15.3. DAC1 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.15.3.1. DAC1 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.

6.15.3.1. DAC1 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.15.4. DAC1 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

6.15.4.1. DAC1 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.15.5. DAC1 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

6.15.5.1. DAC1 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

6.15.6. DAC1 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

6.15.6.1. DAC1 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

6.15.7. DAC1 LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

6.15.7.1. DAC1 LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

6.16. DAC2 Node (NID = 17)

6.16.1. DAC2 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.16.1.1. DAC2 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).

6.16.1.1. DAC2 WCap

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.16.2. DAC2 Cnvtr

	Verb ID	Payload	Response
Get	A00	00	See bitfield table.

6.16.2.1. DAC2 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.

6.16.2.1. DAC2 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

6.16.3. DAC2 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.16.3.1. DAC2 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.

6.16.3.1. DAC2 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.16.4. DAC2 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

6.16.4.1. DAC2 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.16.5. DAC2 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

6.16.5.1. DAC2 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

6.16.6. DAC2 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

6.16.6.1. DAC2 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

6.16.7. DAC2 LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

6.16.7.1. DAC2 LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

6.17. DAC3 Node (NID = 18)

6.17.1. DAC3 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.17.1.1. DAC3 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).

6.17.1.1. DAC3 WCap

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.17.2. DAC3 Cnvtr

	Verb ID	Payload	Response
Get	A00	00	See bitfield table.

6.17.2.1. DAC3 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.

6.17.2.1. DAC3 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

6.17.3. DAC3 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.17.3.1. DAC3 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.

6.17.3.1. DAC3 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.17.4. DAC3 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

6.17.4.1. DAC3 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:0]	Gain	RW	7F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.17.5. DAC3 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

6.17.5.1. DAC3 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

6.17.6. DAC3 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

6.17.6.1. DAC3 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

6.17.7. DAC3 LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

6.17.7.1. DAC3 LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

6.18. Reserved (NID = 19)

6.19. ADC0 Node (NID = 1A)

6.19.1. ADC0 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.19.1.1. ADC0 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	1	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.

6.19.1.1. ADC0 WCap

Bit	Bitfield Name	RW	Reset	Description
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	1	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.19.2. ADC0 ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.19.2.1. ADC0 ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	01	Number of NID entries in connection list.

6.19.3. ADC0 ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.19.3.1. ADC0 ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	20	ADC0Mux Selector widget (0x20)

6.19.4. ADC0 Cnvtr

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.

6.19.4.1. ADC0 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved

6.19.4.1. ADC0 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

6.19.5. ADC0 ProcState

	Verb ID	Payload	Response
Get	F03	00	See bitfield table.

6.19.5.1. ADC0 ProcState

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	HPFOCDIS	RW	0	HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled.
[6.:2]	Rsvd1	R	00	Reserved.
[1.:0]	ADCHPFByp	RW	1	Processing State: 00b= bypass the ADC HPF ("off") 01b-11b= ADC HPF is enabled ("on" or "benign").

6.19.6. ADC0 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

6.19.6.1. ADC0 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

6.19.7. ADC0 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

6.19.7.1. ADC0 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

6.20. ADC1 Node (NID = 1B)

6.20.1. ADC1 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.20.1.1. ADC1 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	1	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	D	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	1	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	1	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

6.20.1.1. ADC1 WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.20.2. ADC1 ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.20.2.1. ADC1 ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	01	Number of NID entries in connection list.

6.20.3. ADC1 ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.20.3.1. ADC1 ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.

6.20.3.1. ADC1 ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	21	ADC1Mux widget (0x21)

6.20.4. ADC1 Cnvtr

	Verb ID	Payload	Response
Get	A00	00	See bitfield table.

6.20.4.1. ADC1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	StrmType	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.

6.20.4.1. ADC1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

6.20.5. ADC1 ProcState

	Verb ID	Payload	Response
Get	F03	00	See bitfield table.

6.20.5.1. ADC1 ProcState

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	HPFOCDIS	RW	0	HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled.
[6.:2]	Rsvd1	R	00	Reserved.
[1.:0]	ADCHPFByp	RW	1	Processing State: 00b= bypass the ADC HPF ("off") 01b-11b= ADC HPF is enabled ("on" or "benign").

6.20.6. ADC1 PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

6.20.6.1. ADC1 PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget.

6.20.7. ADC1 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

6.20.7.1. ADC1 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

6.21. DigBeep Node (NID = 1C)

6.21.1. DigBeep WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.21.1.1. DigBeep WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd3	R	00	Reserved.
[23.:20]	Type	R	7	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:4]	Rsvd2	R	0	Reserved.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes, no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes, 0 = no.
[1.:0]	Rsvd1	R	0	Reserved.

6.21.2. DigBeep OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

6.21.2.1. DigBeep OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes, 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	17	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	03	Number of gains steps (number of possible settings - 1).

6.21.2.1. DigBeep OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	03	Indicates which step is 0dB

6.21.3. DigBeep OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.21.3.1. DigBeep OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	0	Amp mute: 1 = muted, 0 = not muted.
[6.:2]	Rsvd1	R	00	Reserved.
[1.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this wid-get).

6.21.4. DigBeep Gen

	Verb ID	Payload	Response
Get	F0A	00	See bitfield table.

6.21.4.1. DigBeep Gen

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:0]	Divider	RW	00	Enable internal PC-Beep generation. Divider == 00h disables internal PC Beep generation and enables normal operation of the codec. Divider != 00h generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). This part can selectively generate tones with frequency = 48KHz * (257 - Divider) / 1024, yielding a linear range from 12kHz to 93.75Hz in steps of 46.875Hz. If the FreqShift bit is set, then the beep tones generated have frequency = 48KHz * (513 - Divider) / 1024, yielding a range of 24kHz to 12093.75Hz in steps of 46.875Hz.

6.22. Mixer Node (NID = 1D)

6.22.1. Mixer WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.22.1.1. MonoMixer WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	2	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.22.2. Mixer ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.22.2.1. Mixer ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.22.3. Mixer ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.22.3.1. Mixer ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	12	Port I Pin Widget (CD In) (0x12),. Uses InAmpLeft5/InAmpRight5 controls
[15]	ConL1Range	R	2B	1 = ConL0..ConL1 defines a range of selectable inputs.
[14.:8]	ConL1	R	2B	InPort3Mux Selector widget (0x2B). Uses InAmpLeft3/InAmpRight3 controls.
[7.:0]	ConL0	R	28	InPort0Mux Selector widget (0x28). Uses InAmpLeft0/InAmpRight0 controls.

6.22.4. Mixer InAmpCap

	Verb ID	Payload	Response
Get	F00	0D	See bitfield table.

6.22.4.1. Mixer InAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	05	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	1F	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	17	Indicates which step is 0dB

6.22.5. Mixer InAmpLeft0

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.22.5.1. Mixer InAmpLeft0

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.

6.22.5.1. Mixer InAmpLeft0

Bit	Bitfield Name	RW	Reset	Description
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.22.6. Mixer InAmpRight0

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.22.6.1. Mixer InAmpRight0

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.22.7. Mixer InAmpLeft1

	Verb ID	Payload	Response
Get	B20	01	See bitfield table.

6.22.7.1. Mixer InAmpLeft1

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.22.8. Mixer InAmpRight1

	Verb ID	Payload	Response
Get	B00	01	See bitfield table.

6.22.8.1. Mixer InAmpRight1

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.22.9. Mixer InAmpLeft2

	Verb ID	Payload	Response
Get	B20	02	See bitfield table.

6.22.9.1. Mixer InAmpLeft2

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.22.10. Mixer InAmpRight2

	Verb ID	Payload	Response
Get	B00	02	See bitfield table.

6.22.10.1. Mixer InAmpRight0

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.22.11. Mixer InAmpLeft3

	Verb ID	Payload	Response
Get	B20	03	See bitfield table.

6.22.11.1. Mixer InAmpLeft3

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.22.12. Mixer InAmpRight3

	Verb ID	Payload	Response
Get	B00	03	See bitfield table.

6.22.12.1. Mixer InAmpRight3

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.22.13. Mixer InAmpLeft4

	Verb ID	Payload	Response
Get	B20	04	See bitfield table.

6.22.13.1. Mixer InAmpLeft4

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.22.14. Mixer InAmpRight4

	Verb ID	Payload	Response
Get	B00	04	See bitfield table.

6.22.14.1. Mixer InAmpRight0

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	17	Amp gain step number (see InAmpCap parameter pertaining to this widget).

6.23. MixerOutVol Node (NID = 1E)

6.23.1. MixerOutVol WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.23.1.1. MonoMixer WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.23.2. MixerOutVol ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.23.2.1. MixerOutVol ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	1	Number of NID entries in connection list.

6.23.3. MixerOutVol ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.23.3.1. Mixer ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	1D	Mixer Summing widget (0x1D)

6.23.4. MixerOutVol OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

6.23.4.1. MixerOutVol OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	05	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	1F	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	1F	Indicates which step is 0dB

6.23.5. MixerOutVol OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.23.5.1. MixerOutVol OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.

6.23.5.1. MixerOutVol OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	1F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.23.6. MixerOutVol OutAmpRight0

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

6.23.6.1. MixerOutVol OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:5]	Rsvd1	R	0	Reserved.
[4.:0]	Gain	RW	1F	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.24. VolumeKnob Node (NID = 1F)

6.24.1. VolumeKnob WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.24.1.1. VolumeKnob WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	6	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:0]	Rsvd1	R	0	Reserved.

6.24.2. VolumeKnob VolKnobCap

	Verb ID	Payload	Response
Get	F00	13	See bitfield table.

6.24.2.1. VolumeKnob VolKnobCap

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Delta	R	1	Indicates if software can write a base volume to the Volume Control Knob.
[6.:0]	NumSteps	R	7F	Number of gains steps (number of possible settings - 1).

6.24.3. VolumeKnob ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.24.3.1. VolumeKnob ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	02	Number of NID entries in connection list.

6.24.4. VolumeKnob ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.24.4.1. VolumeKnob ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[14.:8]	ConL1	R	18	DAC3 Converter widget (0x18)
[7.:0]	ConL0	R	15	DAC0 Converter widget (0x15)

6.24.5. VolumeKnob UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.24.5.1. VolumeKnob UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled, 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.24.6. VolumeKnob Cntrl

	Verb ID	Payload	Response
Get	F0F	00	See bitfield table.

6.24.6.1. VolumeKnob Cntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	Direct	RW	0	Direct = 1 causes the volume control to directly control the hardware volume of the slave amps. Direct = 0 causes unsolicited responses to be generated.
[6.:0]	Volume	RW	7F	Volume, specified in steps of amplifier gain

6.24.7. VolumeKnob VS

	Verb ID	Payload	Response
Get	FE0	00	See bitfield table.

6.24.7.1. VolumeKnob VS

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	0000000	Reserved.
[4]	Continuous	RW	1	Allow continuous incrementing/decrementing of the volume knob value.
[3.:1]	Rate	RW	0	Volume knob update rate, for continuous mode and de-bouncing (0..7 = 2.5..20Hz, in increments of 2.5Hz)
[0]	Enable	RW	0	Volume knob enable: 0 = DMic uses external pins, 1 = Volume knob uses external pins.

6.25. ADC0Mux Node (NID = 20)

6.25.1. ADC0Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.25.1.1. ADC0Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.

6.25.1.1. ADC0Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParamOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.25.2. ADC0Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.25.2.1. ADC0Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.

6.25.2.1. ADC0Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.25.3. ADC0Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.25.3.1. ADC0Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry
[23.:16]	ConL2	R	1D	Mixer Summing widget (0x1D)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs
[14.:8]	ConL1	R	14	DMic1 Pin widget (0x14)
[7.:0]	ConL0	R	0A	Port A Pin widget (0x0A)

6.25.4. ADC0Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.25.4.1. ADC0Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.25.5. ADC0Mux LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

6.25.5.1. ADC0Mux LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

6.25.6. ADC0Mux OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

6.25.6.1. ADC0Mux OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	05	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	0F	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

6.25.7. ADC0Mux OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.25.7.1. ADC0Mux OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:4]	Rsvd1	R	0	Reserved.
[3.:0]	Gain	RW	0	Amp gain step number (see OutAmpCap parameter pertaining to this widget).

6.25.8. ADC0Mux OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

6.25.8.1. ADC0Mux OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:4]	Rsvd1	R	0	Reserved.
[3.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.26. ADC1Mux Node (NID = 21)

6.26.1. ADC1Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.26.1.1. ADC1Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

6.26.1.1. ADC1Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	1	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	DigitalStrm	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnsolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParamOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.26.2. ADC1Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.26.2.1. ADC1Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	04	Number of NID entries in connection list.

6.26.3. ADC1Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.26.3.1. ADC1Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry
[23.:16]	ConL2	R	1D	Mixer Summing widget (0x1D)
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs
[14.:8]	ConL1	R	14	DMic1 Pin widget (0x14)
[7.:0]	ConL0	R	0A	Port A Pin widget (0x0A)

6.26.4. ADC1Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.26.4.1. ADC1Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.26.5. ADC1Mux LR

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

6.26.5.1. ADC1Mux LR

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd2	R	00000000	Reserved.
[2]	SwapEn	RW	0	Swap enable: 1 = L/R swap enabled 0 = L/R swap disabled.
[1.:0]	Rsvd1	R	0	Reserved.

6.26.6. ADC1Mux OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

6.26.6.1. ADC1Mux OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	05	Size of each step in the gain range: 0 to 127 = .25dB to 32dB in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	0F	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

6.26.7. ADC1Mux OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.26.7.1. ADC1Mux OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:4]	Rsvd1	R	0	Reserved.
[3.:0]	Gain	RW	0	Amp gain step number (see OutAmpCap parameter pertaining to this widget).

6.26.8. ADC1Mux OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

6.26.8.1. ADC1Mux OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	1	Amp mute: 1 = muted 0 = not muted.
[6.:4]	Rsvd1	R	0	Reserved.
[3.:0]	Gain	RW	0	Amp gain step number (see OutAmp-Cap parameter pertaining to this widget).

6.27. Dig0Pin Node (NID = 22)

6.27.1. Dig0Pin WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.27.1.1. Dig0Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined

6.27.1.1. Dig0Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.27.2. Dig0Pin PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.27.2.1. Dig0Pin PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	0	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

6.27.3. Dig0Pin ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.27.3.1. Dig0Pin ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.27.4. Dig0Pin ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.27.4.1. Dig0Pin ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	21	ADC1Mux Summing widget (0x21)
[15.:8]	ConL1	R	20	ADC0Mux Summing widget (0x20)
[7.:0]	ConL0	R	25	SPDIFOut0 Converter widget (0x25)

6.27.5. Dig0Pin ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.27.5.1. Dig0Pin ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.27.6. Dig0Pin PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.27.6.1. Dig0Pin PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	00	Reserved.

6.27.7. Dig0Pin ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.27.7.1. Dig0Pin ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	1	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	4	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	5	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	1	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	5	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

6.28. Dig1Pin Node (NID = 23)

6.28.1. Dig1Pin WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.28.1.1. Dig1Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

6.28.1.1. Dig1Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.28.2. Dig1Pin PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.28.2.1. Dig1Pin PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	0	Input support: 1 = yes 0 = no.
[4]	OutCap	R	1	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	0	Presence detection support: 1 = yes 0 = no.

6.28.2.1. Dig1Pin PinCap

Bit	Bitfield Name	RW	Reset	Description
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

6.28.3. Dig1Pin ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.28.3.1. Dig1Pin ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	03	Number of NID entries in connection list.

6.28.4. Dig1Pin ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.28.4.1. Dig1Pin ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	21	ADC1Mux Summing widget (0x21)
[15.:8]	ConL1	R	20	ADC0Mux Summing widget (0x20)
[7.:0]	ConL0	R	26	SPDIFOut1 Converter widget (0x26)

6.28.5. Dig1Pin ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.28.5.1. Dig1Pin ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.28.6. Dig1Pin PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.28.6.1. Dig1Pin PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0000000	Reserved.
[6]	OutEn	RW	0	Output enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	00	Reserved.

6.28.7. Dig1Pin ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.28.7.1. Dig1Pin ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	2	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	18	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved

6.28.7.1. Dig1Pin ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[23.:20]	Device	RW	5	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	6	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	0	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	6	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

6.29. Dig2Pin Node (NID = 24)

6.29.1. Dig2Pin WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.29.1.1. Dig2Pin WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	4	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.29.2. Dig2Pin PinCap

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

6.29.2.1. Dig2Pin PinCap

Bit	Bitfield Name	RW	Reset	Description
[31.:17]	Rsvd2	R	0000	Reserved.
[16]	EapdCap	R	0	EAPD support: 1 = yes 0 = no.
[15.:8]	VrefCntrl	R	00	Vref support: bit 7 = Reserved; bit 6 = Reserved; bit 5 = 100% support (1 = yes 0 = no); bit 4 = 80% support (1 = yes 0 = no); bit 3 = Reserved; bit 2 = GND support (1 = yes 0 = no); bit 1 = 50% support (1 = yes 0 = no); bit 0 = Hi-Z support (1 = yes 0 = no)
[7]	Rsvd1	R	0	Reserved.
[6]	BalancedIO	R	0	Balanced I/O support: 1 = yes 0 = no.
[5]	InCap	R	1	Input support: 1 = yes 0 = no.
[4]	OutCap	R	0	Output support: 1 = yes 0 = no.
[3]	HdphDrvCap	R	0	Headphone amp present: 1 = yes 0 = no.
[2]	PresDtctCap	R	1	Presence detection support: 1 = yes 0 = no.
[1]	TrigRqd	R	0	Trigger required for impedance sense: 1 = yes 0 = no.
[0]	ImpSenseCap	R	0	Impedance sense support: 1 = yes 0 = no.

6.29.3. Dig2Pin PinWCntrl

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.

6.29.3.1. Dig2Pin PinWCntrl

Bit	Bitfield Name	RW	Reset	Description
[31.:7]	Rsvd2	R	0000000	Reserved.
[6]	1nEn	RW	0	input enable: 1 = enabled 0 = disabled.
[5.:0]	Rsvd1	R	00	Reserved.

6.29.4. Dig2Pin UnsolResp

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.

6.29.4.1. Dig2Pin UnsolResp

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	En	RW	0	Unsolicited response enable: 1 = enabled, 0 = disabled.
[6]	Rsvd1	R	0	Reserved.
[5.:0]	Tag	RW	00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

6.29.5. Dig2Pin ChSense

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.

6.29.5.1. Dig2Pin ChSense

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0	Presence detection indicator: 1 = presence detected; 0 = presence not detected.
[30.:0]	Rsvd	R	0	Reserved.

6.29.6. Dig2Pin PwrState

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.

6.29.6.1. Dig2Pin PwrState

Bit	Bitfield Name	RW	Reset	Description
[31.:6]	Rsvd2	R	0000000	Reserved.
[5.:4]	Act	R	3	Actual power state of this widget.
[3.:2]	Rsvd1	R	0	Reserved.
[1.:0]	Set	RW	3	Current power state setting for this widget, used for EAPD control in this case: 0h-1h = Pin drives the value of the EAPD control bit 2h-3h = Pin tri-stated

6.29.7. Dig2Pin EAPD

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.

6.29.7.1. Dig2Pin EAPD

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd2	R	00000000	Reserved.
[1]	Control	RW	0	EAPD value reflected on the EAPD pin: 0 = Power down external amplifier; 1 = Power up external amplifier
[0]	Rsvd1	R	0	Reserved.

6.29.8. Dig2Pin ConfigDefault

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.

6.29.8.1. Dig2Pin ConfigDefault

Bit	Bitfield Name	RW	Reset	Description
[31.:30]	PortConnectivity	RW	0	Port connectivity: 0h = Port complex is connected to a jack; 1h = No physical connection for port; 2h = Fixed function device is attached; 3h = Both jack and internal device attached (info in all other fields refers to integrated device any presence detection refers to jack)
[29.:24]	Location	RW	01	Location. Bits [5..4]: 0h = External on primary chassis; 1h = Internal; 2h = Separate chassis; 3h = Other. Bits [3..0]: 0h = N/A; 1h = Rear; 2h = Front; 3h = Left; 4h = Right; 5h = Top; 6h = Bottom; 7h-9h = Special; Ah-Fh = Reserved
[23.:20]	Device	RW	C	Default device: 0h = Line out; 1h = Speaker; 2h = HP out; 3h = CD; 4h = SPDIF Out; 5h = Digital other out; 6h = Modem line side; 7h = Modem handset side; 8h = Line in; 9h = Aux; Ah = Mic in; Bh = Telephony; Ch = SPDIF In; Dh = Digital other in; Eh = Reserved; Fh = Other
[19.:16]	ConnectionType	RW	5	Connection type: 0h = Unknown; 1h = 1/8" stereo/mono; 2h = 1/4" stereo/mono; 3h = ATAPI internal; 4h = RCA; 5h = Optical; 6h = Other digital; 7h = Other analog; 8h = Multichannel analog (DIN); 9h = XLR/Professional; Ah = RJ-11 (modem); Bh = Combination; Ch-Eh = Reserved; Fh = Other
[15.:12]	Color	RW	2	Color: 0h = Unknown; 1h = Black; 2h = Grey; 3h = Blue; 4h = Green; 5h = Red; 6h = Orange; 7h = Yellow; 8h = Purple; 9h = Pink; Ah-Dh = Reserved; Eh = White; Fh = Other
[11.:8]	Misc	RW	0	Miscellaneous: Bits [3..1] = Reserved; Bit 0 = Jack detect override
[7.:4]	Association	RW	8	Default assocation.
[3.:0]	Sequence	RW	0	Sequence.

6.30. SPDIFOut0 Node (NID = 25)

6.30.1. SPDIFOut0 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.30.1.1. SPDIFOut0 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	4	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	1	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes 0 = no.

6.30.1.1. SPDIFOut0 WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.30.2. SPDIFOut0 PCMCap

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

6.30.2.1. SPDIFOut0 PCMCap

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	000	Reserved.
[20]	B32	R	0	32 bit audio format support: 1 = yes, 0 = no.
[19]	B24	R	1	24 bit audio format support: 1 = yes, 0 = no.
[18]	B20	R	1	20 bit audio format support: 1 = yes, 0 = no.
[17]	B16	R	1	16 bit audio format support: 1 = yes, 0 = no.
[16]	B8	R	0	8 bit audio format support: 1 = yes, 0 = no.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	R12	R	0	384kHz rate support: 1 = yes, 0 = no.
[10]	R11	R	1	192kHz rate support: 1 = yes, 0 = no.
[9]	R10	R	1	176.4kHz rate support: 1 = yes, 0 = no.
[8]	R9	R	1	96kHz rate support: 1 = yes, 0 = no.
[7]	R8	R	1	88.2kHz rate support: 1 = yes, 0 = no.

6.30.2.1. SPDIFOut0 PCMCap

Bit	Bitfield Name	RW	Reset	Description
[6]	R7	R	1	48kHz rate support: 1 = yes, 0 = no.
[5]	R6	R	1	44.1kHz rate support: 1 = yes, 0 = no.
[4]	R5	R	0	32kHz rate support: 1 = yes, 0 = no.
[3]	R4	R	0	22.05kHz rate support: 1 = yes, 0 = no.
[2]	R3	R	0	16kHz rate support: 1 = yes, 0 = no.
[1]	R2	R	0	11.025kHz rate support: 1 = yes, 0 = no.
[0]	R1	R	0	8kHz rate support: 1 = yes, 0 = no.

6.30.3. SPDIFOut0 StreamCap

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

6.30.3.1. SPDIFOut0 StreamCap

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	00000000	Reserved.
[2]	AC3	R	1	AC-3 formatted data support: 1 = yes, 0 = no.
[1]	Float32	R	0	Float32 formatted data support: 1 = yes, 0 = no.
[0]	PCM	R	1	PCM-formatted data support: 1 = yes, 0 = no.

6.30.4. SPDIFOut0 Cnvtr

	Verb ID	Payload	Response
Get	A00	00	See bitfield table.

6.30.4.1. SPDIFOut0 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	FrmtNonPCM	RW	0	Stream type: 1 = Non-PCM, 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

6.30.5. SPDIFOut0 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

6.30.5.1. SPDIFOut0 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off", 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).

6.30.6. SPDIFOut0 DigCnvtr

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table.

6.30.6.1. SPDIFOut0 DigCnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	Rsvd1	R	0	Reserved.
[14.:8]	CC	RW	00	CC: Category Code.
[7]	L	RW	0	L: Generation Level.
[6]	PRO	RW	0	PRO: Professional.
[5]	AUDIO	RW	0	/AUDIO: Non-Audio.
[4]	COPY	RW	0	COPY: Copyright.

6.30.6.1. SPDIFOut0 DigCnvtr

Bit	Bitfield Name	RW	Reset	Description
[3]	PRE	RW	0	PRE: Preemphasis.
[2]	VCFG	RW	0	VCFG: Validity Config.
[1]	V	RW	0	V: Validity.
[0]	DigEn	RW	0	Digital enable: 1 = converter enabled, 0 = converter disable.

6.30.7. SPDIFOut0 OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

6.30.7.1. SPDIFOut0 OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes, 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	17	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	00	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	03	Indicates which step is 0dB

6.30.8. SPDIFOut0 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.30.8.1. SPDIFOut0 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	0	Amp mute: 1 = muted, 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

6.30.9. SPDIFOut0 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

6.30.9.1. SPDIFOut0 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	0	Amp mute: 1 = muted, 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

6.31. SPDIFOut1 Node (NID = 26)

6.31.1. SPDIFOut1 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.31.1.1. SPDIFOut1 WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	0	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	4	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes, 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes, 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital), 0 = no (analog).
[8]	ConnList	R	0	Connection list present: 1 = yes, 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes, 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes, 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes, 0 = no.
[4]	FormatOvrd	R	1	Stream format override: 1 = yes, 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes, no.
[2]	OutAmpPrsnt	R	1	Output amp present: 1 = yes, 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes, 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo), 0 = no (mono).

6.31.2. SPDIFOut1 PCMCap

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

6.31.2.1. SPDIFOut1 PCMCap

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	000	Reserved.
[20]	B32	R	0	32 bit audio format support: 1 = yes, 0 = no.
[19]	B24	R	1	24 bit audio format support: 1 = yes, 0 = no.
[18]	B20	R	1	20 bit audio format support: 1 = yes, 0 = no.
[17]	B16	R	1	16 bit audio format support: 1 = yes, 0 = no.
[16]	B8	R	0	8 bit audio format support: 1 = yes, 0 = no.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	R12	R	0	384kHz rate support: 1 = yes, 0 = no.
[10]	R11	R	1	192kHz rate support: 1 = yes, 0 = no.
[9]	R10	R	1	176.4kHz rate support: 1 = yes, 0 = no.
[8]	R9	R	1	96kHz rate support: 1 = yes, 0 = no.
[7]	R8	R	1	88.2kHz rate support: 1 = yes, 0 = no.
[6]	R7	R	1	48kHz rate support: 1 = yes, 0 = no.
[5]	R6	R	1	44.1kHz rate support: 1 = yes, 0 = no.
[4]	R5	R	0	32kHz rate support: 1 = yes, 0 = no.
[3]	R4	R	0	22.05kHz rate support: 1 = yes, 0 = no.
[2]	R3	R	0	16kHz rate support: 1 = yes, 0 = no.

6.31.2.1. SPDIFOut1 PCMCap

Bit	Bitfield Name	RW	Reset	Description
[1]	R2	R	0	11.025kHz rate support: 1 = yes, 0 = no.
[0]	R1	R	0	8kHz rate support: 1 = yes, 0 = no.

6.31.3. SPDIFOut1 StreamCap

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

6.31.3.1. SPDIFOut1 StreamCap

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	00000000	Reserved.
[2]	AC3	R	1	AC-3 formatted data support: 1 = yes, 0 = no.
[1]	Float32	R	0	Float32 formatted data support: 1 = yes, 0 = no.
[0]	PCM	R	1	PCM-formatted data support: 1 = yes, 0 = no.

6.31.4. SPDIFOut1 Cnvtr

	Verb ID	Payload	Response
Get	A00	00	See bitfield table.

6.31.4.1. SPDIFOut1 Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	FrmtNonPCM	RW	0	Stream type: 1 = Non-PCM, 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz, 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

6.31.5. SPDIFOut1 CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

6.31.5.1. SPDIFOut1 CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off", 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter).

6.31.6. SPDIFOut1 DigCnvtr

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table.

6.31.6.1. SPDIFOut1 DigCnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	Rsvd1	R	0	Reserved.
[14.:8]	CC	RW	00	CC: Category Code.
[7]	L	RW	0	L: Generation Level.
[6]	PRO	RW	0	PRO: Professional.
[5]	AUDIO	RW	0	/AUDIO: Non-Audio.
[4]	COPY	RW	0	COPY: Copyright.
[3]	PRE	RW	0	PRE: Preemphasis.
[2]	VCFG	RW	0	VCFG: Validity Config.

6.31.6.1. SPDIFOut1 DigCnvtr

Bit	Bitfield Name	RW	Reset	Description
[1]	V	RW	0	V: Validity.
[0]	DigEn	RW	0	Digital enable: 1 = converter enabled, 0 = converter disable.

6.31.7. SPDIFOut1 OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

6.31.7.1. SPDIFOut1 OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes, 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	00	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	00	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

6.31.8. SPDIFOut1 OutAmpLeft

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.

6.31.8.1. SPDIFOut1 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	0	Amp mute: 1 = muted, 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

6.31.9. SPDIFOut1 OutAmpRight

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.

6.31.9.1. SPDIFOut1 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	0	Amp mute: 1 = muted, 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

6.32. SPDIFIn Node (NID = 27)

6.32.1. SPDIFOut1 WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.32.1.1. SPDIFInWCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	1	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	4	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes, 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes, 0 = no.
[9]	Dig	R	1	Digital stream support: 1 = yes (digital), 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes, 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes, 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes, 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes, 0 = no.
[4]	FormatOvrd	R	1	Stream format override: 1 = yes, 0 = no.
[3]	AmpParOvrd	R	1	Amplifier capabilities override: 1 = yes, no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes, 0 = no.
[1]	InAmpPrsnt	R	1	Input amp present: 1 = yes, 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo), 0 = no (mono).

6.32.2. SPDIFInCnvtr

	Verb ID	Payload	Response
Get	A00	00	See bitfield table.

6.32.2.1. SPFIDIn Cnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	FrmtNonPCM	R	0	Stream type: 1 = Non-PCM 0 = PCM.
[14]	FrmtSmplRate	RW	0	Sample base rate: 1 = 44.1kHz 0 = 48kHz.
[13.:11]	SmplRateMultp	RW	0	Sample base rate multiple: 000b= x1 (48kHz/44.1kHz or less); 001b= x2 (96kHz/88.2kHz/32kHz); 010b= x3 (144kHz); 011b= x4 (192kHz/176.4kHz); 100b-111b Reserved
[10.:8]	SmplRateDiv	RW	0	Sample base rate divider: 000b= Divide by 1 (48kHz/44.1kHz); 001b= Divide by 2 (24kHz/20.05kHz); 010b= Divide by 3 (16kHz/32kHz); 011b= Divide by 4 (11.025kHz); 100b= Divide by 5 (9.6kHz); 101b= Divide by 6 (8kHz); 110b= Divide by 7; 111b= Divide by 8 (6kHz)
[7]	Rsvd1	R	0	Reserved.
[6.:4]	BitsPerSmpl	RW	3	Bits per sample: 000b= 8 bits; 001b= 16 bits; 010b= 20 bits; 011b= 24 bits; 100b= 32 bits; 101b-111b= Reserved
[3.:0]	NmbrChan	RW	1	Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels.

6.32.3. SPDIFIn PCMCap

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

6.32.3.1. SPDIFIn PCMCap

Bit	Bitfield Name	RW	Reset	Description
[31.:21]	Rsvd2	R	000	Reserved.
[20]	B32	R	0	32 bit audio format support: 1 = yes, 0 = no.
[19]	B24	R	1	24 bit audio format support: 1 = yes, 0 = no.
[18]	B20	R	1	20 bit audio format support: 1 = yes, 0 = no.
[17]	B16	R	1	16 bit audio format support: 1 = yes, 0 = no.
[16]	B8	R	0	8 bit audio format support: 1 = yes, 0 = no.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	R12	R	0	384kHz rate support: 1 = yes, 0 = no.
[10]	R11	R	0	192kHz rate support: 1 = yes, 0 = no.
[9]	R10	R	0	176.4kHz rate support: 1 = yes, 0 = no.
[8]	R9	R	1	96kHz rate support: 1 = yes, 0 = no.
[7]	R8	R	0	88.2kHz rate support: 1 = yes, 0 = no.
[6]	R7	R	1	48kHz rate support: 1 = yes, 0 = no.
[5]	R6	R	1	44.1kHz rate support: 1 = yes, 0 = no.
[4]	R5	R	0	32kHz rate support: 1 = yes, 0 = no.
[3]	R4	R	0	22.05kHz rate support: 1 = yes, 0 = no.
[2]	R3	R	0	16kHz rate support: 1 = yes, 0 = no.

6.32.3.1. SPDIFIn PCMCap

Bit	Bitfield Name	RW	Reset	Description
[1]	R2	R	0	11.025kHz rate support: 1 = yes, 0 = no.
[0]	R1	R	0	8kHz rate support: 1 = yes, 0 = no.

6.32.4. SPDIFIn StreamCap

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

6.32.4.1. SPDIFIn StreamCap

Bit	Bitfield Name	RW	Reset	Description
[31.:3]	Rsvd	R	00000000	Reserved.
[2]	AC3	R	1	AC-3 formatted data support: 1 = yes, 0 = no.
[1]	Float32	R	0	Float32 formatted data support: 1 = yes, 0 = no.
[0]	PCM	R	1	PCM-formatted data support: 1 = yes, 0 = no.

6.32.5. SPDIFIn ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.32.5.1. SPDIFIn ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	01	Number of NID entries in connection list.

6.32.6. SPDIFIn ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.32.6.1. ADC0 ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry.
[23.:16]	ConL2	R	00	Unused list entry.
[15.:8]	ConL1	R	00	Unused list entry.
[7.:0]	ConL0	R	24	Dig2Pin pin widget (0x24).

6.32.7. SPDIFIn CnvtrID

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.

6.32.7.1. SPDIFIn CnvtrID

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7.:4]	Strm	RW	0	Stream ID: 0h = Converter "off" 1h-Fh = valid IDs.
[3.:0]	Ch	RW	0	Channel assignment ("Ch" and "Ch+1" assigned as a pair for a stereo converter).

6.32.8. SPDIFIn DigCnvtr

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table.

6.32.8.1. SPDIFIn DigCnvtr

Bit	Bitfield Name	RW	Reset	Description
[31.:16]	Rsvd2	R	0000	Reserved.
[15]	Rsvd1	R	0	Reserved.
[14.:8]	CC	RW	00	CC: Category Code.
[7]	L	RW	0	L: Generation Level.
[6]	PRO	RW	0	PRO: Professional.
[5]	AUDIO	RW	0	/AUDIO: Non-Audio.
[4]	COPY	RW	0	COPY: Copyright.
[3]	PRE	RW	0	PRE: Preemphasis.
[2]	VCFG	RW	0	VCFG: Validity Config.

6.32.8.1. SPDIFIn DigCnvtr

Bit	Bitfield Name	RW	Reset	Description
[1]	V	RW	0	V: Validity.
[0]	DigEn	RW	0	Digital enable: 1 = converter enabled, 0 = converter disable.

6.32.9. SPDIFIn OutAmpCap

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

6.32.9.1. SPDIFIn OutAmpCap

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	1	Mute support: 1 = yes, 0 = no.
[30.:23]	Rsvd3	R	00	Reserved.
[22.:16]	StepSize	R	00	Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps.
[15]	Rsvd2	R	0	Reserved.
[14.:8]	NumSteps	R	00	Number of gains steps (number of possible settings - 1).
[7]	Rsvd1	R	0	Reserved.
[6.:0]	Offset	R	00	Indicates which step is 0dB

6.32.10. SPDIFIn InAmpLeft

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.

6.32.10.1. SPDIFOut1 OutAmpLeft

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	0	Amp mute: 1 = muted, 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

6.32.11. SPDIFIn InAmpRight

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.

6.32.11.1. SPDIFOut1 OutAmpRight

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd2	R	000000	Reserved.
[7]	Mute	RW	0	Amp mute: 1 = muted, 0 = not muted.
[6.:0]	Rsvd1	R	00	Reserved.

6.32.12. SPDIFIn VS

	Verb ID	Payload	Response
Get	FE0	00	See bitfield table.

6.32.12.1. SPDIFIn VS

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	0000000	Reserved.
[1]	RoundDis	RW	0	SPDIF Input rounding disable: 0 = rounding is enabled, 1 = rounding is disabled
[0]	LoLvlSel	RW	0	SPDIF Input level select: 0 = standard level, 1 = low level (input buffer enabled).

6.32.13. SPDIFIn Status

	Verb ID	Payload	Response
Get	FE0	80	See bitfield table.

6.32.13.1. SPDIFIn Status

Bit	Bitfield Name	RW	Reset	Description
[31.:29]	RcvSmplRate	R	7	Received Sample Rate: 000b = 44.1kHz 001b = 48kHz 010b = 88.2kHz 011b = 96kHz 100b = 176.4kHz 101b = 192kHz 11Xb = Invalid Rate
[28.:26]	Rsvd2	R	0	Reserved

6.32.13.1. SPDIFIn Status

Bit	Bitfield Name	RW	Reset	Description
[25.:22]	OrigFS	R	0	Original Sample Rate (per IEC60958-3 spec): 0000b = Original sampling frequency not indicated 0001b = 192kHz 0010b = 12kHz 0011b = 176.4kHz 0100b = Reserved 0101b = 96kHz 0110b = 8kHz 0111b = 88.2kHz 1000b = 16kHz 1001b = 24kHz 1010b = 11.025kHz 1011b = 22.05kHz 1100b = 32kHz 1101b = 48khz 1110b = Reserved 1111b = 44.1kHz
[21.:20]	CA	R	0	Clock Accuracy (per IEC60958-3 spec): 00b = Level II 01b = Level I 10b = Level III 11b = Reserved
[19.:16]	FS	R	0	Sample Rate (per IEC60958-3 spec): 0000b = 44.1kHz 0001b = Original sampling frequency not indicated 0010b = 48kHz 0011b = 32kHz 0100b = 22.05kHz 0101b = Reserved 0110b = 24kHz 0111b = Reserved 1000b = 88.2kHz 1001b = Reserved 1010b = 96kHz 1011b = Reserved 1100b = 176.4kHz 1101b = Reserved 1110b = 192kHz 1111b = Reserved

6.32.13.1. SPDIFIn Status

Bit	Bitfield Name	RW	Reset	Description
[15.:12]	CN	R	0	Channel Number (per IEC60958-3 spec): 0000b = Do not take into account 0001b = Channel 1 (Left channel for stereo channel format) 0010b = Channel 2 (Right channel for stereo channel format) 0011b-1111b = Channel 3-15
[11.:9]	SmplWrdL	R	0	Sample Word Length (per IEC60958-3 spec): 000b = Word length not indicated 001b = Max length - 4 010b = Max length - 2 011b = Reserved 100b = Max length - 1 101b = Max length - 0 110b = Max length - 3 111b = Reserved
[8]	MaxWrdL	R	0	Max Word Length (per IEC60958-3 spec): 0 = 20 bits, 1 = 24 bits.
[7]	NoBlkChk	RW	0	Disable Sample Block Checking
[6.:5}	Rsvd	R	0	Reserved
[4.:3]	ParityLimit	RW	0	SPDIFIn Parity Limit: 00b = 4 Parity errors 01b = 3 Parity errors 10b = 2 Parity errors 11b = 1 Parity error
[2]	SPRun	R	0	SPDIFIn Running 0 = no signal on SPDIFIn Pin, 1 = Signal on SPDIFIn pin.
[1]	SiPerr	RW	0	SPDIFIn Parity Error: 0 = No error detected, 1 = Error detected (write 0 to clear).
[0]	CopyInv	RW	0	Copyright Invert: 0 = Do not invert COPY bit, 1 = Invert COPY bit.

6.33. InPort0Mux Node (NID = 28)

6.33.1. InPort0Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.33.1.1. InPort0Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.

6.33.1.1. InPort0Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.33.2. InPort0Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.33.2.1. InPort0Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	04	Number of NID entries in connection list.

6.33.3. InPort0Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.33.3.1. InPort0Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	0F	Port F Pin widget (0x0F).
[23.:16]	ConL2	R	0D	Port D Pin widget (0x0D)

6.33.3.1. InPort0Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[15.:8]	ConL1	R	0B	Port B Pin widget (0x0B)
[7.:0]	ConL0	R	0A	Port A Pin widget (0x0A)

6.33.4. InPort0Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.33.4.1. InPort0Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.34. InPort1Mux Node (NID = 29)

6.34.1. InPort1Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.34.1.1. InPort1Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.34.2. InPort1Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.34.2.1. InPort1Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	04	Number of NID entries in connection list.

6.34.3. InPort1Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.34.3.1. InPort1Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	11	Port H Pin widget (0x11)
[23.:16]	ConL2	R	10	Port G Pin widget (0x10)
[15.:8]	ConL1	R	0E	Port E Pin widget (0x0E)
[7.:0]	ConL0	R	0A	Port A Pin widget (0x0A)

6.34.4. InPort1Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

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6.34.4.1. InPort1Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.35. InPort2Mux Node (NID = 2A)

6.35.1. InPort2Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.35.1.1. InPort2Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.

6.35.1.1. InPort2Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.35.2. InPort2Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.35.2.1. InPort2Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.

6.35.2.1. InPort2Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	04	Number of NID entries in connection list.

6.35.3. InPort2Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.35.3.1. InPort2Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	11	Port H Pin widget (0x11)
[23.:16]	ConL2	R	10	Port G Pin widget (0x10)
[15.:8]	ConL1	R	0C	Port C Pin widget (0x0C)
[7.:0]	ConL0	R	0B	Port B Pin widget (0x0B)

6.35.4. InPort1Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

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6.35.4.1. InPort1Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

6.36. InPort3Mux Node (NID = 2B)

6.36.1. InPort3Mux WCap

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

6.36.1.1. InPort3Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	Rsvd2	R	00	Reserved.
[23.:20]	Type	R	3	Widget type: 0h = Out Converter; 1h = In Converter; 2h = Summing (Mixer); 3h = Selector (Mux); 4h = Pin Complex; 5h = Power; 6h = Volume Knob; 7h = Beep Generator; 8h-Eh = Reserved; Fh = Vendor Defined
[19.:16]	Delay	R	0	Number of sample delays through widget.
[15.:12]	Rsvd1	R	0	Reserved.
[11]	SwapCap	R	0	Left/right swap support: 1 = yes 0 = no.
[10]	PwrCntrl	R	0	Power state support: 1 = yes 0 = no.
[9]	Dig	R	0	Digital stream support: 1 = yes (digital) 0 = no (analog).
[8]	ConnList	R	1	Connection list present: 1 = yes 0 = no.

6.36.1.1. InPort3Mux WCap

Bit	Bitfield Name	RW	Reset	Description
[7]	UnSolCap	R	0	Unsolicited response support: 1 = yes 0 = no.
[6]	ProcWidget	R	0	Processing state support: 1 = yes 0 = no.
[5]	Stripe	R	0	Striping support: 1 = yes 0 = no.
[4]	FormatOvrd	R	0	Stream format override: 1 = yes 0 = no.
[3]	AmpParOvrd	R	0	Amplifier capabilities override: 1 = yes no.
[2]	OutAmpPrsnt	R	0	Output amp present: 1 = yes 0 = no.
[1]	InAmpPrsnt	R	0	Input amp present: 1 = yes 0 = no.
[0]	Stereo	R	1	Stereo stream support: 1 = yes (stereo) 0 = no (mono).

6.36.2. InPort3Mux ConLst

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

6.36.2.1. InPort3Mux ConLst

Bit	Bitfield Name	RW	Reset	Description
[31.:8]	Rsvd	R	000000	Reserved.
[7]	LForm	R	0	Connection list format: 1 = long-form (15-bit) NID entries 0 = short-form (7-bit) NID entries.
[6.:0]	ConL	R	04	Number of NID entries in connection list.

6.36.3. InPort3Mux ConLstEntry0

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

6.36.3.1. InPort3Mux ConLstEntry0

Bit	Bitfield Name	RW	Reset	Description
[31.:24]	ConL3	R	00	Unused list entry
[23.:16]	ConL2	R	00	Unused list entry
[15]	ConL1Range	R	1	1 = ConL0..ConL1 defines a range of selectable inputs.
[14.:8]	ConL1	R	18	DAC3 (0x18)
[7.:0]	ConL0	R	15	DAC0 (0x15)

6.36.4. InPort3Mux ConSelectCtrl

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.

6.36.4.1. InPort3Mux ConSelectCtrl

Bit	Bitfield Name	RW	Reset	Description
[31.:2]	Rsvd	R	00000000	Reserved.
[1.:0]	Index	RW	0	Connection select control index.

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8. PINOUTS

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8.1. Pin Assignment

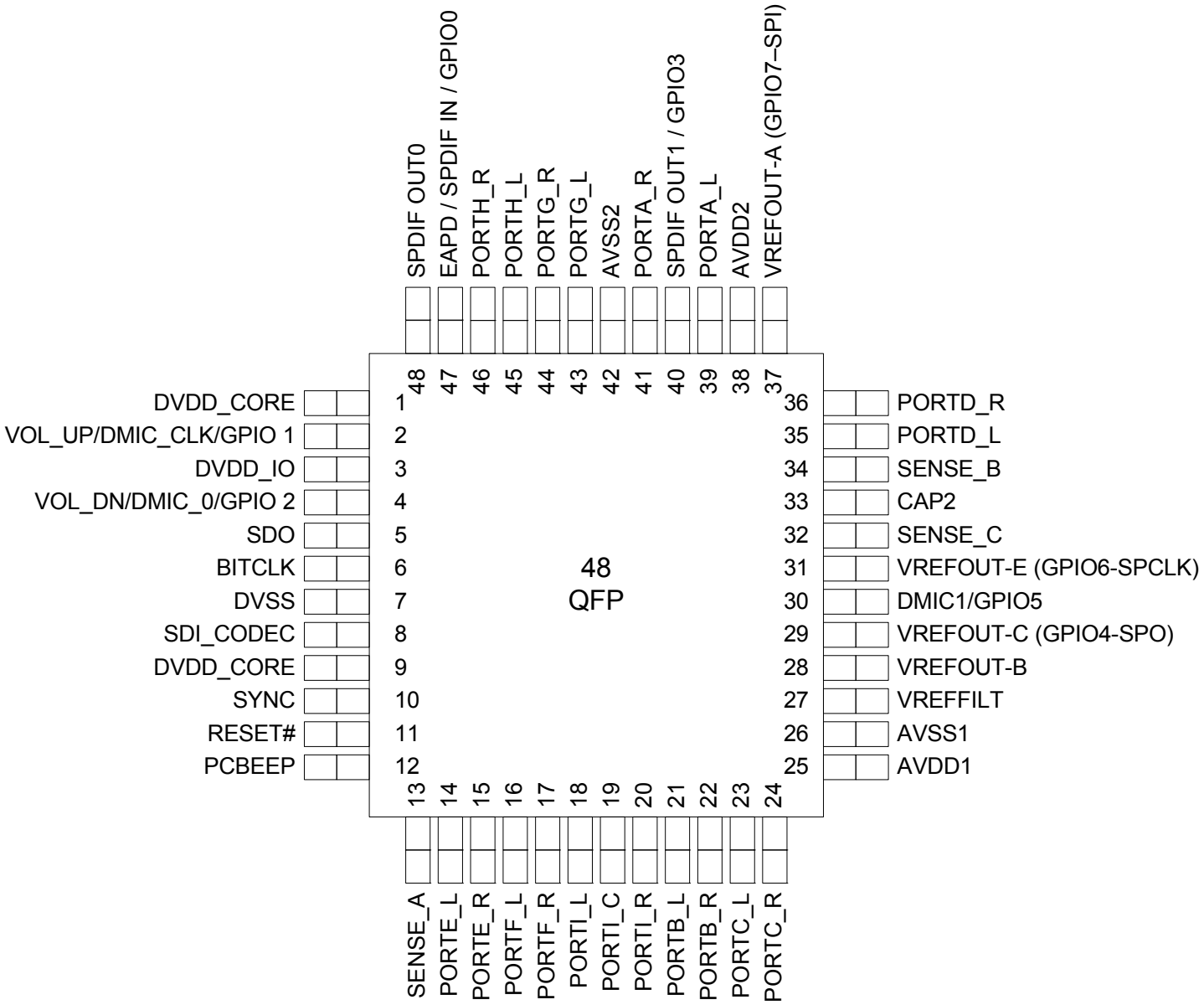


Figure 13. Pin Assignment

8.2. Pin Tables for 48-pin QFP

Pin Name	Pin Function	I/O	Internal Pull-up/Pull-down	48 pin location
Volume Up/DMIC_CLK/GPIO1	Volume Control **OR** Digital Mic clock output **OR** General Purpose I/O	I/O(Digital)	60k Pull-Up with Volume/GPIO or 60k Pull-down with Digital Mic	2
Volume Down/DMIC0/GPIO2	Volume Control **OR** Digital Mic 01 Input **OR** General Purpose I/O	I/O(Digital)	60k Pull-Up with Volume/GPIO or 60k Pull-down with Digital Mic	4
SDO	HD Audio Serial Data output (inbound stream)	I/O(Digital)	None	5
BITCLK	HD Audio Bit Clock	I(Digital)	None	6
SDI_CODEC	HD Audio Serial Data (outbound stream), audio module	I/O(Digital)	None	8
SYNC	HD Audio Frame Sync	I(Digital)	None	10
RESET#	HD Audio Reset	I(Digital)	None	11
DMIC 1 / GPIO5	Second digital mic input or Analog GPIO5	I/O(Analog)	60k Pull-Up with GPIO or 60k Pull-Down with Digital Mic	30
SPDIF OUT1	SECOND SPDIF OUT / Analog GPIO3	I/O(Analog)	60K Pull-Down with SPDIF or 60K pull-up with GPIO	40
GPIO0/EAPD/SPDIF-IN	General Purpose I/O,EAPD, SPDIF In	I/O(Digital)	60K Pull-Down with SPDIF-IN and EAPD, 60K Pull-Up with GPIO	47
S/PDIF-OUT0	SPDIF digital output (60K internal pull-down	O(Digital)	60K Pull-Down	48

Table 23. Digital Pins

Pin Name	Pin Function	I/O	Internal Pull-up/Pull-down	48 pin location
PCBEEP	Analog PC Beep	I(Analog)	None	12
SENSE_A	Jack insertion detection Ports A,B,C,D	I(Analog)	None	13
PORTE_L	Port E I/O Left	I/O(Analog)	None	14
PORTE_R	Port E I/O Right	I/O(Analog)	None	15

Table 24. Analog Pins

Pin Name	Pin Function	I/O	Internal Pull-up/Pull-down	48 pin location
PORTF_L	Port F I/O Left	I/O(Analog)	None	16
PORTF_R	Port F I/O Right	I/O(Analog)	None	17
PORTI_L	Port I Input Left	I(Analog)	None	18
PORTI_Comm	Port I signal Common	I(Analog)	None	19
PORTI_R	Port I Input Right	I(Analog)	None	20
PORTB_L (HP)	Port B I/O Left	I/O(Analog)	None	21
PORTB_R (HP)	Port B I/O Right	I/O(Analog)	None	22
PORTC_L	Port C I/O Left	I/O(Analog)	None	23
PORTC_R	Port C I/O Right	I/O(Analog)	None	24
VREFFILT	Analog Virtual Ground	O(Analog)	None	27
VREFOUT-B	Reference Voltage out drive (intended for mic bias) for Port B	O(Analog)	None	28
VREFOUT-C / GPIO4	Reference Voltage out drive (intended for mic bias) for Port C / Analog GPIO4	I/O(Analog)	60k Pull-Up with GPIO	29
VREFOUT-E / GPIO6	Reference Voltage out drive (intended for mic bias) for Port E / Analog GPIO6	I/O(Analog)	60k Pull-Up with GPIO	31
SENSE C	Jack insertion detection Port I	I(Analog)	None	32
CAP2	ADC reference Cap	O(Analog)	None	33
SENSE B	Jack insertion detection Ports E, F, G, H	I(Analog)	None	34
PORTD_L (HP)	Port D I/O Left	I/O(Analog)	None	35
PORTD_R (HP)	Port D I/O Right	I/O(Analog)	None	36
VREFOUT-A / GPIO7	Reference Voltage out drive (intended for mic bias) for Port A / Analog GPIO7	I/O(Analog)	60k Pull-Up with GPIO	37
PORTA_L (HP)	Port A Output Left	I/O(Analog)	None	39
PORTA_R (HP)	Port A I/O Right	I/O(Analog)	None	41
PORTG_L	Port G I/O Left	I/O(Analog)	None	43
PORTG_R	Port G I/O Right	I/O(Analog)	None	44
PORTH_L	Port H I/O Left	I/O(Analog)	None	45
PORTH_R	Port H I/O Right	I/O(Analog)	None	46

Table 24. Analog Pins

Pin Name	Pin Function	I/O	Internal Pull-up/Pull-down	48 pin location
DVDD_CORE	Digital Vdd = 3.3V	I(Digital)	None	1

Table 25. Power Pins

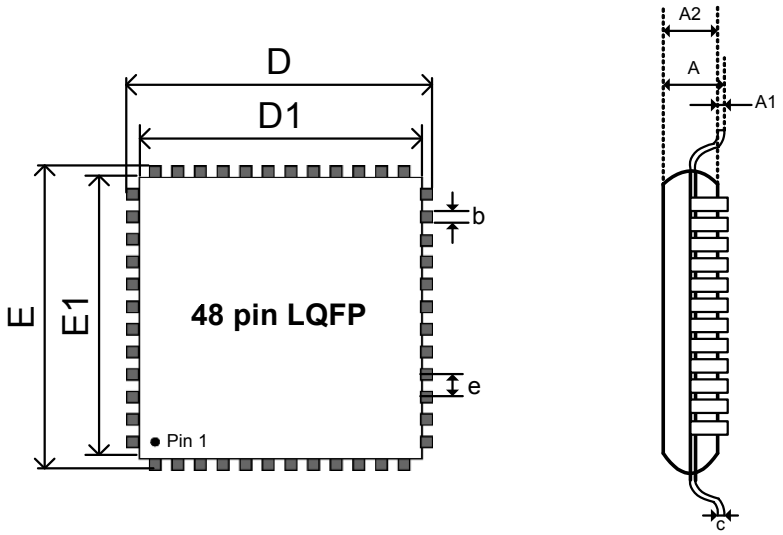
Pin Name	Pin Function	I/O	Internal Pull-up/Pull-down	48 pin location
DVDD_IO	Reference Voltage (1.5V or 3.3V)	I(Digital)	None	3
DVSS	Digital Ground	I(Digital)	None	7
DVDD_CORE	Digital Vdd= 3.3V	I(Digital)	None	9
AVDD1	Analog Vdd=5.0V or 3.3V	I(Analog)	None	25
AVSS1	Analog Ground	I(Analog)	None	26
AVDD2	Analog Vdd=5.0V or 3.3V	I(Analog)	None	38
AVSS2	Analog Ground	I(Analog)	None	42

Table 25. Power Pins

9. PACKAGE OUTLINE AND PACKAGE DIMENSIONS

Package dimensions are kept current with JEDEC Publication No. 95

9.1. 48-Pin QFP Package



Key	QFP Dimensions in mm		
	Min	Nom	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
L	0.45	0.60	0.75
e		0.50	
c	0.09	-	0.20
b	0.17	0.22	0.27

Figure 14. 48-pin QFP Package Drawing

10. SOLDER REFLOW PROFILE

10.1. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices" (www.jedec.org/download).

Profile Feature		Pb Free Assembly
Average Ramp-Up Rate (Ts_{max} - Tp)		3 °C / second max
Preheat:	Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (ts_{min} - ts_{max})	150 °C 200 °C 60 - 180 seconds
Time maintained above:	Temperature (T_L) Time (t_L)	217 °C 60 - 150 seconds
Peak / Classification Temperature (Tp)		See "Package Classification Reflow Temperatures"
Time within 5 °C of actual Peak Temperature (tp)		20 - 40 seconds
Ramp-Down rate		6 °C / second max
Time 25 °C to Peak Temperature		8 minutes max
Note: All temperatures refer to topside of the package, measured on the package body surface.		

Table 26. Standard Reflow Profile

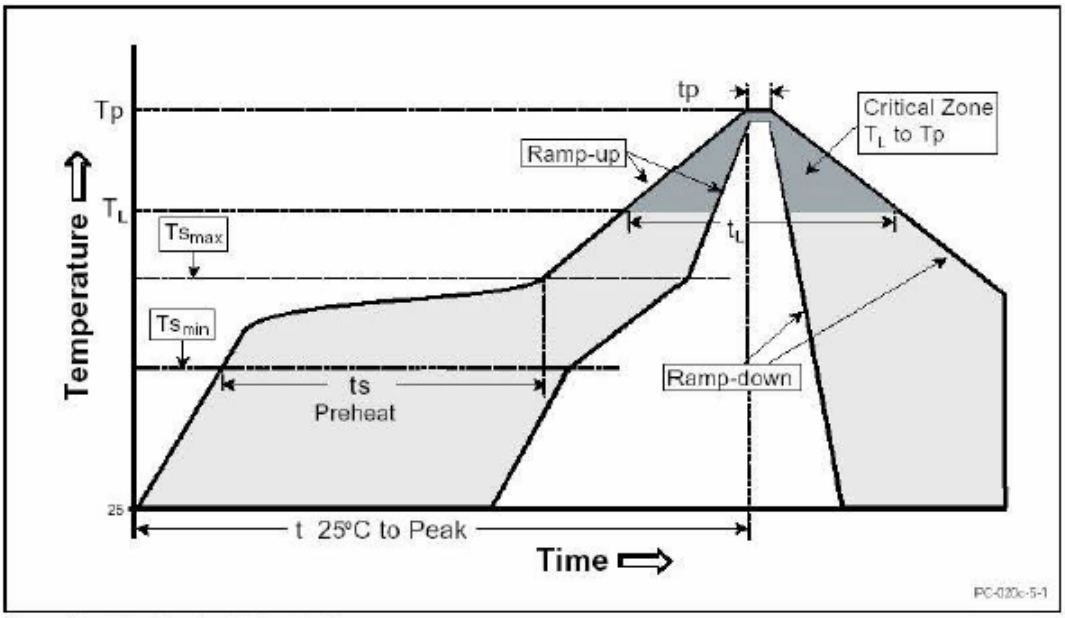


Figure 15. Solder Reflow Profile

10.2. Pb Free Process - Package Classification Reflow Temperatures

Package Type	MSL	Reflow Temperature
QFP 48-pin	3	260 ^{o}C

Table 27. Pb-Free Process Reflow

11. REVISION HISTORY

Revision	Date	Description of Change
0.5	April 25, 2007	Initial release
0.6	July 19, 2007	corrected type-os, replaced TBD in power consumption, updated widget and pinout description table and widget diagram, updated port configuration diagram
0.9	Oct 9, 2007	added detailed widget information, updated power consumption specification
0.91	Dec 14, 2007	updated Analog BC Peep description, updated the functional and widget diagrams for the new Analog PC Beep typology, added AnaBeep widget in AFG NID=-01h
1.0	March 19, 2008	removed preliminary, updated performance numbers
1.0	May 2011	Industrial temperature version created, 92HD73D1T
1.3	August 2011	Consolidated standard and Industrial Temp datasheets into one file. Set revision at 1.3 to match version of additional product family parts.

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