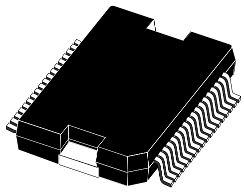
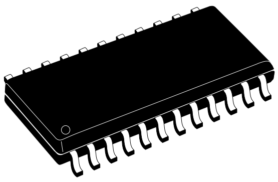
DMOS dual full bridge driver with PWM current controller

Datasheet - production data



PowerSO36



SO24
(20 + 2 + 2)

Ordering numbers:

L6227PD (PowerSO36)
L6227D (SO24)

Features

- Operating supply voltage from 8 to 52 V
- 2.8 A output peak current (1.4 A DC)
- $R_{DS(ON)}$ 0.73 Ω typ. value at T_j = 25 °C
- Operating frequency up to 100 KHz
- Non-dissipative overcurrent protection
- Dual independent constant t_{OFF} PWM current controllers
- Slow decay synchronous rectification
- Cross conduction protection
- Thermal shutdown
- Undervoltage lockout
- Integrated fast freewheeling diodes

Applications

- Bipolar stepper motor
- Dual DC motor

Description

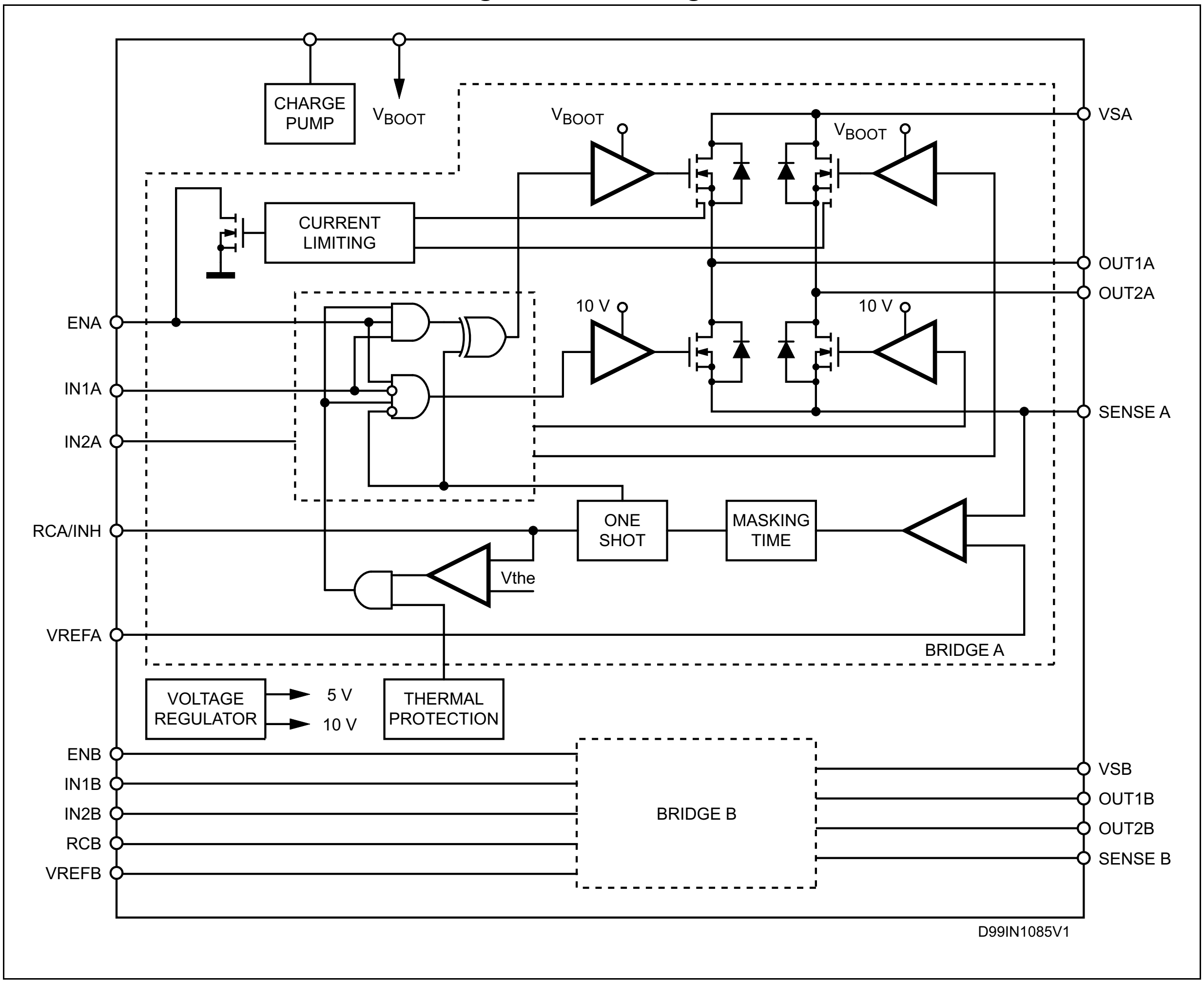
The L6227 device is a DMOS dual full bridge designed for motor control applications, realized in BCD technology, which combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip. The device also includes two independent constant off time PWM current controllers that performs the chopping regulation. Available in PowerSO36 and SO24 (20 + 2 + 2) packages, the L6227 device features a non-dissipative overcurrent protection on the high-side power MOSFETs and thermal shutdown.

This is information on a product in full production. www.st.com

Contents

1 Block diagram

Figure 1. Block diagram



2 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test conditions	Value	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	60	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S = 60$ V; $V_{SENSEA} = V_{SENSEB} = GND$	60	V
V_{BOOT}	Bootstrap peak voltage	$V_{SA} = V_{SB} = V_S$	$V_S + 10$	V
V_{IN}, V_{EN}	Input and enable voltage range	-	-0.3 to +7	V
V_{REFA}, V_{REFB}	Voltage range at pins V_{REFA} and V_{REFB}	-	-0.3 to +7	V
V_{RCA}, V_{RCB}	Voltage range at pins RC_A and RC_B	-	-0.3 to +7	V
V_{SENSEA}, V_{SENSEB}	Voltage range at pins $SENSE_A$ and $SENSE_B$	-	-1 to +4	V
$I_{S(peak)}$	Pulsed supply current (for each V_S pin), internally limited by the overcurrent protection	$V_{SA} = V_{SB} = V_S$; $t_{PULSE} < 1$ ms	3.55	A
I_S	RMS supply current (for each V_S pin)	$V_{SA} = V_{SB} = V_S$	1.4	A
T_{stg}, T_{OP}	Storage and operating temperature range	-	-40 to 150	°C

Table 2. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Max.	Unit
V_S	Supply voltage	$V_{SA} = V_{SB} = V_S$	8	52	V
V_{OD}	Differential voltage between VS_A, $OUT1_A$, $OUT2_A$, $SENSE_A$ and VS_B, $OUT1_B$, $OUT2_B$, $SENSE_B$	$V_{SA} = V_{SB} = V_S$; $V_{SENSEA} = V_{SENSEB}$	-	52	V
V_{REFA}, V_{REFB}	Voltage range at pins V_{REFA} and V_{REFB}	-	-0.1	5	V
V_{SENSEA}, V_{SENSEB}	Voltage range at pins $SENSE_A$ and $SENSE_B$	(pulsed $t_W < t_{rr}$) (DC)	-6 -1	6 1	V V
I_{OUT}	RMS output current	-	-	1.4	A
f_{sw}	Switching frequency	-	-	100	KHz

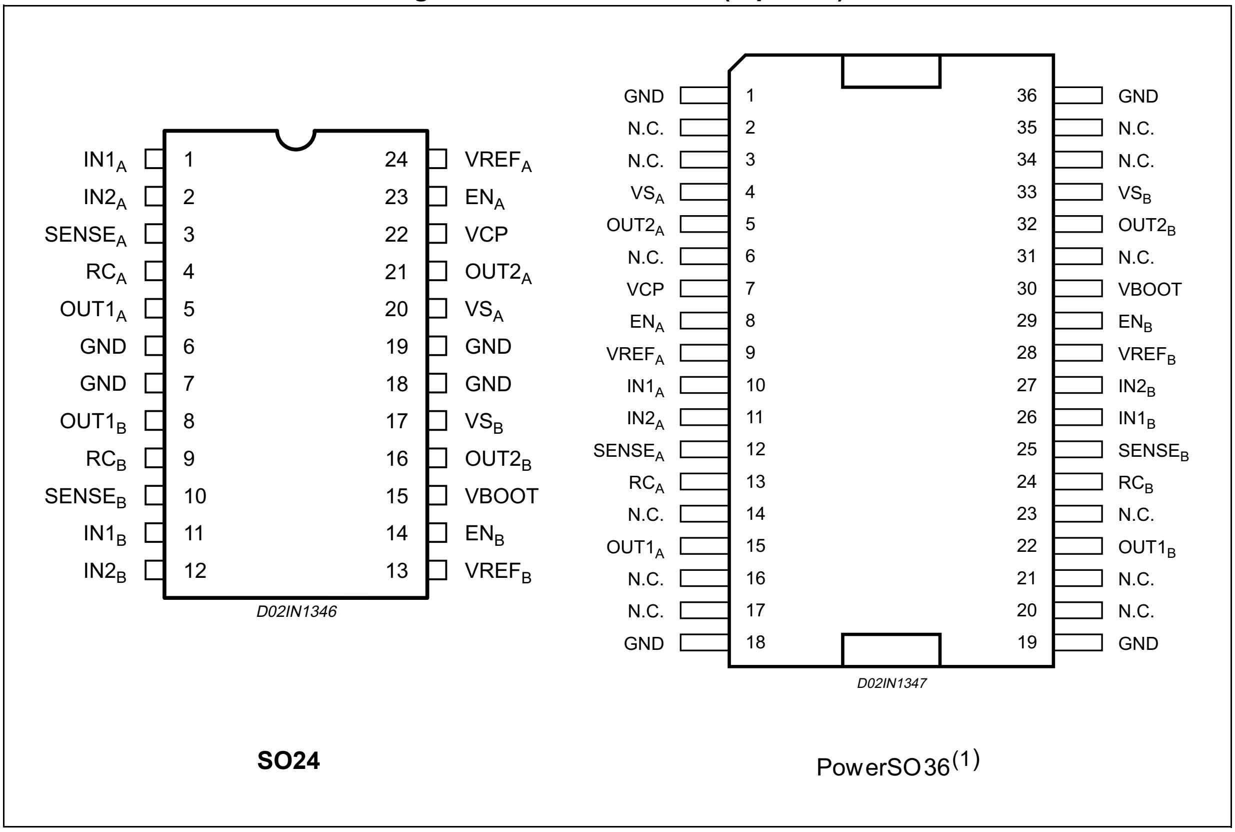
Table 3. Thermal data

Symbol	Description	SO24	PowerSO36	Unit
$R_{th\text{-}j\text{-}pins}$	Maximum thermal resistance junction pins	15	-	°C/W
$R_{th\text{-}j\text{-}case}$	Maximum thermal resistance junction case	-	2	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum thermal resistance junction ambient[(1)]	52	-	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum thermal resistance junction ambient[(2)]	-	36	°C/W
$R_{th\text{-}j\text{-}amb1}$	Maximum thermal resistance junction ambient[(3)]	-	16	°C/W
$R_{th\text{-}j\text{-}amb2}$	Maximum thermal resistance junction ambient[(4)]	78	63	°C/W

1. Mounted on a multilayer FR4 PCB with a dissipating copper surface on the bottom side of 6 cm^2 (with a thickness of 35 µm).
2. Mounted on a multilayer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm).
3. Mounted on a multilayer FR4 PCB with a dissipating copper surface on the top side of 6 cm^2 (with a thickness of 35 µm), 16 via holes and a ground layer.
4. Mounted on a multilayer FR4 PCB without any heat sinking surface on the board.

3 Pin connections

Figure 2. Pin connections (top view)



1. The slug is internally connected to pins 1, 18, 19 and 36 (GND pins).

Table 4. Pin description

Package		Name	Type	Function
SO24	PowerSO36			
Pin no.	Pin no.			
1	10	IN1$_A$	Logic input	Bridge A logic input 1.
2	11	IN2$_A$	Logic input	Bridge A logic input 2.
3	12	SENSE$_A$	Power supply	Bridge A source pin. This pin must be connected to power ground through a sensing power resistor.
4	13	RC$_A$	RC pin	RC network pin. A parallel RC network connected between this pin and ground sets the current controller OFF-time of the bridge A.
5	15	OUT1$_A$	Power output	Bridge A output 1.

Table 4. Pin description (continued)

Package SO24 Pin no.	Package PowerSO36 Pin no.	Name	Type	Function
6, 7, 18, 19	1, 18, 19, 36	GND	GND	Signal ground terminals. In SO packages, these pins are also used for heat dissipation toward the PCB.
8	22	$OUT1_B$	Power output	Bridge B output 1.
9	24	RC_B	RC pin	RC network pin. A parallel RC network connected between this pin and ground sets the current controller OFF-time of the bridge B.
10	25	$SENSE_B$	Power supply	Bridge B source pin. This pin must be connected to power ground through a sensing power resistor.
11	26	$IN1_B$	Logic input	Bridge B input 1
12	27	$IN2_B$	Logic input	Bridge B input 2
13	28	$VREF_B$	Analog input	Bridge B current controller reference voltage. Do not leave this pin open or connect to GND.
14	29	EN_B	Logic input(1)	Bridge B enable. LOW logic level switches OFF all power MOSFETs of bridge B. This pin is also connected to the collector of the overcurrent and thermal protection transistor to implement overcurrent protection. If not used, it has to be connected to +5 V through a resistor.
15	30	VBOOT	Supply voltage	Bootstrap voltage needed for driving the upper power MOSFETs of both bridge A and bridge B.
16	32	$OUT2_B$	Power output	Bridge B output 2.
17	33	VS_B	Power supply	Bridge B power supply voltage. It must be connected to the supply voltage together with pin VS_A.
20	4	VS_A	Power supply	Bridge A power supply voltage. It must be connected to the supply voltage together with pin VS_B.
21	5	$OUT2_A$	Power output	Bridge A output 2.
22	7	VCP	Output	Charge pump oscillator output.
23	8	EN_A	Logic input(1)	Bridge A enable. LOW logic level switches OFF all power MOSFETs of bridge A. This pin is also connected to the collector of the overcurrent and thermal protection transistor to implement overcurrent protection. If not used, it has to be connected to +5 V through a resistor.
24	9	$VREF_A$	Analog input	Bridge A current controller reference voltage. Do not leave this pin open or connect to GND.

1. Also connected at the output drain of the overcurrent and thermal protection MOSFET. Therefore, it has to be driven putting in series a resistor with a value in the range of 2.2 KΩ - 180 KΩ, recommended 100 KΩ.

4 Electrical characteristics

Table 5. Electrical characteristics
(T_{amb} = 25 °C, V_s = 48 V, unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{Sth(ON)}$	Turn-on threshold	-	5.8	6.3	6.8	V
$V_{Sth(OFF)}$	Turn-off threshold	-	5	5.5	6	V
I_S	Quiescent supply current	All bridges OFF; T_j = -25 °C to 125 °C(1)	-	5	10	mA
$T_{j(OFF)}$	Thermal shutdown temperature	-	-	165	-	°C
Output DMOS transistors						
$R_{DS(ON)}$	High-side + low-side switch ON resistance	T_j = 25 °C	-	1.47	1.69	W
		T_j = 125 °C(1)	-	2.35	2.7	W
I_{DSS}	Leakage current	EN = low; OUT = V_S	-	-	2	mA
		EN = low; OUT = GND	-0.3	-	-	mA
Source drain diodes						
V_{SD}	Forward ON voltage	I_{SD} = 1.4 A, EN = LOW	-	1.15	1.3	V
t_{rr}	Reverse recovery time	I_f = 1.4 A	-	300	-	ns
t_{fr}	Forward recovery time	-	-	200	-	ns
Logic input						
V_{IL}	Low level logic input voltage	-	-0.3	-	0.8	V
V_{IH}	High level logic input voltage	-	2	-	7	V
I_{IL}	Low level logic input current	GND logic input voltage	-10	-		µA
I_{IH}	High level logic input current	7 V logic input voltage	-	-	10	µA
$V_{th(ON)}$	Turn-on input threshold	-	-	1.8	2.0	V
$V_{th(OFF)}$	Turn-off input threshold	-	0.8	1.3	-	V
$V_{th(HYS)}$	Input threshold hysteresis	-	0.25	0.5	-	V
Switching characteristics						
$t_{D(on)EN}$	Enable to out turn ON delay time(2)	I_{LOAD} = 1.4 A, resistive load	500	-	800	ns
$t_{D(on)IN}$	Input to out turn ON delay time	I_{LOAD} = 1.4 A, resistive load (deadtime included)	-	1.9	-	µs
t_{RISE}	Output rise time(2)	I_{LOAD} = 1.4 A, resistive load	40		250	ns
$t_{D(off)EN}$	Enable to out turn OFF delay time(2)	I_{LOAD} = 1.4 A, resistive load	500	800	1000	ns
$t_{D(off)IN}$	Input to out turn OFF delay time	I_{LOAD} = 1.4 A, resistive load	500	800	1000	ns
t_{FALL}	Output fall time(2)	I_{LOAD} = 1.4 A, resistive load	40	-	250	ns
t_{dt}	Deadtime protection	-	0.5	1	-	µs
f_{CP}	Charge pump frequency	-25 °C <T_j < 125 °C	-	0.6	1	MHz

Table 5. Electrical characteristics
(T_{amb} = 25 °C, V_s = 48 V, unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PWM comparator and monostable						
I_{RCA}, I_{RCB}	Source current at pins RC_A and RC_B	V_{RCA} = V_{RCB} = 2.5 V	3.5	5.5	-	mA
V_{offset}	Offset voltage on sense comparator	V_{REFA}, V_{REFB} = 0.5 V	-	±5	-	mV
t_{PROP}	Turn OFF propagation delay(3)	-	-	500	-	ns
t_{BLANK}	Internal blanking time on SENSE pins	-	-	1	-	µs
$t_{ON(MIN)}$	Minimum On time	-	-	2.5	3	µs
t_{OFF}	PWM recirculation time	R_{OFF} = 20 KΩ; C_{OFF} = 1 nF	-	13	-	µs
		R_{OFF} = 100 KΩ; C_{OFF} = 1 nF	-	61	-	µs
I_{BIAS}	Input bias current at pins $VREF_A$ and $VREF_B$	-	-	-	10	µA
Overcurrent protection						
I_{SOVER}	Input supply overcurrent protection threshold	T_j = -25 °C to 125 °C(1)	2	2.8	3.55	A
R_{OPDR}	Open drain ON resistance	I = 4 mA	-	40	60	W
$t_{OCD(ON)}$	OCD turn-on delay time(4)	I = 4 mA; C_{EN} < 100 pF	-	200	-	ns
$t_{OCD(OFF)}$	OCD turn-off delay time(4)	I = 4 mA; C_{EN} < 100 pF	-	100	-	ns

1. Tested at 25 °C in a restricted range and guaranteed by characterization.
2. See *Figure 3: Switching characteristic definition*.
3. Measured applying a voltage of 1 V to pin SENSE and a voltage drop from 2 V to 0 V to pin VREF.
4. See *Figure 4: Overcurrent detection timing definition*.

Figure 3. Switching characteristic definition

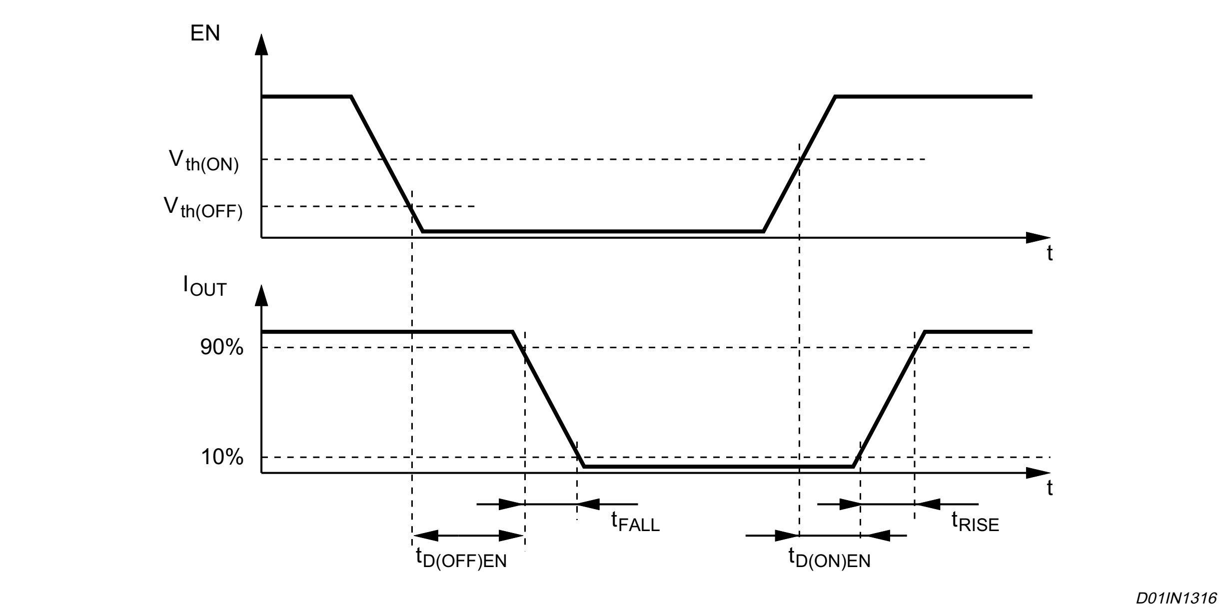
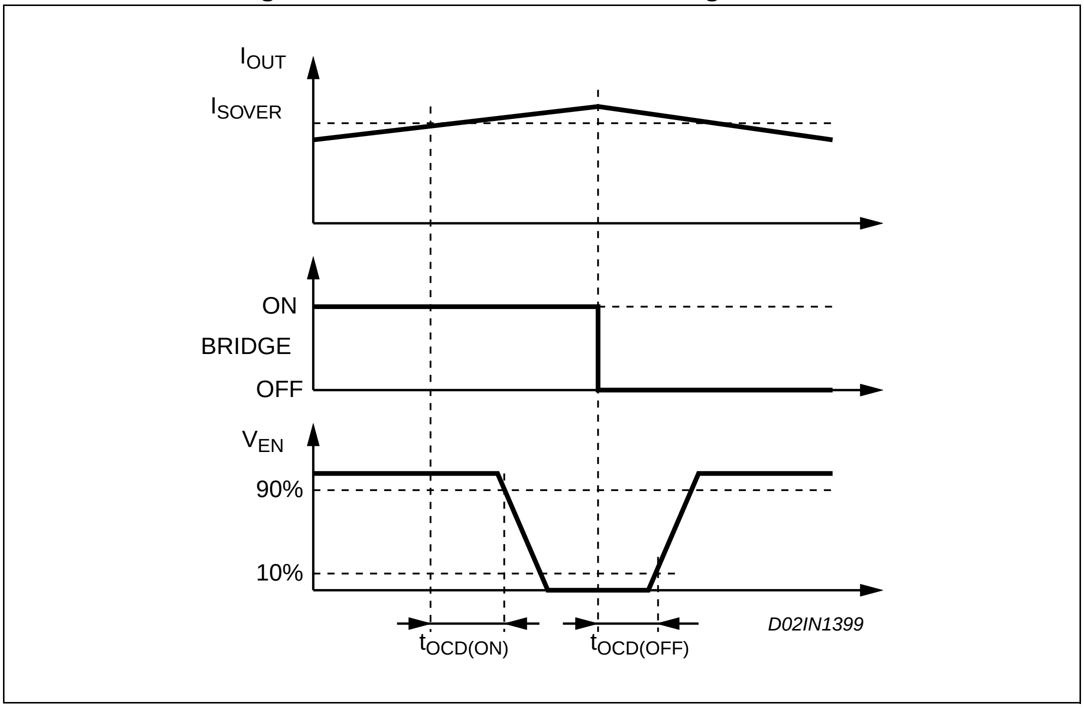


Figure 4. Overcurrent detection timing definition



5 Circuit description

5.1 Power stages and charge pump

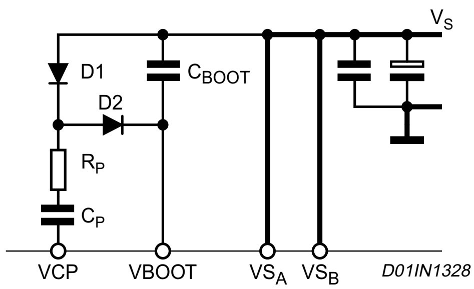
The L6227 device integrates two independent power MOS full bridges. Each power MOS has an $R_{DS(ON)}$ = 0.73 Ω (typical value at 25 °C), with intrinsic fast freewheeling diode. Cross conduction protection is achieved using a deadtime (t_d = 1 µs typical) between the switch off and switch on of two power MOS in one leg of a bridge.

Using N-channel power MOS for the upper transistors in the bridge requires a gate drive voltage above the power supply voltage. The bootstrapped (V_{BOOT}) supply is obtained through an internal oscillator and few external components to realize a charge pump circuit as shown in *Figure 5*. The oscillator output (VCP) is a square wave at 600 kHz (typical) with 10 V amplitude. Recommended values/part numbers for the charge pump circuit are shown in *Table 6*.

Table 6. Charge pump external components values

Component	Value
C_{BOOT}	220 nF
C_P	10 nF
R_P	100 Ω
D1	1N4148
D2	1N4148

Figure 5. Charge pump circuit



5.2 Logic inputs

Pins $IN1_A$, $IN2_B$, $IN1_B$ and $IN2_B$ are TTL/CMOS compatible logic inputs. The internal structure is shown in *Figure 6*. Typical value for turn-on and turn-off thresholds are respectively V_{thon} = 1.8 V and V_{thoff} = 1.3 V.

Pins EN_A and EN_B have identical input structure with the exception that the drains of the overcurrent and thermal protection MOSFETs (one for the bridge A and one for the bridge B) are also connected to these pins. Due to these connections some care needs to be taken in driving these pins. The EN_A and EN_B inputs may be driven in one of two configurations as shown in *Figure 7* or *8*. If driven by an open drain (collector) structure, a pull-up resistor R_{EN} and a capacitor C_{EN} are connected as shown in *Figure 7*. If the driver is a standard push-pull structure the resistor R_{EN} and the capacitor C_{EN} are connected as shown in *Figure 8*. The resistor R_{EN} should be chosen in the range from 2.2 kΩ to 180 KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 KΩ and 5.6 nF. More information on selecting the values is found in *Section 7.1: Non-dissipative overcurrent protection on page 18*.

Figure 6. Logic inputs internal structure

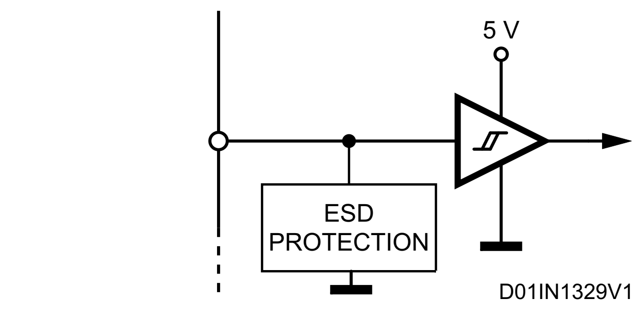


Figure 7. EN_A and EN_B pins open collector driving

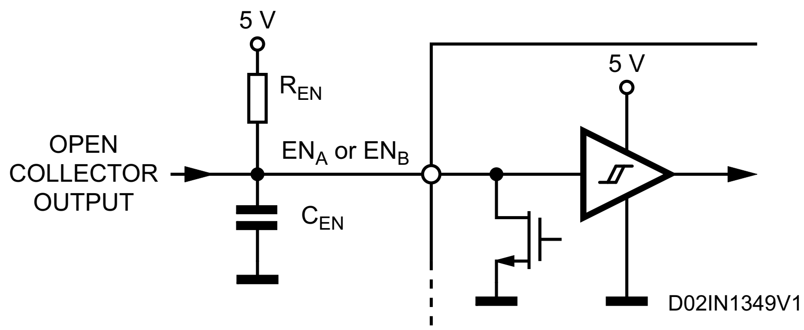


Figure 8. EN_A and EN_B pins push-pull driving

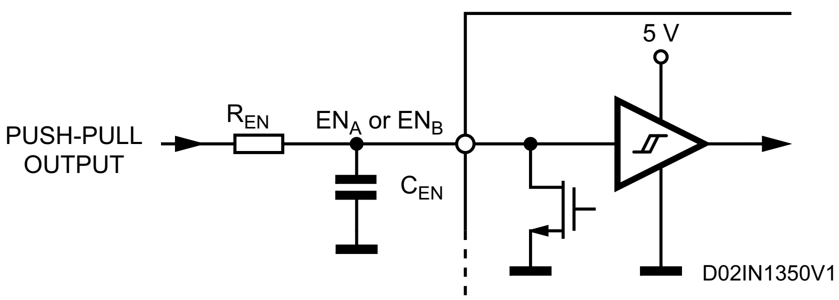


Table 7. Truth table

Inputs			Outputs		Description(1)
EN	IN1	IN2	OUT1	OUT2	
L	X(2)	X(2)	High Z(3)	High Z(3)	Disable
H	L	L	GND	GND	Brake mode (lower path)
H	H	L	Vs	GND (Vs)(4)	Forward
H	L	H	GND (Vs)	Vs	Reverse
H	H	H	Vs	Vs	Brake mode (upper path)

1. Valid only in case of load connected between OUT1 and OUT2.
2. X = don't care.
3. High Z= high impedance output.
4. GND (Vs) = GND during t_{ON}, Vs during t_{OFF}.

6 PWM current control

The L6227 device includes a constant off time PWM current controller for each of the two bridges. The current control circuit senses the bridge current by sensing the voltage drop across an external sense resistor connected between the source of the two lower power MOS transistors and ground, as shown in *Figure 9*. As the current in the load builds up the voltage across the sense resistor increases proportionally. When the voltage drop across the sense resistor becomes greater than the voltage at the reference input ($VREF_A$ or $VREF_B$), the sense comparator triggers the monostable switching the low-side MOS off. The low-side MOS remains off for the time set by the monostable and the motor current recirculates in the upper path. When the monostable times out the bridge will again turn on. Since the internal deadtime, used to prevent cross conduction in the bridge, delays the turn on of the power MOS, the effective off time is the sum of the monostable time plus the deadtime.

Figure 9. PWM current controller simplified schematic

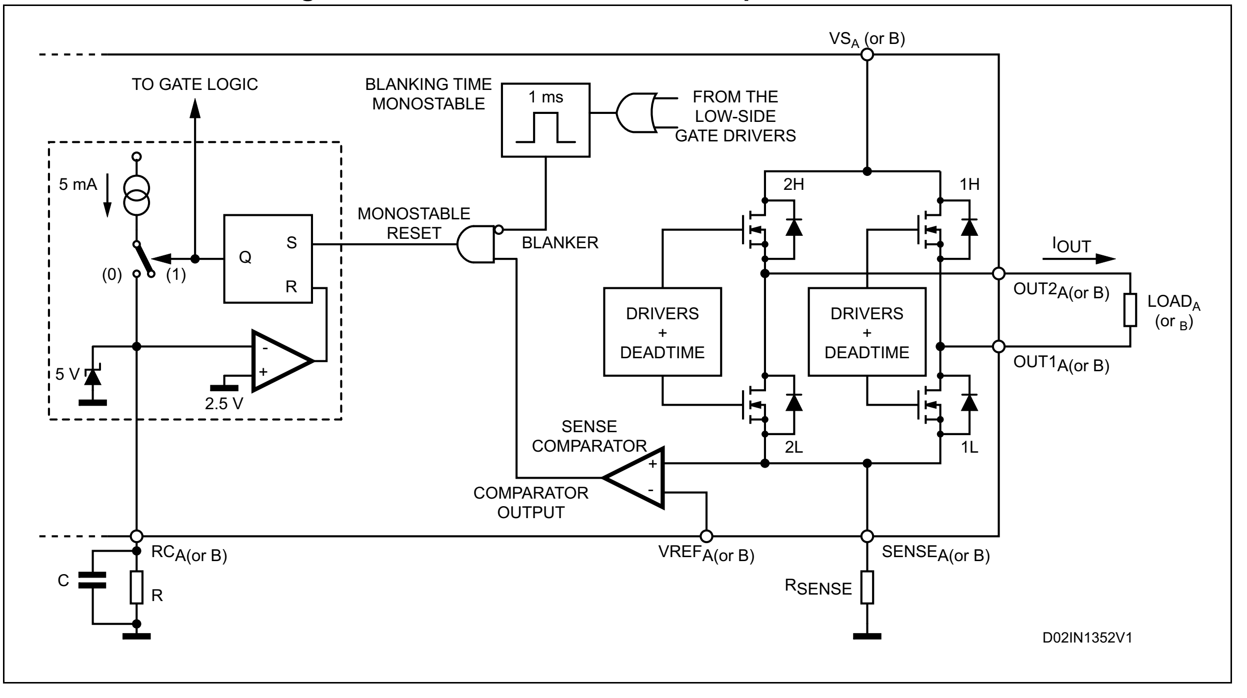


Figure 10 shows the typical operating waveforms of the output current, the voltage drop across the sensing resistor, the RC pin voltage and the status of the bridge. Immediately after the low-side power MOS turns on, a high peak current flows through the sensing resistor due to the reverse recovery of the freewheeling diodes. The L6227 device provides a 1 µs blanking time t_{BLANK} that inhibits the comparator output so that this current spike cannot prematurely retrigger the monostable.

Figure 10. Output current regulation waveforms

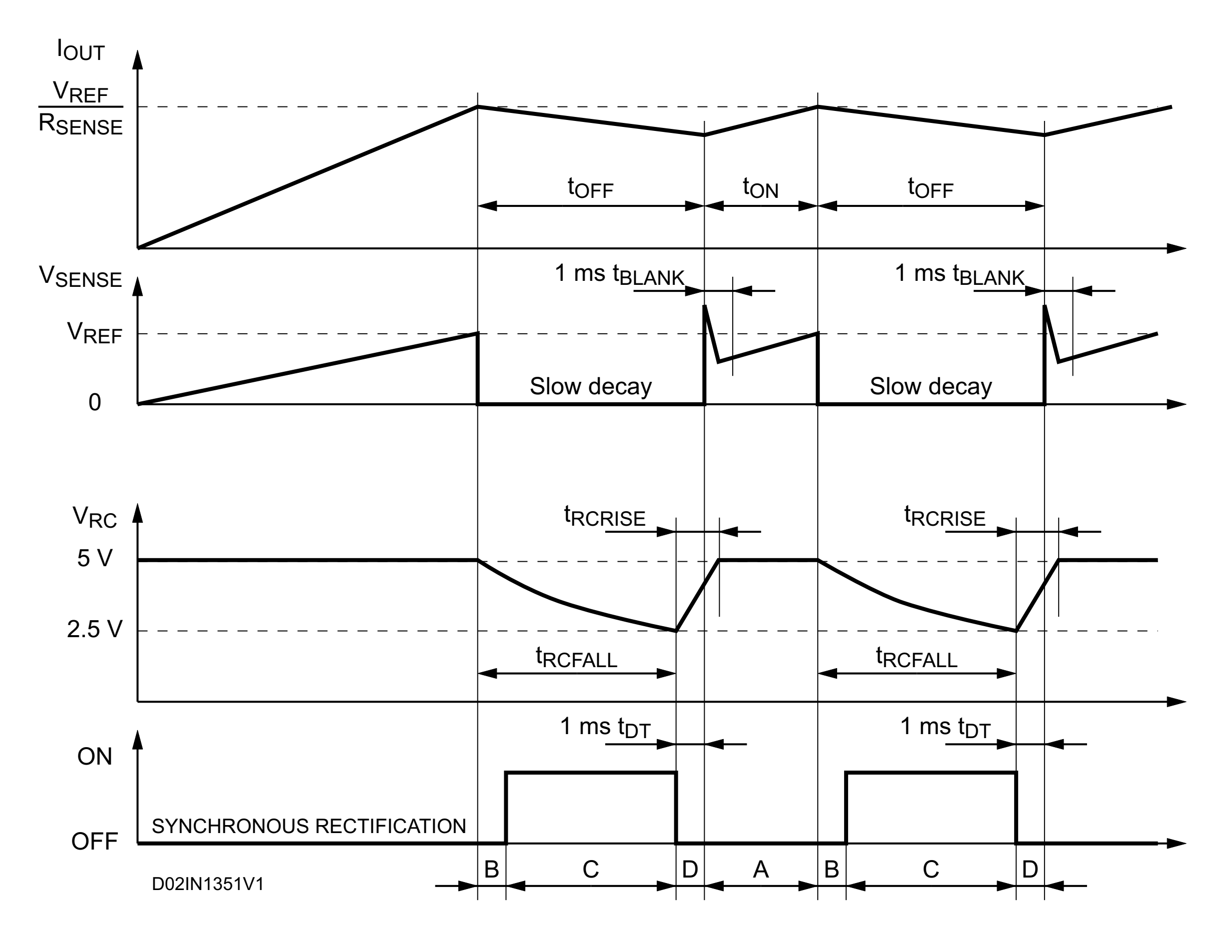


Figure 11 shows the magnitude of the Off time t_{OFF} versus C_{OFF} and R_{OFF} values. It can be approximately calculated from the equations:

Equation 1

$$t_{RCFALL} = 0.6 \cdot R_{OFF} \cdot C_{OFF}$$

$$t_{OFF} = t_{RCFALL} + t_{DT} = 0.6 \cdot R_{OFF} \cdot C_{OFF} + t_{DT}$$

where R_{OFF} and C_{OFF} are the external component values and t_{DT} is the internally generated deadtime with:

Equation 2

$$20\ K\Omega \le R_{OFF} \le 100\ K\Omega$$

$$0.47\ nF \le C_{OFF} \le 100\ nF$$

$$t_{DT} = 1\ \mu s \text{ (typical value)}$$

Therefore:

Equation 3

$$t_{OFF(MIN)} = 6.6\ \mu s$$

$$t_{OFF(MAX)} = 6\ ms$$

These values allow a sufficient range of t_{OFF} to implement the drive circuit for most motors.

The capacitor value chosen for C_{OFF} also affects the rise time t_{RCRISE} of the voltage at the pin RCOFF. The rise time t_{RCRISE} will only be an issue if the capacitor is not completely charged before the next time the monostable is triggered. Therefore, the on time t_{ON}, which depends by motors and supply parameters, has to be bigger than t_{RCRISE} for allowing a good current regulation by the PWM stage. Furthermore, the on time t_{ON} can not be smaller than the minimum on time $t_{ON(MIN)}$.

Equation 4

$$\begin{cases} t_{ON} > t_{ON(MIN)} = 2.5\mu s \text{ (typ. value)} \\ t_{ON} > t_{RCRISE} - t_{DT} \end{cases}$$

$$t_{RCRISE} = 600 \cdot C_{OFF}$$

Figure 12 shows the lower limit for the on time t_{ON} for having a good PWM current regulation capacity. It has to be said that t_{ON} is always bigger than $t_{ON(MIN)}$ because the device imposes this condition, but it can be smaller than t_{RCRISE} - t_{DT}. In this last case the device continues to work but the off time t_{OFF} is not more constant.

So, small C_{OFF} value gives more flexibility for the applications (allows smaller on time and, therefore, higher switching frequency), but, the smaller is the value for C_{OFF}, the more influential will be the noises on the circuit performance.

Figure 11. t_{OFF} versus C_{OFF} and R_{OFF}

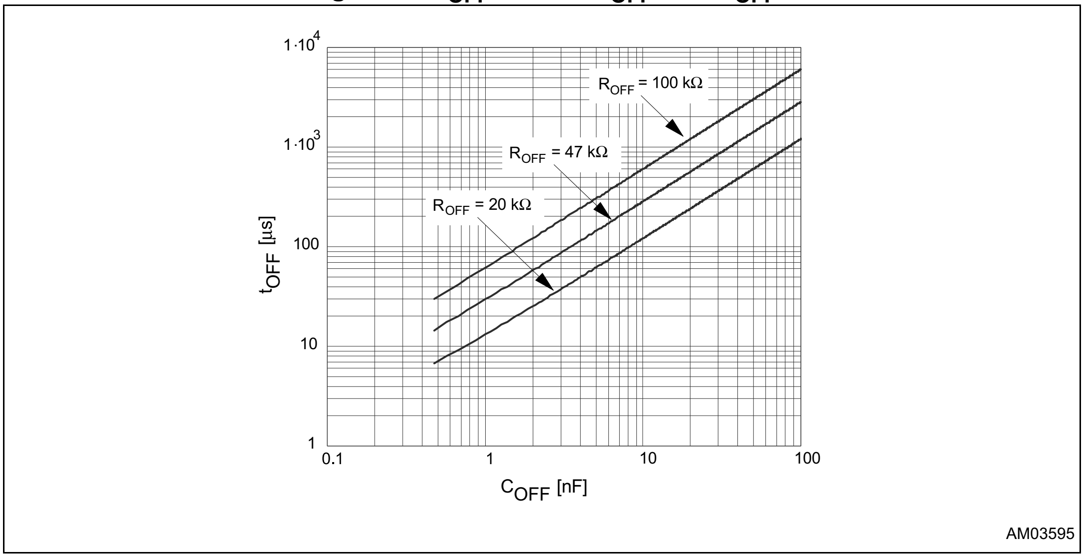
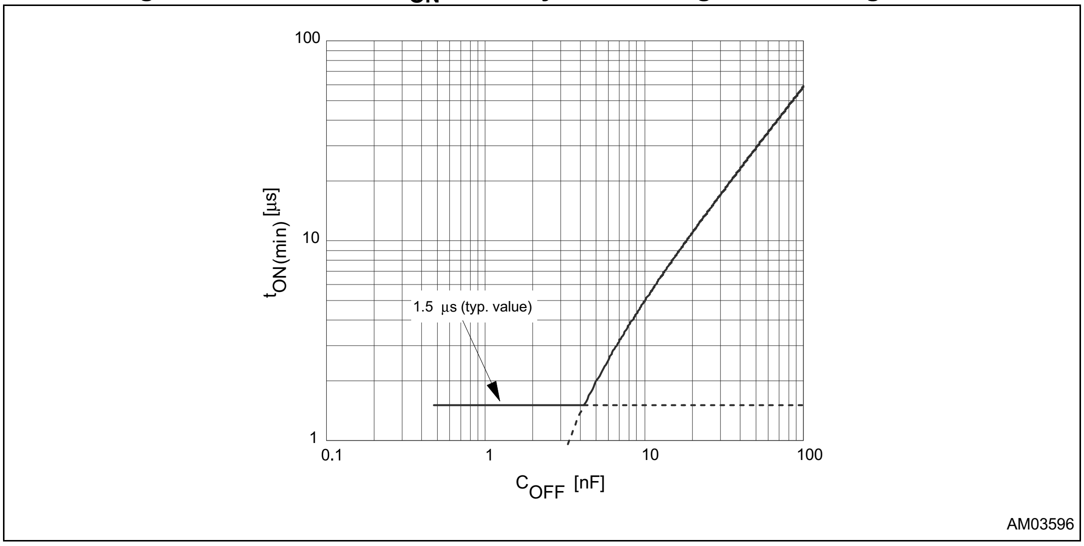


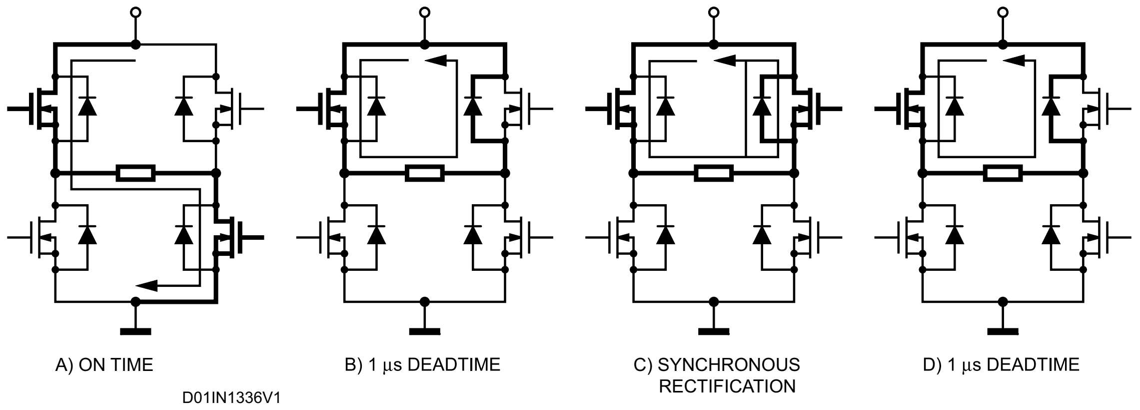
Figure 12. Area where t_{ON} can vary maintaining the PWM regulation



7 Slow decay mode

Figure 13 shows the operation of the bridge in the slow decay mode. At the start of the off time, the lower power MOS is switched off and the current recirculates around the upper half of the bridge. Since the voltage across the coil is low, the current decays slowly. After the deadtime the upper power MOS is operated in the synchronous rectification mode. When the monostable times out, the lower power MOS is turned on again after some delay set by the deadtime to prevent cross conduction.

Figure 13. Slow decay mode output stage configurations



7.1 Non-dissipative overcurrent protection

The L6227 integrates an “Overcurrent Detection” circuit (OCD). This circuit provides protection against a short-circuit to ground or between two phases of the bridge. With this internal overcurrent detection, the external current sense resistor normally used and its associated power dissipation are eliminated. *Figure 14* shows a simplified schematic of the overcurrent detection circuit.

To implement the overcurrent detection, a sensing element that delivers a small but precise fraction of the output current is implemented with each high-side power MOS. Since this current is a small fraction of the output current there is very little additional power dissipation. This current is compared with an internal reference current I_{REF}. When the output current in one bridge reaches the detection threshold (typically 2.8 A) the relative OCD comparator signals a fault condition. When a fault condition is detected, the EN pin is pulled below the turn off threshold (1.3 V typical) by an internal open drain MOS with a pull down capability of 4 mA. By using an external R-C on the EN pin, the off time before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs.

Figure 14. Overcurrent protection simplified schematic

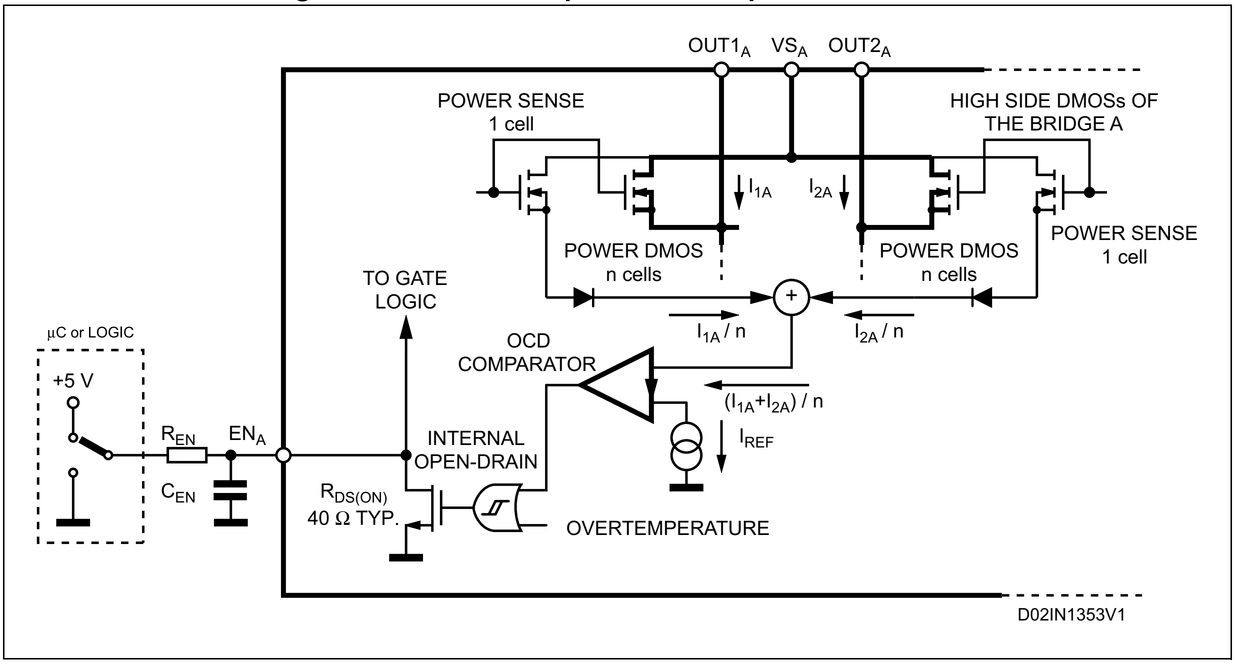


Figure 15 shows the overcurrent detection operation. The disable time $t_{DISABLE}$ before recovering normal operation can be easily programmed by means of the accurate thresholds of the logic inputs. It is affected whether by C_{EN} and R_{EN} values and its magnitude is reported in *Figure 16*. The delay time t_{DELAY} before turning off the bridge when an overcurrent has been detected depends only by C_{EN} value. Its magnitude is reported in *Figure 17*.

C_{EN} is also used for providing immunity to pin EN against fast transient noises. Therefore the value of C_{EN} should be chosen as big as possible according to the maximum tolerable delay time and the R_{EN} value should be chosen according to the desired disable time.

The resistor R_{EN} should be chosen in the range from 2.2 KΩ to 180 KΩ. Recommended values for R_{EN} and C_{EN} are respectively 100 KΩ and 5.6 nF that allow obtaining 200 µs disable time.

Figure 15. Overcurrent protection waveforms

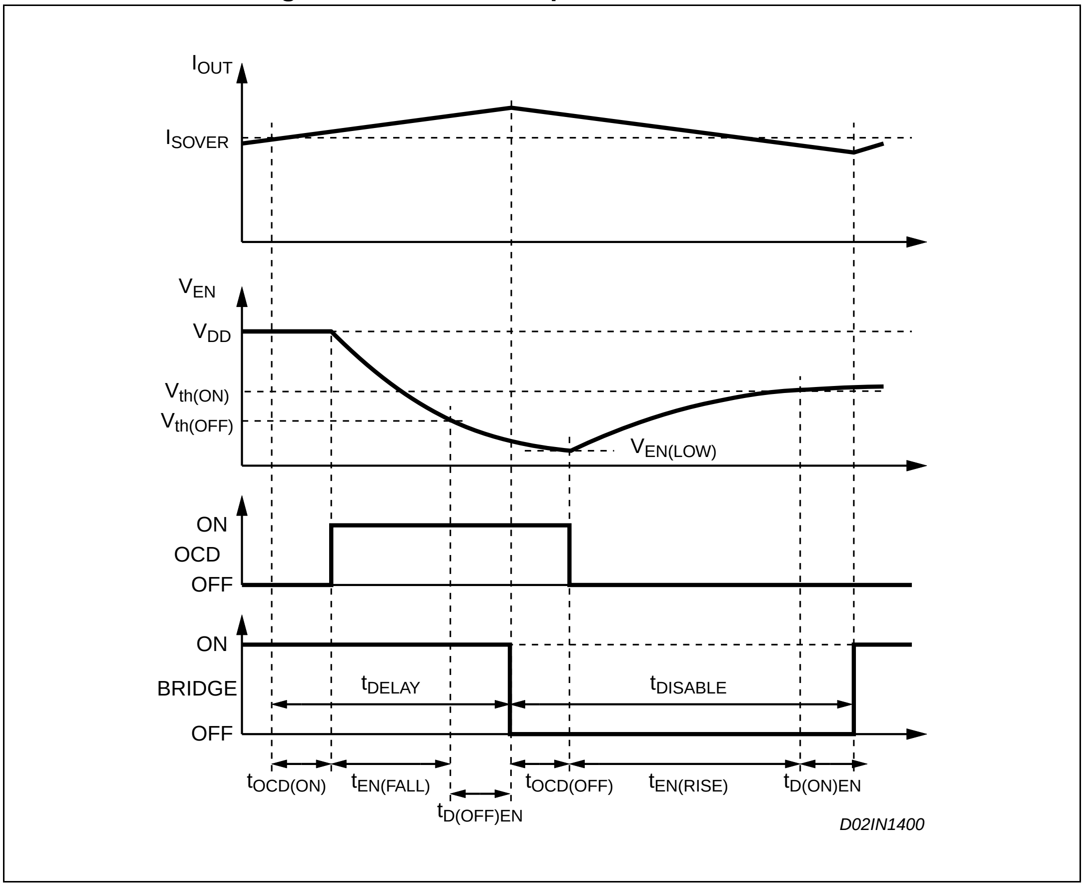


Figure 16. $t_{DISABLE}$ versus C_{EN} and R_{EN} (V_{DD} = 5 V)

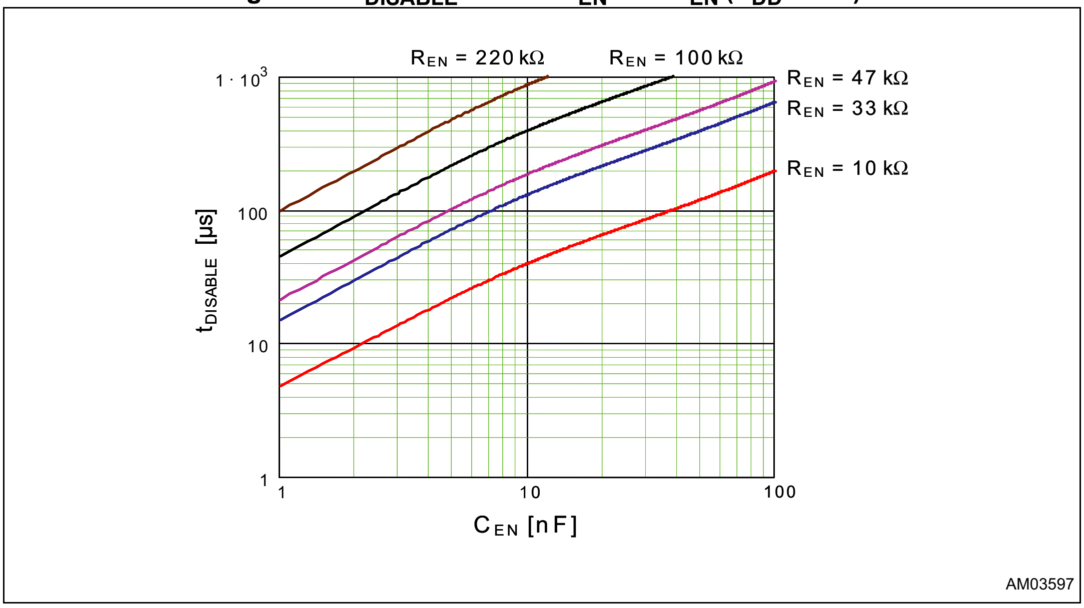
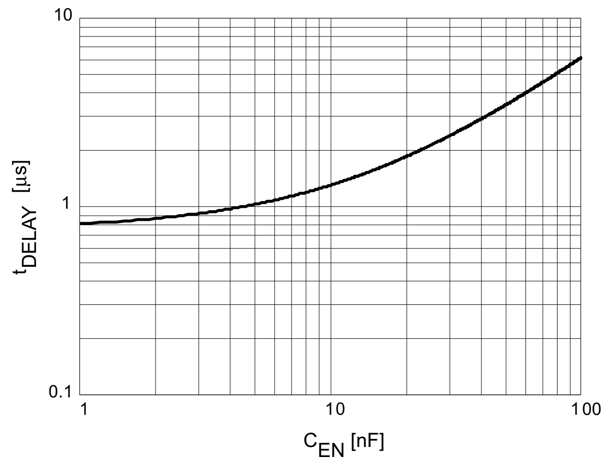


Figure 17. t_{DELAY} versus C_{EN} (V_{DD} = 5 V)



7.2 Thermal protection

In addition to the overcurrent protection, the L6227 device integrates a thermal protection for preventing the device destruction in case of junction overtemperature. It works sensing the die temperature by means of a sensible element integrated in the die. The device switches-off when the junction temperature reaches 165 °C (typ. value) with 15 °C hysteresis (typ. value).

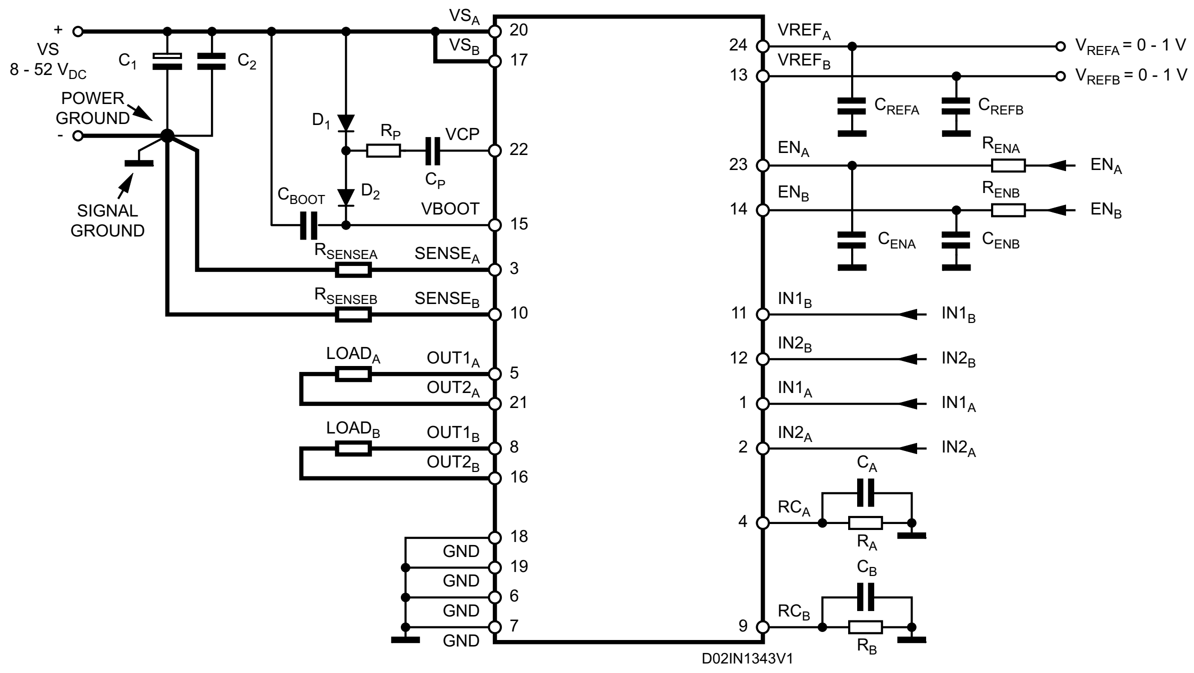
8 Application information

A typical application using the L6227 device is shown in *Figure 18*. Typical component values for the application are shown in Table 3. A high quality ceramic capacitor in the range of 100 to 200 nF should be placed between the power pins (VS_A and VS_B) and ground near the L6227 to improve the high frequency filtering on the power supply and reduce high frequency transients generated by the switching. The capacitors connected from the EN_A and EN_B inputs to ground set the shutdown time for the bridge A and bridge B respectively when an overcurrent is detected (see *Section 7.1: Non-dissipative overcurrent protection*). The two current sensing inputs ($SENSE_A$ and $SENSE_B$) should be connected to the sensing resistors with a trace length as short as possible in the layout. The sense resistors should be non-inductive resistors to minimize the di/dt transients across the resistor. To increase noise immunity, unused logic pins (except EN_A and EN_B) are best connected to 5 V (high logic level) or GND (low logic level) (see *Table 4: Pin description on page 6*). It is recommended to keep power ground and signal ground separated on the PCB.

Table 8. Component values for typical application

Component	Value
C_1	100 µF
C_2	100 nF
C_A	1 nF
C_B	1 nF
C_{BOOT}	220 nF
C_P	10 nF
C_{ENA}	5.6 nF
C_{ENB}	5.6 nF
C_{REFA}	68 nF
C_{REFB}	68 nF
D_1	1N4148
D_2	1N4148
R_A	39 KΩ
R_B	39 KΩ
R_{ENA}	100 KΩ
R_{ENB}	100 KΩ
R_P	100 Ω
R_{SENSEA}	0.6 Ω
R_{SENSEB}	0.6 Ω

Figure 18. Typical application



8.1 Output current capability and IC power dissipation

In *Figure 19* and *Figure 20* are shown the approximate relation between the output current and the IC power dissipation using PWM current control driving two loads, for two different driving types:

- One full bridge ON at a time (*Figure 19*) in which only one load at a time is energized.
- Two full bridges ON at the same time (*Figure 20*) in which two loads at the same time are energized.

For a given output current and driving type the power dissipated by the IC can be easily evaluated, in order to establish which package should be used and how large must be the on-board copper dissipating area to guarantee a safe operating junction temperature (125 °C maximum).

Figure 19. IC power dissipation versus output current with one full bridge ON at a time

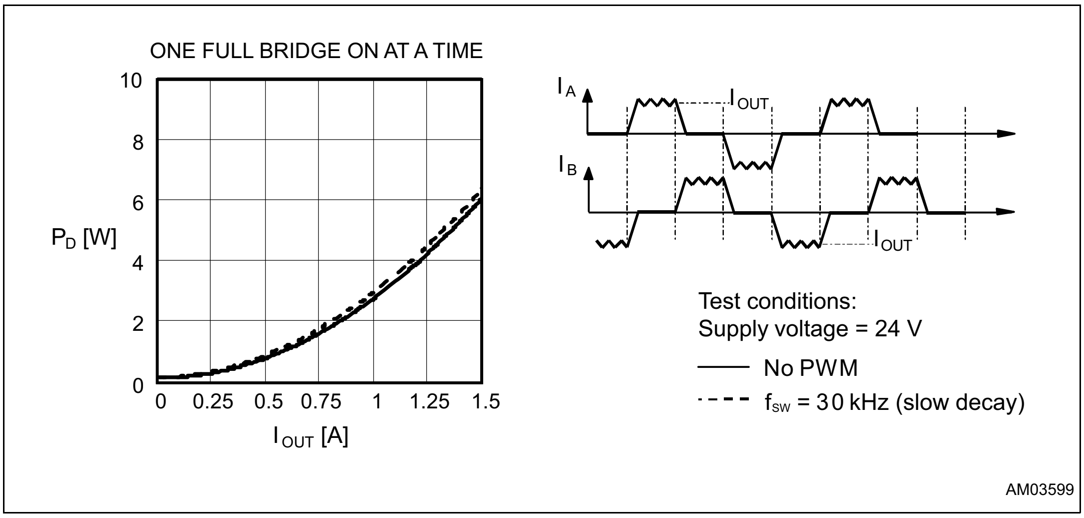
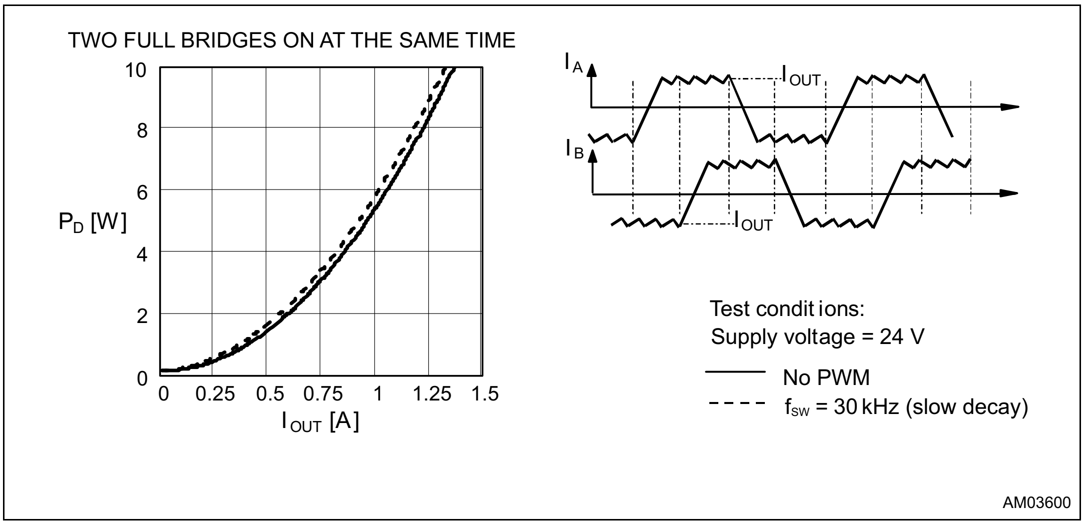


Figure 20. IC power dissipation versus output current with two full bridges ON at the same time



8.2 Thermal management

In most applications the power dissipation in the IC is the main factor that sets the maximum current that can be delivered by the device in a safe operating condition. Therefore, it has to be taken into account very carefully. Besides the available space on the PCB, the right package should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. *Figure 22* and *23* show the junction to ambient thermal resistance values for the PowerSO36 and SO24 packages.

For instance, using a PowerSO package with a copper slug soldered on a 1.5 mm copper thickness FR4 board with a 6 cm^2 dissipating footprint (copper thickness of 35 µm), the $R_{th\ j\text{-}amb}$ is about 35 °C/W. *Figure 21* shows mounting methods for this package. Using a multilayer board with vias to a ground plane, thermal impedance can be reduced down to 15 °C/W.

Figure 21. Mounting the PowerSO package

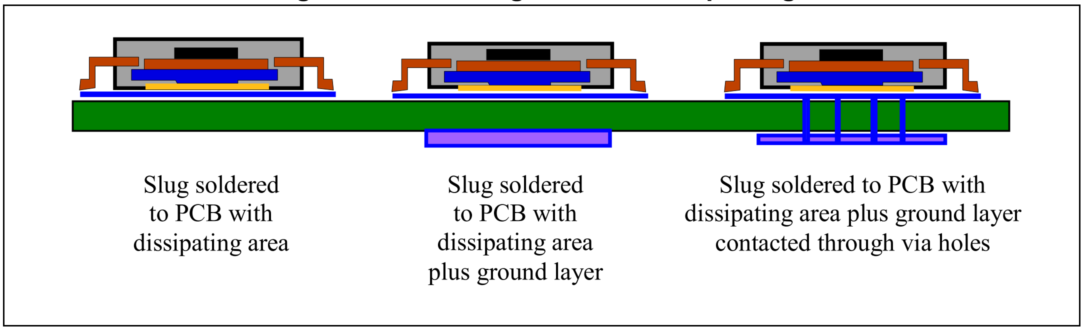


Figure 22. PowerSO36 junction ambient thermal resistance versus on-board copper area

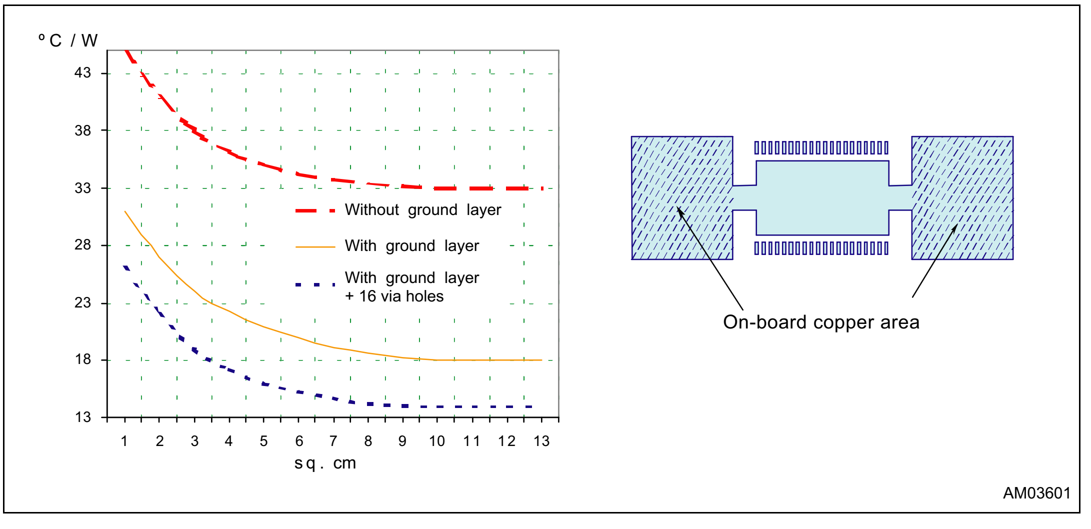
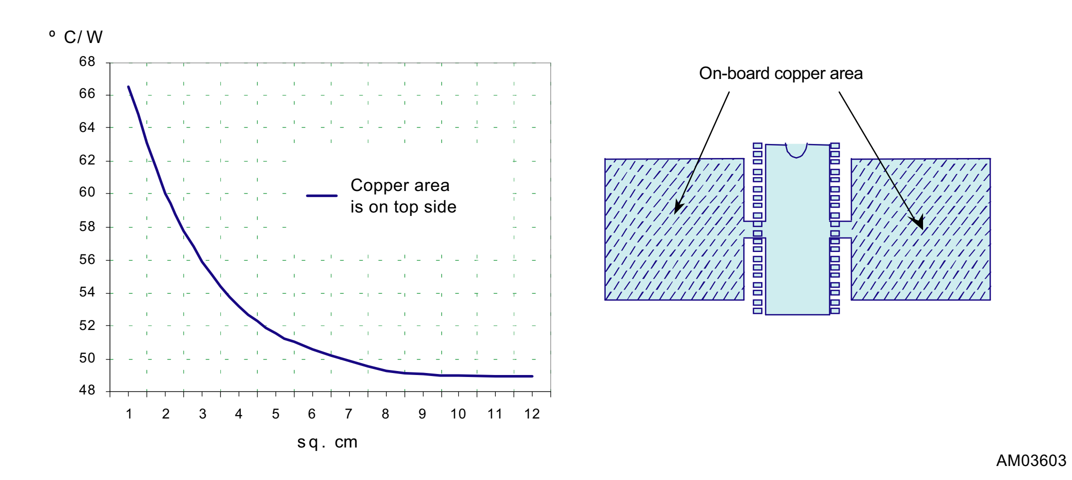


Figure 23. SO24 junction ambient thermal resistance versus on-board copper area



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

9.1 PowerSO36 package information

Figure 24. PowerSO36 package outline

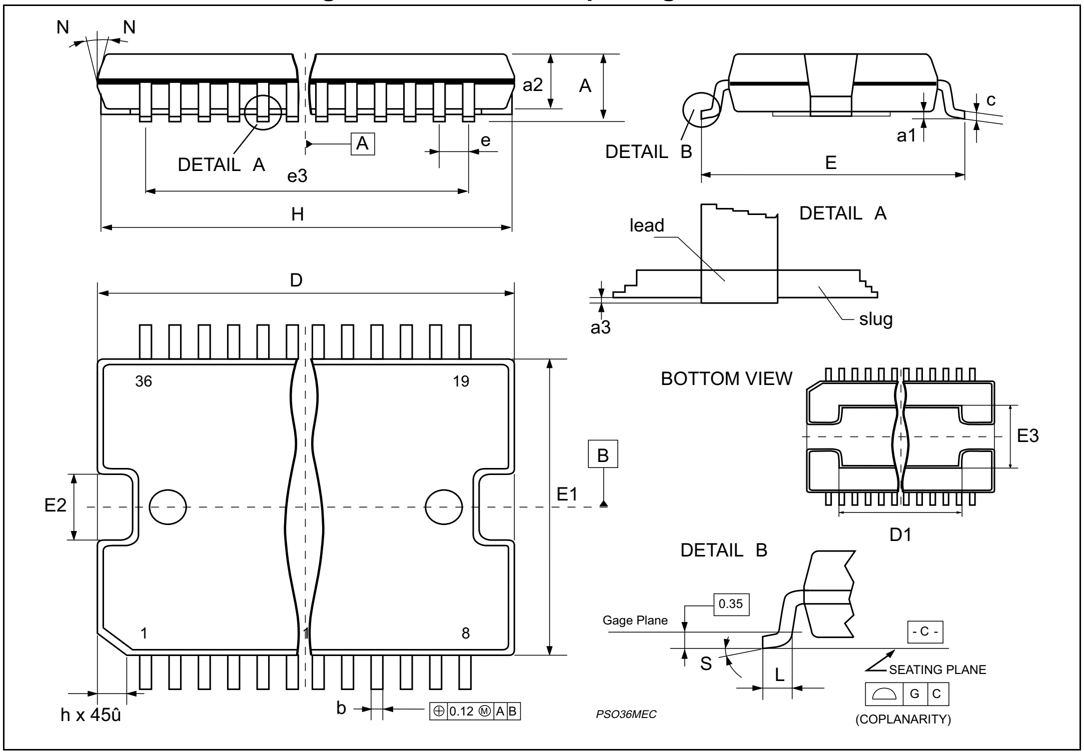


Table 9. PowerSO36 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	3.60	-	-	0.141
a1	0.10	-	0.30	0.004	-	0.012
a2	-	-	3.30	-	-	0.130
a3	0	-	0.10	0	-	0.004
b	0.22	-	0.38	0.008	-	0.015
c	0.23	-	0.32	0.009	-	0.012
D(1)	15.80	-	16.00	0.622	-	0.630
D1	9.40	-	9.80	0.370	-	0.385
E	13.90	-	14.50	0.547	-	0.570
e	-	0.65	-	-	0.0256	-
e3	-	11.05	-	-	0.435	-
E1(1)	10.90	-	11.10	0.429	-	0.437
E2	-	-	2.90	-	-	0.114
E3	5.80	-	6.20	0.228	-	0.244
E4	2.90	-	3.20	0.114	-	0.126
G	0	-	0.10	0	-	0.004
H	15.50	-	15.90	0.610	-	0.626
h	-	-	1.10	-	-	0.043
L	0.80	-	1.10	0.031	-	0.043
N	10° (max.)					
S	8° (max.)					

1. “D” and “E1” do not include mold flash or protrusions.
   - Mold flash or protrusions shall not exceed 0.15 mm (0.006 inch).
   - Critical dimensions are “a3”, “E” and “G”.

9.2 SO24 package information

Figure 25. SO24 package outline

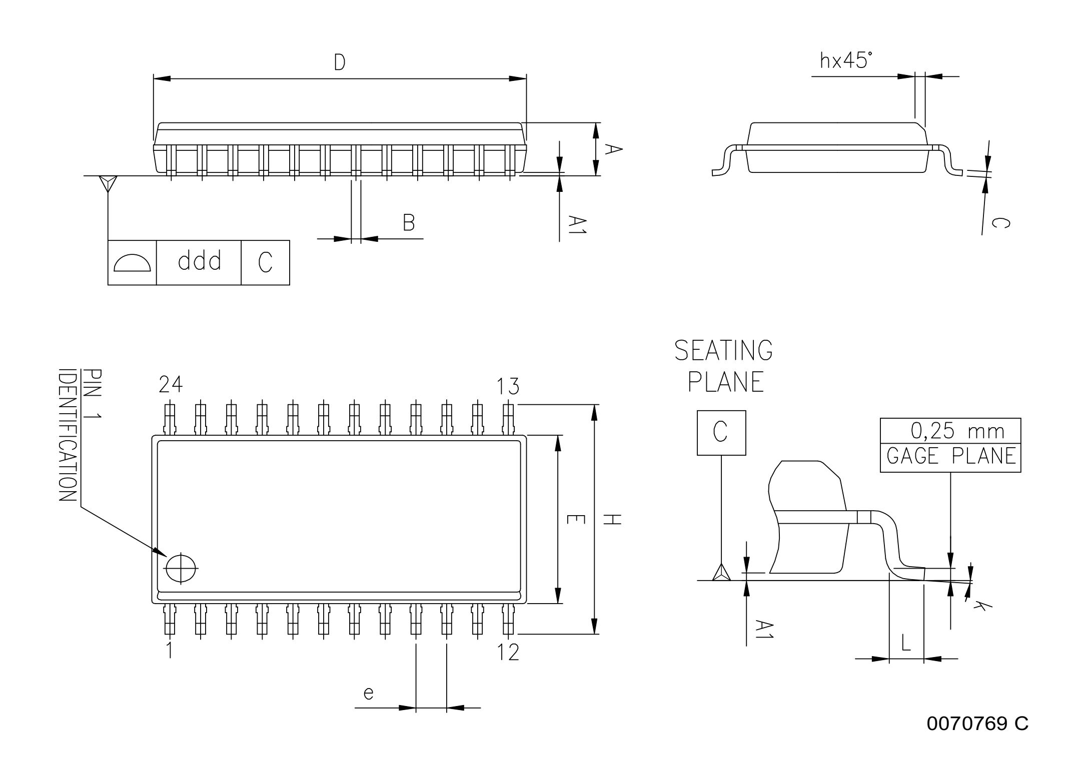


Table 10. SO24 package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35	-	2.65	0.093	-	0.104
A1	0.10	-	0.30	0.004	-	0.012
B	0.33	-	0.51	0.013	-	0.020
C	0.23	-	0.32	0.009	-	0.013
D(1)	15.20	-	15.60	0.598	-	0.614
E	7.40	-	7.60	0.291	-	0.299
e	-	1.27	-	-	0.050	-
H	10.0	-	10.65	0.394	-	0.419
h	0.25	-	0.75	0.010	-	0.030
L	0.40	-	1.27	0.016	-	0.050
k	0° (min.), 8° (max.)					
ddd	-	-	0.10	-	-	0.004

1. D” dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.

10 Revision history

Table 11. Document revision history

Date	Revision	Changes
03-Sep-2003	1	Initial release.
18-Feb-2014	2	Updated *Section : Description on page 1* (removed “MultiPower-” from “MultiPower-BCD technology”. Added *Contents on page 2*. Updated *Section 1: Block diagram* (added section title, numbered and moved *Figure 1: Block diagram* to page 3. Added title to *Section 2: Maximum ratings on page 4*, added numbers and titles from *Table 1: Absolute maximum ratings* to *Table 3: Thermal data*. Added title to *Section 3: Pin connections on page 6*, added number and title to *Figure 2: Pin connections (top view)*, renumbered note *1* below *Figure 2*, added title to *Table 4: Pin description*, renumbered note *1* below *Table 4*. Added title to *Section 4: Electrical characteristics on page 8*, added title and number to *Table 5*, renumbered notes *1* to *4* below *Table 5*. Renumbered *Figure 3* and *Figure 4*. Added title numbers to *Section 5: Circuit description on page 11* (including *Section 5.1* to *Section 5.2*). Removed “and µC” from first sentence of *Section 5.2*. Renumbered *Table 6* and *Table 7*, added header to *Table 6* and *Table 7*. Renumbered *Figure 5* to *Figure 8*. Added title numbers to *Section 6: PWM current control on page 14*. Renumbered *Figure 9* to *Figure 12*. Added titles to *Equation 1: on page 16* till *Equation 4: on page 16*. Added title numbers to *Section 7: Slow decay mode on page 18* (including *Section 7.1* and *Section 7.2*). Renumbered *Figure 13* to *Figure 17*. Added title numbers to *Section 8: Application information on page 22* (including *Section 8.1* and *Section 8.2*). Renumbered *Table 8*, added header to *Table 8*. Renumbered *Figure 18* to *Figure 24*. Updated *Section 9: Package information on page 27* (added main title and ECOPACK text. Added titles from *Table 9: PowerSO36 package mechanical data* to *Table 11: SO24 package mechanical data* and from *Figure 25: PowerSO36 package outline* to *Figure 27: SO24 package outline*, reversed order of named tables and figures. Removed 3D figures of packages, replaced 0.200 by 0.020 inch of max. B value in *Table 11*). Added cross-references throughout document. Added *Section 10: Revision history* and *Table 12*. Minor modifications throughout document.
03-Oct-2018	3	Removed PowerDIP24 package from the whole document. Removed “T_j“ from *Table 2 on page 4*. Minor modifications throughout document.

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