

74CBTLV3125

4-bit bus switch

Rev. 5 — 8 October 2018

Product data sheet

1. General description

The 74CBTLV3125 provides a 4-bit high-speed bus switch with separate output enable inputs ($1\overline{OE}$ to $4\overline{OE}$). The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The switch is disabled (high-impedance OFF-state) when the output enable ($n\overline{OE}$) input is HIGH.

To ensure the high-impedance OFF-state during power-up or power-down, $n\overline{OE}$ should be tied to the V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- Standard '125'-type pinout
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM AEC-Q100-011 revision B exceeds 1000 V
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|---------------|-------------------|------------|--|----------|
| | Temperature range | Name | Description | Version |
| 74CBTLV3125DS | -40 °C to +125 °C | SSOP16 [1] | plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm | SOT519-1 |
| 74CBTLV3125PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74CBTLV3125BQ | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm | SOT762-1 |

[1] Also known as QSOP16.

4. Functional diagram

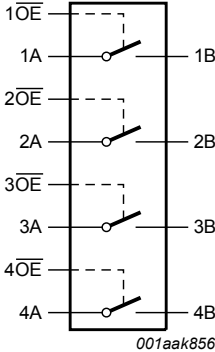


Fig. 1. Logic symbol

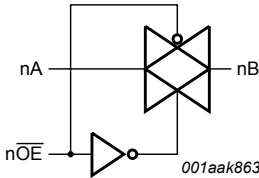
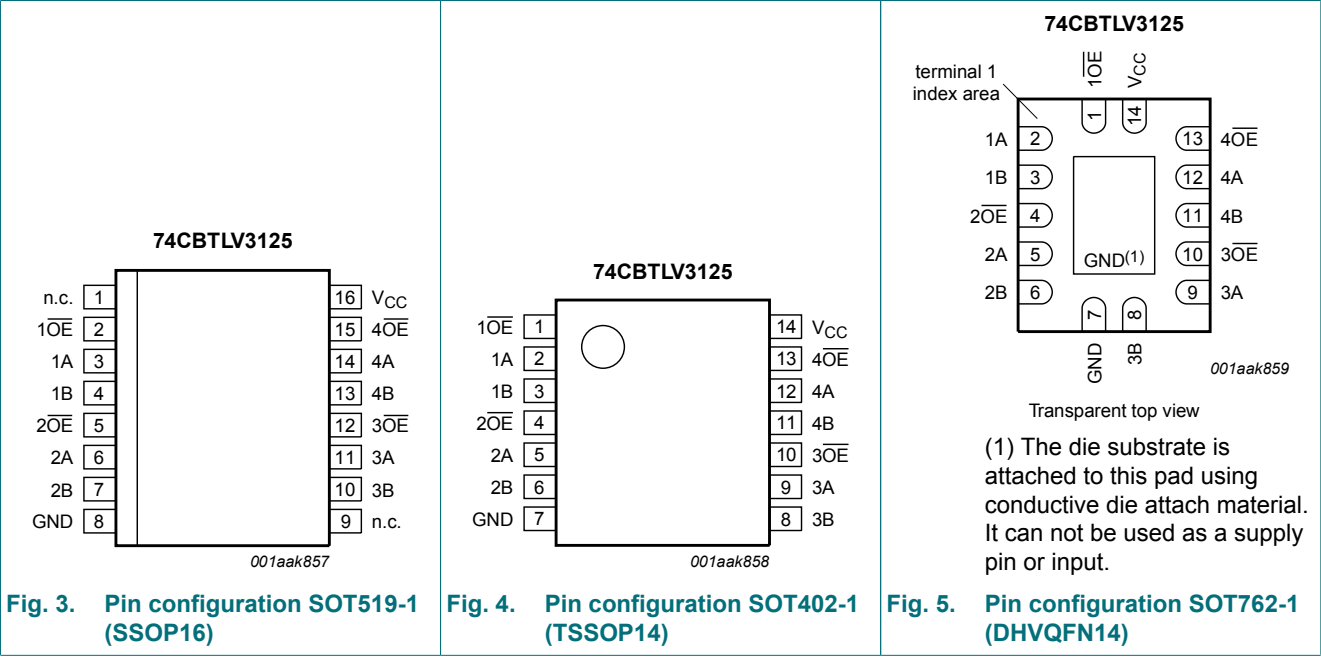


Fig. 2. Logic diagram (one switch)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | | Description |
|--------------------|--------------|-----------------------|-------------------------|
| | SOT519-1 | SOT402-1 and SOT762-1 | |
| 1OE, 2OE, 3OE, 4OE | 2, 5, 12, 15 | 1, 4, 10, 13 | output enable input |
| 1A, 2A, 3A, 4A, | 3, 6, 11, 14 | 2, 5, 9, 12 | A input/output |
| 1B, 2B, 3B, 4B | 4, 7, 10, 13 | 3, 6, 8, 11 | B output/input |
| GND | 8 | 7 | ground (0 V) |
| VCC | 16 | 14 | positive supply voltage |
| n.c. | 1, 9 | - | not connected |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

| Output enable input OE | Function switch |
|------------------------|-----------------|
| L | ON-state |
| H | OFF-state |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-----------------------------------|------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +4.6 | V |
| V_I | input voltage | control inputs [1] | -0.5 | +4.6 | V |
| V_{SW} | switch voltage | enable and disable mode [2] | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V | -50 | - | mA |
| I_{SK} | switch clamping current | $V_I < -0.5$ V | -50 | - | mA |
| I_{SW} | switch current | $V_{SW} = 0$ V to V_{CC} | - | ±128 | mA |
| I_{CC} | supply current | | - | +100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C [3] | - | 500 | mW |

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.

[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed.

[3] For SSOP16 and TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|-------------------------------------|------------------------------------|-----|----------|------|
| V_{CC} | supply voltage | | 2.3 | 3.6 | V |
| V_I | input voltage | control inputs | 0 | 3.6 | V |
| V_{SW} | switch voltage | enable and disable mode | 0 | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | pin nOE; $V_{CC} = 2.3$ V to 3.6 V | 0 | 200 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|---------------------|---------------------------|---|-------------------------------------|--------|------|--------------------------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | V _{CC} = 3.0 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | V _{CC} = 3.0 V to 3.6 V | - | - | 0.9 | - | 0.9 | V |
| I _I | input leakage current | pin nOE; V _I = GND to V _{CC} ; V _{CC} = 3.6 V | - | - | ±1.0 | - | ±20 | µA |
| I _{S(OFF)} | OFF-state leakage current | V _{CC} = 3.6 V; see Fig. 6 | - | - | ±1 | - | ±20 | µA |
| I _{S(ON)} | ON-state leakage current | V _{CC} = 3.6 V; see Fig. 7 | - | - | ±1 | - | ±20 | µA |
| I _{OFF} | power-off leakage current | V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V | - | - | ±10 | - | ±50 | µA |
| I _{CC} | supply current | V _I = GND or V _{CC} ; I _O = 0 A; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V | - | - | 10 | - | 50 | µA |
| ΔI _{CC} | additional supply current | pin nOE; V _I = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V [2] | - | - | 300 | - | 2000 | µA |
| C _I | input capacitance | pin nOE; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V | - | 0.9 | - | - | - | pF |
| C _{S(OFF)} | OFF-state capacitance | V _{CC} = 3.3 V; V _I = 0 V to 3.3 V | - | 5.2 | - | - | - | pF |
| C _{S(ON)} | ON-state capacitance | V _{CC} = 3.3 V; V _I = 0 V to 3.3 V | - | 14.3 | - | - | - | pF |

[1] All typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1. Test circuits

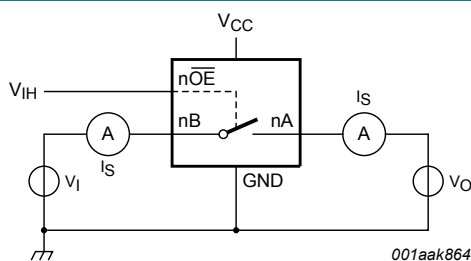
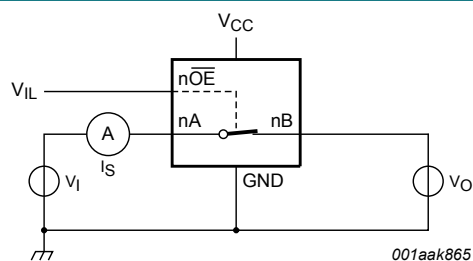

$$V_I = V_{CC} \text{ or GND and } V_O = \text{GND or } V_{CC}.$$

Fig. 6. Test circuit for measuring OFF-state leakage current (one switch)



$V_I = V_{CC}$ or GND and $V_O =$ open circuit.

Fig. 7. Test circuit for measuring ON-state leakage current (one switch)

9.2. ON resistance

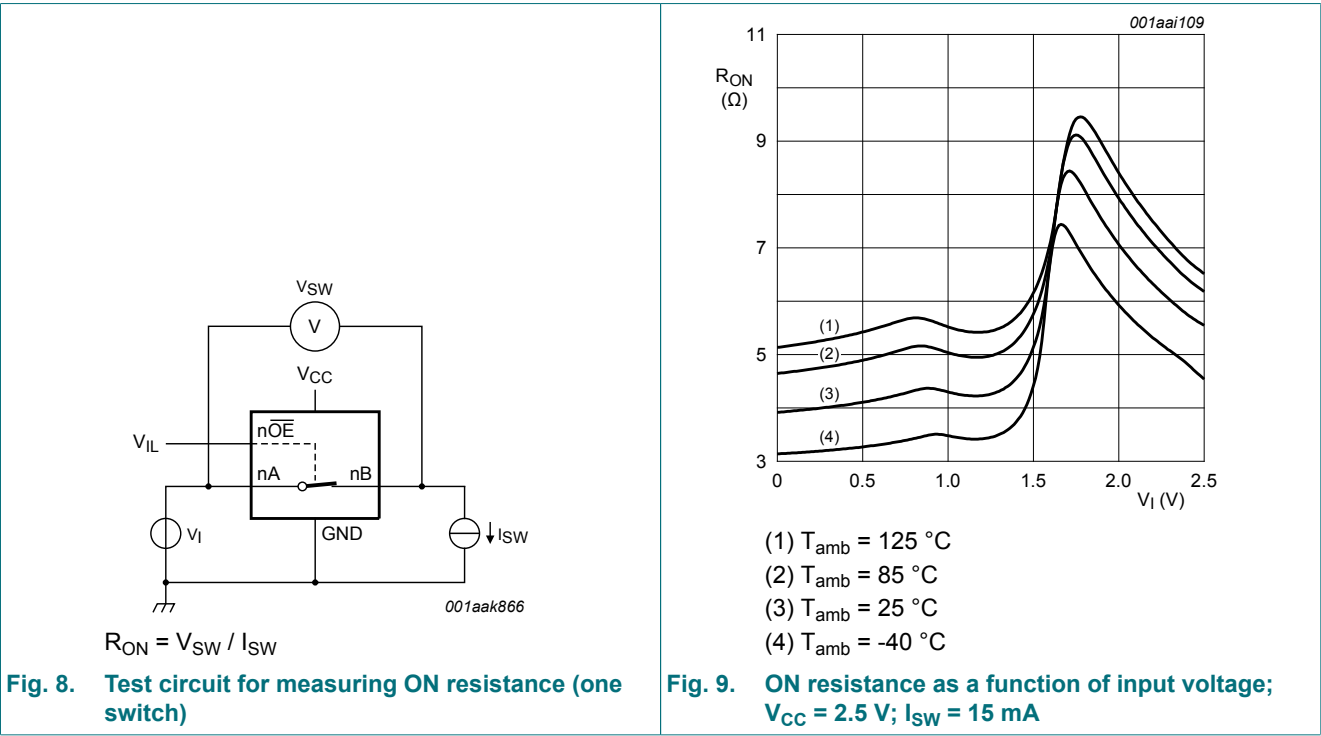
Table 7. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

| Symbol | Parameter | Conditions | T _{amb} = -40 °C to +85 °C | | | T _{amb} = -40 °C to +125 °C | | Unit |
|-----------------|---------------|---|-------------------------------------|---------|------|--------------------------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| R _{ON} | ON resistance | V _{CC} = 2.3 V to 2.7 V; see Fig. 9 to Fig. 11 [2] | | | | | | |
| | | I _{SW} = 64 mA; V _I = 0 V | - | 4.2 | 8.0 | - | 15.0 | Ω |
| | | I _{SW} = 24 mA; V _I = 0 V | - | 4.2 | 8.0 | - | 15.0 | Ω |
| | | I _{SW} = 15 mA; V _I = 1.7 V | - | 8.4 | 40.0 | - | 60.0 | Ω |
| | | V _{CC} = 3.0 V to 3.6 V; see Fig. 12 to Fig. 14 | | | | | | |
| | | I _{SW} = 64 mA; V _I = 0 V | - | 4.0 | 7.0 | - | 11.0 | Ω |
| | | I _{SW} = 24 mA; V _I = 0 V | - | 4.0 | 7.0 | - | 11.0 | Ω |
| | | I _{SW} = 15 mA; V _I = 2.4 V | - | 6.2 | 15.0 | - | 25.5 | Ω |

- [1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.3. ON resistance test circuit and graphs



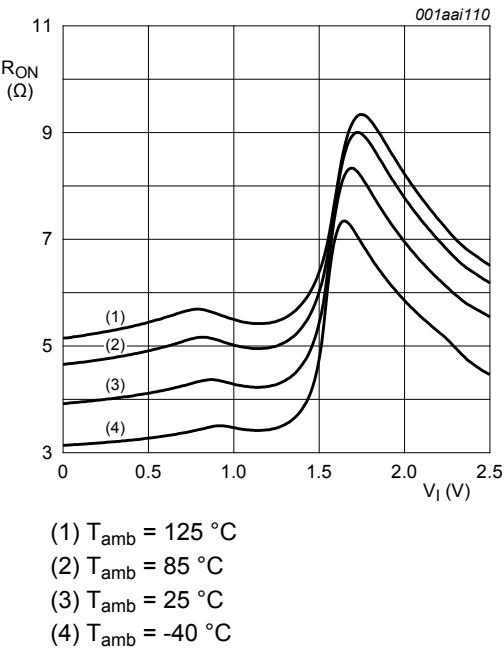


Fig. 10. ON resistance as a function of input voltage;
 $V_{CC} = 2.5\text{ V}$; $I_{SW} = 24\text{ mA}$

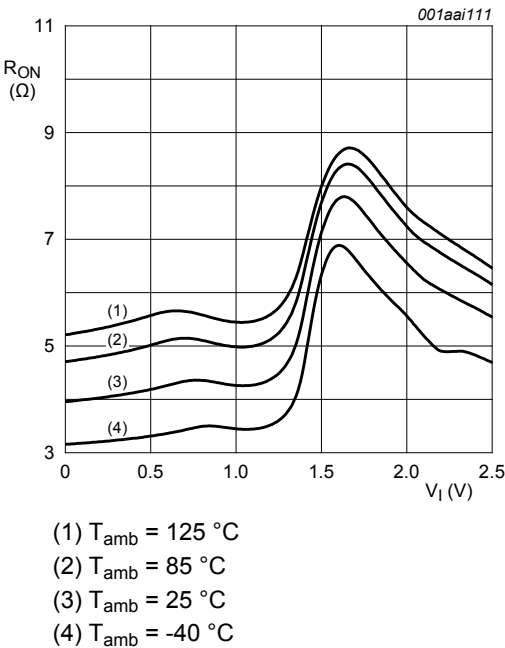


Fig. 11. ON resistance as a function of input voltage;
 $V_{CC} = 2.5\text{ V}$; $I_{SW} = 64\text{ mA}$

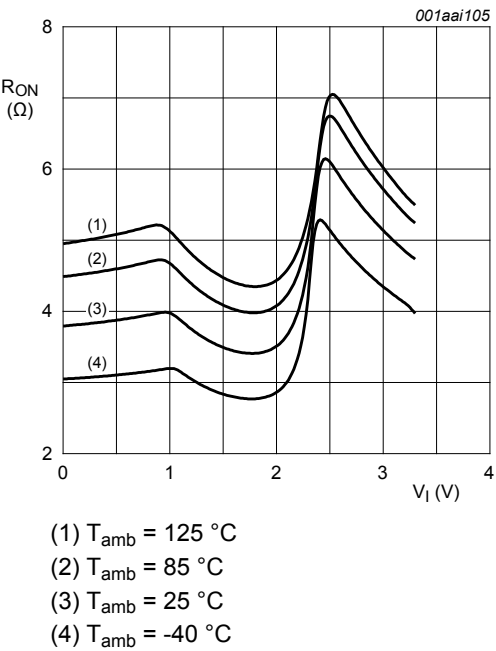


Fig. 12. ON resistance as a function of input voltage;
 $V_{CC} = 3.3\text{ V}$; $I_{SW} = 15\text{ mA}$

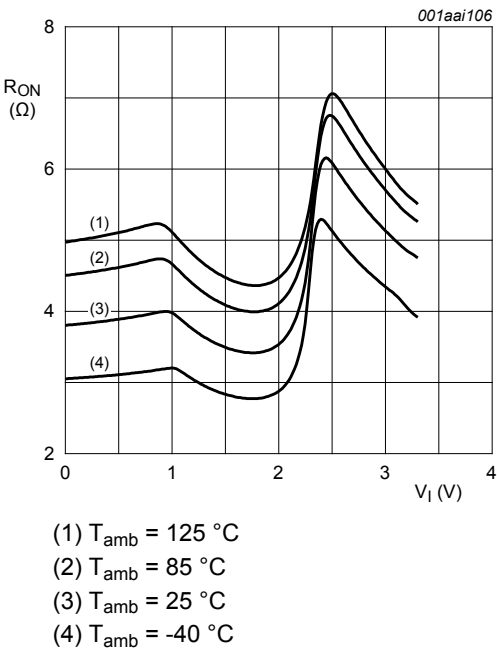
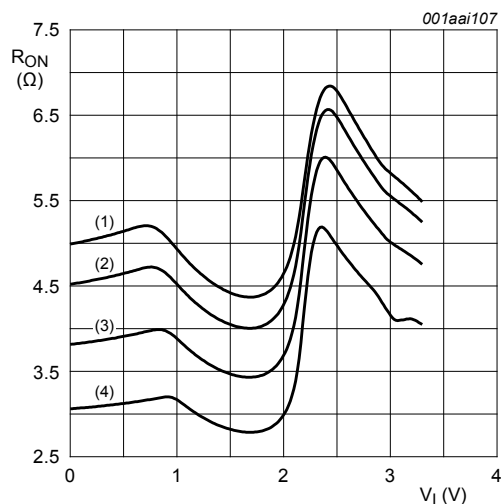


Fig. 13. ON resistance as a function of input voltage;
 $V_{CC} = 3.3\text{ V}$; $I_{SW} = 24\text{ mA}$



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$
 (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$
 (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$

Fig. 14. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$; $I_{SW} = 64\text{ mA}$

10. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit see Fig. 17

| Symbol | Parameter | Conditions | $T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$ | | | $T_{amb} = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}$ | | Unit |
|-----------|-------------------|---|---|--------|------|--|------|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| t_{pd} | propagation delay | nA to nB or nB to nA; see Fig. 15 [2] [3] | | | | | | |
| | | $V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ | - | - | 0.13 | - | 0.20 | ns |
| | | $V_{CC} = 3.0\text{ V to } 3.6\text{ V}$ | - | - | 0.20 | - | 0.31 | ns |
| t_{en} | enable time | nOE to nA or nB; see Fig. 16 [4] | | | | | | |
| | | $V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ | 1.0 | 2.7 | 4.6 | 1.0 | 6.0 | ns |
| | | $V_{CC} = 3.0\text{ V to } 3.6\text{ V}$ | 1.0 | 2.4 | 4.4 | 1.0 | 6.0 | ns |
| t_{dis} | disable time | nOE to nA or nB; see Fig. 16 [5] | | | | | | |
| | | $V_{CC} = 2.3\text{ V to } 2.7\text{ V}$ | 1.0 | 2.2 | 3.9 | 1.0 | 5.5 | ns |
| | | $V_{CC} = 3.0\text{ V to } 3.6\text{ V}$ | 1.0 | 2.9 | 4.2 | 1.0 | 5.5 | ns |

- [1] All typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$ and at nominal V_{CC} .
 [2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
 [3] t_{pd} is the same as t_{PLH} and t_{PHL} .
 [4] t_{en} is the same as t_{PZH} and t_{PZL} .
 [5] t_{dis} is the same as t_{PHZ} and t_{PLZ} .

10.1. Waveforms and test circuit

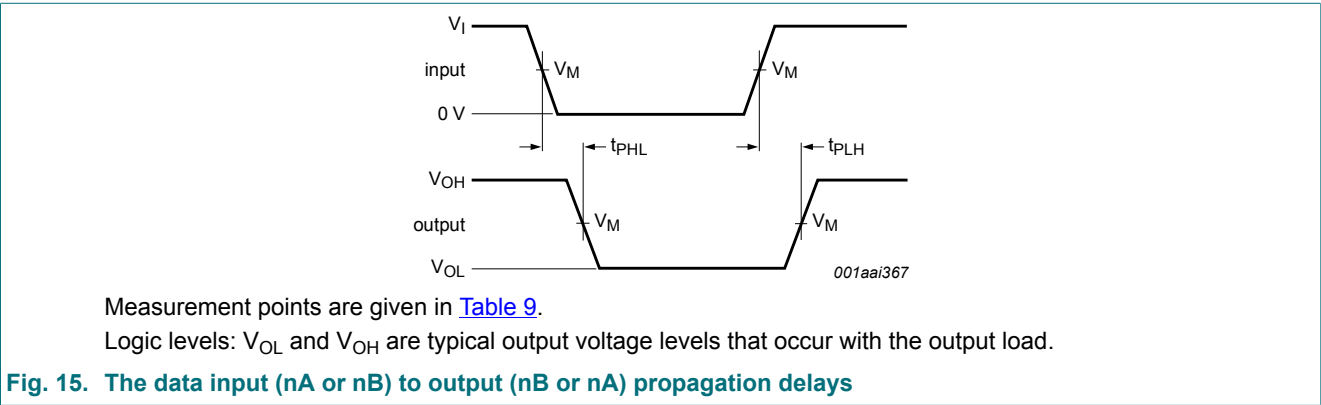
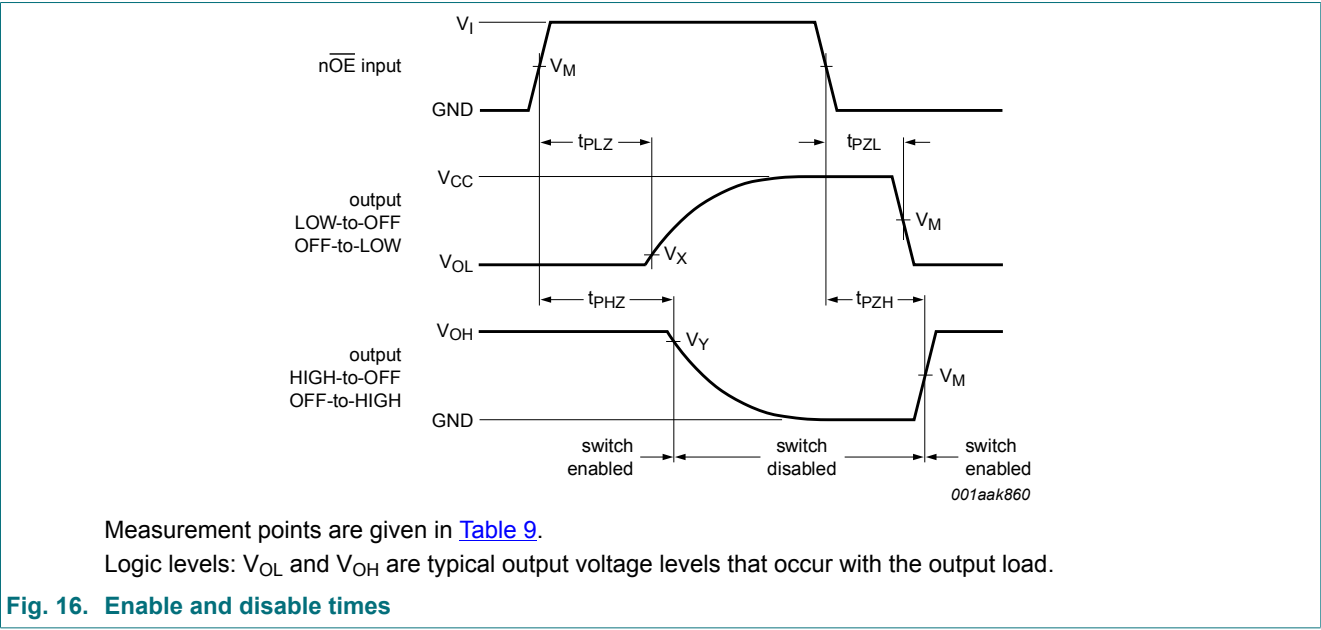
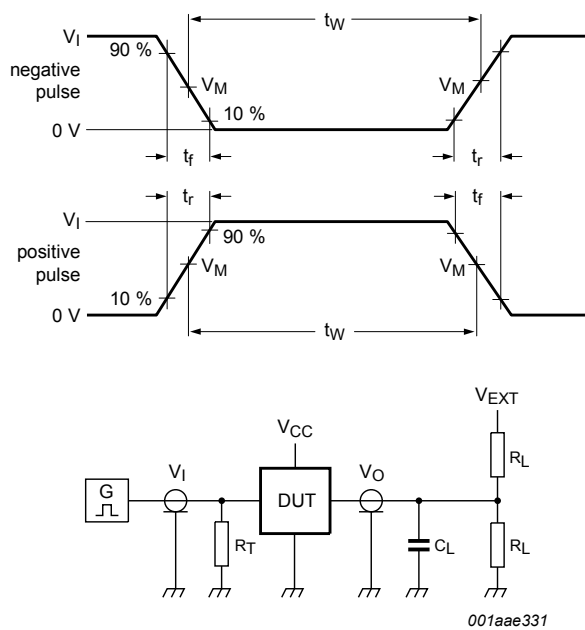


Table 9. Measurement points

| Supply voltage | Input | | | Output | | |
|----------------|-------------|----------|---------------|-------------|-------------------|-------------------|
| V_{CC} | V_M | V_I | $t_r = t_f$ | V_M | V_X | V_Y |
| 2.3 V to 2.7 V | $0.5V_{CC}$ | V_{CC} | ≤ 2.0 ns | $0.5V_{CC}$ | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 3.0 V to 3.6 V | $0.5V_{CC}$ | V_{CC} | ≤ 2.0 ns | $0.5V_{CC}$ | $V_{OL} + 0.3$ V | $V_{OH} - 0.3$ V |





Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig. 17. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Load | | V_{EXT} | | |
|----------------|-------|--------------|-----------------------|-----------------------|-----------------------|
| V_{CC} | C_L | R_L | t_{PLH} , t_{PHL} | t_{PZH} , t_{PHZ} | t_{PZL} , t_{PLZ} |
| 2.3 V to 2.7 V | 30 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 3.0 V to 3.6 V | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |

10.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | Unit |
|---------------------|--------------------------|---|--------------------------|-----|-----|------|
| | | | Min | Typ | Max | |
| f _(-3dB) | -3 dB frequency response | V _I = GND or V _{CC} ; t _r = t _f ≤ 2.5 ns; V _{CC} = 3.3 V; R _L = 50 Ω; see Fig. 18 | - | 406 | - | MHz |

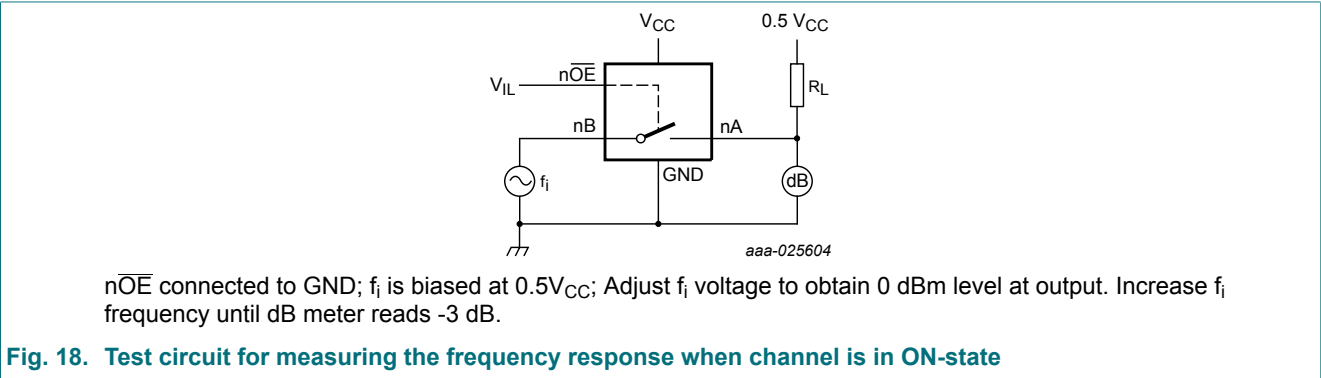


Fig. 18. Test circuit for measuring the frequency response when channel is in ON-state

11. Package outline

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

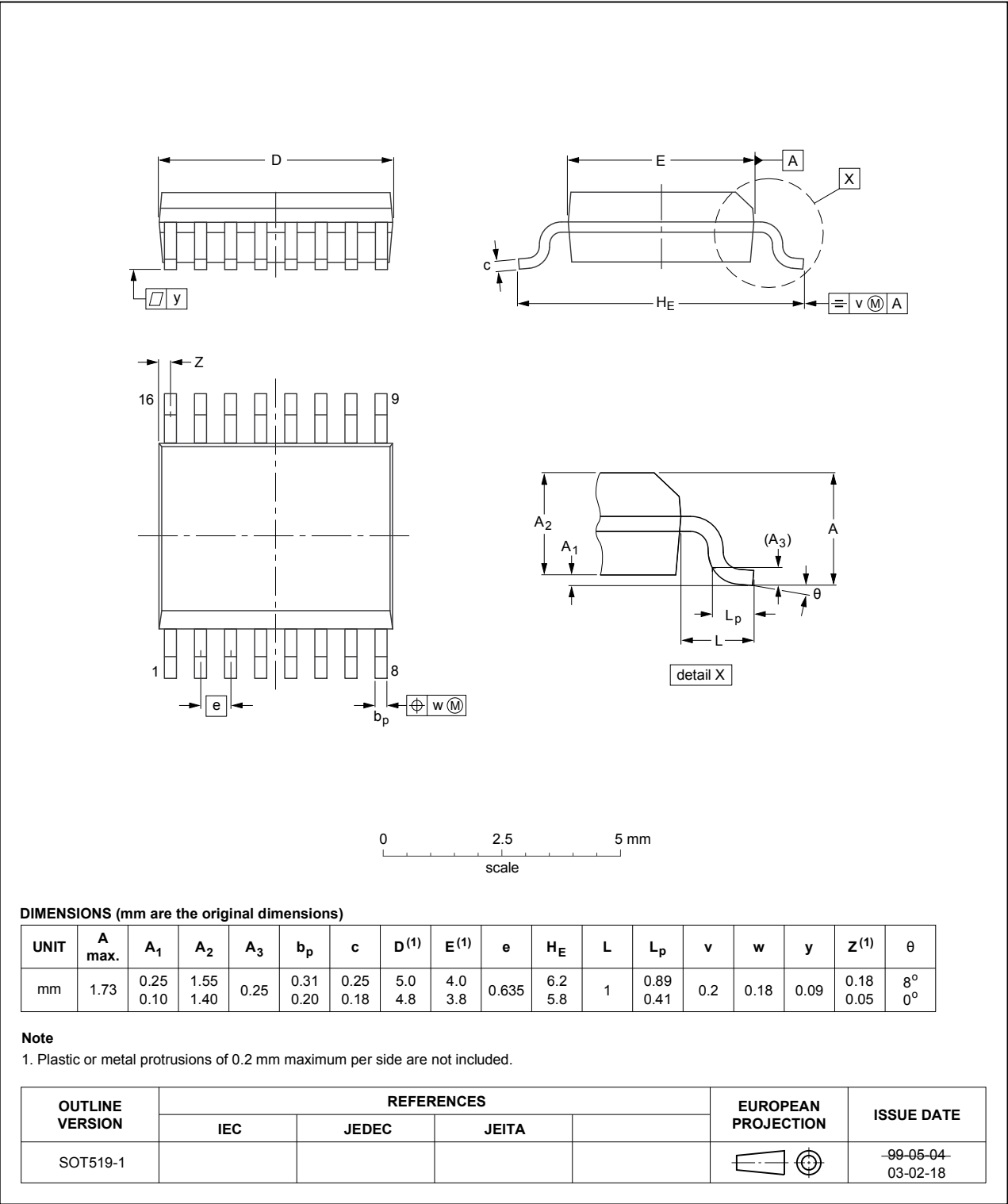
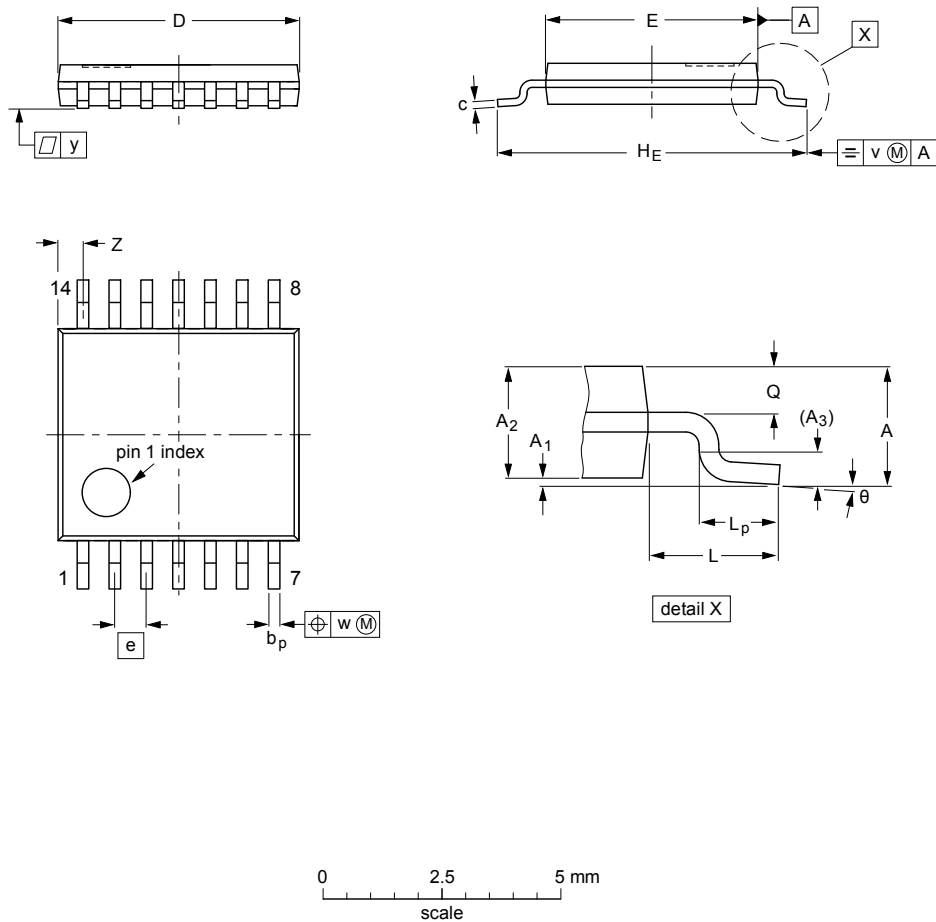


Fig. 19. Package outline SOT519-1 (SSOP16)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|-----------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|---|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.72 0.38 | 8° 0° |

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.


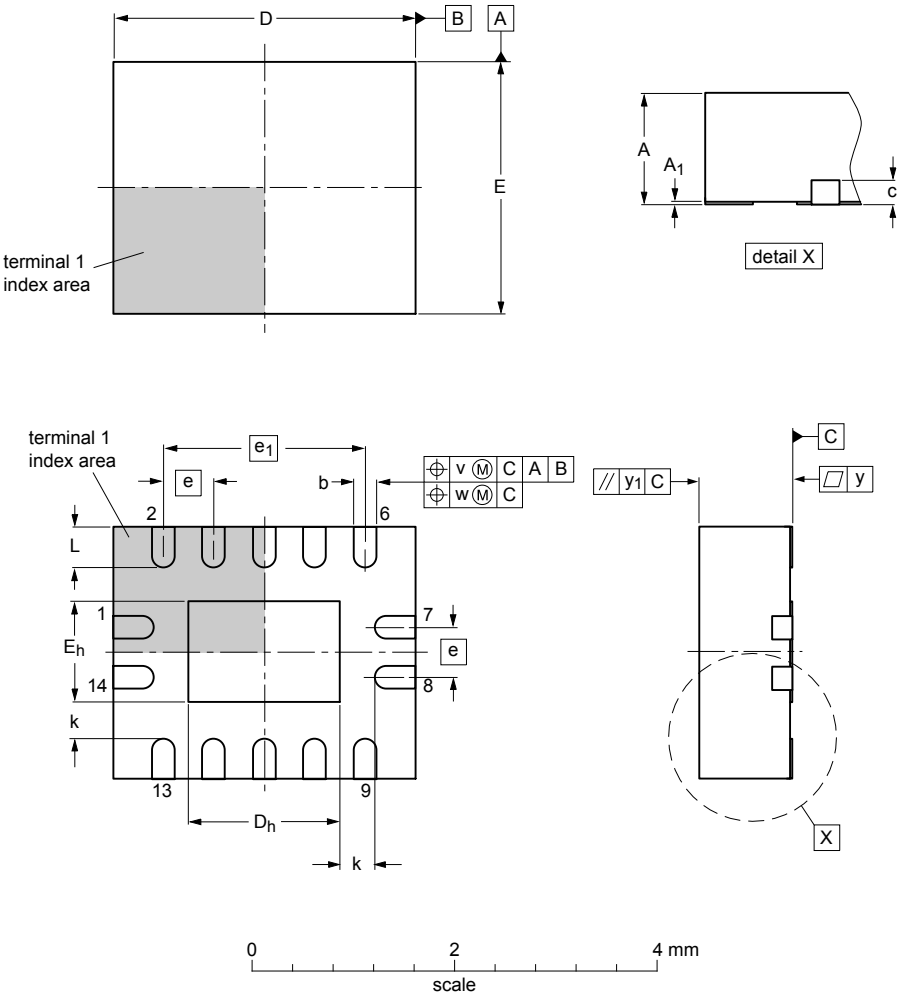
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|--------|-------|--|---|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | |  | 99-12-27 03-02-18 |

Fig. 20. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

| Unit | A ⁽¹⁾ | A ₁ | b | c | D ⁽¹⁾ | D _h | E ⁽¹⁾ | E _h | e | e ₁ | k | L | v | w | y | y ₁ |
|------|------------------|----------------|------|-----|------------------|----------------|------------------|----------------|-----|----------------|-----|-----|-----|------|------|----------------|
| max | 1 | 0.05 | 0.30 | | 3.1 | 1.65 | 2.6 | 1.15 | | | | 0.5 | | | | |
| nom | | 0.02 | 0.25 | 0.2 | 3.0 | 1.50 | 2.5 | 1.00 | 0.5 | 2 | | 0.4 | 0.1 | 0.05 | 0.05 | 0.1 |
| min | | 0.00 | 0.18 | | 2.9 | 1.35 | 2.4 | 0.85 | | | 0.2 | 0.3 | | | | |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.


| | | | | | | |
|-----------------|------------|-------|-------|--|---|----------------------|
| Outline version | References | | | | European projection | Issue date |
| | IEC | JEDEC | JEITA | | | |
| SOT762-1 | MO-241 | | | |  | 15-04-10 15-05-05 |

Fig. 21. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |

13. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--|--------------------|---------------|-----------------|
| 74CBTLV3125 v.5 | 20181008 | Product data sheet | - | 74CBTLV3125 v.4 |
| Modifications: | <ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate. | | | |
| 74CBTLV3125 v.4 | 20161109 | Product data sheet | - | 74CBTLV3125 v.3 |
| Modifications: | <ul style="list-style-type: none">Section 10.2 added. | | | |
| 74CBTLV3125 v.3 | 20111215 | Product data sheet | - | 74CBTLV3125 v.2 |
| Modifications: | <ul style="list-style-type: none">Legal pages updated. | | | |
| 74CBTLV3125 v.2 | 20110104 | Product data sheet | - | 74CBTLV3125 v.1 |
| 74CBTLV3125 v.1 | 20100108 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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