MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1 GBIT (128M × 8 BIT) CMOS NAND E^{2}PROM

DESCRIPTION

The TC58BYG0S3HBAI6 is a single 1.8V 1Gbit (1,107,296,256 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^{2}PROM) organized as (2048 + 64) bytes × 64 pages × 1024 blocks. The device has a 2112-byte static register which allows program and read data to be transferred between the register and the memory cell array in 2112-bytes increments. The Erase operation is implemented in a single block unit (128 Kbytes + 4 Kbytes: 2112 bytes × 64 pages).

The TC58BYG0S3HBAI6 is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

The TC58BYG0S3HBAI6 has ECC logic on the chip and 8bit read errors for each 528Bytes can be corrected internally.

FEATURES

- Organization x8
  - Memory cell array 2112 × 64K × 8
  - Register 2112 × 8
  - Page size 2112 bytes
  - Block size (128K + 4K) bytes
- Modes
  - Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy, ECC Status Read
- Mode control
  - Serial input/output
  - Command control
- Number of valid blocks
  - Min 1004 blocks
  - Max 1024 blocks
- Power supply
  - V_{CC} = 1.7V to 1.95V
- Access time
  - Cell array to register 40 μs typ.
  - Read Cycle Time 25 ns min (C_L=30pF)
- Program/Erase time
  - Auto Page Program 330 μs/page typ.
  - Auto Block Erase 3.5 ms/block typ.
- Operating current
  - Read (25 ns cycle) 30 mA max
  - Program (avg.) 30 mA max
  - Erase (avg.) 30 mA max
  - Standby 50 μA max
- Package
  - P-VFBGA67-0608-0.80-001 (Weight: 0.095 g typ.)
- 8bit ECC for each 528Bytes is implemented on a chip.

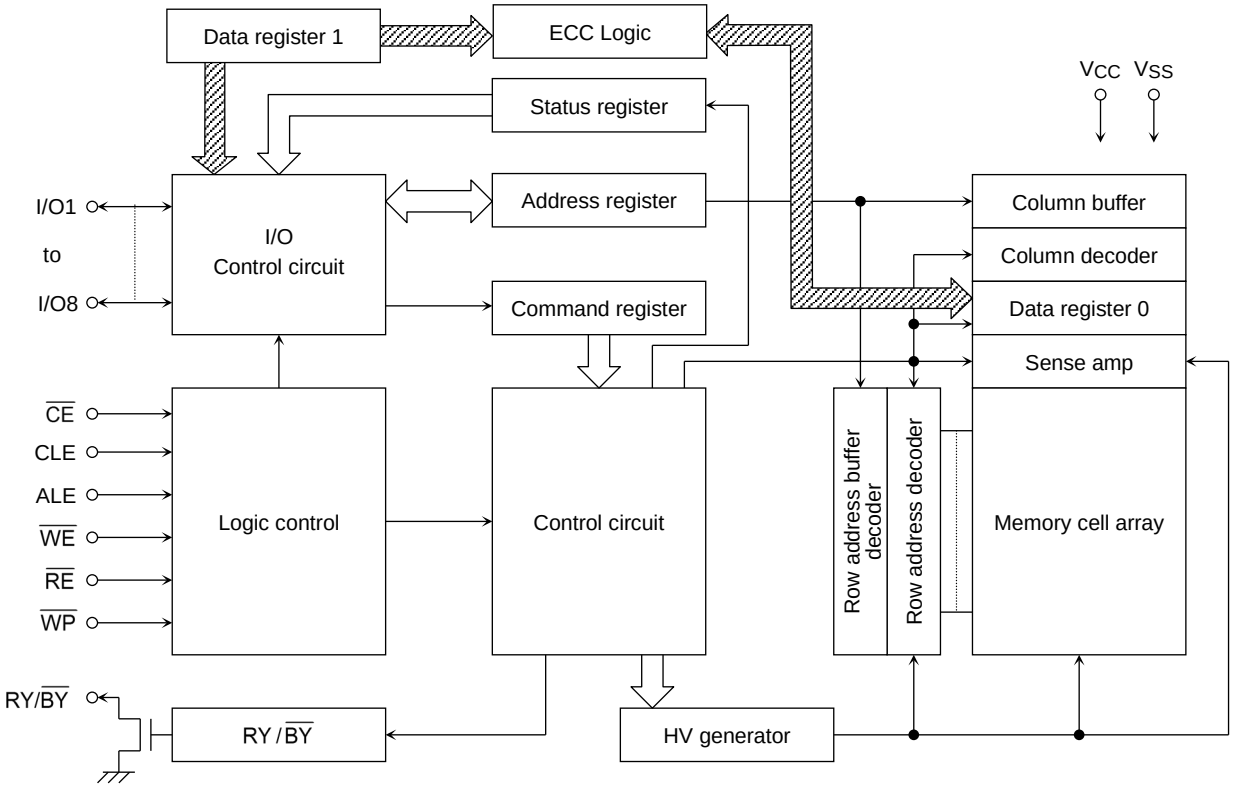
PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8
A		NC	NC			NC	NC	NC
B	NC	$\overline{WP}$	ALE	V_{SS}	$\overline{CE}$	$\overline{WE}$	RY/$\overline{BY}$	NC
C	NC	NC	$\overline{RE}$	CLE	NC	NC	NC	NC
D		NC	NC	NC	NC	NC	NC	
E		NC	NC	NC	NC	NC	NC	
F		NC	NC	NC	NC	NC	NC	
G		NC	I/O1	NC	NC	NC	V_{CC}	
H	NC	NC	I/O2	NC	V_{CC}	I/O6	I/O8	NC
J	NC	V_{SS}	I/O3	I/O4	I/O5	I/O7	V_{SS}	NC
K	NC	NC	NC			NC	NC	NC

PIN NAMES

I/O1 to I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
V_{CC}	Power supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 2.5	V
V_{IN}	Input Voltage	−0.6 to 2.5	V
$V_{I/O}$	Input /Output Voltage	−0.6 to V_{CC} + 0.3 (≤ 2.5 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	−55 to 125	°C
T_{OPR}	Operating Temperature	-40 to 85	°C

CAPACITANCE *(Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.

VALID BLOCKS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
N_{VB}	Number of Valid Blocks	1004	—	1024	Blocks

NOTE: The device occasionally contains unusable blocks. Refer to Application Note (13) toward the end of this document.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{CC}	Power Supply Voltage	1.7	—	1.95	V
V_{IH}	High Level Input Voltage	V_{CC} x 0.8	—	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	–0.3*	—	V_{CC} x 0.2	V

* –2 V (pulse width lower than 20 ns)

DC CHARACTERISTICS (Ta = -40 to 85°C, V_{CC} = 1.7 to 1.95V)

SYMBOL	PARAMETER	CONDITION	MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	—	—	±10	μA
I_{CCO1}	Serial Read Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, t_{RC} = 25 ns	—	—	30	mA
I_{CCO2}	Programming Current	—	—	—	30	mA
I_{CCO3}	Erasing Current	—	—	—	30	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} – 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	—	—	50	μA
V_{OH}	High Level Output Voltage	I_{OH} = –0.1 mA	V_{CC} – 0.2	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1 mA	—	—	0.2	V
I_{OL} (RY/$\overline{BY}$)	Output Current of RY/$\overline{BY}$ pin	V_{OL} = 0.2 V	—	4	—	mA

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(Ta = -40 to 85°C, V_{CC} = 1.7 to 1.95V)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CLS}	CLE Setup Time	12	—	ns
t_{CLH}	CLE Hold Time	5	—	ns
t_{CS}	$\overline{CE}$ Setup Time	20	—	ns
t_{CH}	$\overline{CE}$ Hold Time	5	—	ns
t_{WP}	Write Pulse Width	12	—	ns
t_{ALS}	ALE Setup Time	12	—	ns
t_{ALH}	ALE Hold Time	5	—	ns
t_{DS}	Data Setup Time	12	—	ns
t_{DH}	Data Hold Time	5	—	ns
t_{WC}	Write Cycle Time	25	—	ns
t_{WH}	$\overline{WE}$ High Hold Time	10	—	ns
t_{WW}	$\overline{WP}$ High to $\overline{WE}$ Low	100	—	ns
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20	—	ns
t_{RW}	Ready to $\overline{WE}$ Falling Edge	20	—	ns
t_{RP}	Read Pulse Width	12	—	ns
t_{RC}	Read Cycle Time	25	—	ns
t_{REA}	$\overline{RE}$ Access Time	—	20	ns
t_{CEA}	$\overline{CE}$ Access Time	—	25	ns
t_{CLR}	CLE Low to $\overline{RE}$ Low	10	—	ns
t_{AR}	ALE Low to $\overline{RE}$ Low	10	—	ns
t_{RHOH}	$\overline{RE}$ High to Output Hold Time	25	—	ns
t_{RLOH}	$\overline{RE}$ Low to Output Hold Time	5	—	ns
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	—	60	ns
t_{CHZ}	$\overline{CE}$ High to Output High Impedance	—	20	ns
t_{CSD}	$\overline{CE}$ High to ALE or CLE Don't Care	0	—	ns
t_{REH}	$\overline{RE}$ High Hold Time	10	—	ns
t_{IR}	Output-High-Impedance-to-$\overline{RE}$ Falling Edge	0	—	ns
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	30	—	ns
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	30	—	ns
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	60	—	ns
t_{WB}	$\overline{WE}$ High to Busy	—	100	ns
t_{RST}	Device Reset Time (Ready/Read/Program/Erase)	—	5/5/10/500	μs

*1: tCLS and tALS can not be shorter than tWP.

*2: tCS should be longer than tWP + 8ns.

AC TEST CONDITIONS

PARAMETER	CONDITION
	V_{CC}: 1.7 to 1.95
Input level	V_{CC}-0.2V, 0.2V
Input pulse rise and fall time	3 ns
Input comparison level	V_{CC} / 2
Output data comparison level	V_{CC} / 2
Output load	C_L (30 pF) + 1 TTL

Note: Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.
(Refer to Application Note (9) toward the end of this document)

PROGRAMMING / ERASING / READING CHARACTERISTICS

(Ta = -40 to 85°C, V_{CC} = 1.7 to 1.95V)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT	NOTES
t_{PROG}	Average Programming Time	—	330	700	μs	
N	Number of Partial Program Cycles in the Same Page	—	—	4		(1)
t_{BERASE}	Block Erasing Time	—	3.5	10	ms	
t_R	Memory Cell Array to Starting Address	—	40	120	μs	

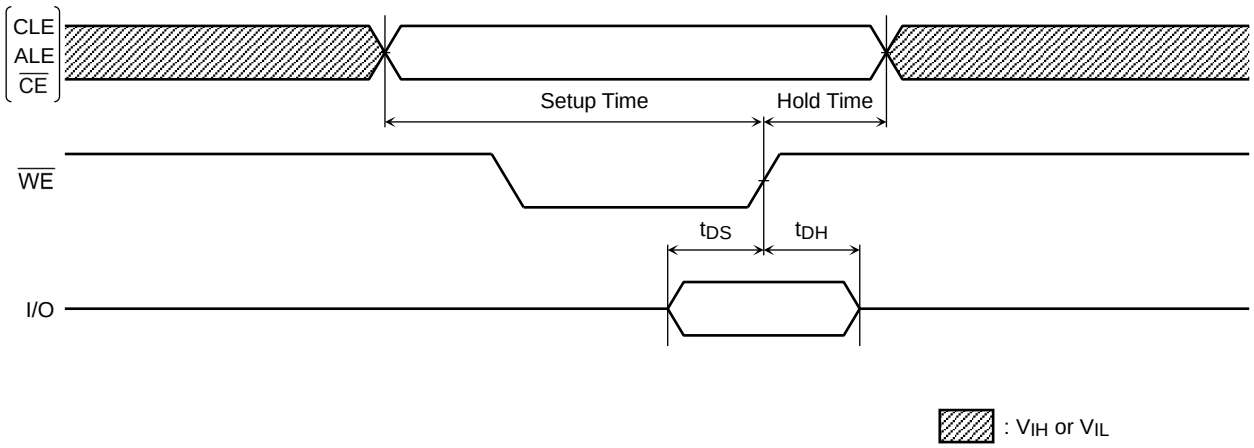
(1) Refer to Application Note (12) toward the end of this document.

Data Output

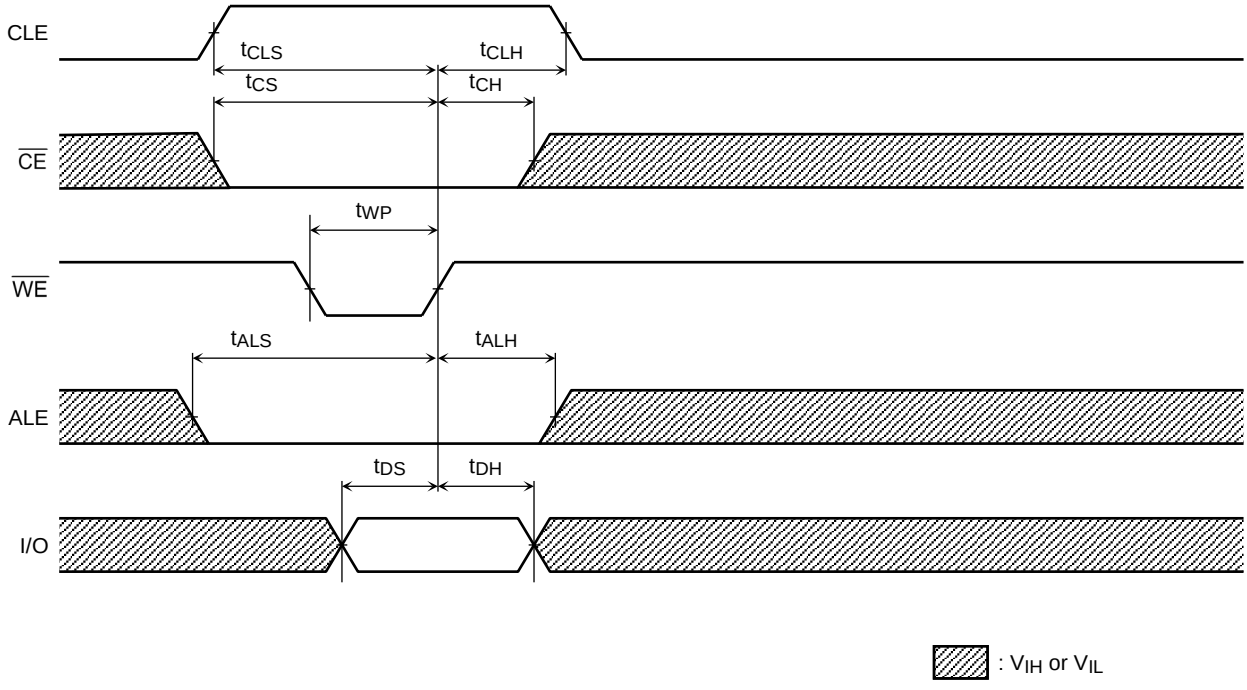
When tREH is long, output buffers are disabled by /RE=High, and the hold time of data output depend on tRHOH (25ns MIN). On this condition, waveforms look like normal serial read mode.
When tREH is short, output buffers are not disabled by /RE=High, and the hold time of data output depend on tRLOH (5ns MIN). On this condition, output buffers are disabled by the rising edge of CLE, ALE, /CE or falling edge of /WE, and waveforms look like Extended Data Output Mode.

TIMING DIAGRAMS

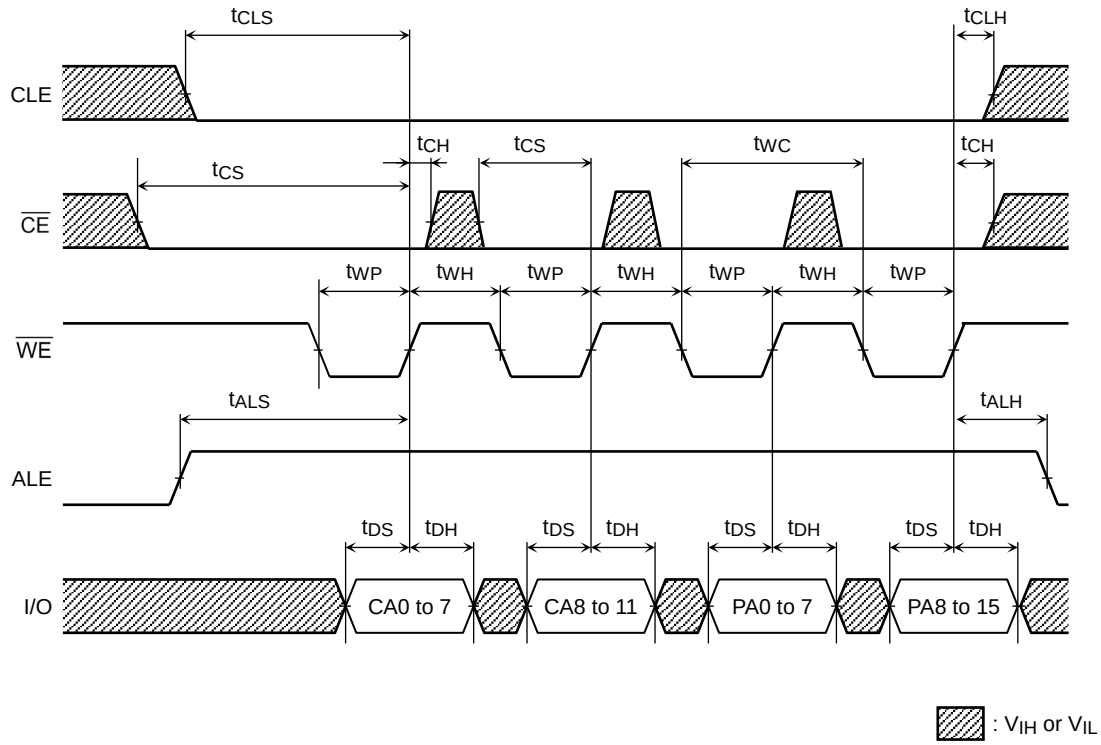
Latch Timing Diagram for Command/Address/Data



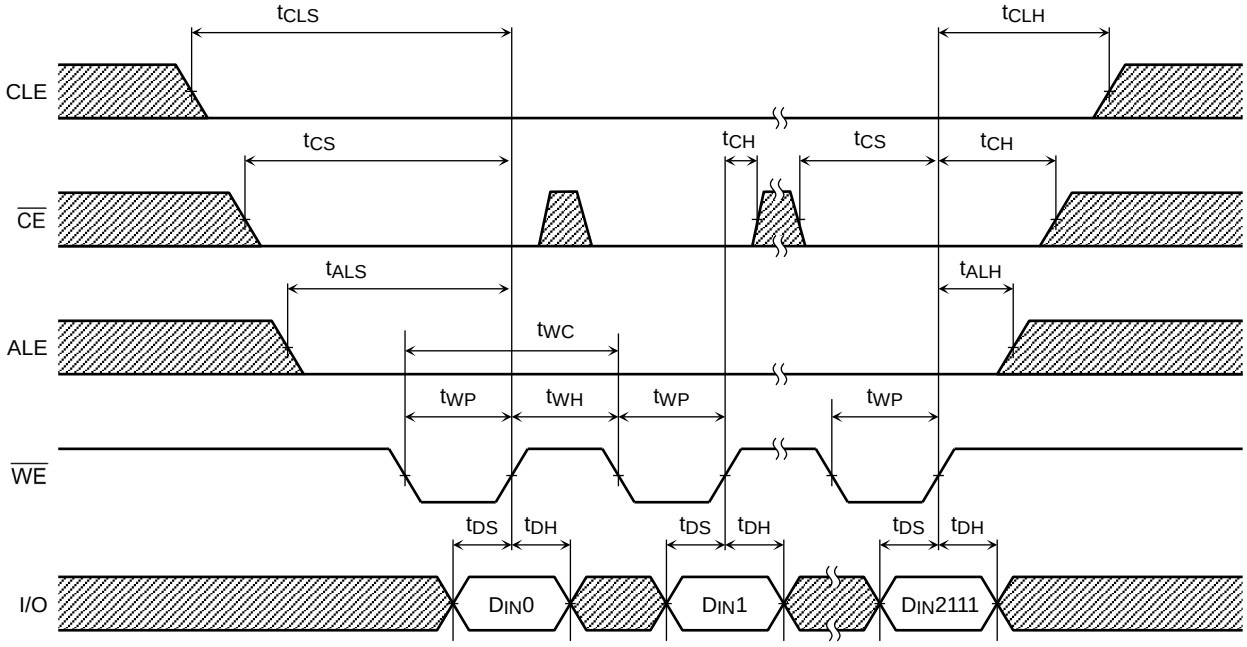
Command Input Cycle Timing Diagram



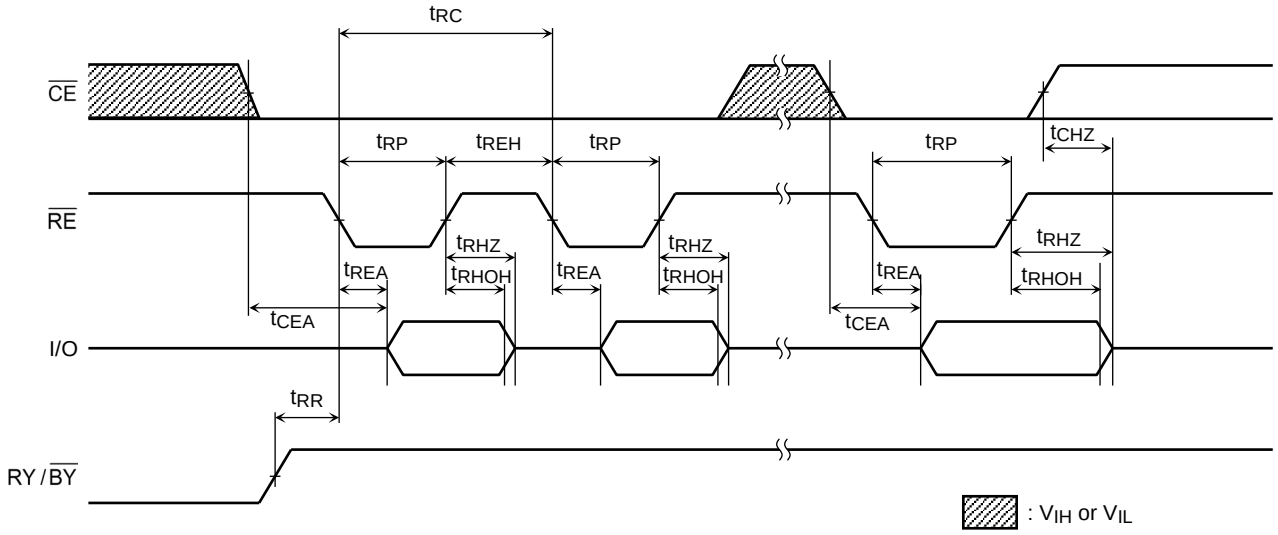
Address Input Cycle Timing Diagram



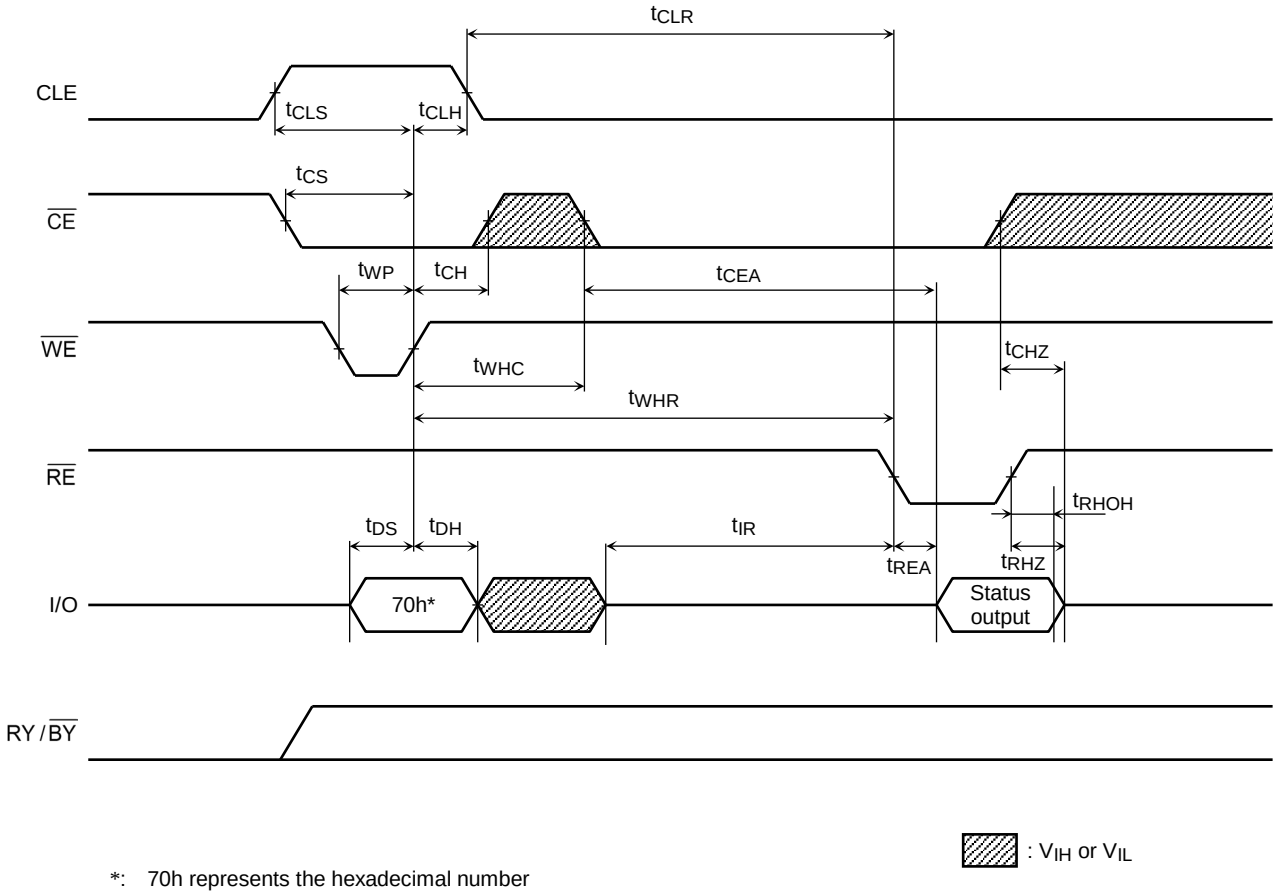
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram

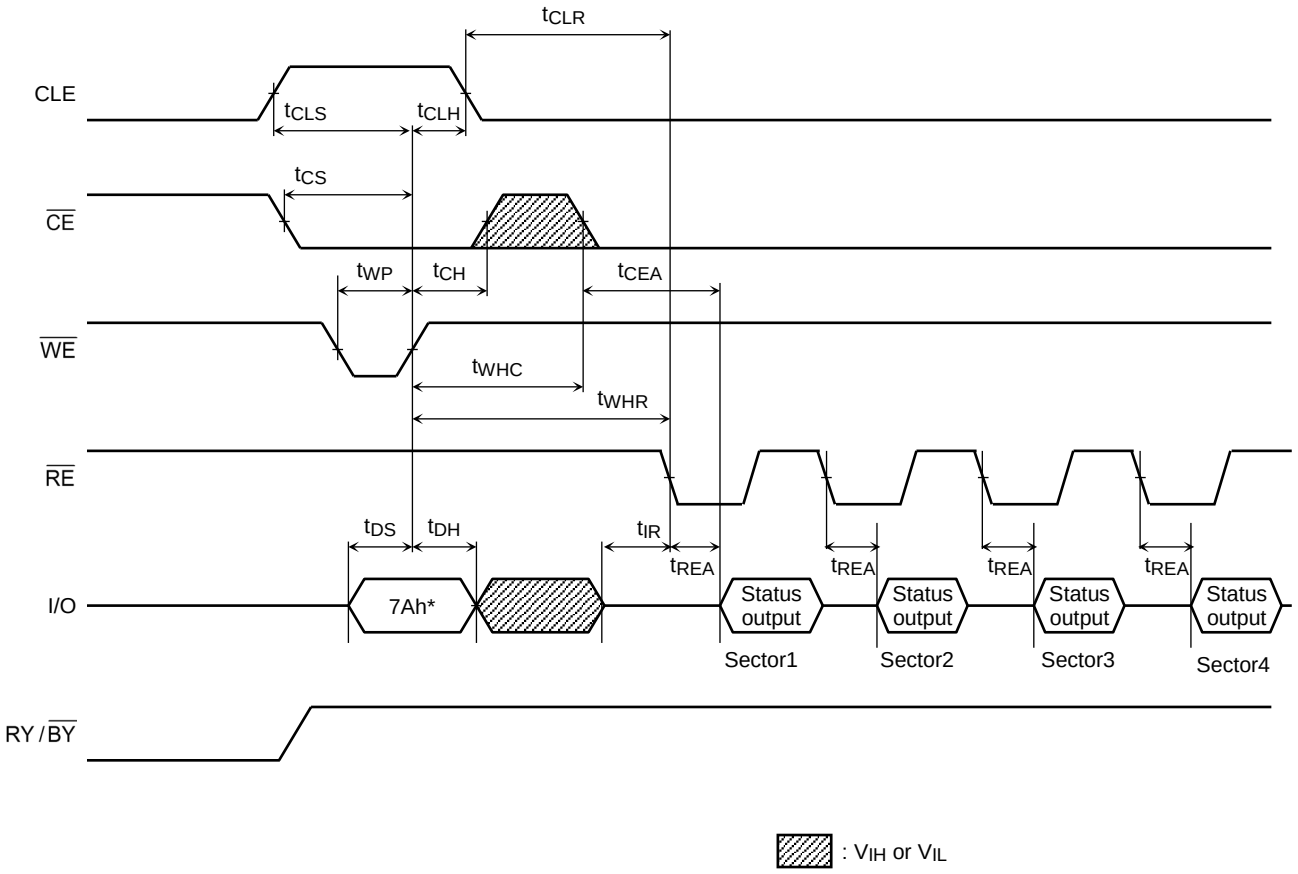


Status Read Cycle Timing Diagram



*: 70h represents the hexadecimal number

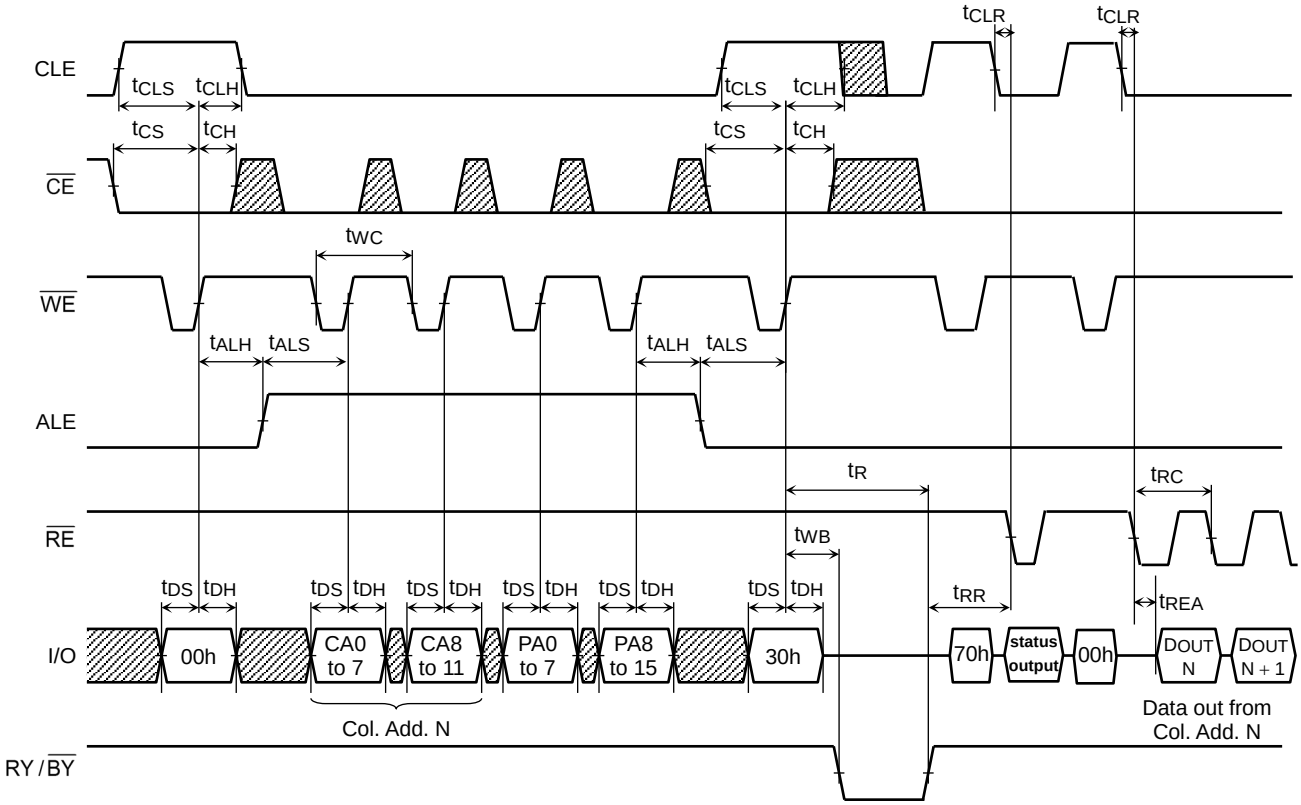
ECC Status Read Cycle Timing Diagram



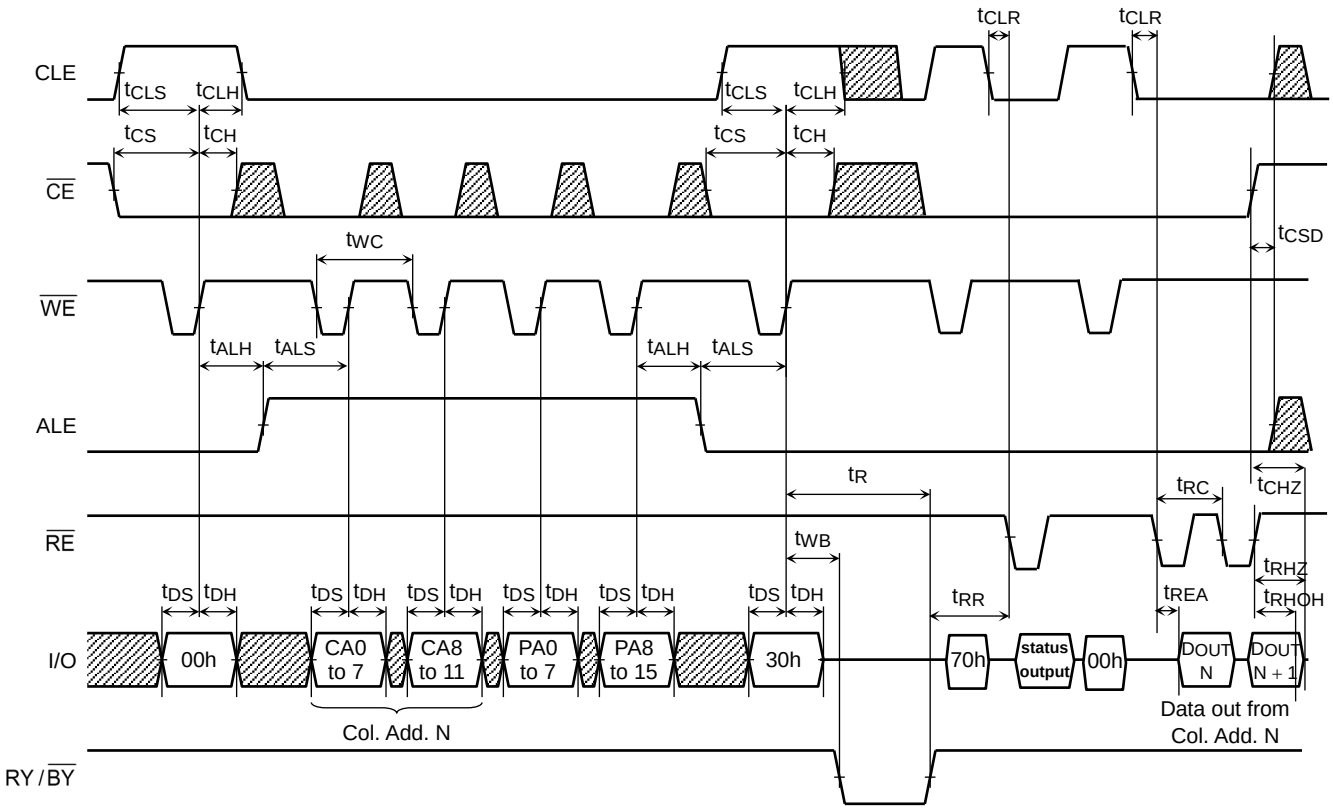
* :ECC Status output should be read for all 4 sector information

** :7Ah command can be input to the device from [after RY/$\overline{BY}$ returns to High] to [before Dout or Next command input].

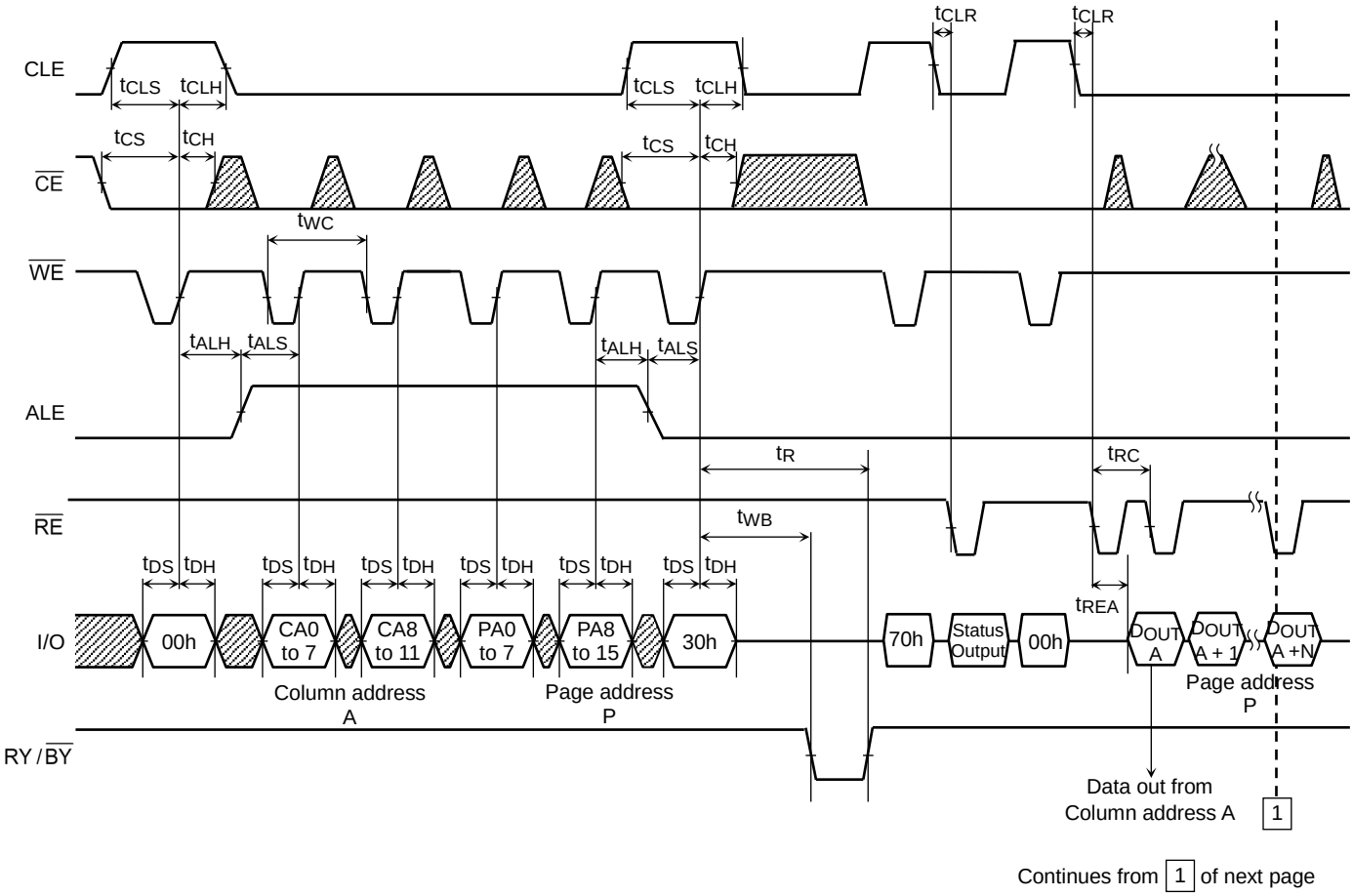
Read Cycle Timing Diagram



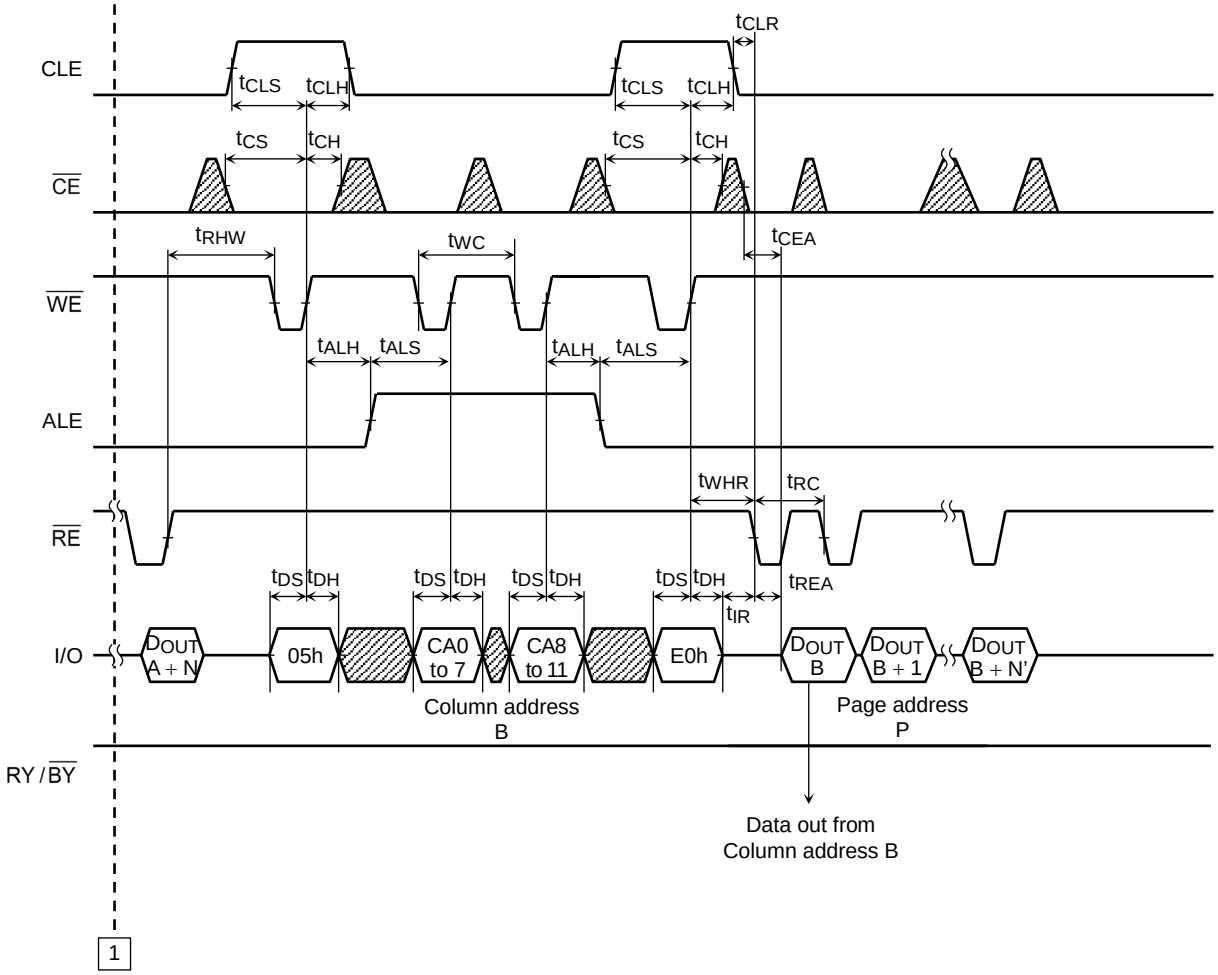
Read Cycle Timing Diagram: When Interrupted by $\overline{CE}$



Column Address Change in Read Cycle Timing Diagram (1/2)



Column Address Change in Read Cycle Timing Diagram (2/2)



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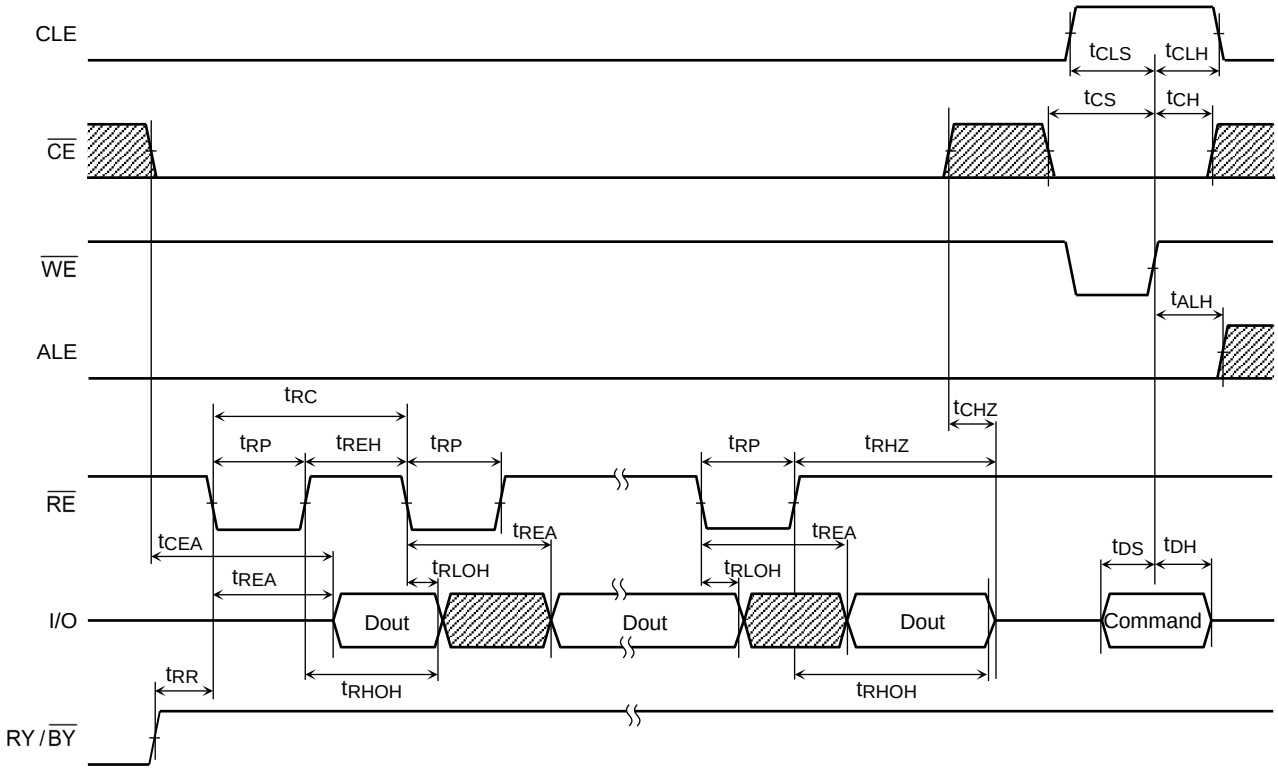
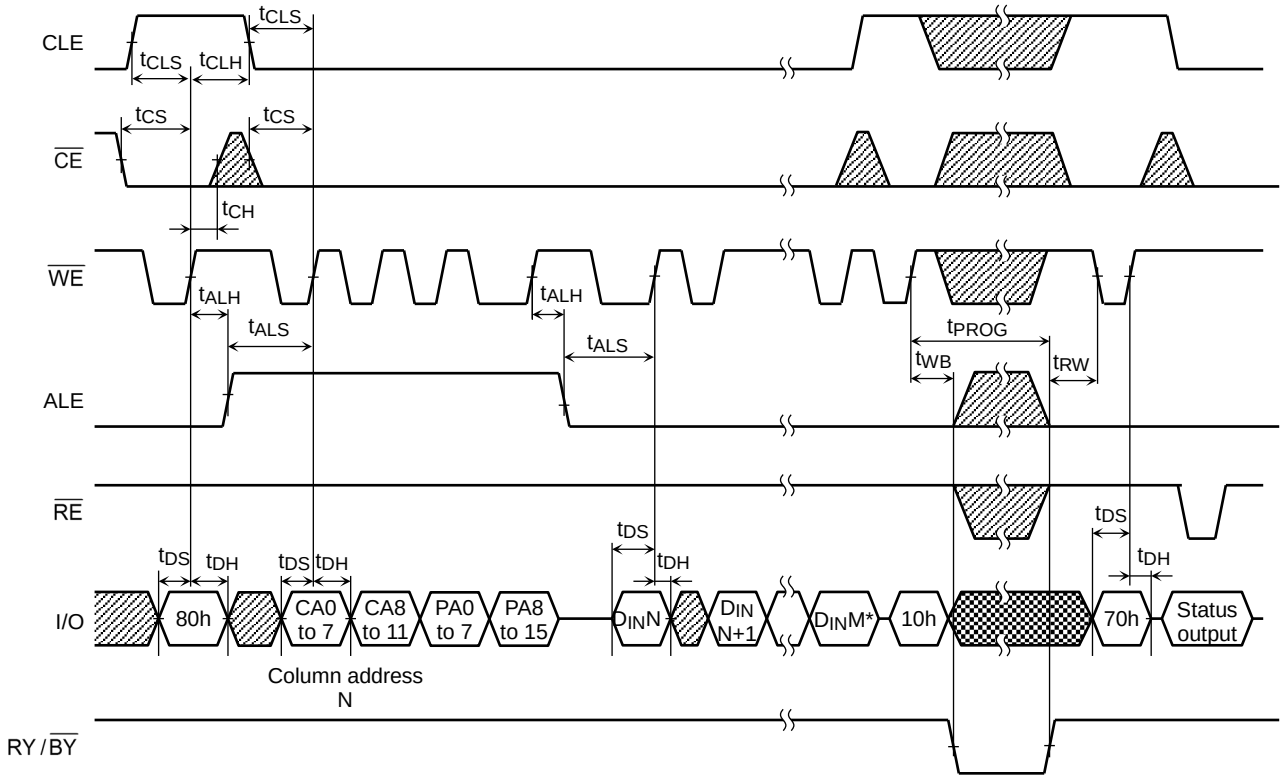
Data Output Timing Diagram



Auto-Program Operation Timing Diagram

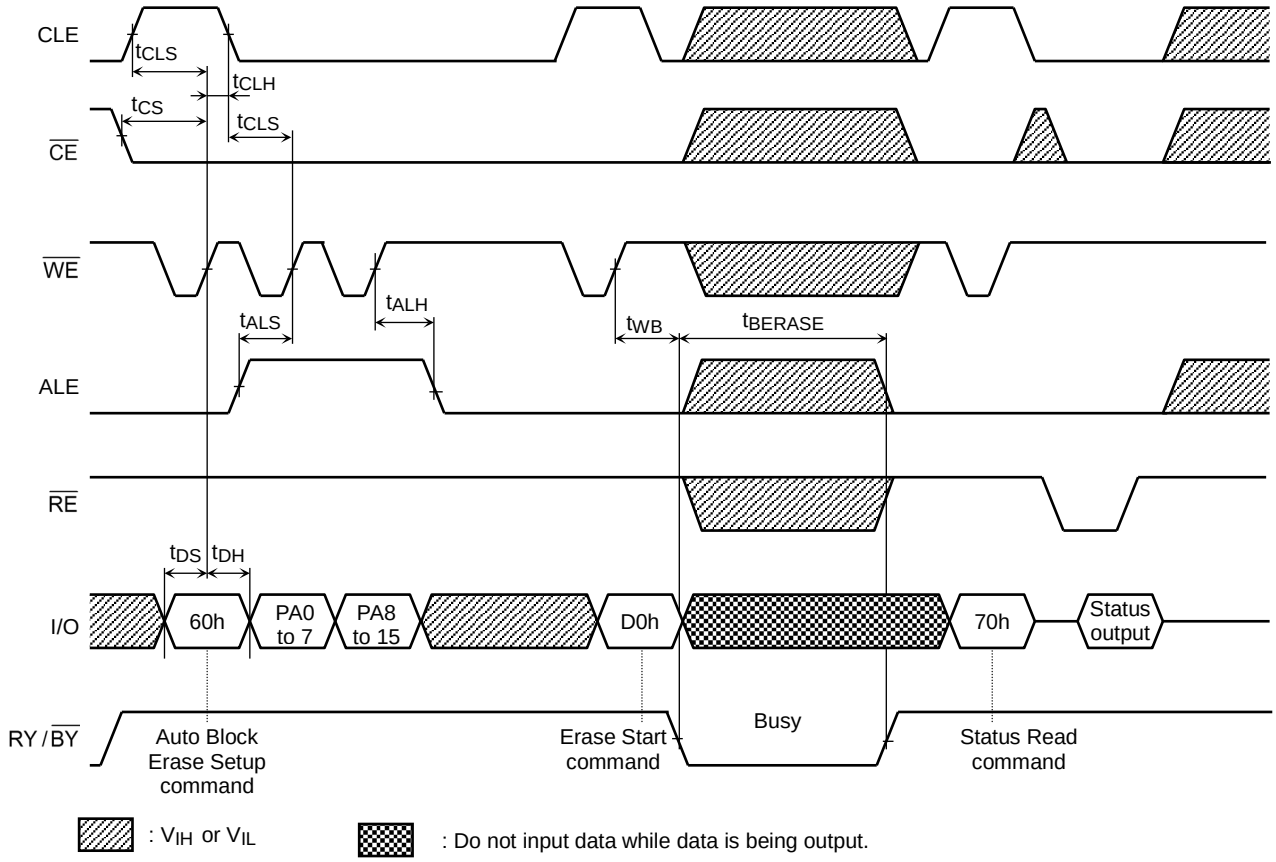


: Do not input data while data is being output.

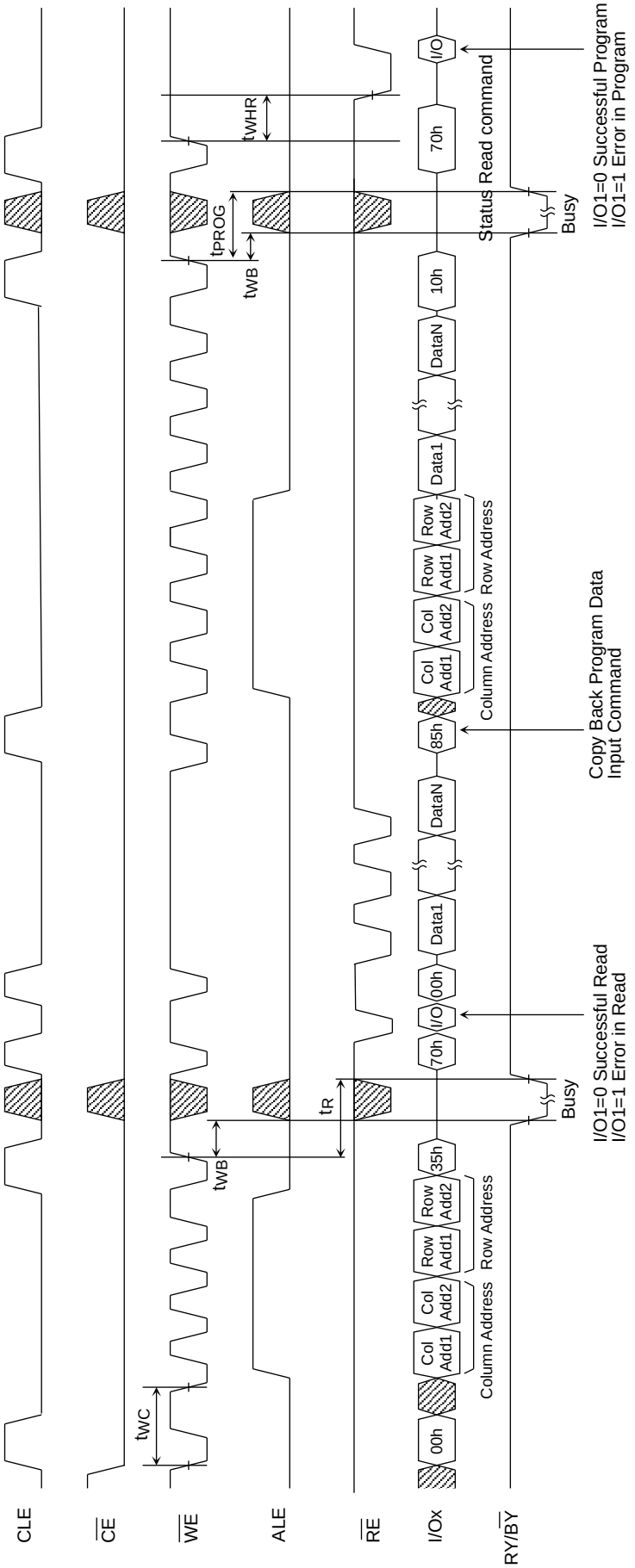
: V_{IH} or V_{IL}

*) M: up to 2111

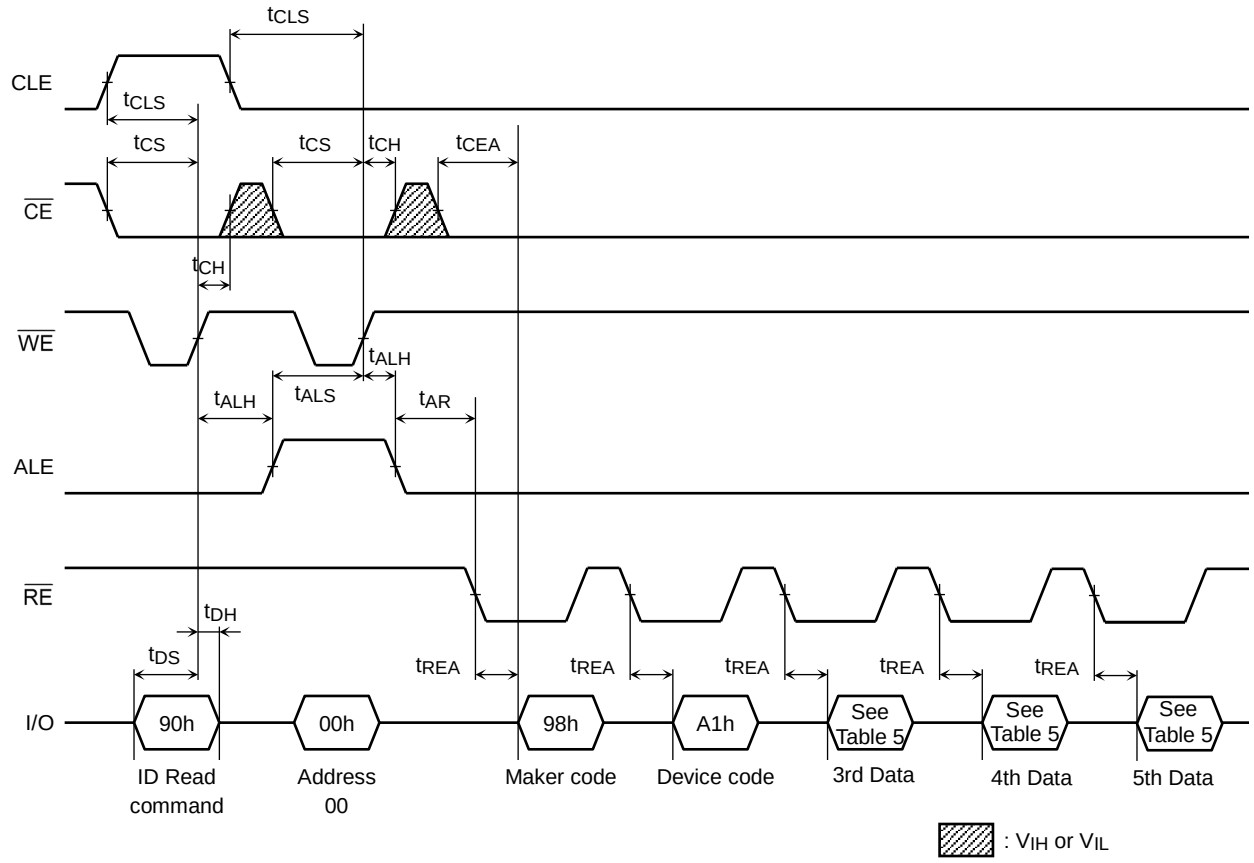
Auto Block Erase Timing Diagram



Copy Back Program with Random Data Input



ID Read Operation Timing Diagram



PIN FUNCTIONS

The device is a serial access memory which utilizes time-sharing input of address information.

Command Latch Enable: CLE

The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High.

Address Latch Enable: ALE

The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of $\overline{WE}$ while ALE is High.

Chip Enable: $\overline{CE}$

The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state ($RY/\overline{BY}$ = L), such as during a Program, Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High.

Write Enable: $\overline{WE}$

The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.

Read Enable: $\overline{RE}$

The $\overline{RE}$ signal controls serial data output. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal column address counter is also incremented (Address = Address + 1) on this falling edge.

I/O Port: I/O1 to 8

The I/O1 to 8 pins are used as a port for transferring address, command and input/output data to and from the device.

Write Protect: $\overline{WP}$

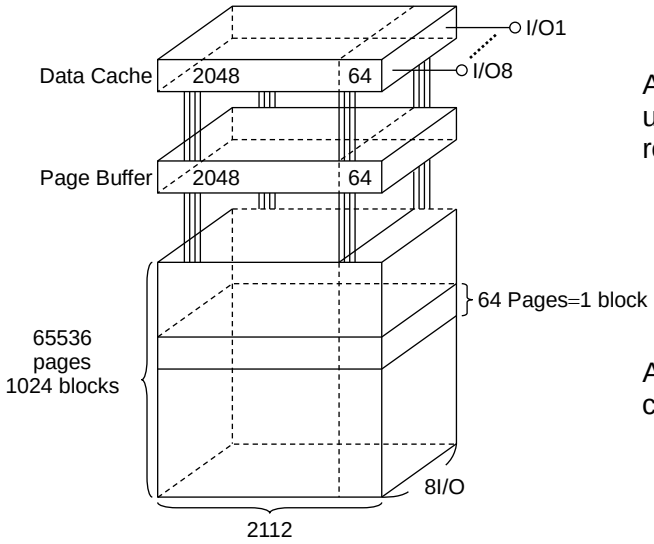
The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

Ready/Busy: $RY/\overline{BY}$

The $RY/\overline{BY}$ output signal is used to indicate the operating condition of the device. The $RY/\overline{BY}$ signal is in Busy state ($RY/\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state ($RY/\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to V_{CC} with an appropriate resistor.

Schematic Cell Layout and Address Assignment

The Program operation works on page units while the Erase operation works on block units.



A page consists of 2112 bytes in which 2048 bytes are used for main memory storage and 64 bytes are for redundancy or for other uses.

1 page = 2112 bytes
1 block = 2112 bytes × 64 pages = (128K + 4K) bytes
Capacity = 2112 bytes × 64 pages × 1024 blocks

An address is read in via the I/O port over four consecutive clock cycles, as shown in Table 1.

Table 1. Addressing

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
First cycle	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second cycle	L	L	L	L	CA11	CA10	CA9	CA8
Third cycle	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth cycle	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8

CA0 to CA11: Column address
PA0 to PA5: Page address in block
PA6 to PA15: Block address

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by command operations shown in Table 3. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Table 2.

Table 2. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$ *1
Command Input	H	L	L	↑	H	*
Data Input	L	L	L	↑	H	H
Address Input	L	H	L	↑	H	*
Serial Data Output	L	L	L	H	↓	*
During Program (Busy)	*	*	*	*	*	H
During Erase (Busy)	*	*	*	*	*	H
During Read (Busy)	*	*	H	*	*	*
	*	*	L	H (*2)	H (*2)	*
Program, Erase Inhibit	*	*	*	*	*	L
Standby	*	*	H	*	*	0 V/V_{CC}

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

*1: Refer to Application Note (10) toward the end of this document regarding the $\overline{WP}$ signal when Program or Erase Inhibit.

*2: If $\overline{CE}$ is low during read busy, $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to the device or read to device. Reset or Status Read command can be input during Read Busy.

Table 3. Command table (HEX)

	First Set	Second Set	Acceptable while Busy
Serial Data Input	80	—	
Read	00	30	
Column Address Change in Serial Data Output	05	E0	
Auto Page Program	80	10	
Column Address Change in Serial Data Input	85	—	
Read for Copy-Back	00	35	
Copy-Back Program	85	10	
Auto Block Erase	60	D0	
ID Read	90	—	
Status Read	70	—	○
ECC Status Read	7A	—	
Reset	FF	—	○

HEX data bit assignment

(Example)

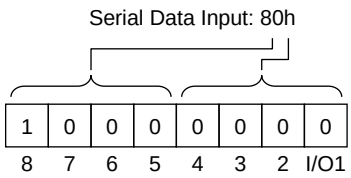


Table 4. Read mode operation states

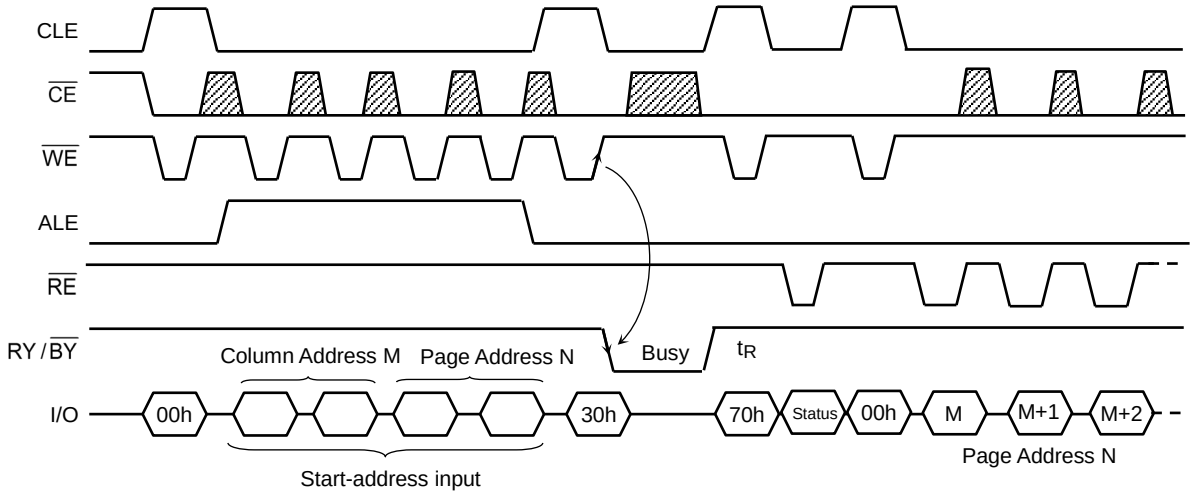
	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O1 to I/O8	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

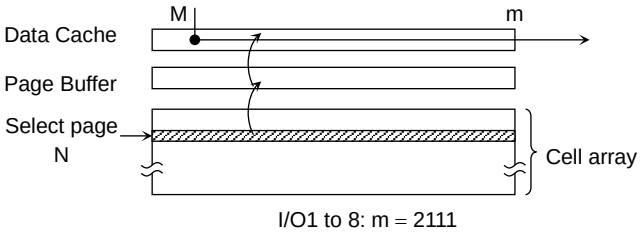
H: V_{IH}, L: V_{IL}

DEVICE OPERATION

Read Mode

Read mode is set when the "00h" and “30h” commands are issued to the Command register. Between the two commands, a start address for the Read mode needs to be issued. After initial power on sequence, “00h” command is latched into the internal command register. Therefore read operation after power on sequence is executed by the setting of only four address cycles and “30h” command. Refer to the figures below for the sequence and the block diagram (Refer to the detailed timing chart).

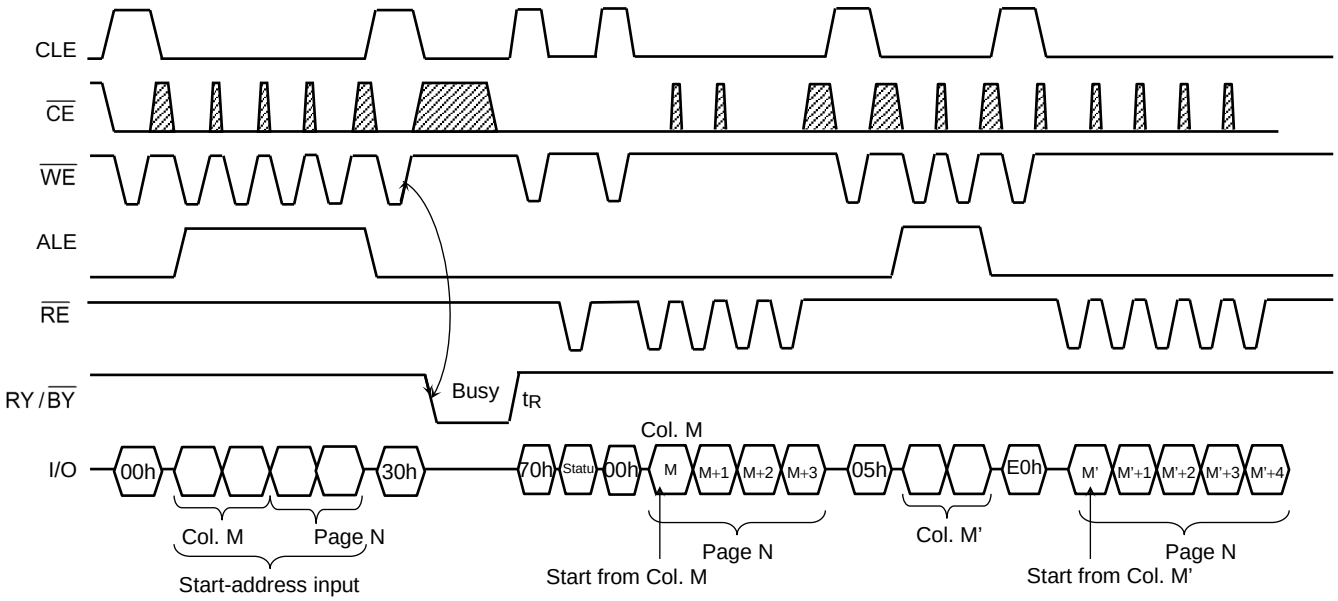


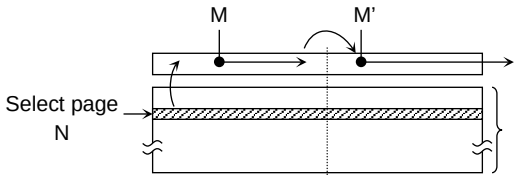


A data transfer operation from the cell array to the Data Cache via Page Buffer starts on the rising edge of $\overline{WE}$ in the 30h command input cycle (after the address information has been latched). The device will be in the Busy state during this transfer period.

After the transfer period, the device returns to Ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the start address designated in the address input cycle.

Random Column Address Change in Read Cycle





During the serial data output from the register, the column address can be changed by inputting a new column address using the 05h and E0h commands. The data is read out in serial starting at the new column address. Random Column Address Change operation can be done multiple times within the same page.

ECC & Sector definition for ECC

Internal ECC logic generates Error Correction Code during busy time in program operation. The ECC logic manages 9bit error detection and 8bit error correction in each 528Bytes of main data and spare data.
A section of main field (512Bytes) and spare field (16Bytes) are paired for ECC. During read, the device executes ECC of itself. Once read operation is executed, Status Read Command (70h) can be issued to check the read status. The read status remains until other valid commands are executed.

To use ECC function, below limitation must be considered.

- A sector is the minimum unit for program operation and the number of program per page must not exceed 4.

2KByte Page Assignment

1st Main	2nd Main	3rd Main	4th Main	1st Spare	2nd Spare	3rd Spare	4th Spare
512B	512B	512B	512B	16B	16B	16B	16B

Note) Internal ECC manages all data of Main area and Spare area.

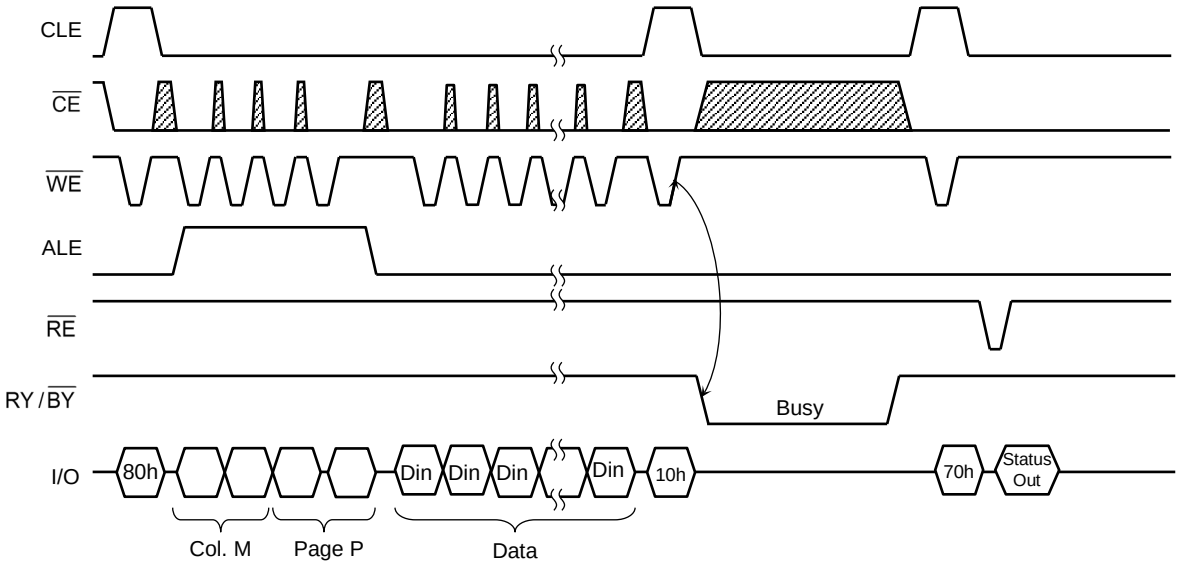
Definition of 528Byte Sector

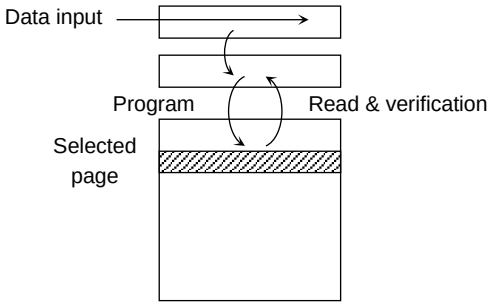
Sector	**Column Address (Byte)**	
	Main Field	**Spare Field**
1st Sector	0 to 511	2,048 to 2,063
2nd Sector	512 to 1,023	2,064 to 2,079
3rd Sector	1,024 to 1,535	2,080 to 2,095
4th Sector	1,536 to 2,047	2,096 to 2,111

Note) The ECC parity code generated by internal ECC is stored in column addresses 2112-2175 and the user cannot access to these specific addresses.
While using the Partial Page Program, the user must program the data to main field and spare field simultaneously by the definition of sector.

Auto Page Program Operation

The device carries out an Automatic Page Program operation when it receives a "10h" Program command after the address and data have been input. The sequence of command, address and data input is shown below (Refer to the detailed timing chart).



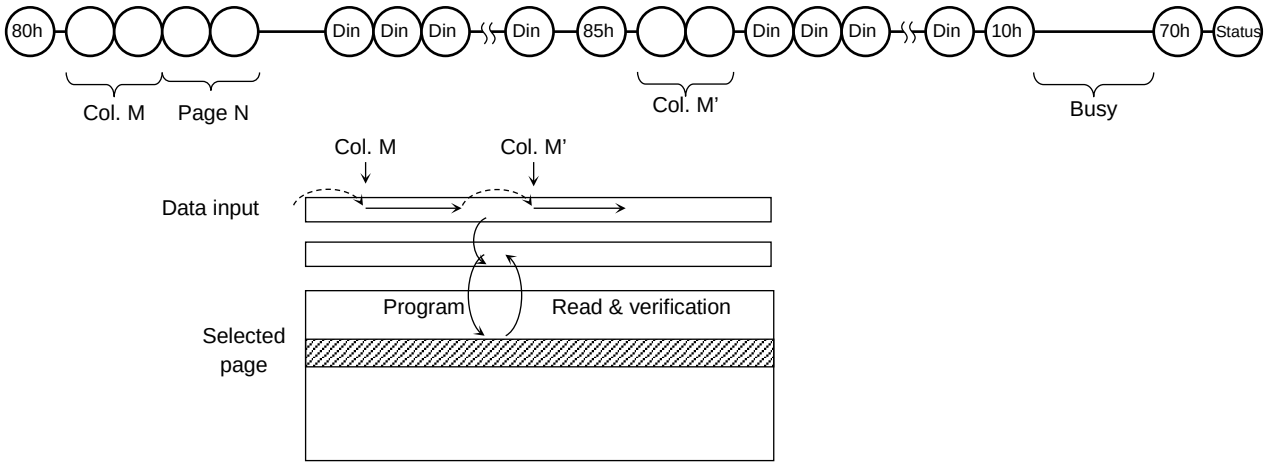


The data is transferred (programmed) from the Data Cache via the Page Buffer to the selected page on the rising edge of $\overline{WE}$ following input of the “10h” command. After programming, the programmed data is transferred back to the Page Buffer to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum loop number set in the device is reached.

Random Column Address Change in Auto Page Program Operation

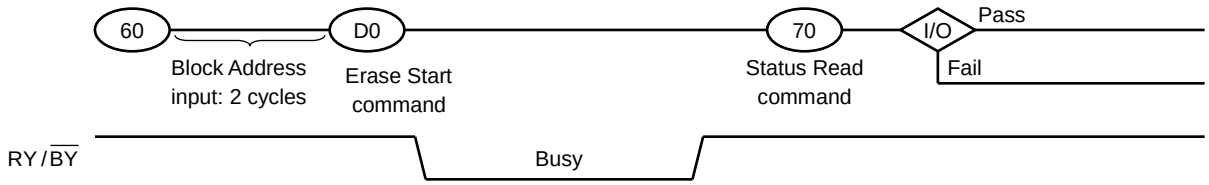
The column address can be changed by the 85h command during the data input sequence of the Auto Page Program operation.

Two address input cycles after the 85h command are recognized as a new column address for the data input. After the new data is input to the new column address, the 10h command initiates the actual data program into the selected page automatically. The Random Column Address Change operation can be repeated multiple times within the same page.



Auto Block Erase

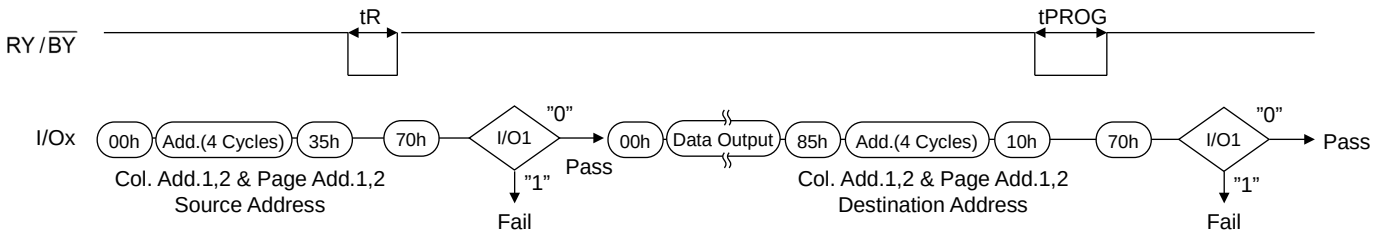
The Auto Block Erase operation starts on the rising edge of $\overline{WE}$ after the Erase Start command “D0h” which follows the Erase Setup command “60h”. This two-cycle process for Erase operations acts as an extra layer of protection from accidental erasure of data due to external noise. The device automatically executes the Erase and Verify operations.



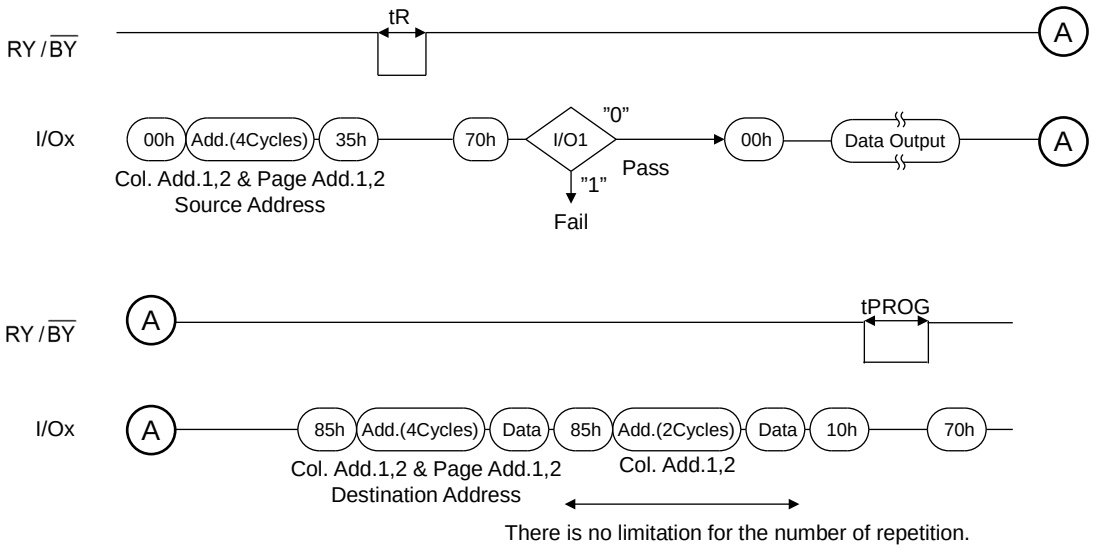
READ FOR COPY-BACK WITH DATA OUTPUT TIMING GUIDE

Copy-Back operation is a sequence execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with “35h” command and the address of source page moves the whole 2112 bytes data into the internal data buffer. Bit errors are checked by sequential reading the data or by reading the status in read after read busy time (tR) to check if uncorrectable error occurs. In the case where there is no bit error or no uncorrectable error, the data don’t need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Status Read command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the $RY/\overline{BY}$ output, or the Status Bit (I/O7) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit (I/O1) may be checked. The command register remains in Status Read mode until another valid command is written to the command register. During copy-Back program, data modification is possible using random data input command (85h) as shown below.

Page Copy-Back Program Operation



Page Copy-Back Program Operation with Random Data Input



ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

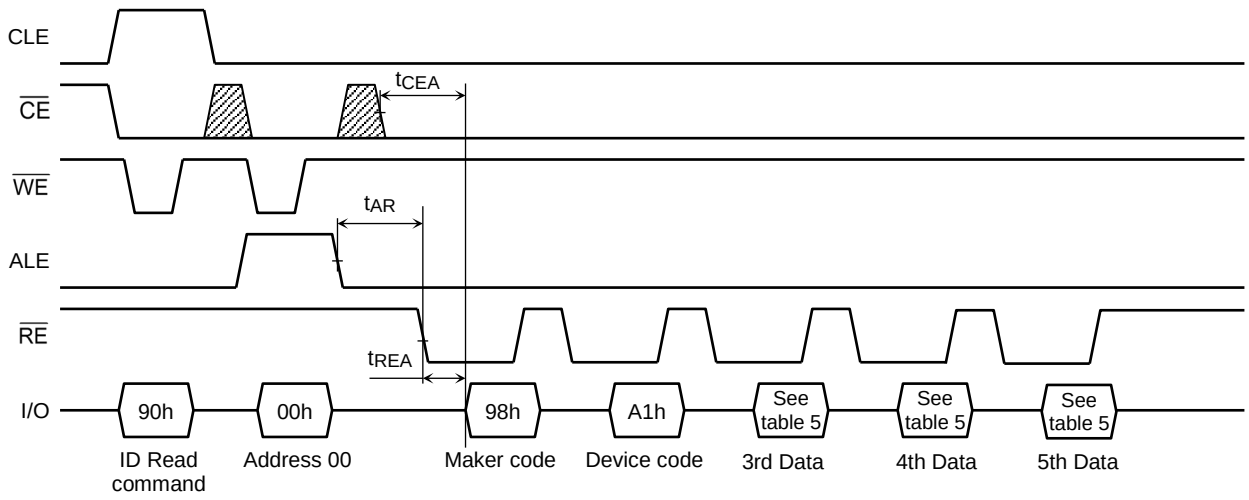


Table 5. Code table

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98h
2nd Data	Device Code	1	0	1	0	0	0	0	1	A1h
3rd Data	Chip Number, Cell Type	1	0	0	0	0	0	0	0	80h
4th Data	Page Size, Block Size	0	0	0	1	0	1	0	1	15h
5th Data	District Number	1	1	1	1	0	0	1	0	F2h

3rd Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 level cell 4 level cell 8 level cell 16 level cell					0 0 1 1	0 1 0 1		
Reserved		1	0	0	0				

4th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
Page Size (without redundant area)	1 KB 2 KB 4 KB 8 KB							0 0 1 1	0 1 0 1
Block Size (without redundant area)	64 KB 128 KB 256 KB 512 KB			0 0 1 1	0 1 0 1				
I/O Width	x8 x16		0 1						
Reserved		0				0	1		

5th Data

	Description	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1
District Number	1 District 2 District 4 District 8 District					0 0 1 1	0 1 0 1		
ECC engine on chip	With ECC engine	1							
Reserved			1	1	1			1	0

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The Status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass /fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using $\overline{RE}$ after a “70h” command input. The Status Read can also be used during a Read operation to monitor the Ready/Busy status and to find out the ECC result (pass/fail).

The resulting information is outlined in Table 6.

Table 6. Status output table

	Definition	Page Program	Block Erase	Read
I/O1	Chip Status Pass: 0 Fail: 1	Pass/Fail	Pass/Fail	Pass/Fail(Uncorrectable)
I/O2	Not Used	Invalid	Invalid	Invalid
I/O3	Not Used	0	0	0
I/O4	Chip Read Status Normal or uncorrectable: 0 Recommended to rewrite : 1	0	0	Normal or uncorrectable / Recommended to rewrite
I/O5	Not Used	0	0	0
I/O6	Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O7	Ready/Busy Ready: 1 Busy: 0	Ready/Busy	Ready/Busy	Ready/Busy
I/O8	Write Protect Not Protected :1 Protected: 0	Write Protect	Write Protect	Write Protect

The Pass/Fail status on I/O1 is only valid during a Program/Erase/Read operation when the device is in the Ready state.

ECC Status Read

The ECC Status Read function is used to monitor the Error Correction Status. The device can correct up to 8bit errors. ECC can be performed on the NAND Flash main and spare areas.

The ECC Status Read function can also show the number of errors in a sector as a result of an ECC check in during a read operation.

8	7	6	5	4	3	2	I/O1
Sector Information				ECC Status			

ECC Status

I/O4 to I/O1	ECC Status
0000	No Error
0001	1bit error(Correctable)
0010	2bit error(Correctable)
0011	3bit error(Correctable)
0100	4bit error(Correctable)
0101	5bit error(Correctable)
0110	6bit error(Correctable)
0111	7bit error(Correctable)
1000	8bit error(Correctable)
1111	Uncorrectable Error

Sector Information

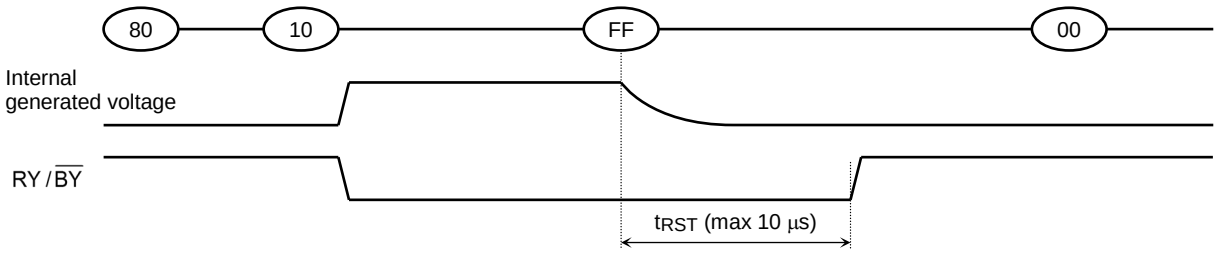
I/O8 to I/O5	Sector Information
0000	1st Sector (Main and Spare area)
0001	2nd Sector (Main and Spare area)
0010	3rd Sector (Main and Spare area)
0011	4th Sector (Main and Spare area)
Other	Reserved

Reset

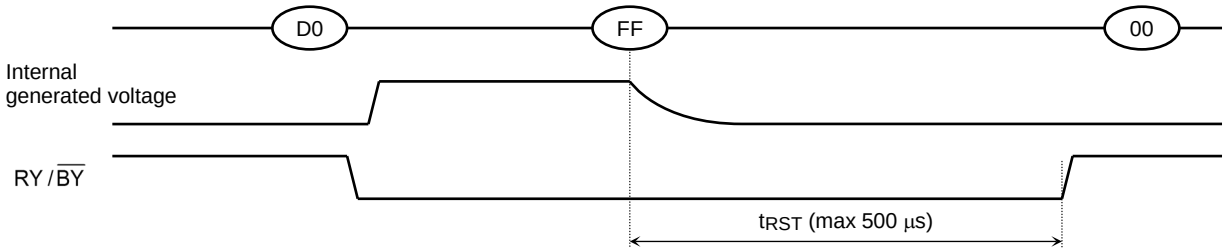
The Reset mode stops all operations. For example, in case of a Program or Erase operation, the internally generated voltage is discharged to 0 volt and the device enters the Wait state.

The response to a “FFh” Reset command input during the various device operations is as follows:

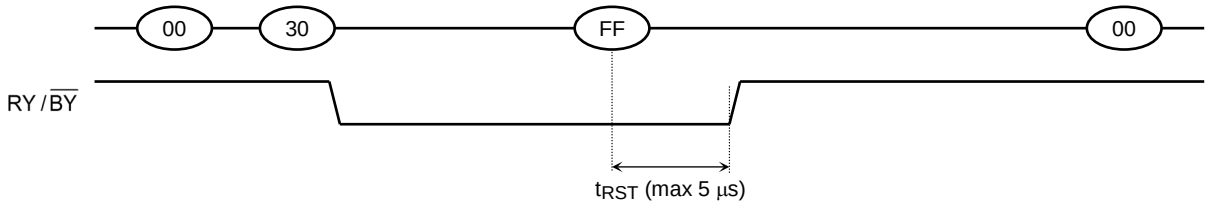
When a Reset (FFh) command is input during Program operation



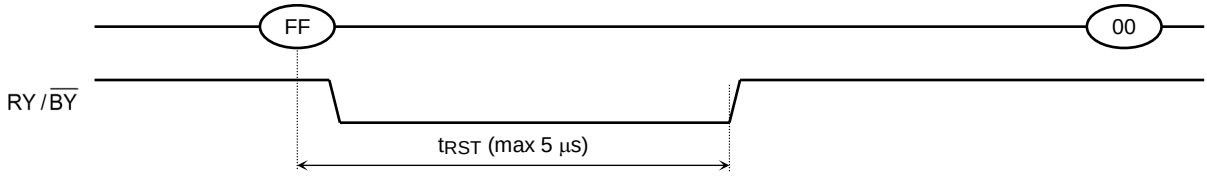
When a Reset (FFh) command is input during Erase operation



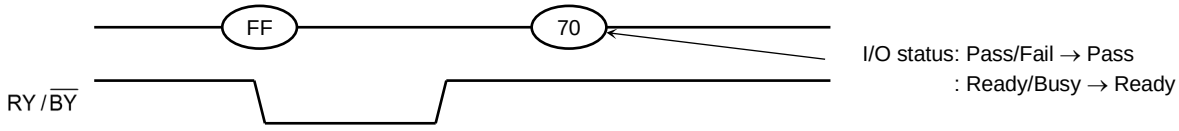
When a Reset (FFh) command is input during Read operation



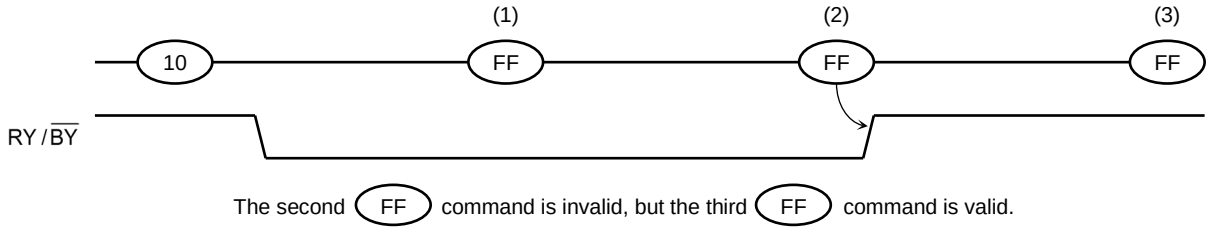
When a Reset (FFh) command is input during Ready



When a Status Read command (70h) is input after a Reset



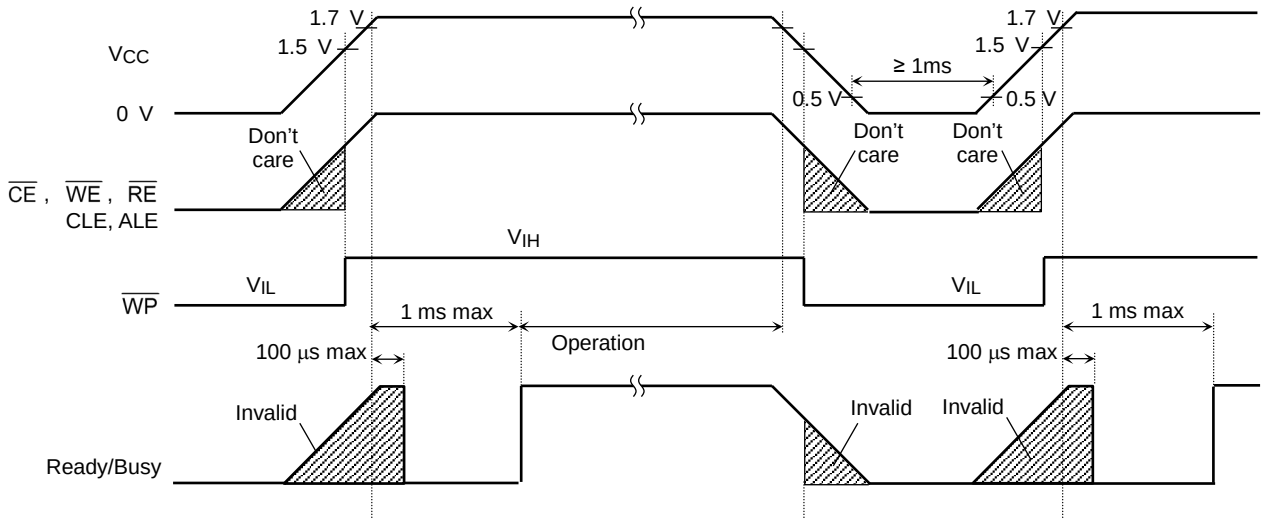
When two or more Reset commands are input in succession



APPLICATION NOTES AND COMMENTS

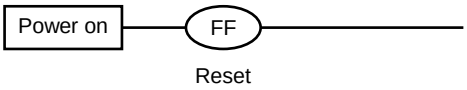
(1) Power-on/off sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.
The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.
The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.



(2) Power-on Reset

The following sequence is necessary because some input signals may not be stable at power-on.



(3) Prohibition of unspecified commands

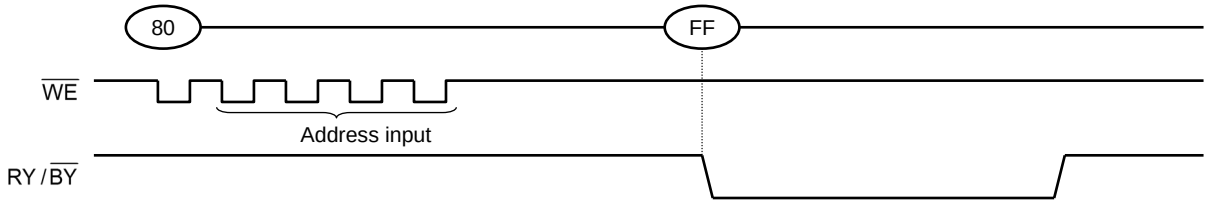
The operation commands are listed in Table 3. Input of a command other than those specified in Table 3 is prohibited. Stored data may be corrupted if an unknown command is entered during the command cycle.

(4) Restriction of commands while in the Busy state

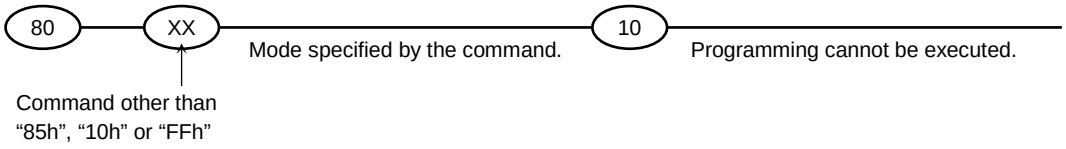
During the Busy state, do not input any command except 70h and FFh.

(5) Acceptable commands after Serial Input command “80h”

Once the Serial Input command “80h” has been input, do not input any command other than the Column Address Change in Serial Data Input command “85h”, Auto Program command “10h” or the Reset command “FFh”.

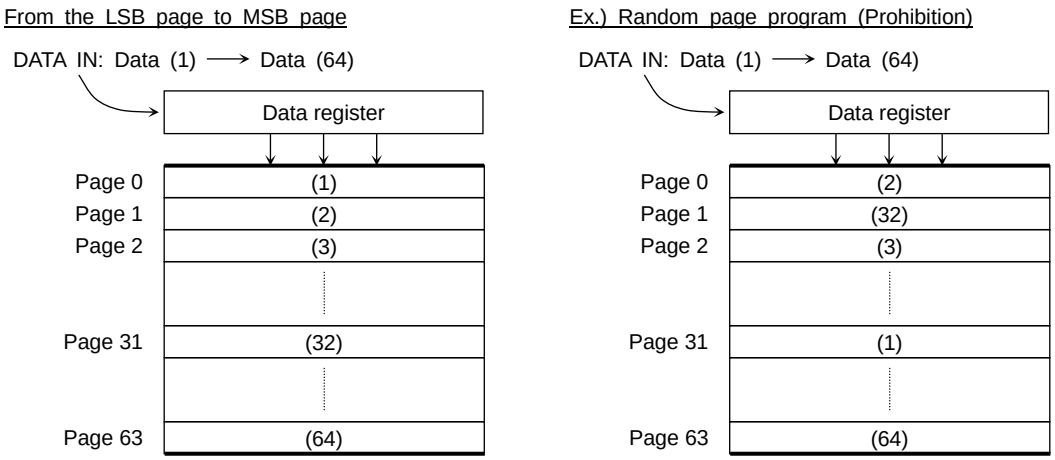


If a command other than “85h”, “10h” or “FFh” is input, the Program operation is not performed and the device operation is set to the mode which the input command specifies.

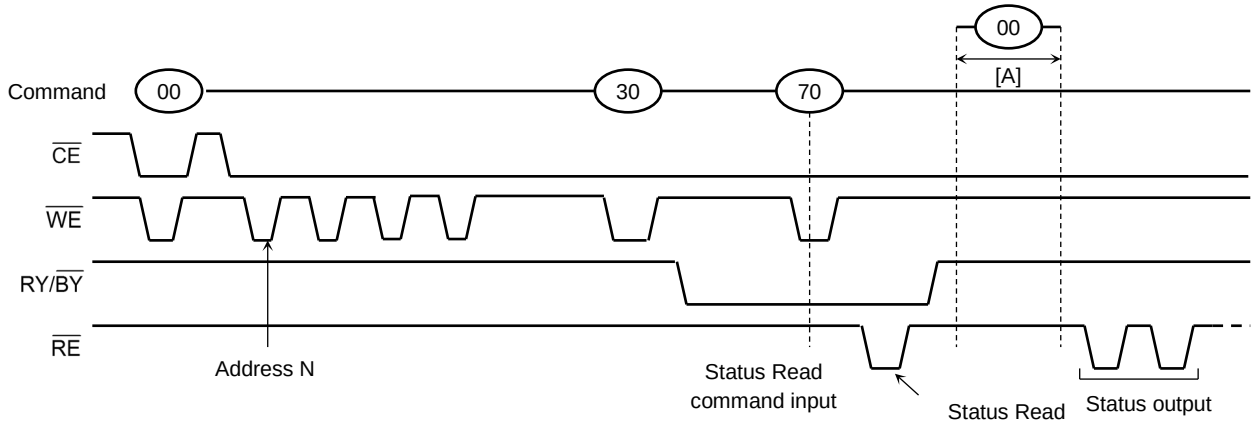


(6) Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) page of the block. Random page address programming is prohibited.

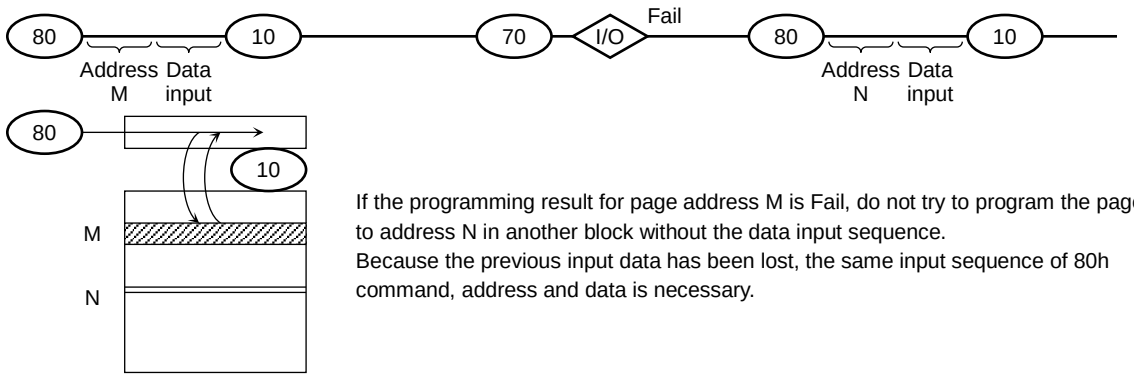


(7) Status Read during a Read operation



The device status can be read out by inputting the Status Read command “70h” in Read mode. Once the device has been set to Status Read mode by a “70h” command, the device will not return to Read mode unless the Read command “00h” is input during [A]. If the Read command “00h” is input during [A], Status Read mode is reset, and the device returns to Read mode. In this case, data output starts automatically from address N and address input is unnecessary.

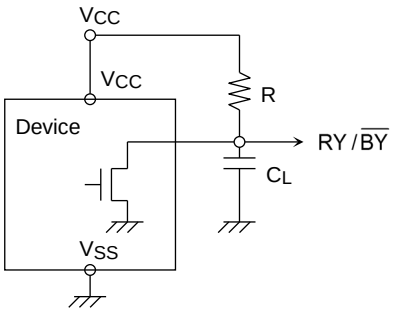
(8) Auto programming failure



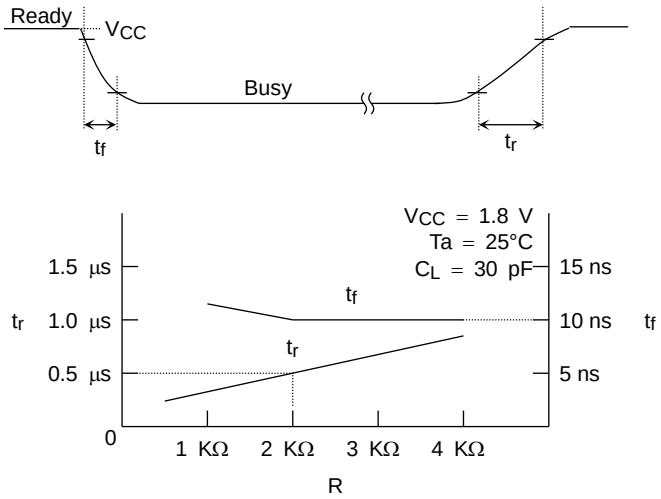
If the programming result for page address M is Fail, do not try to program the page to address N in another block without the data input sequence.
Because the previous input data has been lost, the same input sequence of 80h command, address and data is necessary.

(9) $\mathrm{RY}/\overline{\mathrm{BY}}$: termination for the Ready/Busy pin ($\mathrm{RY}/\overline{\mathrm{BY}}$)

A pull-up resistor needs to be used for termination because the $\mathrm{RY}/\overline{\mathrm{BY}}$ buffer consists of an open drain circuit.



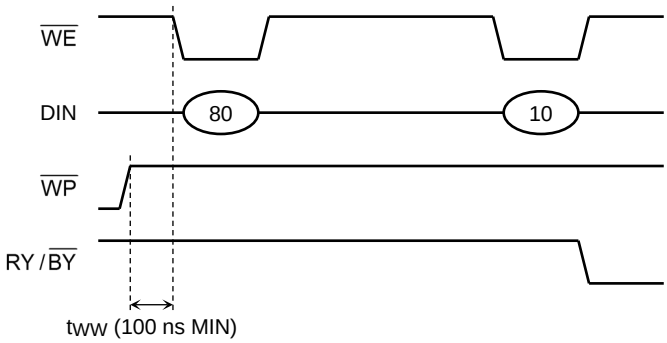
This data may vary from device to device. We recommend that you use this data as a reference when selecting a resistor value.



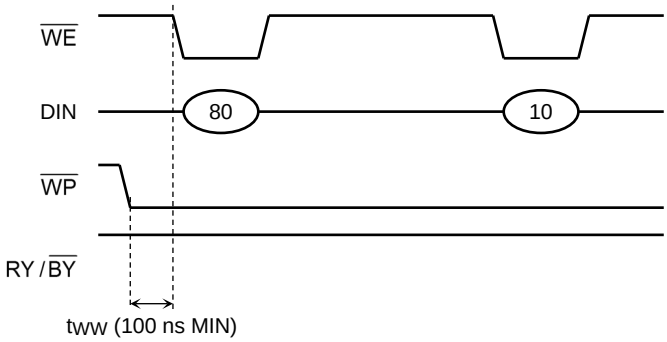
(10) Note regarding the $\overline{WP}$ signal

The Erase and Program operations are automatically reset when $\overline{WP}$ goes Low. The operations are enabled and disabled as follows:

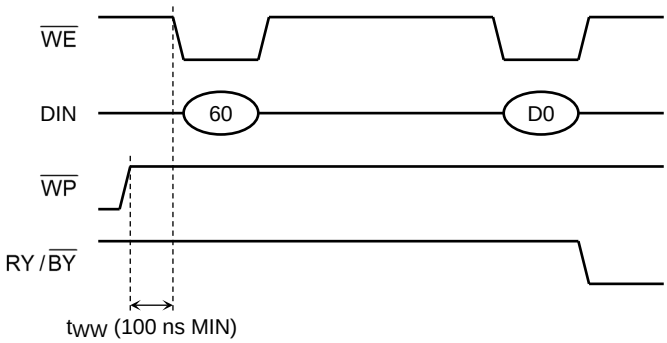
Enable Programming



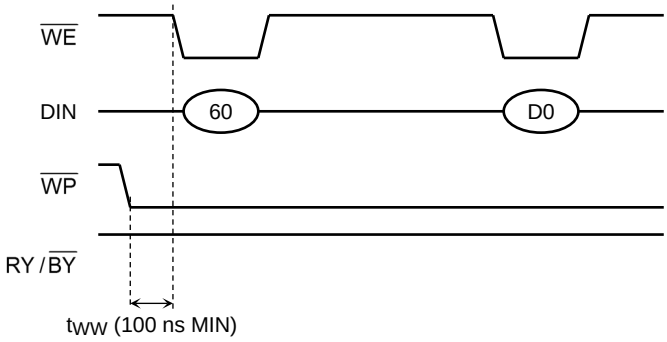
Disable Programming



Enable Erasing



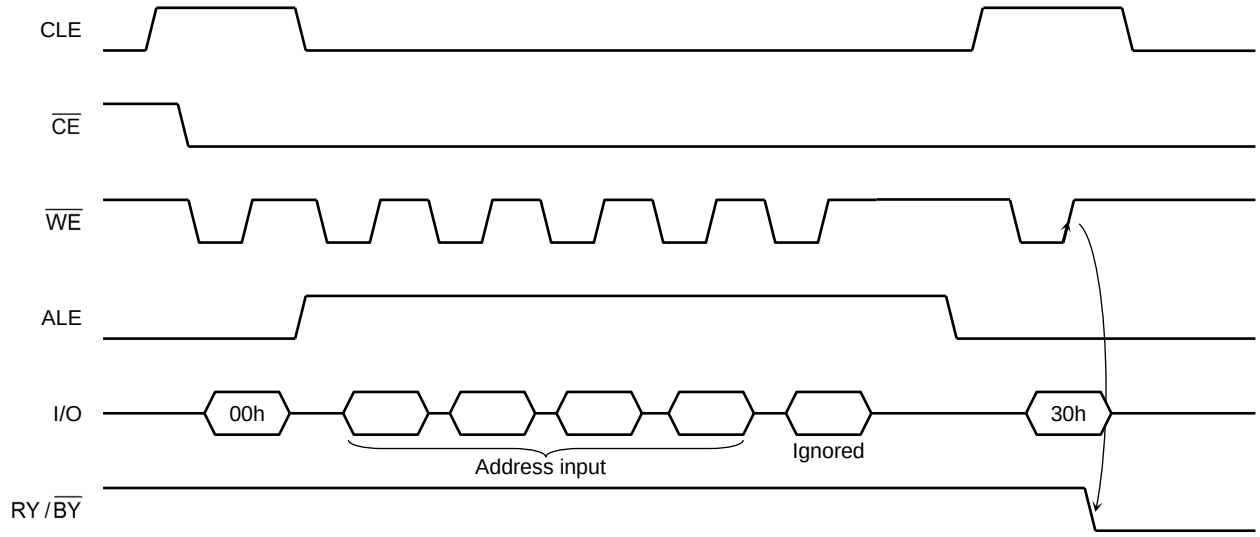
Disable Erasing



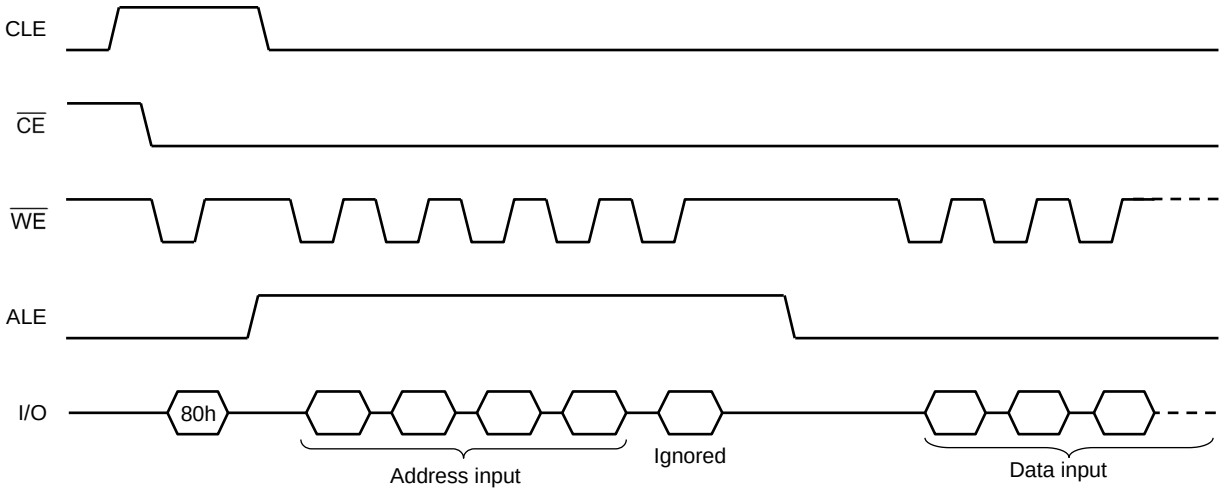
(11) When five address cycles are input

Although the device may read in a fifth address, it is ignored inside the chip.

Read operation



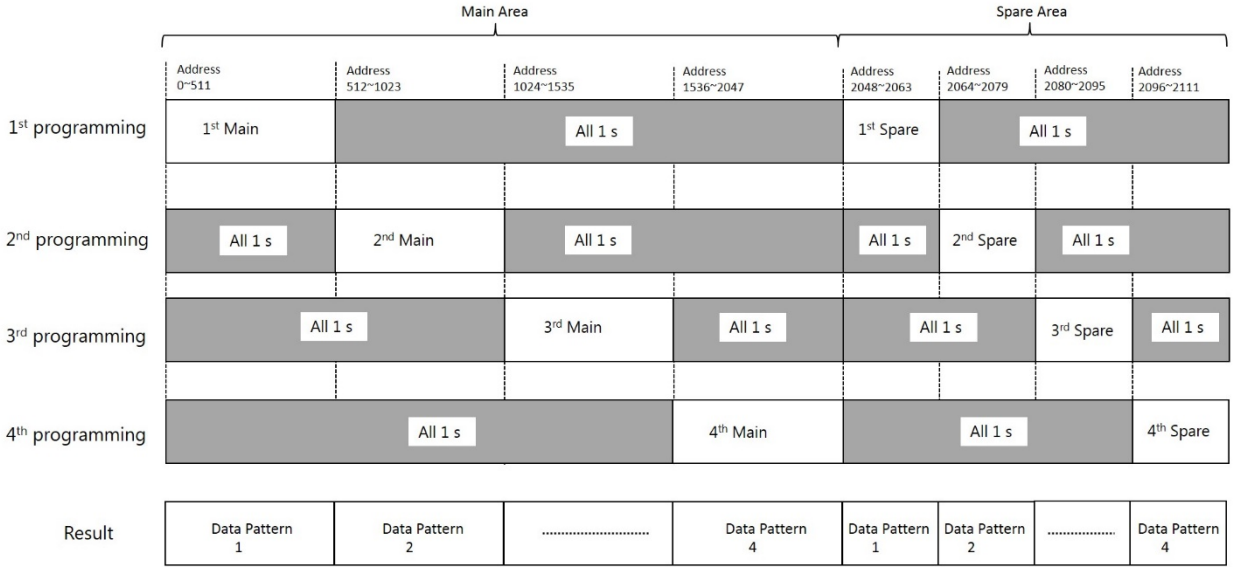
Program operation



(12) Several programming cycles on the same page (Partial Page Program)

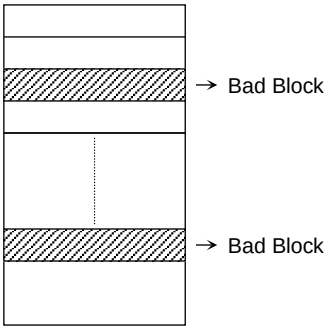
ECC Parity Code is generated during program operation on Main area (512 byte) + Spare area (16byte). While using the Partial Page Program, the user must program the data to main field and spare field simultaneously by the definition of sector in section “ECC & Sector definition for ECC”.

For example, each segment can be programmed individually as follows:



(13) Invalid blocks (bad blocks)

The device occasionally contains unusable blocks. Therefore, the following issues must be recognized:



Please do not perform an erase operation to bad blocks. It may be impossible to recover the bad block information if the information is erased.

Check if the device has any bad blocks after installation into the system. Refer to the test flow for bad block detection. Bad blocks which are detected by the test flow must be managed as unusable blocks by the system.

A bad block does not affect the performance of good blocks because it is isolated from the bit lines by select gates.

The number of valid blocks over the device lifetime is as follows:

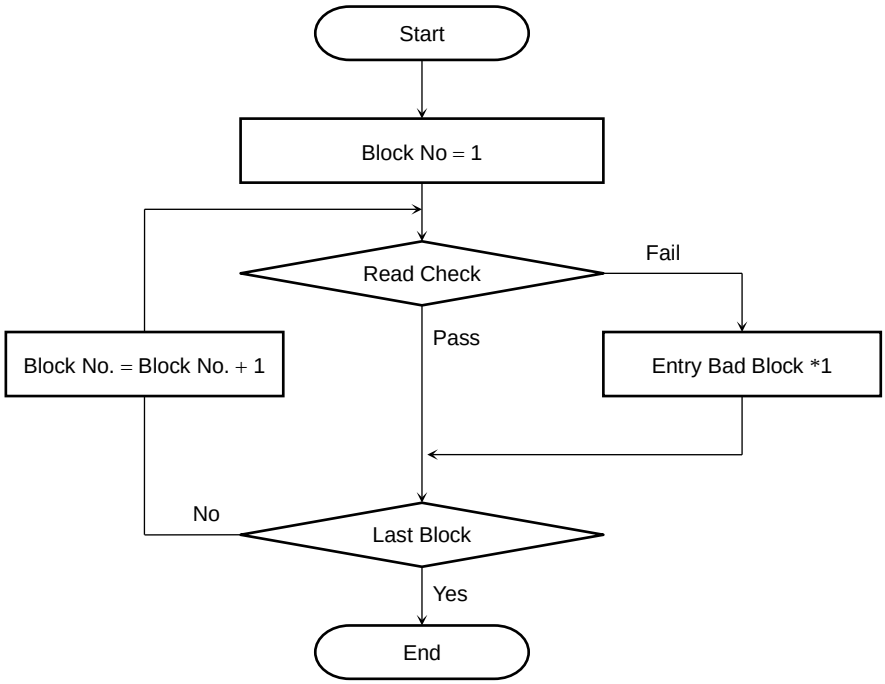
	MIN	TYP.	MAX	UNIT
Valid (Good) Block Number	1004	—	1024	Blocks

Bad Block Test Flow

Regarding invalid blocks, bad block mark is in whole pages.

Please read one column of any page in each block. If the data of the column is 00 (Hex), define the block as a bad block.

For Bad Block Test Flow, during Read Check, regardless of Status Read result (ECC Pass or Fail), use the read data value to make judgement for Bad Block.



*1: No erase operation is allowed to detected bad blocks.

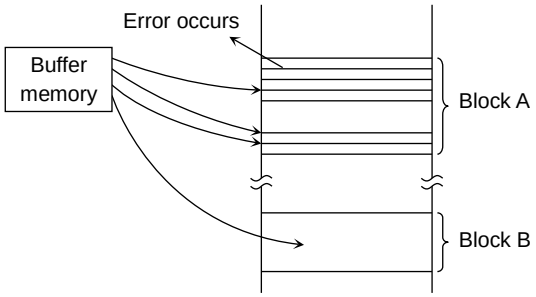
(14) Failure phenomena for Program, Erase and Read operations

The device may fail during a Program, Erase or Read operation.
The following possible failure modes should be considered when implementing a highly reliable system.

FAILURE MODE		DETECTION AND COUNTERMEASURE SEQUENCE
Block	Erase Failure	Status Read after Erase → Block Replacement
Page	Programming Failure	Status Read after Program → Block Replacement
Read	9bit Failure(uncorrectable error)	Check the ECC correction status by Status Read or ECC Status Read and take appropriate measures such as rewrite in consideration of Wear Leveling before uncorrectable ECC error occurs.

- ECC: Error Correction Code. 8 bit correction per 528Bytes is executed in a device.
- Block Replacement

Program



When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using another appropriate scheme).

Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (by creating a table within the system or by using another appropriate scheme).

(15) Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

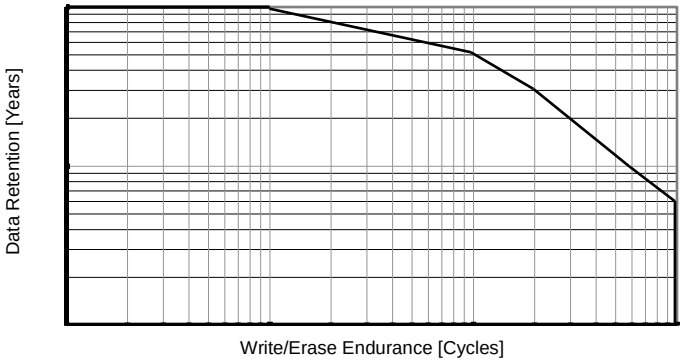
(16) Reliability Guidance

This reliability guidance is intended to notify some guidance related to using NAND Flash with 8 bit ECC for each 512 bytes. NAND Flash memory cells are gradually worn out and the reliability level of memory cells is degraded by repeating Write and Erase operation of '0' data in each block. For detailed reliability data, please refer to the reliability note for each product.
Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected.
The reliability of NAND Flash memory cells during the actual usage on system level depends on the usage and environmental conditions. TOSHIBA MEMORY adopts the checker pattern data, 0x55 & 0xAA for alternative Write/Erase cycles, for the reliability test.

- **Write/Erase Endurance**
  Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a Status Read after either an Auto Program or Auto Block Erase operation. The cumulative bad block count will increase along with the number of Write/Erase cycles.

- **Data Retention**
  The data in NAND Flash memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Data Retention time is generally influenced by the number of Write/Erase cycles and temperature.

  Here is the combined characteristics image of Write/Erase Endurance and Data Retention.



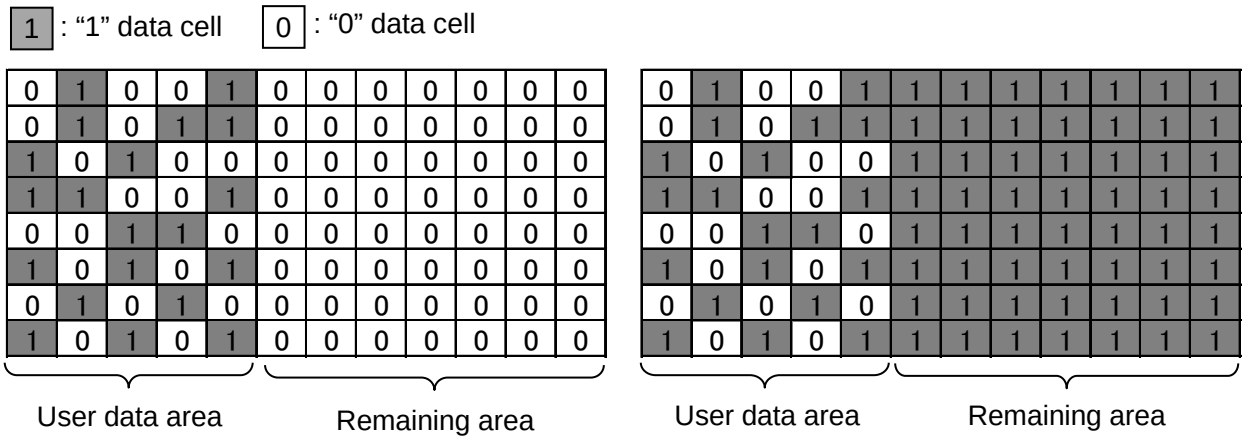
- **Read Disturb**
  A Read operation may disturb the data in NAND Flash memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again. Read Disturb capability is generally influenced by the number of Write/Erase cycles.

(17) NAND Management

NAND Management such as Bad Block Management, ECC treatment and Wear Leveling, but not limited to these treatments, should be recognized and incorporated in the system design.
ECC treatment for read data is mandatory against random bit errors, and host should monitor ECC status to take appropriate measures such as rewrite in consideration of Wear Leveling before uncorrectable Error occurs. To realize robust system design, generally it is necessary to prevent the concentration of Write/Erase cycles at the specific blocks by adopting Wear Leveling which manages to distribute Write/Erase cycles evenly among NAND Flash memory. And also it is necessary to avoid dummy '0' data write, e.g. '0' data padding, which accelerate block endurance degradation.

Continuous Write and Erase cycling with high percentage of '0' bits in data pattern can lead to faster block endurance degradation.

Example: NAND cell array with '0' data padding



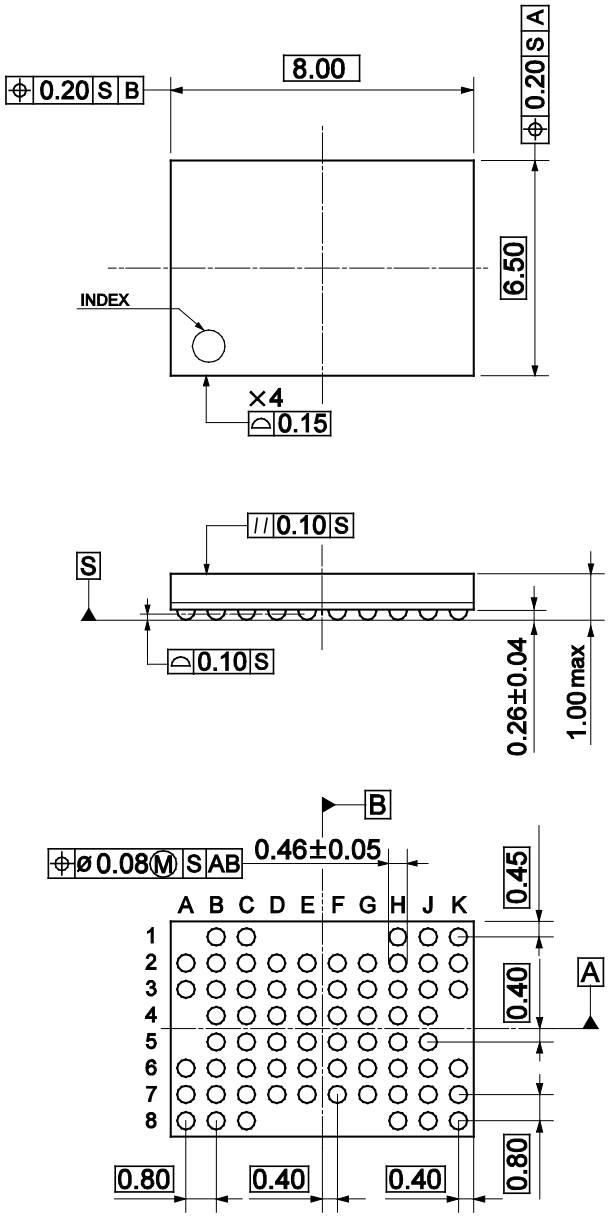
(a) Accelerate block endurance degradation by fixed dummy "0" data write

(b) "1" data for Remaining area (Recommended)

Package Dimensions

P-VFBGA67-0608-0.80-001

Unit: mm



Weight: 0.095g (typ.)

Revision History

Date	Rev.	Description
2012-02-17	0.10	Preliminary version
2012-03-21	0.11	Miss-pin assignments (TOP VIEW) are corrected.
2012-07-06	0.2	Revised ID Table. Corrected typo.
2012-08-31	1.00	Deleted TENTATIVE/TBD notation.
2018-06-01	1.10	Corrected typo, and described some notes. Attached Reliability Guidance and NAND Management. Changed “RESTRICTIONS ON PRODUCT USE”.

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