

N-Channel 30-V (D-S) MOSFET

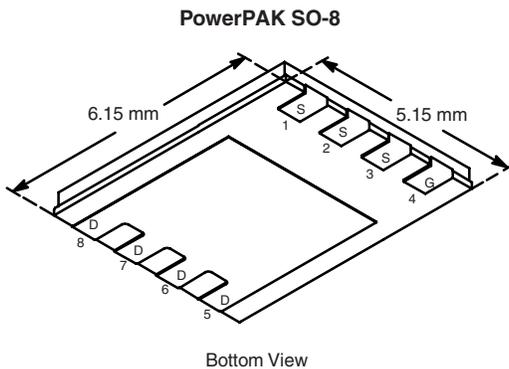
PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
30	0.0036 at V _{GS} = 10 V	25	58
	0.0045 at V _{GS} = 4.5 V	23	

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET
- Optimized for “Low Side” Synchronous Rectifier Operation
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R_g Tested



RoHS
COMPLIANT
HALOGEN
FREE
Available

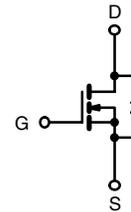


Bottom View

Ordering Information: Si7894ADP-T1-E3 (Lead (Pb)-free)
Si7894ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- DC/DC Converters
- Synchronous Rectifiers



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	30		V	
Gate-Source Voltage	V _{GS}	± 12			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	25	17	A
		T _A = 70 °C	19	13	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	60			
Continuous Source Current (Diode Conduction) ^a	I _S	4.5	1.6		
Avalanche Current	L = 0.1 mH	I _{AS}		45	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	5.4	1.9	W
		T _A = 70 °C	3.4	1.2	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 s	18	23	°C/W
		Steady State	50	65	
Maximum Junction-to-Case (Drain)	R _{thJC}	1.0	1.5		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



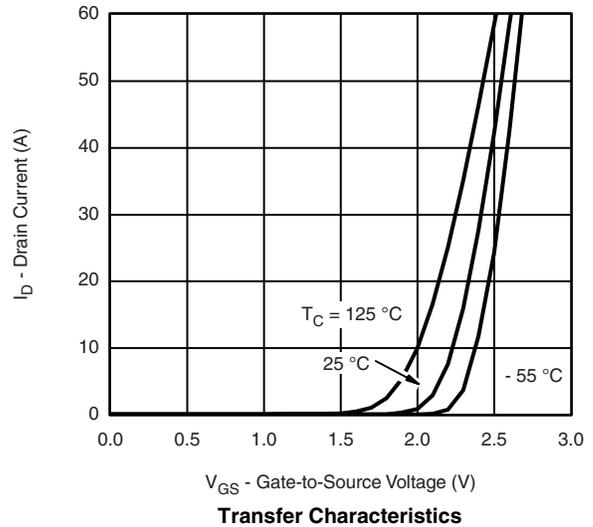
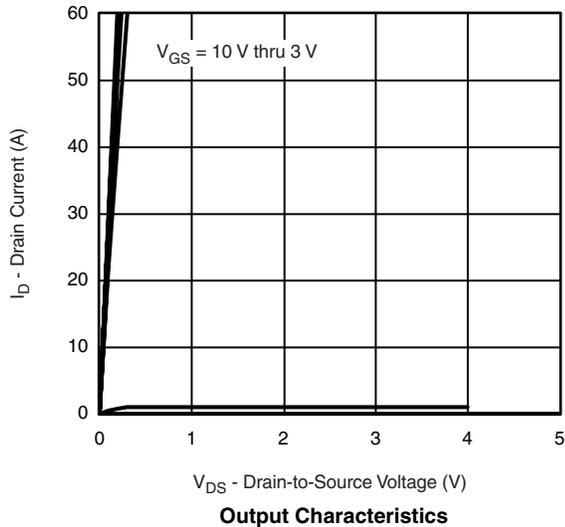
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		1.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		0.0028	0.0036	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 23\text{ A}$		0.0035	0.0045	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 25\text{ A}$		110		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9\text{ A}, V_{GS} = 0\text{ V}$		0.70	1.1	V
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		7330		pF
Output Capacitance	C_{oss}			910		
Reverse Transfer Capacitance	C_{riss}			490		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$		58	85	nC
Gate-Source Charge	Q_{gs}			11.5		
Gate-Drain Charge	Q_{gd}			11.5		
Gate Resistance	R_g		0.5	1.0	1.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$		22	35	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			190	290	
Fall Time	t_f			45	65	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		50	80	

Notes:

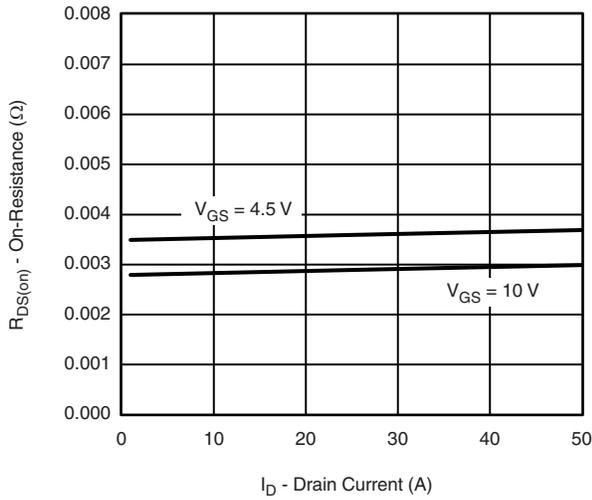
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

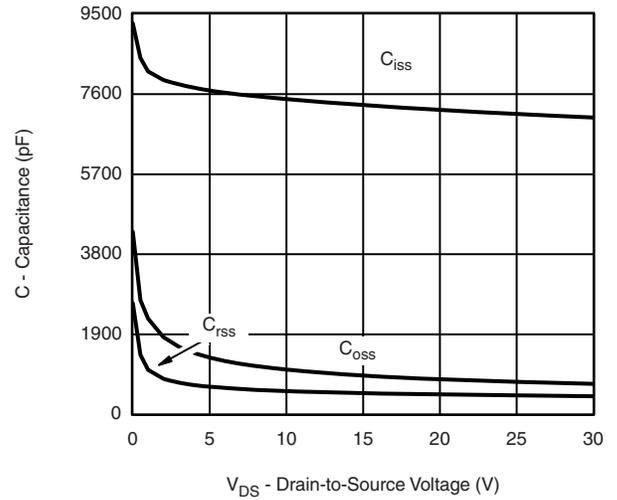
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted



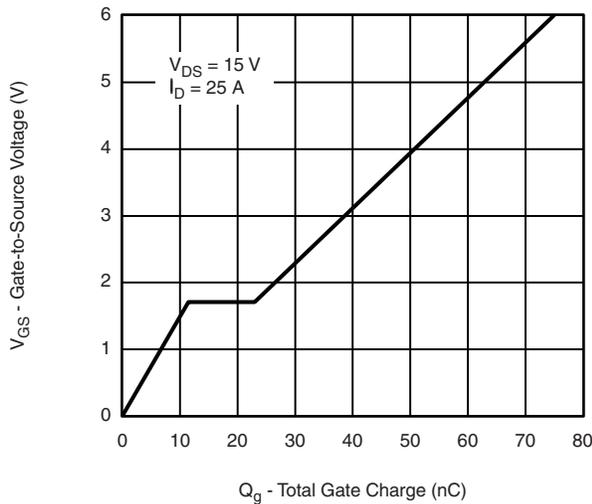
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



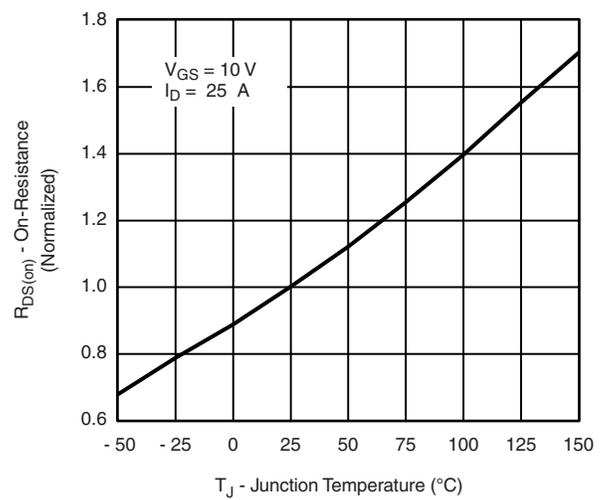
On-Resistance vs. Drain Current



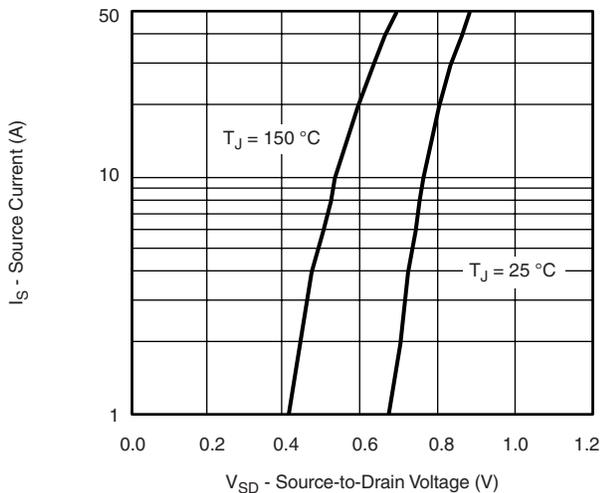
Capacitance



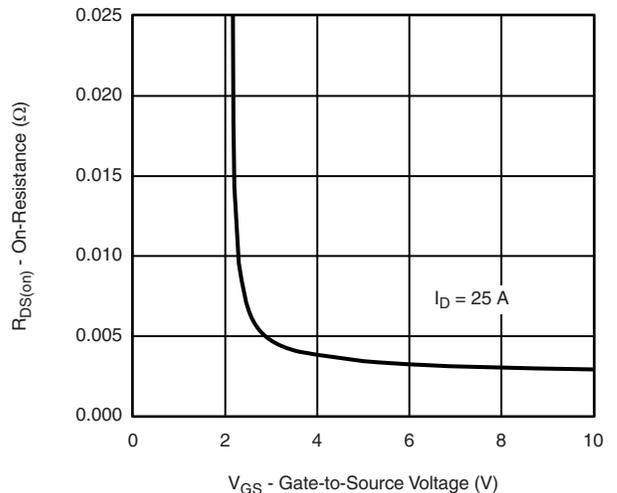
Gate Charge



On-Resistance vs. Junction Temperature

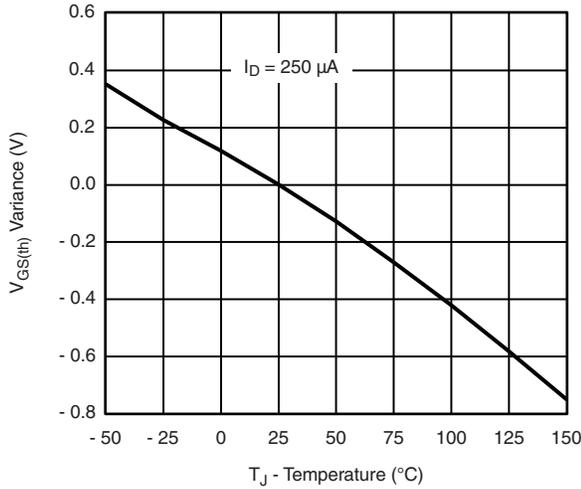


Source-Drain Diode Forward Voltage

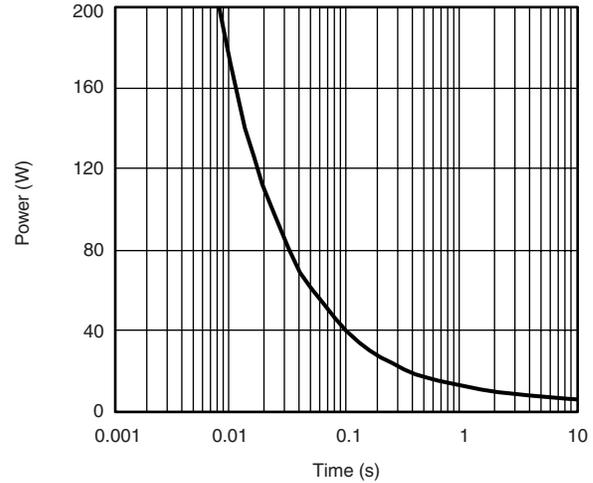


On-Resistance vs. Gate-to-Source Voltage

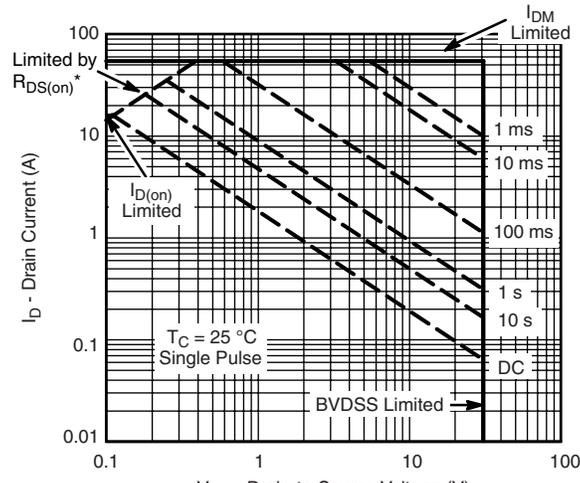
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



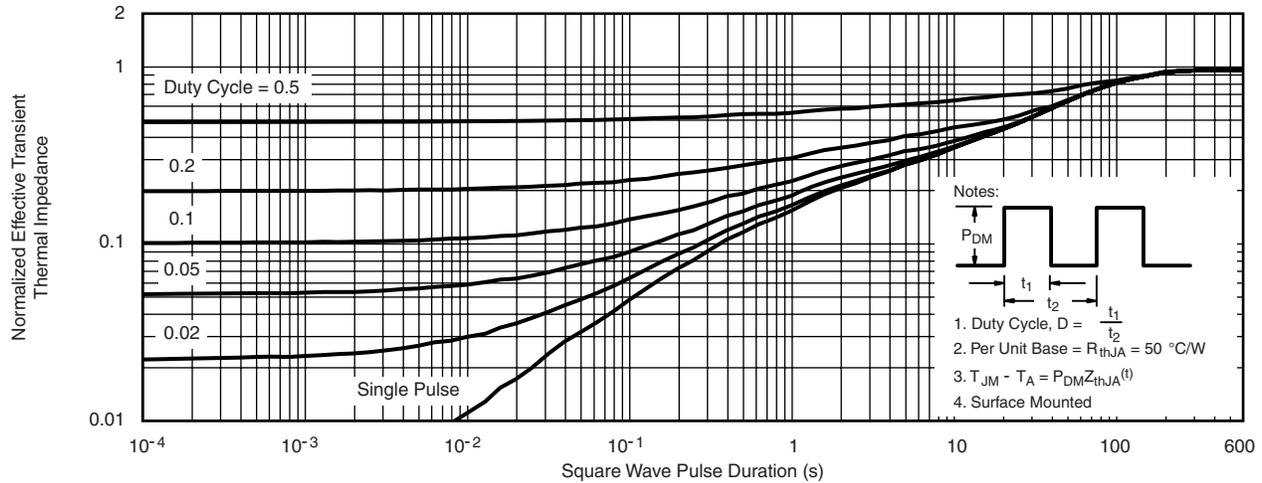
Threshold Voltage



Single Pulse Power

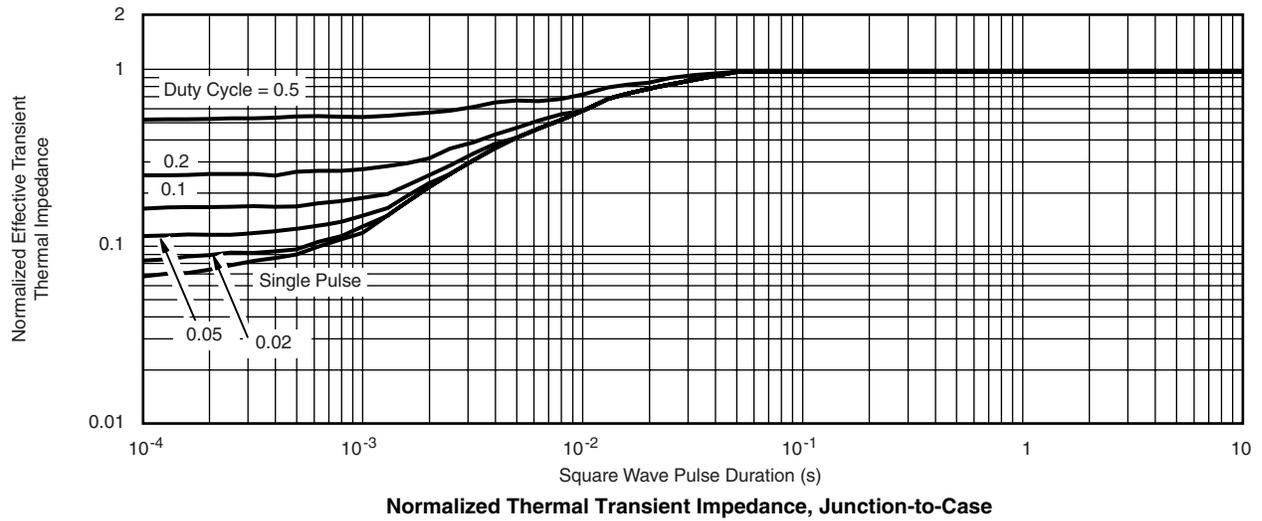


Safe Operating Area
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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