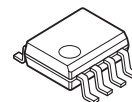


Precision Operational Amplifier

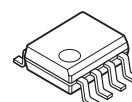
■ FEATURES

- Precision $V_{IO}=60\mu\text{V max.}$
 $V_{IO}=100\mu\text{V max. (Ta= -40}^{\circ}\text{C to +85}^{\circ}\text{C)}$
 $\Delta V_{IO}/\Delta T=1.2\mu\text{V}/^{\circ}\text{C max. (Ta= -40}^{\circ}\text{C to +85}^{\circ}\text{C)}$
- Low Offset Drift 115dB min.
- CMR $V_{NI}=80\text{nVrms typ. at f=1 to 100Hz}$
- Low Noise $en=8\text{nV}/\sqrt{\text{Hz typ. at f=100Hz}}$
- Open Loop Gain $A_v=126\text{dB min.}$
- Operating Temperature $T_{opr}=-40^{\circ}\text{C to +105}^{\circ}\text{C}$
- Guaranteed Temperature $T_{opr}=-40^{\circ}\text{C to +85}^{\circ}\text{C}$
- Unity Gain Stable
- Operating Voltage $V_{opr}=\pm 3\text{V to } \pm 18\text{V}$
- Unity Gain Frequency $f_t=1.1\text{MHz typ.}$
- Package NJMOP177GE(Single): SOP8 JEDEC 150mil
 NJMOP1772E(Dual): SOP8 JEDEC 150mil
- REPLACES INDUSTRY-STANDARD OPAMPS OP-07, OP-77, OP-177, OPA-177, AD707, etc.

■ PACKAGE OUTLINE



NJMOP177GE
(Single)



NJMOP1772E
(Dual)

■ GENERAL DESCRIPTION

The NJMOP177/NJMOP1772 are high precision operational amplifier features very low offset voltage and drift.

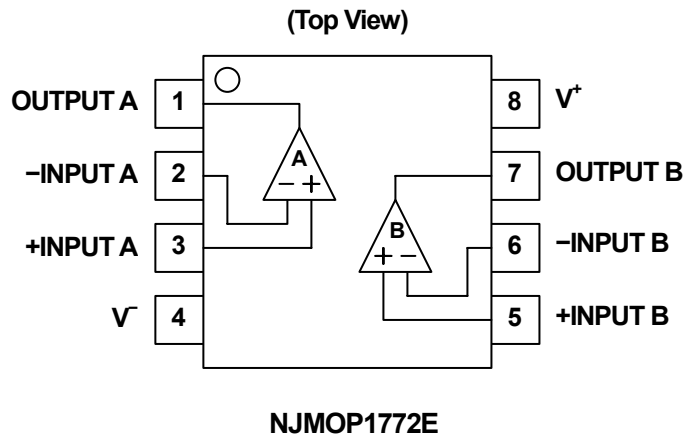
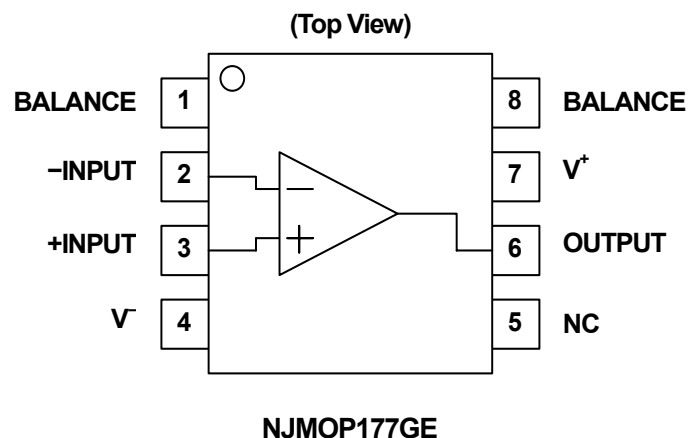
It also achieves high common mode rejection, low noise and high open loop gain. DC characteristics are 100% tested and specified from -40 to 85°C .

The NJMOP177/NJMOP1772 are suitable for high gain circuit amplified small signal and sets required stable behavior over a wide temperature range.

■ APPLICATION

- Thermocouple sensor
- Bridge Amplifier
- Current Sensor
- Instrumentation Amplifier
- Reference Voltage Circuit

■ PACKAGE DESCRIPTION



NJMOP177/NJMOP1772

■ ABSOLUTE MAXIMUM RATING(Ta=25°C Unless Otherwise Specified)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+V^-	±20	V
Common Mode Input Voltage (Note1)	V_{ICM}	±20	V
Differential Input Voltage	V_{ID}	±30	V
Power Dissipation	P_D	640(Note 2) 950(Note 3)	mW
Operating Temperature	T_{opr}	-40~+105	°C
Storage Temperature	T_{stg}	-50~+125	°C

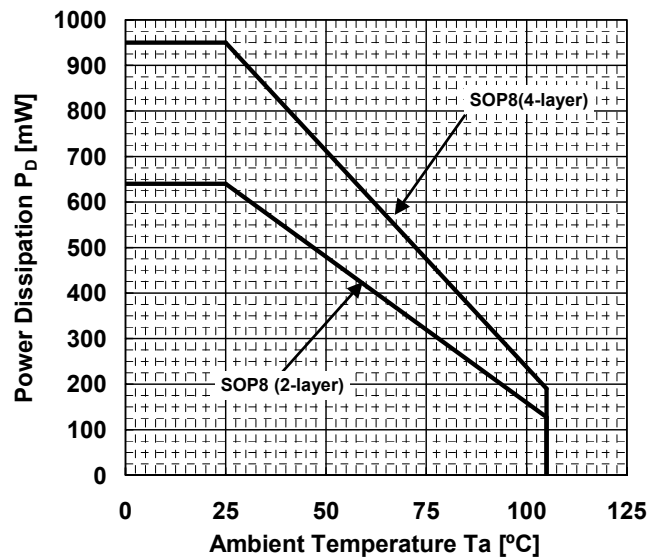
(Note1) For supply voltage less than ±20V, the maximum input voltage is equal to the supply voltage.

(Note2) Mounted on the EIA/JEDEC standard board (76.2×114.3×1.6mm, two layer, FR-4).

(Note3) Mounted on the EIA/JEDEC standard board (76.2×114.3×1.6mm, four layer, FR-4).

Refer to following Fig. A for a permissible loss when ambient temperature (Ta) is Ta≥25°C.

Fig. A Power Dissipation Derating Curve



■ RECOMMENDED OPERATING VOLTAGE

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+V^-		±3	-	±18	V

■ **ELECTRONIC CHARACTERISTICS** ($V^+ / V^- = \pm 15V$, $T_a = +25^\circ C$, $V_{CM} = 0V$ unless otherwise specified)

● **DC CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Characteristics						
Input Offset Voltage	V_{IO1}	$T_a = -40$ to $+85^\circ C$	—	20	60	μV
	V_{IO2}		—	20	100	μV
Input Offset Voltage Drift	$\Delta V_{IO} / \Delta T$	$T_a = -40 \rightarrow +25^\circ C$ / $T_a = +25^\circ C \rightarrow +85^\circ C$	—	0.3	1.2	$\mu V / ^\circ C$
Common Mode Input Voltage	V_{ICM1}	$T_a = -40$ to $+85^\circ C$	± 13	± 14	—	V
	V_{ICM2}		± 13	± 13.5	—	V
Common Mode Rejection Ratio	CMR1	$V_{CM} = 0V \rightarrow -13V$ / $V_{CM} = 0V \rightarrow +13V$	115	140	—	dB
	CMR2	$T_a = -40$ to $+85^\circ C$, $V_{CM} = 0V \rightarrow -13V$ / $V_{CM} = 0V \rightarrow +13V$	110	140	—	dB
Supply Voltage Rejection Ratio	SVR1	$V^+ / V^- = \pm 3V$ to $\pm 18V$	110	125	—	dB
	SVR2	$T_a = -40$ to $+85^\circ C$, $V^+ / V^- = \pm 3V$ to $\pm 18V$	106	120	—	dB
Input Bias Current	I_B1	$T_a = -40$ to $+85^\circ C$	-2.8	1.2	2.8	nA
	I_B2		-6	1.7	6	nA
Input Bias Current Drift	$\Delta I_B / \Delta T$	$T_a = -40 \rightarrow +85^\circ C$	—	8	60	$pA / ^\circ C$
Input Offset Current	I_{IO1}	$T_a = -40$ to $+85^\circ C$	—	0.3	2.8	nA
	I_{IO2}		—	0.3	4.5	nA
Input Offset Current Drift	$\Delta I_{IO} / \Delta T$	$T_a = -40 \rightarrow +85^\circ C$	—	1.5	72	$pA / ^\circ C$
Differential Input Impedance	R_{ID}	(Note 4)	—	90	—	$M\Omega$
Common-Mode Input Impedance	R_{IC}	(Note 4)	—	800	—	$G\Omega$
Voltage Gain	A_{v1}	$R_L = 2k\Omega$, $V_o = -10V \rightarrow 0V$ / $0V \rightarrow +10V$ / $-10V \rightarrow +10V$	126	142	—	dB
	A_{v2}	$T_a = -40$ to $+85^\circ C$, $R_L = 2k\Omega$, $V_o = -10V \rightarrow 0V$ / $0V \rightarrow +10V$ / $-10V \rightarrow +10V$	120	136	—	dB
Input Offset Voltage Trim (only NJMOP177)	V_{iotri}	$R_p = 20k\Omega$	—	± 3	—	mV
Channel Separation (only NJMOP1772)	CS	DC	—	0.01	—	$\mu V / V$
Output Characteristics						
Maximum Output Voltage	V_{OM1}	$R_L = 10k\Omega$	± 13.5	± 14.0	—	V
	V_{OM2}	$T_a = -40$ to $+85^\circ C$, $R_L = 10k\Omega$	± 13.0	± 14.0	—	V
	V_{OM3}	$R_L = 2k\Omega$	± 12.5	± 13.0	—	V
	V_{OM4}	$T_a = -40$ to $+85^\circ C$, $R_L = 2k\Omega$	± 12.0	± 13.0	—	V
	V_{OM5}	$R_L = 1k\Omega$	± 12.0	± 12.5	—	V
Output Impedance	R_O	Open-Loop	—	60	—	Ω

(Note 4) Theoretical value by design

NJMOP177/NJMOP1772

● DC CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Characteristics						
Supply Current (only NJMOP177)	I _{CC1}	A _V = +1, R _L = ∞	—	1.6	2.0	mA
	I _{CC2}	T _a = -40 to +85°C, A _V = +1, R _L = ∞	—	1.7	2.5	mA
	I _{CC3}	V ⁺ /V ⁻ = ±3V, A _V = +1, R _L = ∞	—	0.70	0.75	mA
	P _{D1}	A _V = +1, R _L = ∞	—	50	60	mW
	P _{D2}	V ⁺ /V ⁻ = ±3V, A _V = +1, R _L = ∞	—	4.2	4.5	mW
Supply Current (only NJMOP1772)	I _{CC1}	A _V = +1, R _L = ∞	—	2.6	3.2	mA
	I _{CC2}	T _a = -40 to +85°C, A _V = +1, R _L = ∞	—	2.7	3.4	mA
	I _{CC3}	V ⁺ /V ⁻ = ±3V, A _V = +1, R _L = ∞	—	1.3	1.6	mA
	P _{D1}	A _V = +1, R _L = ∞	—	78	96	mW
	P _{D2}	V ⁺ /V ⁻ = ±3V, A _V = +1, R _L = ∞	—	7.8	9.6	mW

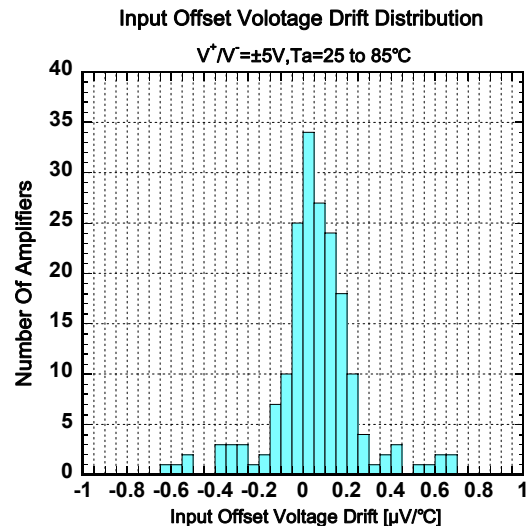
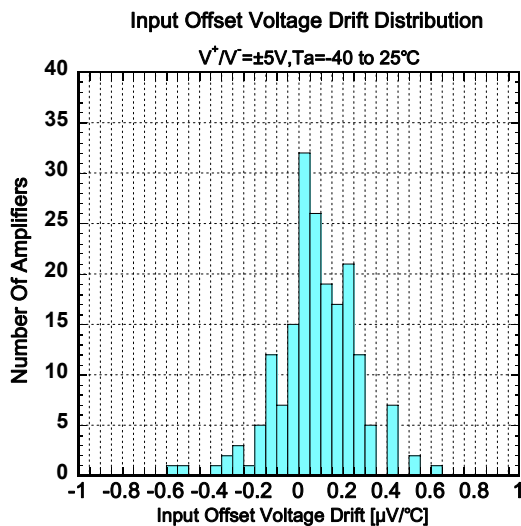
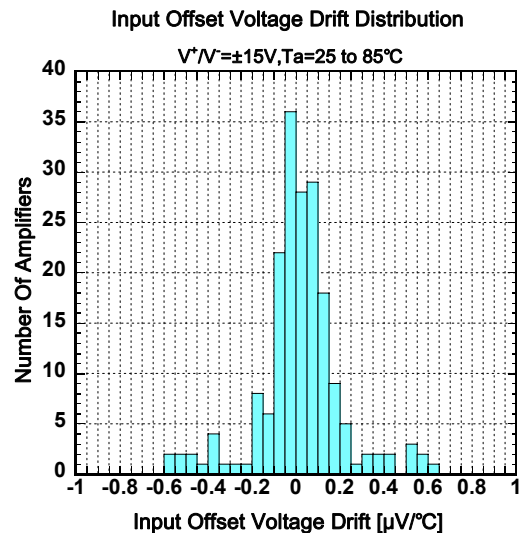
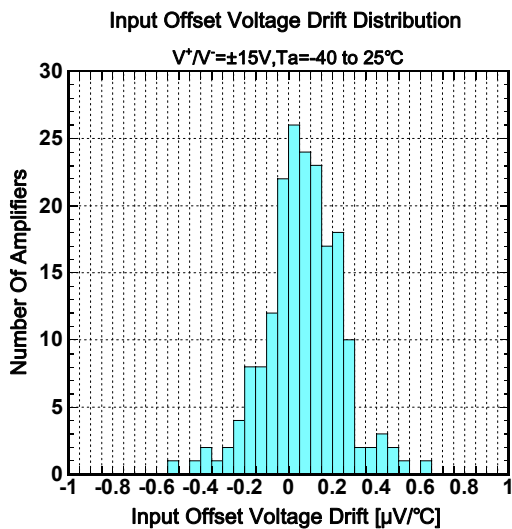
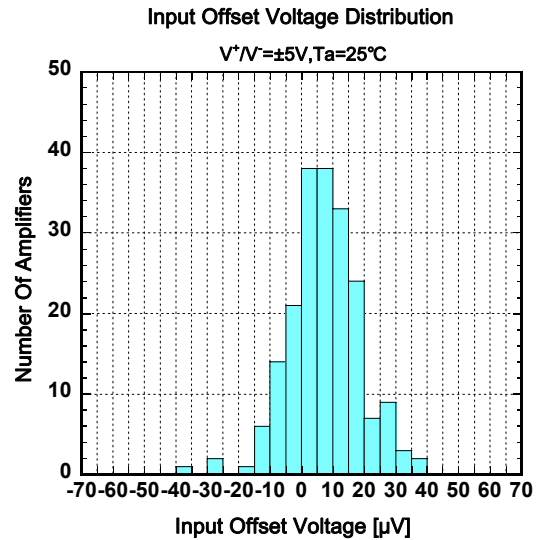
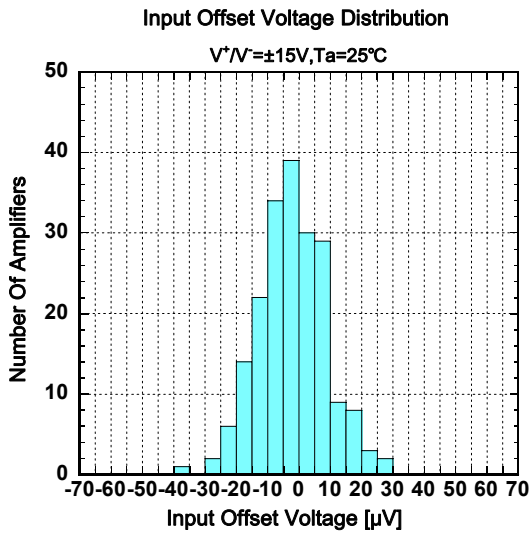
● AC CHARACTERISTICS

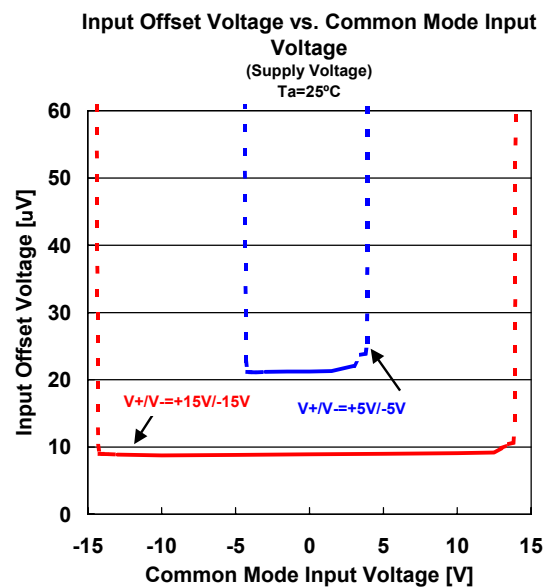
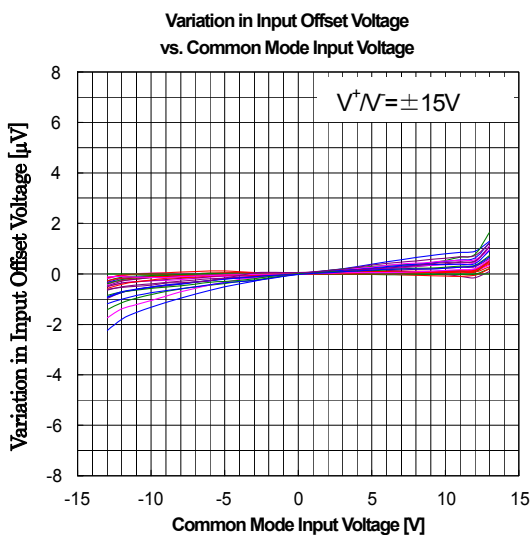
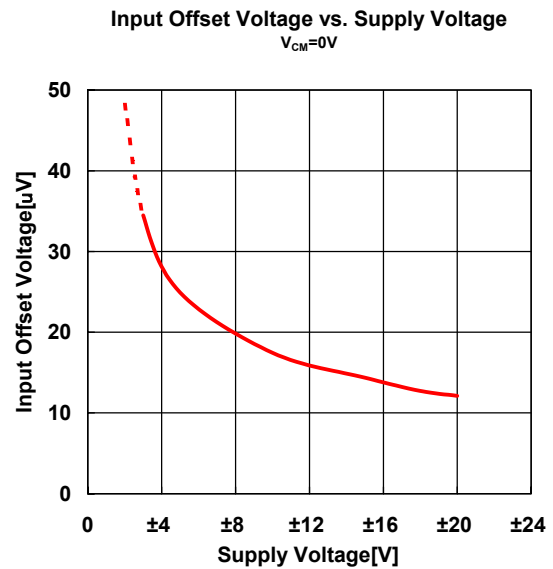
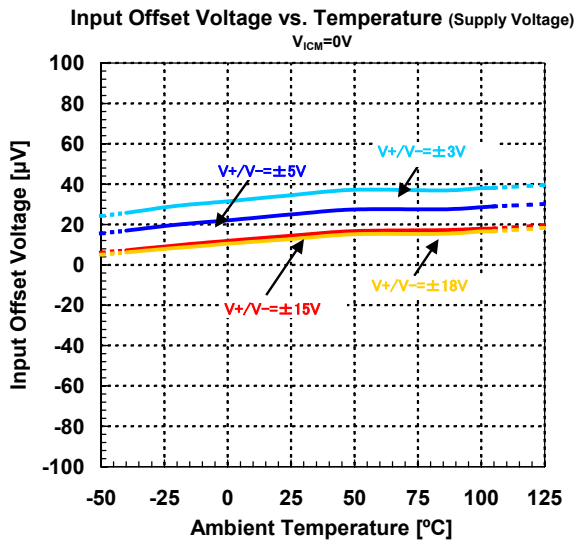
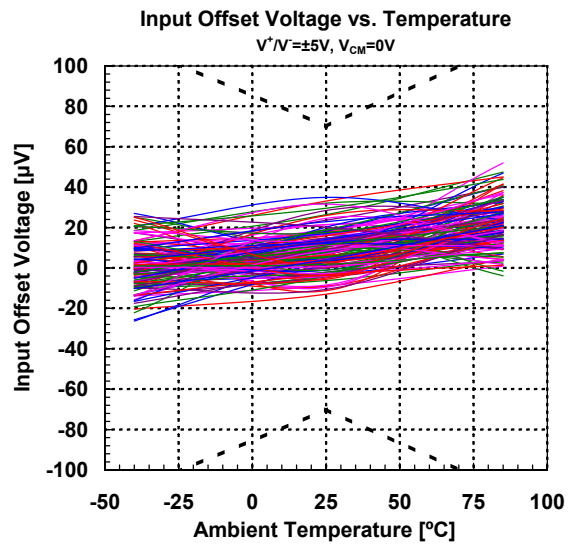
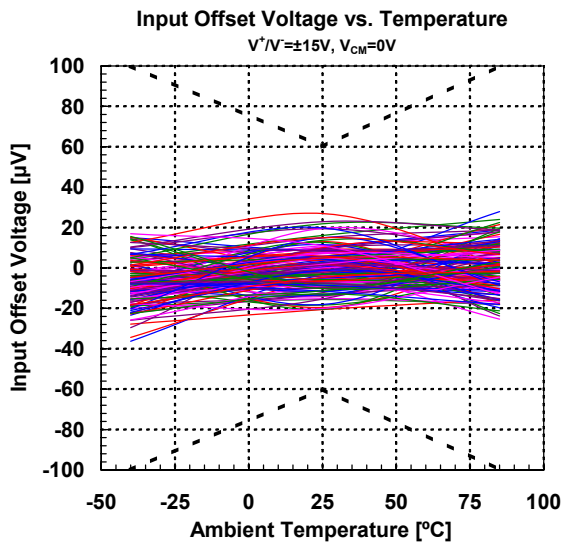
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Frequency Characteristics						
Unity Gain Frequency	f _T	A _V = +100, R _L = 2kΩ, C _L = 10pF	—	1.1	—	MHz
Slew Rate	+SR	RISE, A _V = +1, V _{IN} = 1Vpp, R _L = 2kΩ, C _L = 10pF	0.1	0.3	—	V/μs
	-SR	FALL, A _V = +1, V _{IN} = 1Vpp, R _L = 2kΩ, C _L = 10pF	0.1	0.3	—	V/μs
Noise Characteristics						
Equivalent Input Noise Voltage	V _{NI}	f _o = 1Hz to 100Hz	—	80	—	nVrms
Equivalent Input Noise Current	I _{NI}	f _o = 1Hz to 100Hz	—	3	—	pArms

●EXPLANATION OF MEASUREMENT CONDITION

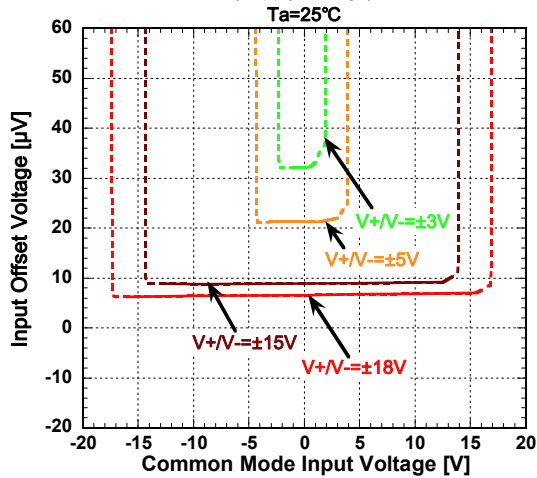
PARAMETER	Explanation
Input Offset Voltage Drift	$\text{Input Offset Voltage Drift} = \Delta V_{IO} / \Delta T$ ΔT : Amount of Temperature Change. ΔV_{IO} : Amount of Input Offset Voltage.
Common Mode Input Voltage range	A range of input voltage at which the operational amplifier can function.
Common Mode Rejection Ratio	$\text{CMR} = 20\log (\Delta V_{CM} / \Delta V_{IO}) $ ΔV_{CM} : Amount of Input Voltage. ΔV_{IO} : Amount of Input Offset Voltage.
Supply Voltage Rejection Ratio	$\text{SVR} = 20\log (\Delta V_S / \Delta V_{IO}) $ ΔV_S : Amount of Supply Voltage. ΔV_{IO} : Amount of Input Offset Voltage.
Common Mode Input Impedance	$R_{IC} = \Delta V_{CM} / \Delta I_B$ ΔV_{CM} : Amount of Input Voltage. ΔI_B : Amount of Input Bias Current.
Voltage Gain	$\text{AV} = 20\log (\Delta V_O / \Delta V_{IO}) $ ΔV_O : Amount of Output Voltage. ΔV_{IO} : Amount of Input Offset Voltage.

■ TYPICAL CHARACTERISTICS

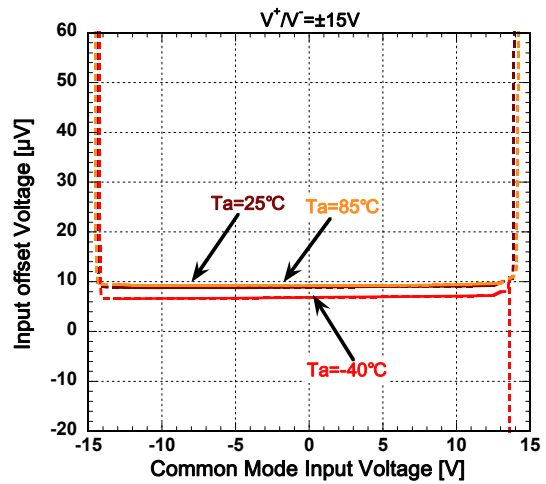




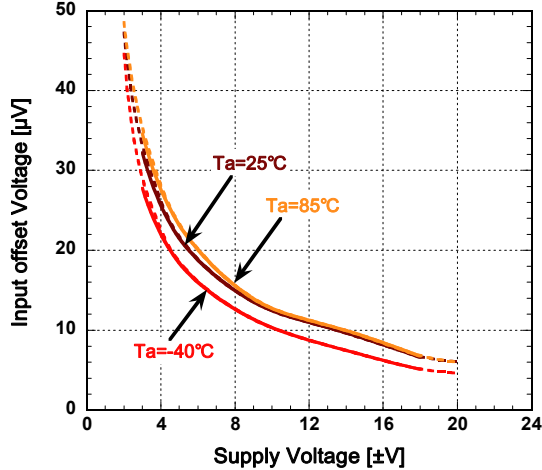
Input Offset Voltage vs. Common Mode Input Voltage
(Supply Voltage)



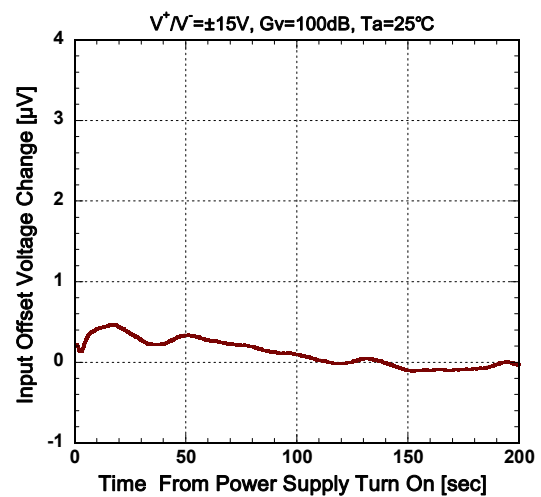
Input Offset Voltage vs. Common Mode Input Voltage
(Temperature)



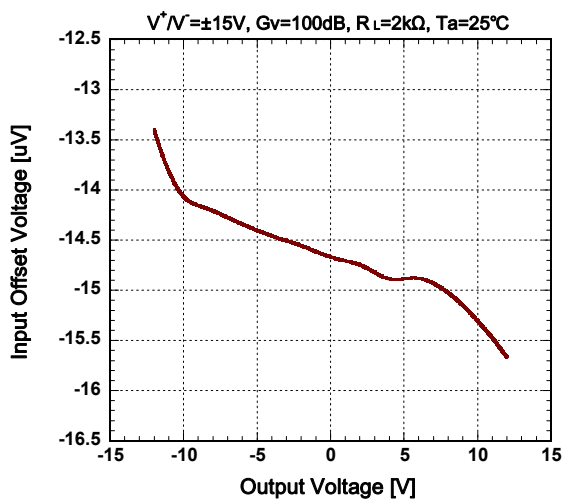
Input Offset Voltage vs. Supply Voltage
(Temperature)



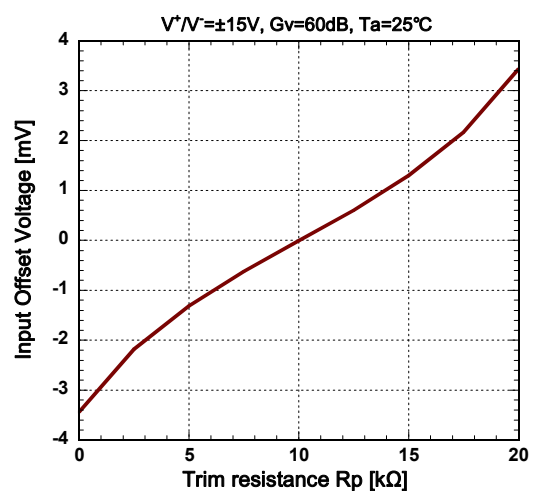
Warm Up Input Offset Voltage Drift

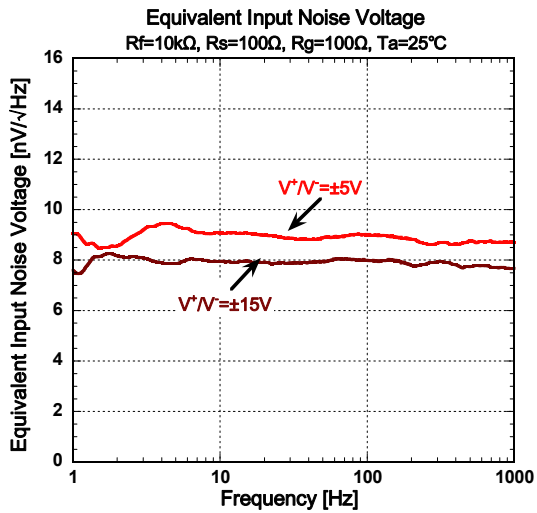
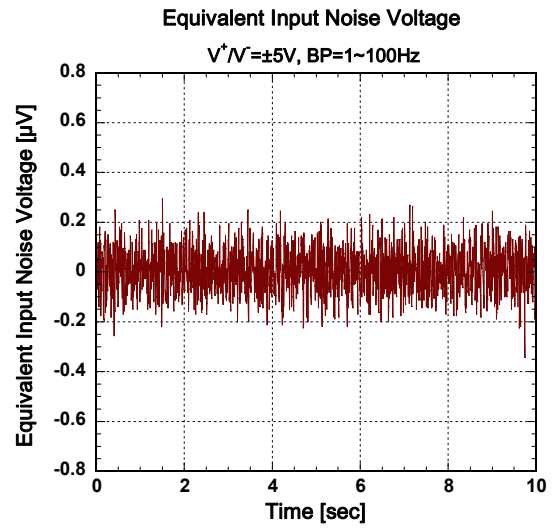
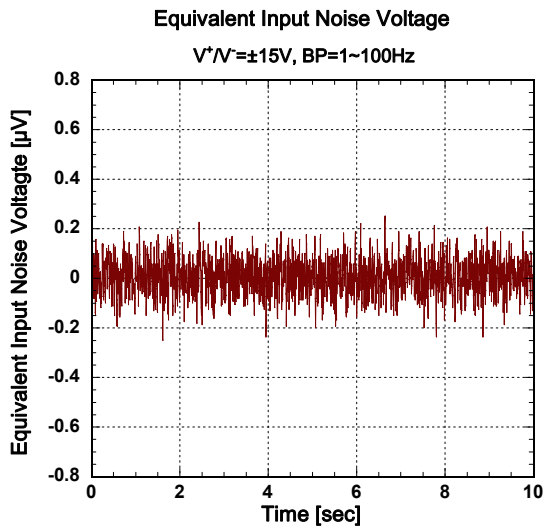


Input Offset Voltage vs. Output Voltage

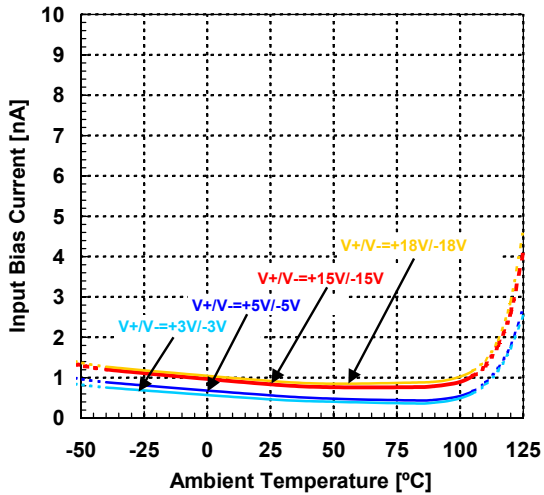


Input Offset Voltage vs. Trim Resistance

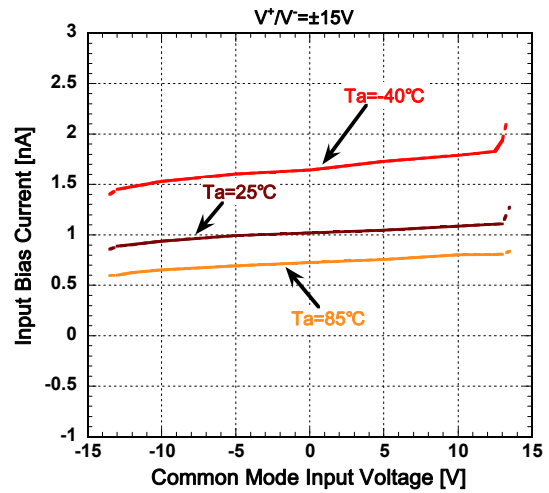




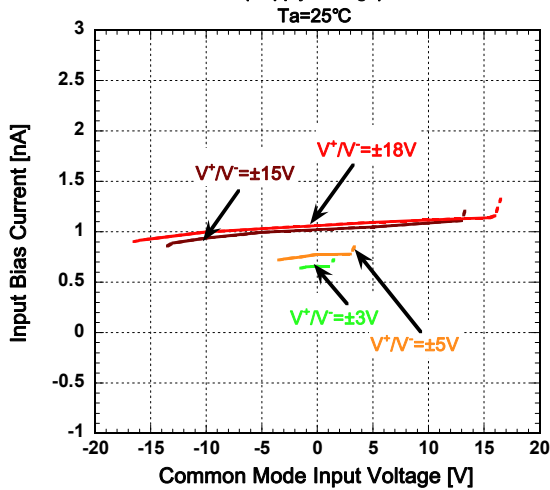
Input Bias Current vs. Temperature



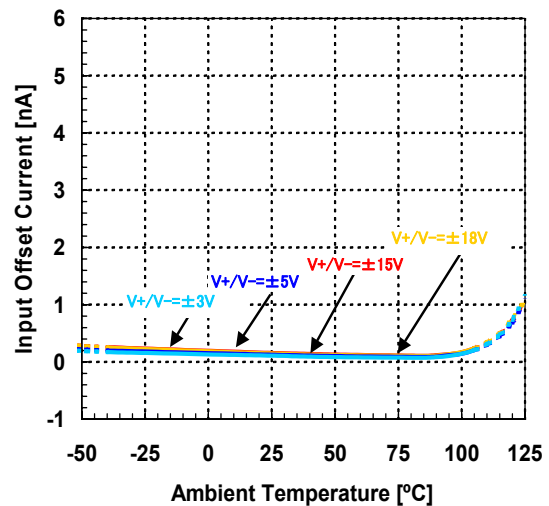
Input Bias Current vs. Common Mode Input Voltage (Temperature)



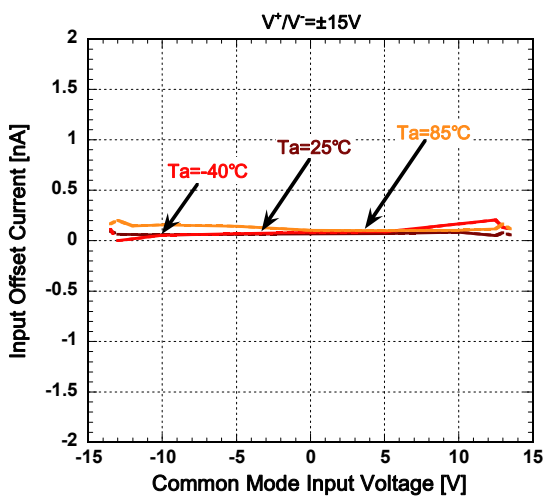
Input Bias Current vs. Common Mode Input Voltage (Supply Voltage)



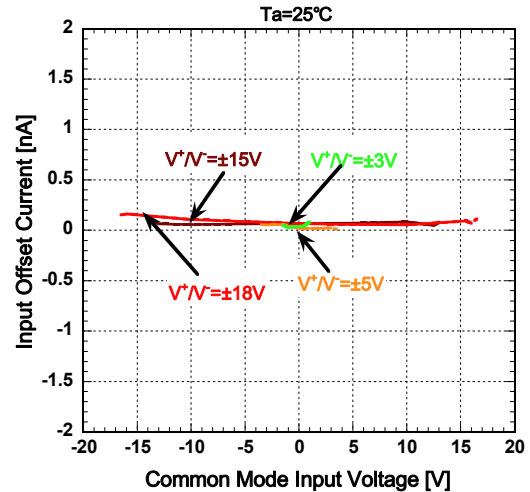
Input Offset Current vs. Temperature



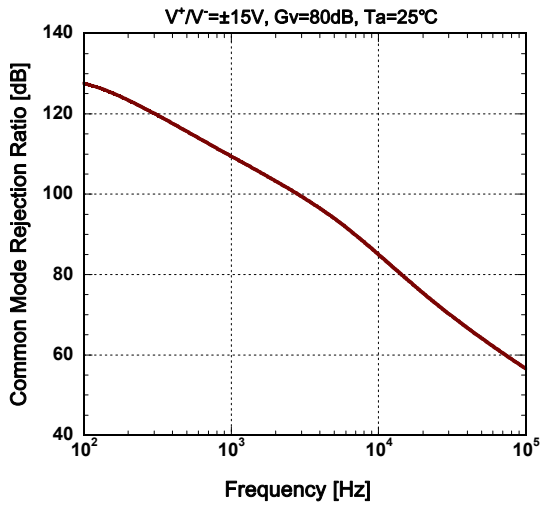
Input Offset Current vs. Common Mode Input Voltage (Temperature)



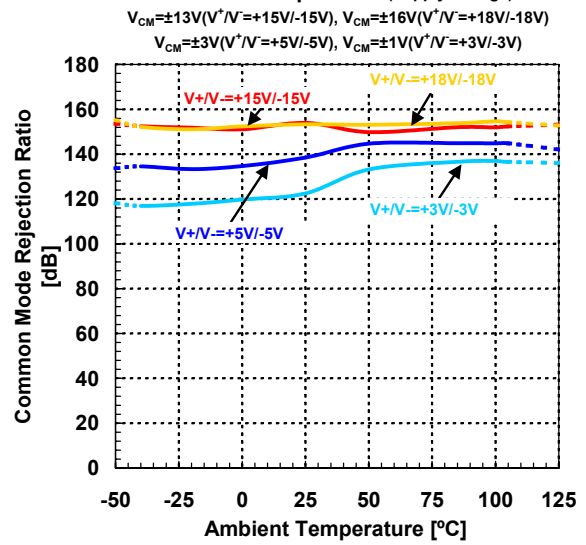
Input Offset Current vs. Common Mode Input Voltage (Supply Voltage)



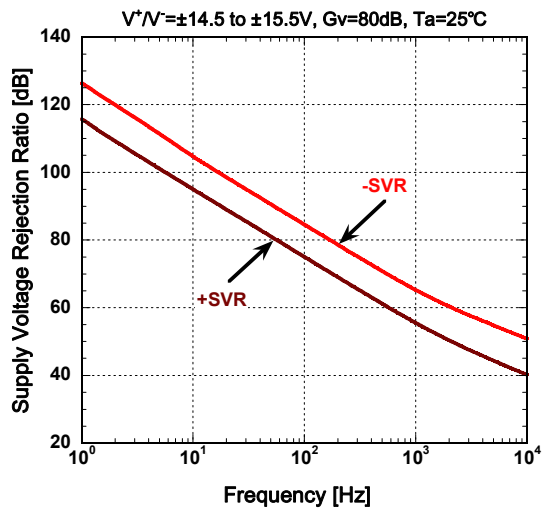
Common Mode Rejection Ratio vs. Frequency



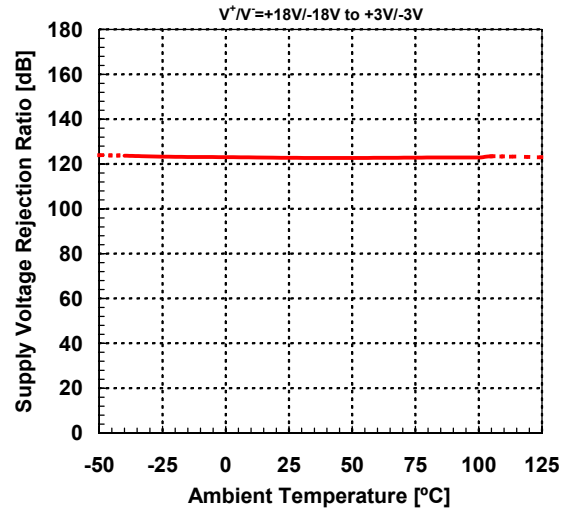
CMR vs. Temperature (Supply Voltage)

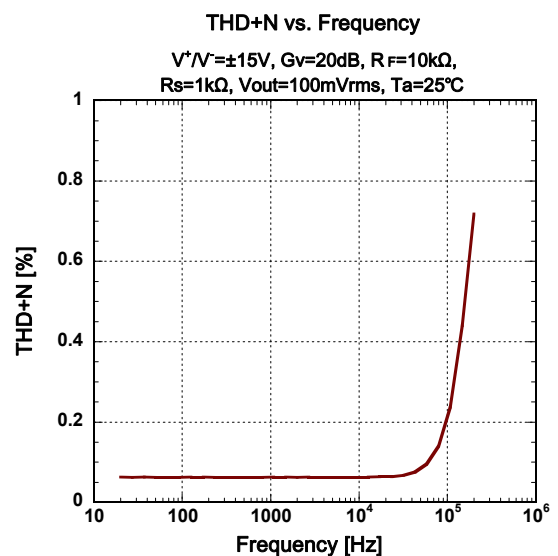
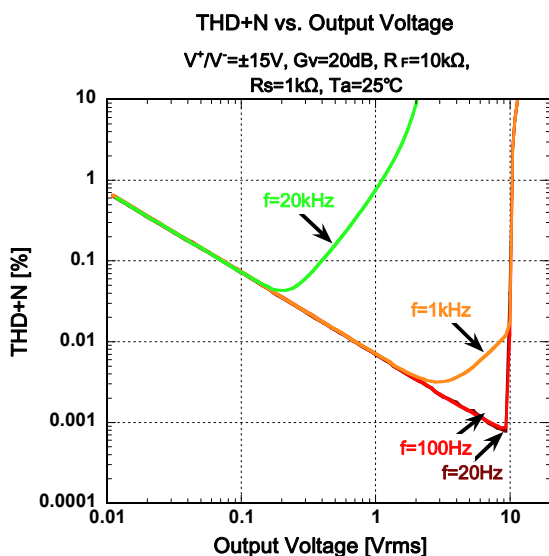
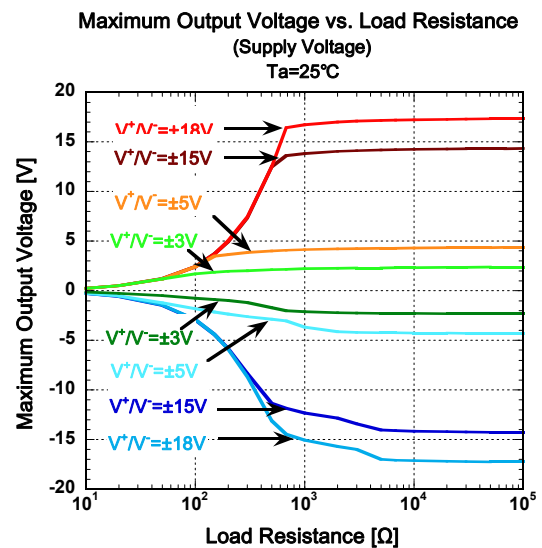
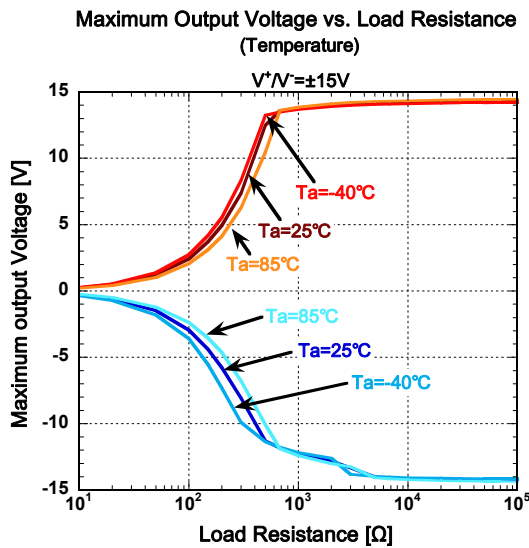
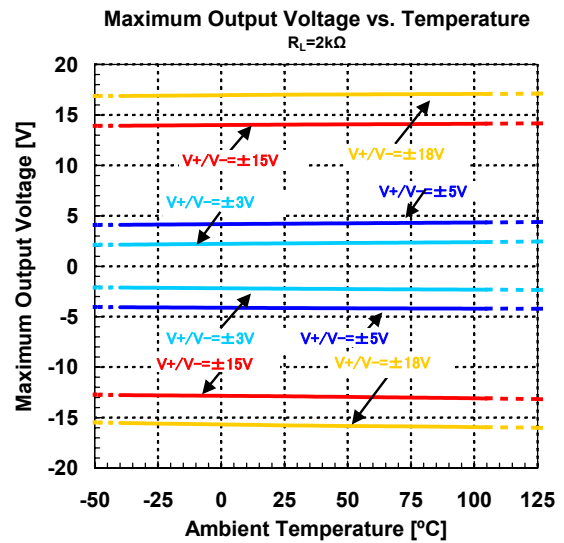
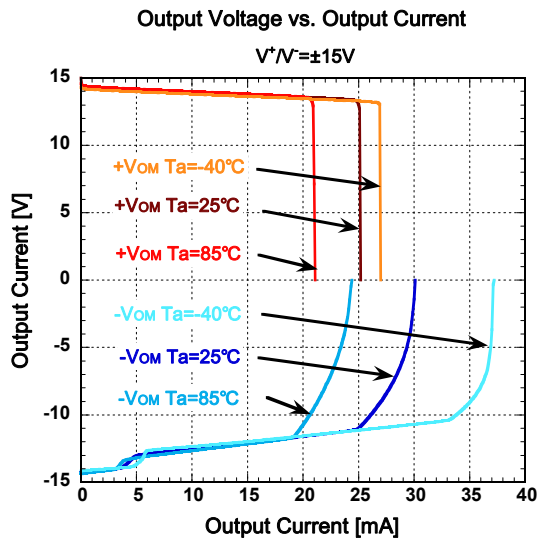


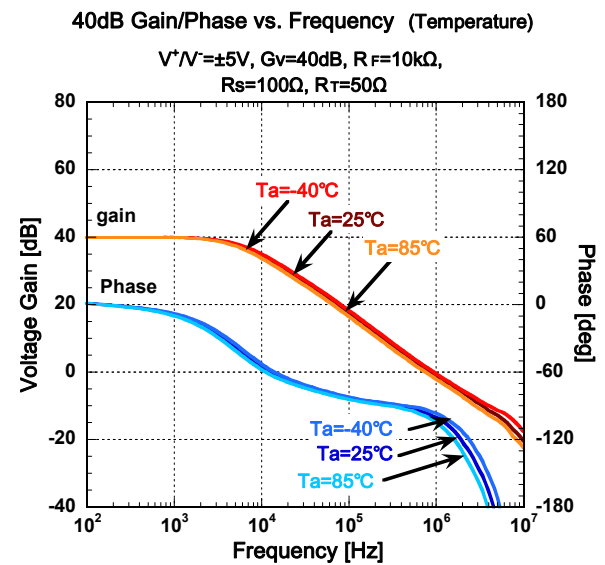
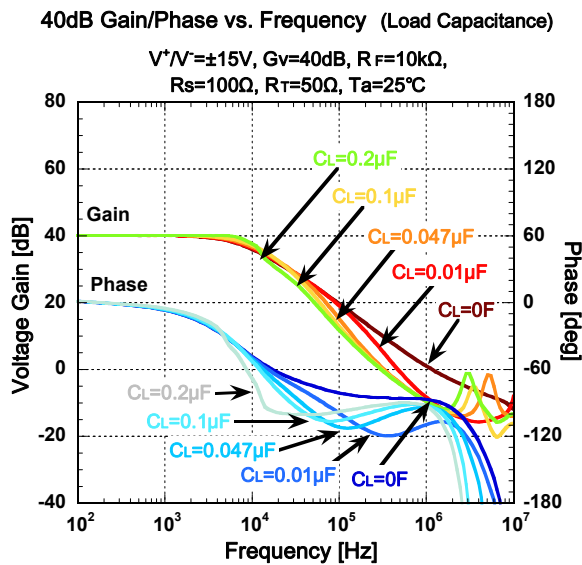
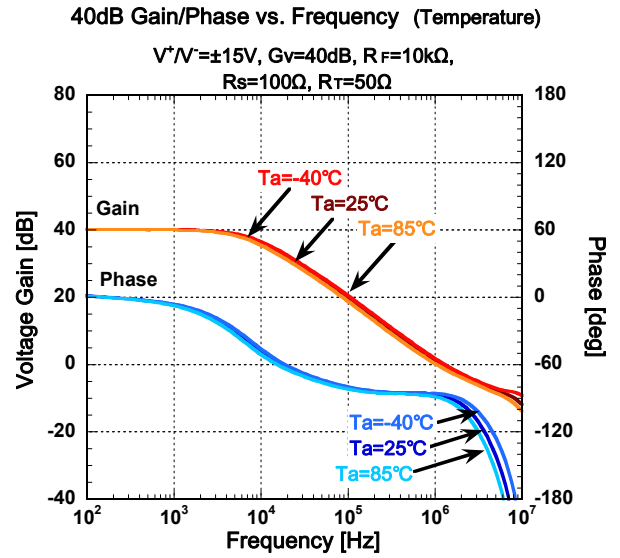
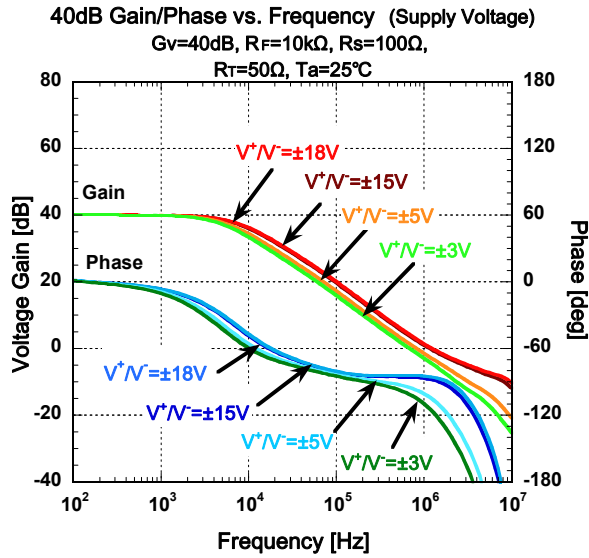
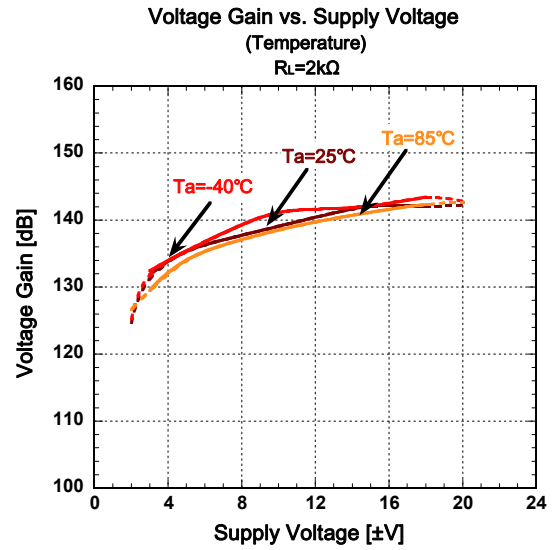
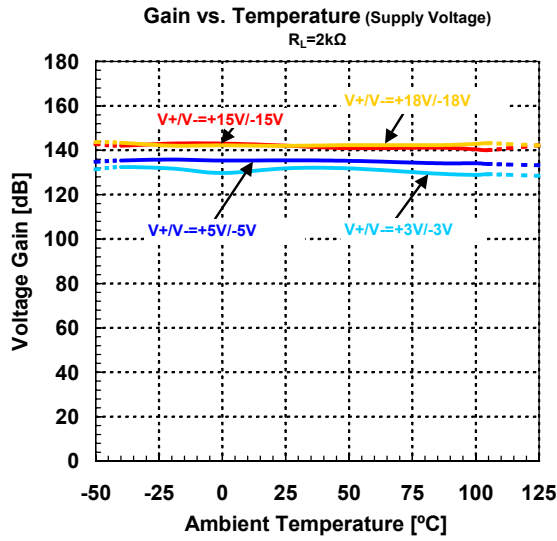
Supply Voltage Rejection Ratio vs. Frequency

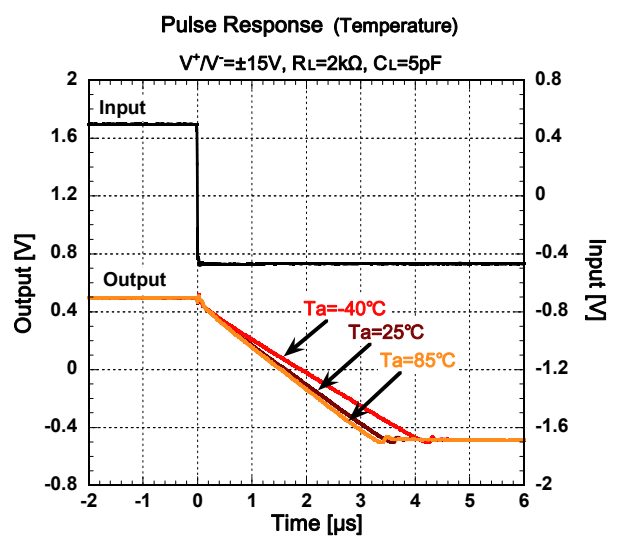
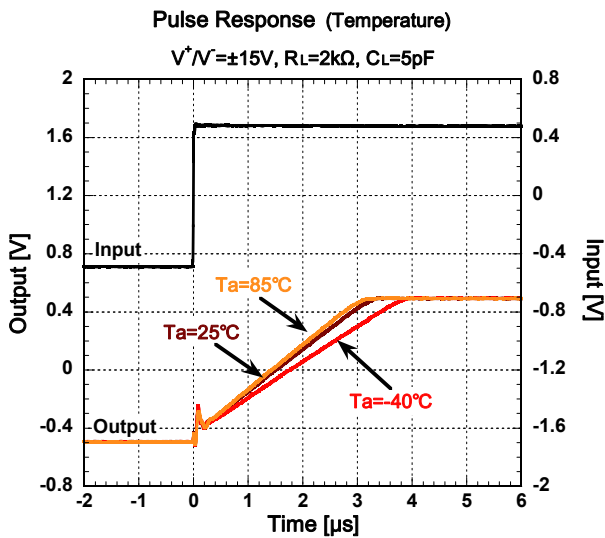
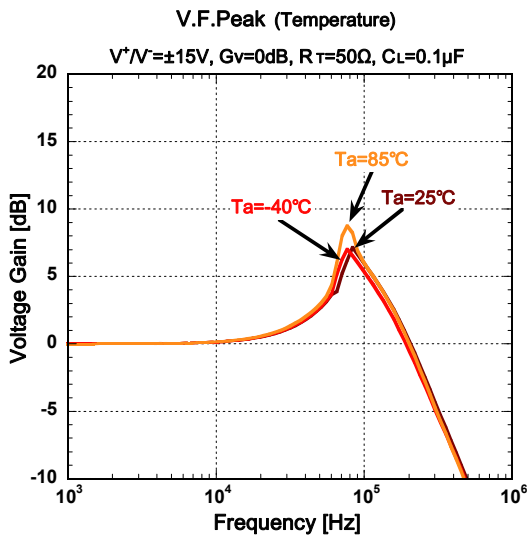
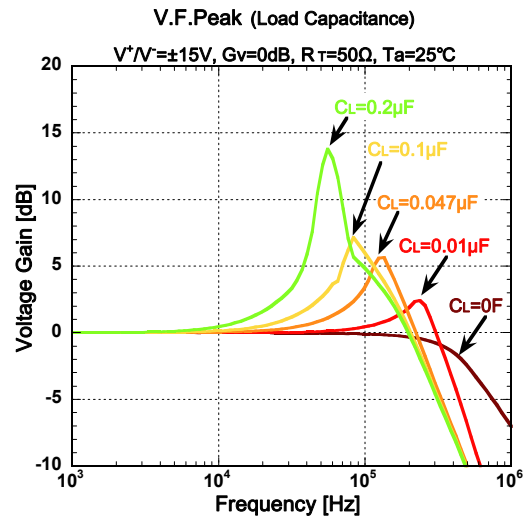
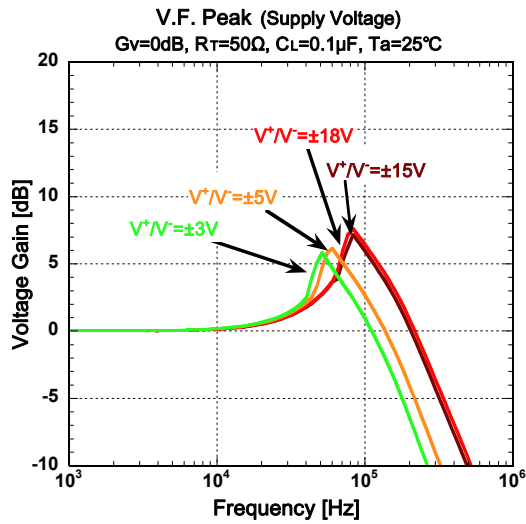


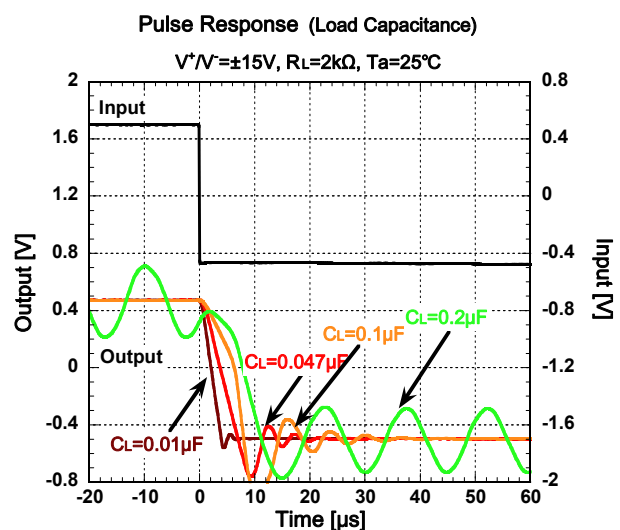
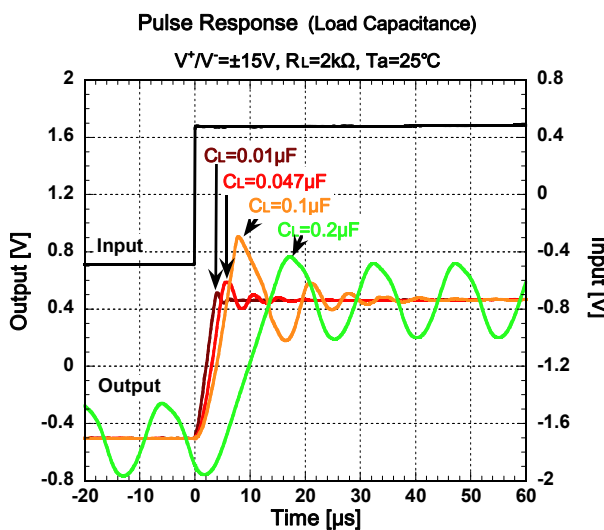
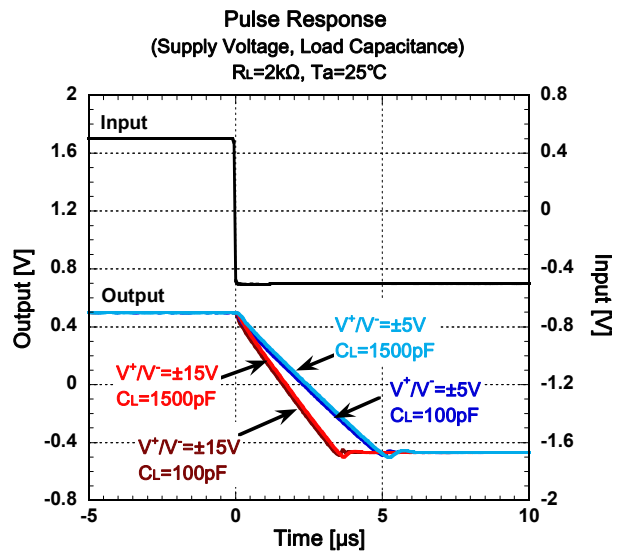
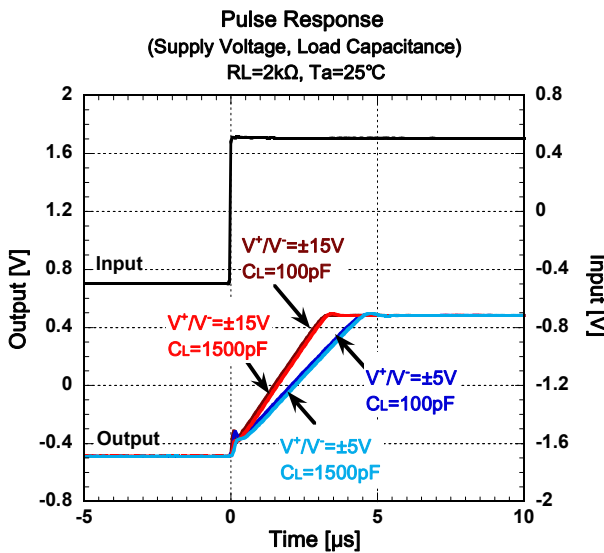
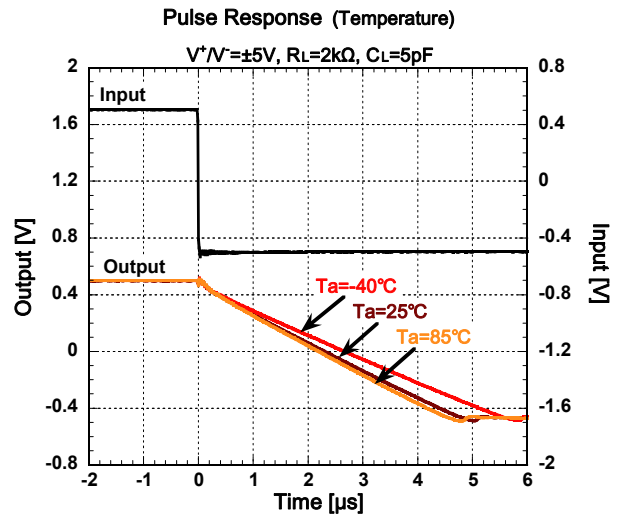
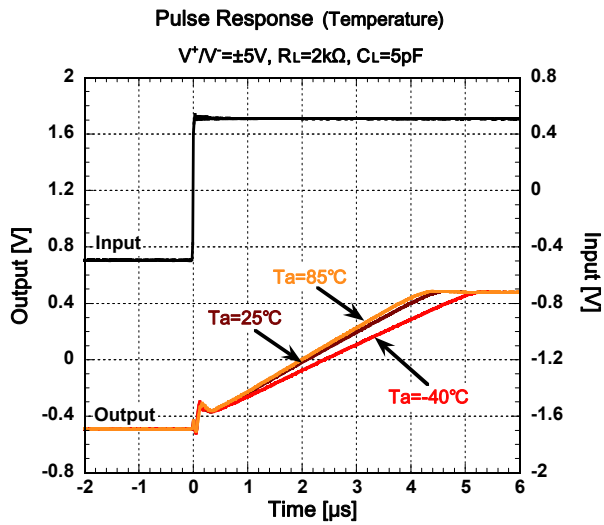
SVR vs. Temperature

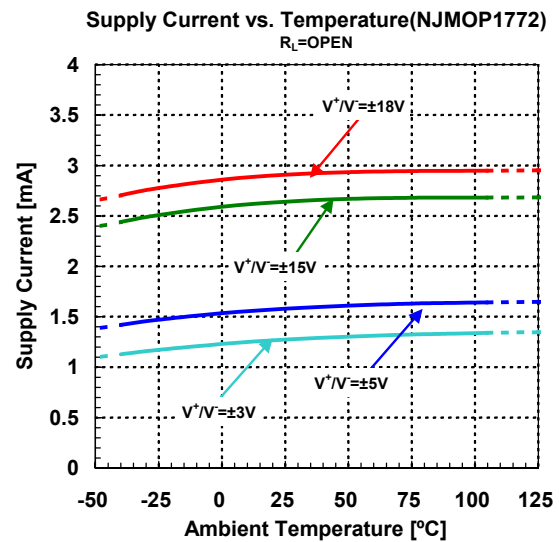
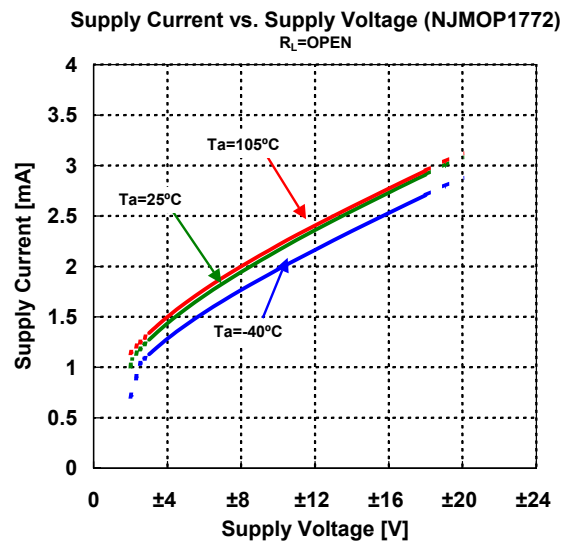
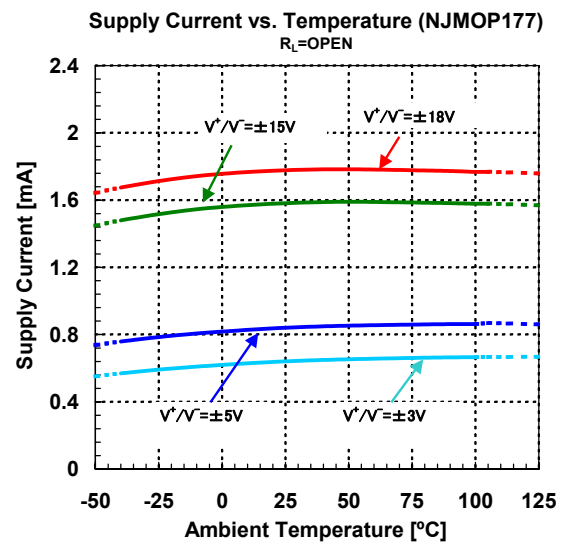
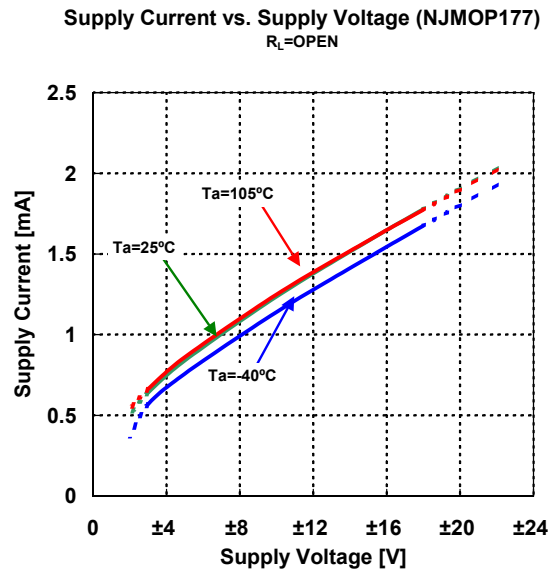
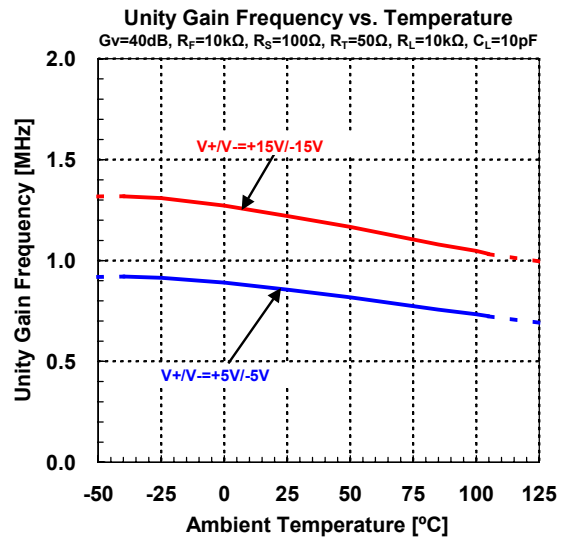
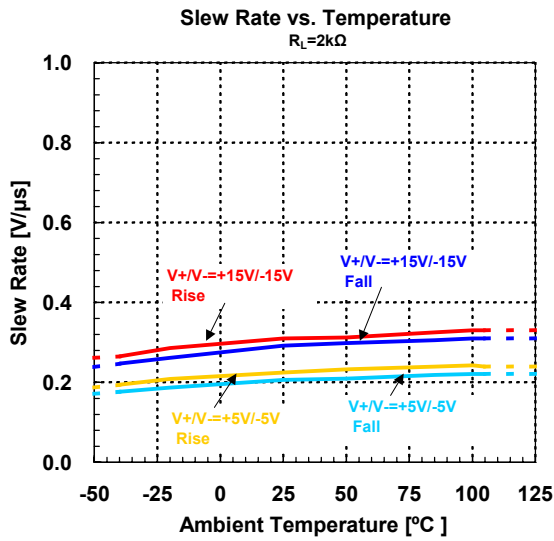












■Application Information

●Power Supply Bypassing

The NJMOP177/NJMOP1772 are high precision operational amplifiers featuring low offset voltage, high voltage gain, high CMR, high SVR and so on. To maximize such a high performance with stable operation, the NJMOP177/NJMOP1772 should be operated by clean and low impedance supply voltage. So, the bypass capacitor should be connected to the NJMOP177/NJMOP1772's both power supply terminals (V+ and V-) as shown in Fig.1. The bypass capacitors should be placed as close as possible to IC package.

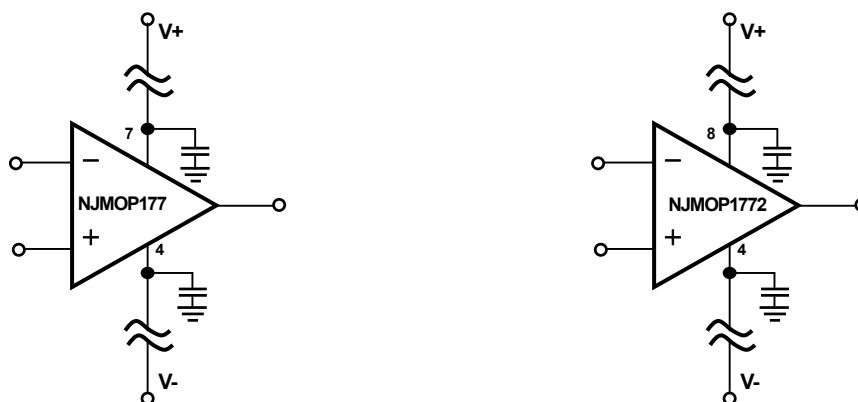


Fig.1 Power Supply Bypassing Circuit

●Thermoelectric Effect

The NJMOP177/NJMOP1772 are high precision operational amplifiers featuring low offset voltage and low offset voltage thermal drift.

To achieve such a high performance, take care about thermoelectric effect possibly occurs on each input terminal of the NJMOP177/NJMOP1772. Generally, if there are thermal mismatches at the junction of different types of metals, the thermoelectric voltage (Seebeck effect) occurs at the junction. The thermoelectric voltages possibly occur at the junction of PCB metal patterns and NJMOP177/NJMOP1772's each input terminal metal. If there is thermal mismatch in-between NJMOP177/NJMOP1772's each input terminal metal, the thermoelectric voltages generated on each input terminal possibly have different voltage each. This voltage difference causes offset voltage and offset voltage thermal drift of the NJMOP177 /NJMOP1772.

To minimize this voltage difference, the thermal mismatch in-between NJMOP177/NJMOP1772's each input terminal and PCB metal should be minimized.

NJMOP177/NJMOP1772

●Offset Voltage Adjustment (only NJMOP177)

The NJMOP177 has offset voltage trim terminals (pin1 and pin8) as shown in below Fig.2. By connecting external potentiometer in the range of 20Kohm, the offset voltage trim range is $\pm 3\text{mV}$. This offset voltage trim is effective only for offset voltage at room temperature, not for offset voltage thermal drift.

If offset voltage adjustment is not in use, leave pin1 and pin8 open (un-connected).

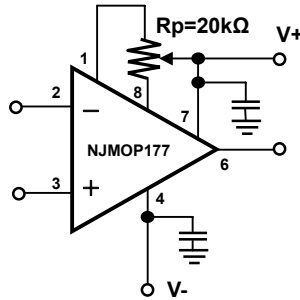


Fig.2 Offset Voltage Trim Circuit

●Differential Amplifier

Differential amplifier (see below Fig.3) is used in high accuracy circuit to improve common mode rejection ratio (CMR).

A matching between the ratio $R_1/R_2 = R_3/R_4$ and $R_1=R_3$ makes the high CMR.

For example, acceptable error range to obtain CMR of 130dB or more is about 0.1ppm.

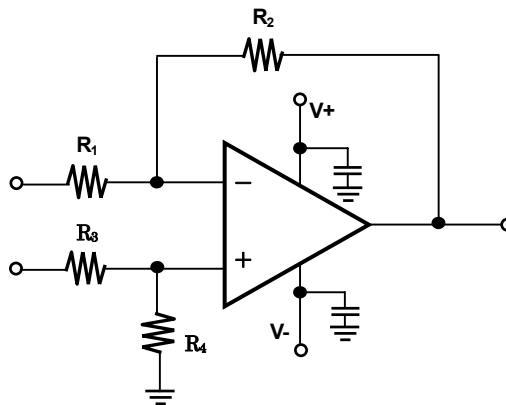
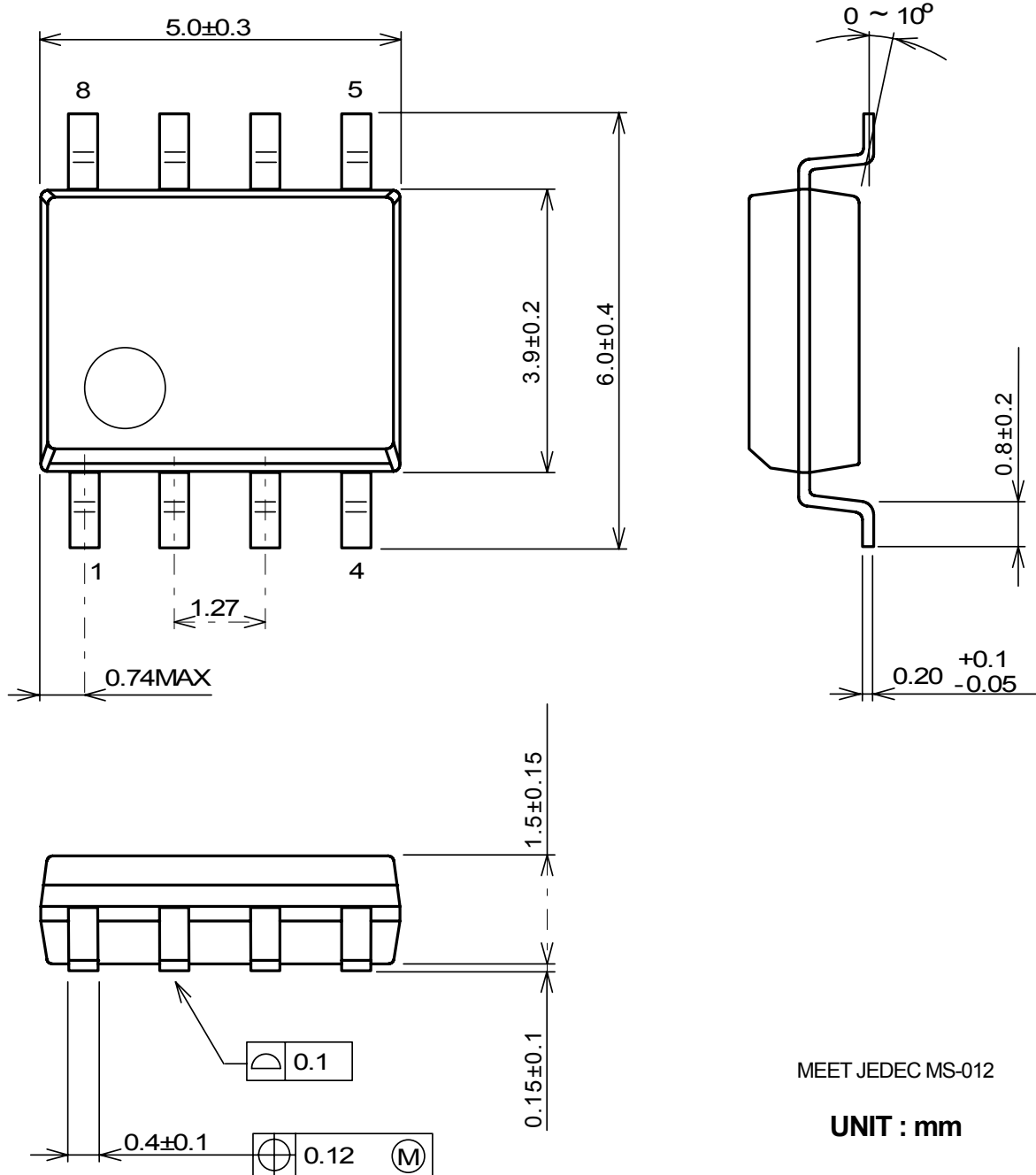


Fig.3 Differential Amplifier

■ PACKAGE DIMENSIONS

SOP8 JEDEC 150 mil



MEET JEDEC MS-012

UNIT : mm

[CAUTION]

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