

RoHS Compliant

2GB DDR3 SDRAM UDIMM

Product Specifications

January 17, 2014

Version 1.1



Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist., New Taipei City 236, Taiwan

Tel: +886-2-2267-8000 Fax: +886-2-2267-2261

www.apacer.com

Table of Contents

| | |
|---|----|
| General Description | 2 |
| Ordering Information | 2 |
| Key Parameters | 2 |
| Specifications: | 3 |
| Features: | 4 |
| Pin Assignments | 5 |
| Pin Descriptions | 7 |
| Functional Block Diagram | 8 |
| Absolute Maximum Ratings | 9 |
| DRAM Component Operating Temperature Range..... | 10 |
| Operating Conditions | 11 |
| Mechanical Drawing | 12 |

General Description

Apacer **78.A1GDE.4000C** is a 256M x 64 DDR3 SDRAM (Synchronous DRAM) DIMM. This high-density memory module consists of 8 pieces 256M x 8 bits with 8 banks DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM. The module is a 240-pins memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM. The following provides general specifications of this module.

Ordering Information

| Part Number | Bandwidth | Speed Grade | Max Frequency | CAS Latency |
|----------------|-------------|-------------|---------------|-------------|
| 78.A1GDE.4000C | 10.6 GB/sec | 1333 Mbps | 666 MHz | CL9 |

| Density | Organization | Component | Rank |
|---------|--------------|-----------|------|
| 2GB | 256M x 64 | 256M x8*8 | 1 |

Key Parameters

| MT/s | DDR3-1066 | DDR3-1333 | DDR3-1600 | Unit |
|-------------|-----------|-----------|-----------|------|
| Grade | -CL7 | -CL9 | -CL11 | |
| tCK (min) | 1.875 | 1.5 | 1.25 | ns |
| CAS latency | 7 | 9 | 11 | tCK |
| tRCD (min) | 13.125 | 13.5 | 13.75 | ns |
| tRP (min) | 13.125 | 13.5 | 13.75 | ns |
| tRAS (min) | 37.5 | 36 | 35 | ns |
| tRC (min) | 50.625 | 49.5 | 48.75 | ns |
| CL-tRCD-tRP | 7-7-7 | 9-9-9 | 11-11-11 | tCK |

Specifications:

- ◆ On-DIMM thermal sensor : No
- ◆ Organization: 256 words x 64 bits, 1 rank
- ◆ Integrating 8 pieces of 2G bits DDR3 SDRAM sealed FBGA
- ◆ Package: 240-pin socket type dual in-line memory module (DIMM)
- ◆ PCB: height 30.0 mm, lead pitch 1.0 mm (pin), lead-free (RoHS compliant)
- ◆ Power supply VDD: 1.5V ± 0.075V
- ◆ Serial Presence Detect (SPD)
- ◆ Eight Internal banks for concurrent operation (Components)
- ◆ Interface: SSTL_15
- ◆ Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- ◆ /CAS Latency (CL): 6, 7, 8, 9
- ◆ /CAS Write Latency (CWL): 5, 6, 7
- ◆ Supports auto pre-charge option for each burst access
- ◆ Supports auto-refresh/self-refresh
- ◆ Refresh cycles: 7.8 μ s at 0°C ≤ TC ≤ +85°C

Features:

- ◆ Double-data-rate architecture: 2 data transfers per clock cycle
- ◆ The high-speed data transfer is realized by the 8-bits prefetch pipelined architecture.
- ◆ Bi-directional differential data strobe (DQS and /DQS) is transmitted / received with data for capturing data at the receiver
- ◆ DQS: edge-aligned with data for read; center aligned with data for write
- ◆ Differential clock inputs (CK and /CK)
- ◆ DLL aligns DQ and DQS transitions with CK transitions
- ◆ Data mask (DM) for writing data
- ◆ Posted /CAS by programmable additive latency for enhanced command and data bus efficiency
- ◆ On-Die-Termination (ODT) for improved signal quality: Synchronous ODT/Dynamic ODT/Asynchronous ODT
- ◆ Multi-Purpose Register (MPR) for temperature read out
- ◆ ZQ calibration for DQ drive and ODT
- ◆ Programmable Partial Array Self-Refresh (PASR)
- ◆ /Reset pin for power-up sequence and reset function
- ◆ SRT range: normal/extended, auto/manual self-refresh
- ◆ Programmable output driver impedance control
- ◆ Commands entered at each positive clock input, while data and data mask are referenced to both edges of DQS

Pin Assignments

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 1 | VREFDQ | 31 | DQ25 | 61 | A2 | 91 | DQ41 |
| 2 | VSS | 32 | VSS | 62 | VDD | 92 | VSS |
| 3 | DQ0 | 33 | /DQS3 | 63 | CK1(NC) | 93 | /DQS5 |
| 4 | DQ1 | 34 | DQS3 | 64 | /CK1(NC) | 94 | DQS5 |
| 5 | VSS | 35 | VSS | 65 | VDD | 95 | VSS |
| 6 | /DQS0 | 36 | DQ26 | 66 | VDD | 96 | DQ42 |
| 7 | DQS0 | 37 | DQ27 | 67 | VREFCA | 97 | DQ43 |
| 8 | VSS | 38 | VSS | 68 | NC | 98 | VSS |
| 9 | DQ2 | 39 | NC | 69 | VDD | 99 | DQ48 |
| 10 | DQ3 | 40 | NC | 70 | A10(AP) | 100 | DQ49 |
| 11 | VSS | 41 | VSS | 71 | BA0 | 101 | VSS |
| 12 | DQ8 | 42 | NC | 72 | VDD | 102 | /DQS6 |
| 13 | DQ9 | 43 | NC | 73 | /WE | 103 | DQS6 |
| 14 | VSS | 44 | VSS | 74 | /CAS | 104 | VSS |
| 15 | /DQS1 | 45 | NC | 75 | VDD | 105 | DQ50 |
| 16 | DQS1 | 46 | NC | 76 | /CS1(NC) | 106 | DQ51 |
| 17 | VSS | 47 | VSS | 77 | ODT1(NC) | 107 | VSS |
| 18 | DQ10 | 48 | NC | 78 | VDD | 108 | DQ56 |
| 19 | DQ11 | 49 | NC | 79 | NC | 109 | DQ57 |
| 20 | VSS | 50 | CKE0 | 80 | VSS | 110 | VSS |
| 21 | DQ16 | 51 | VDD | 81 | DQ32 | 111 | /DQS7 |
| 22 | DQ17 | 52 | BA2 | 82 | DQ33 | 112 | DQS7 |
| 23 | VSS | 53 | NC | 83 | VSS | 113 | VSS |
| 24 | /DQS2 | 54 | VDD | 84 | /DQS4 | 114 | DQ58 |
| 25 | DQS2 | 55 | A11 | 85 | DQS4 | 115 | DQ59 |
| 26 | VSS | 56 | A7 | 86 | VSS | 116 | VSS |
| 27 | DQ18 | 57 | VDD | 87 | DQ34 | 117 | SA0 |
| 28 | DQ19 | 58 | A5 | 88 | DQ35 | 118 | SCL |
| 29 | VSS | 59 | A4 | 89 | VSS | 119 | SA2 |
| 30 | DQ24 | 60 | VDD | 90 | DQ40 | 120 | VTT |

| Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name | Pin No. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|
| 121 | VSS | 151 | VSS | 181 | A1 | 211 | VSS |
| 122 | DQ4 | 152 | DM3 | 182 | VDD | 212 | DM5 |
| 123 | DQ5 | 153 | NC | 183 | VDD | 213 | NC |
| 124 | VSS | 154 | VSS | 184 | CK0 | 214 | VSS |
| 125 | DM0 | 155 | DQ30 | 185 | /CK0 | 215 | DQ46 |
| 126 | NC | 156 | DQ31 | 186 | VDD | 216 | DQ47 |
| 127 | VSS | 157 | VSS | 187 | NC | 217 | VSS |
| 128 | DQ6 | 158 | NC | 188 | A0 | 218 | DQ52 |
| 129 | DQ7 | 159 | NC | 189 | VDD | 219 | DQ53 |
| 130 | VSS | 160 | VSS | 190 | BA1 | 220 | VSS |
| 131 | DQ12 | 161 | NC | 191 | VDD | 221 | DM6 |
| 132 | DQ13 | 162 | NC | 192 | /RAS | 222 | NC |
| 133 | VSS | 163 | VSS | 193 | /CS0 | 223 | VSS |
| 134 | DM1 | 164 | NC | 194 | VDD | 224 | DQ54 |
| 135 | NC | 165 | NC | 195 | ODT0 | 225 | DQ55 |
| 136 | VSS | 166 | VSS | 196 | A13 | 226 | VSS |
| 137 | DQ14 | 167 | NC | 197 | VDD | 227 | DQ60 |
| 138 | DQ15 | 168 | /RESET | 198 | NC | 228 | DQ61 |
| 139 | VSS | 169 | CKE1(NC) | 199 | VSS | 229 | VSS |
| 140 | DQ20 | 170 | VDD | 200 | DQ36 | 230 | DM7 |
| 141 | DQ21 | 171 | A15(NC) | 201 | DQ37 | 231 | NC |
| 142 | VSS | 172 | A14(NC) | 202 | VSS | 232 | VSS |
| 143 | DM2 | 173 | VDD | 203 | DM4 | 233 | DQ62 |
| 144 | NC | 174 | A12 | 204 | NC | 234 | DQ63 |
| 145 | VSS | 175 | A9 | 205 | VSS | 235 | VSS |
| 146 | DQ22 | 176 | VDD | 206 | DQ38 | 236 | VDDSPD |
| 147 | DQ23 | 177 | A8 | 207 | DQ39 | 237 | SA1 |
| 148 | VSS | 178 | A6 | 208 | VSS | 238 | SDA |
| 149 | DQ28 | 179 | VDD | 209 | DQ44 | 239 | VSS |
| 150 | DQ29 | 180 | A3 | 210 | DQ45 | 240 | VTT |

*Note:

1. CS1, ODT1, CKE1: Used for dual-rank UDIMMs; NC on single-rank UDIMMs
2. CK1,NC and CK1,NC : Used for dual-rank UDIMMs; not used on single-rank UDIMMs, but terminated

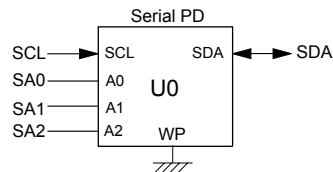
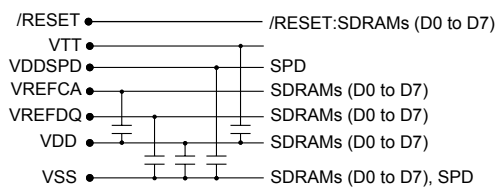
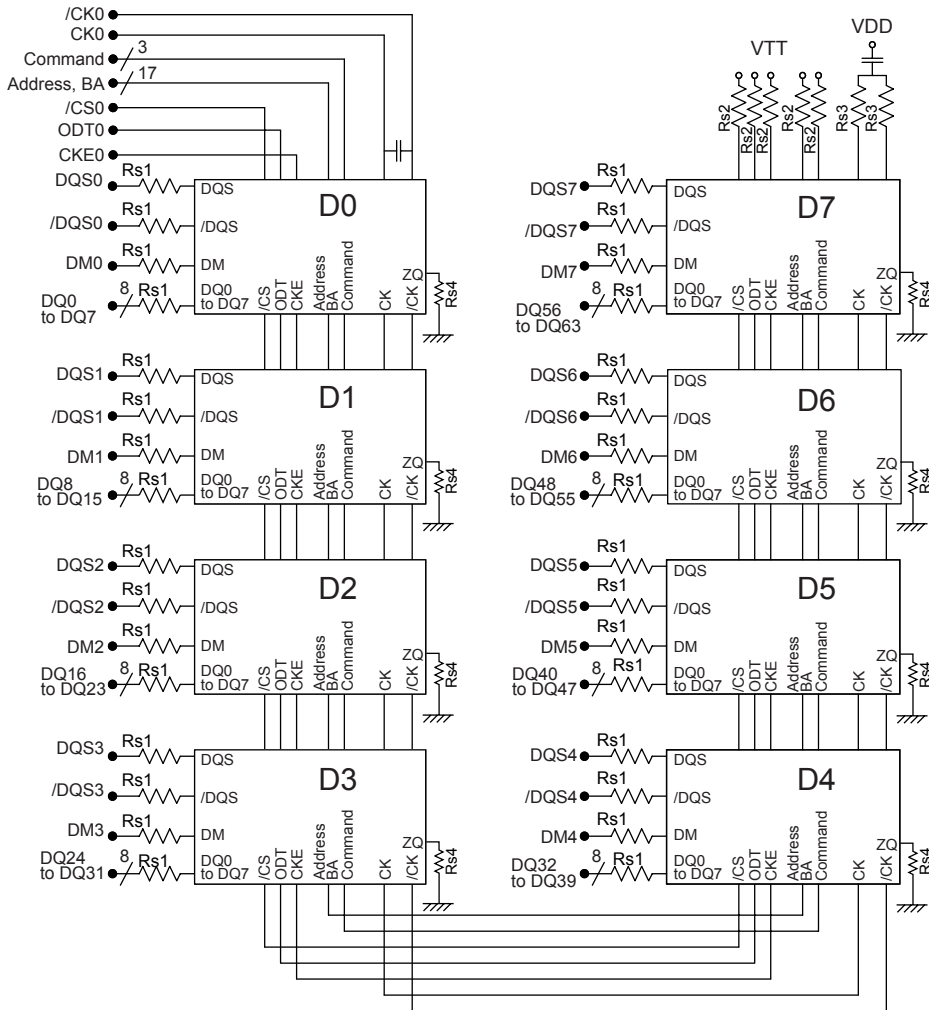
Pin Descriptions

| Pin Name | Description |
|----------|--|
| Ax* | SDRAM address bus |
| BAx | SDRAM bank select |
| DQx | DIMM memory data bus |
| /RAS | SDRAM row address strobe |
| /CAS | SDRAM column address strobe |
| /WE | SDRAM write enable |
| /CSx | SDRAM Chip select lines |
| CKEx | SDRAM clock enable lines |
| CKx | SDRAM clock input |
| /CKx | SDRAM Differential clock input |
| DQSx | SDRAM data strobes(positive line of differential pair) |
| /DQSx | SDRAM data strobes(negative line of differential pair) |
| DMx | SDRAM input mask |
| SCL | Clock input for serial PD |
| SDA | Data input/output for serial PD |
| SAX | Serial address input |
| VDD | Power for internal circuit |
| VDDSPD | Serial EEPROM positive power supply |
| VREFDQ | SDRAM I/O reference supply |
| VREFCA | SDRAM command/address reference supply |
| VSS | Power supply return(ground) |
| VTT | SDRAM I/O termination supply |
| /RESET | Set DRAM to known state |
| ODTx | On-die termination control lines |
| NC | Spare pins(no connect) |

*IC Component Composition:

| | |
|---------|--------|
| 128Mx8 | A0~A13 |
| 256Mx8 | A0~A14 |
| 512Mx8 | A0~A15 |
| 1024Mx8 | A0~A15 |

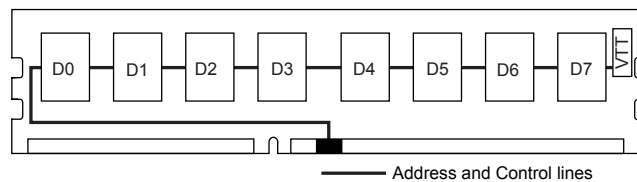
Functional Block Diagram



Notes :

1. DQ wiring may be changed within a byte.
2. DQ, DQS, /DQS, ODT, DM, CKE, /CS relationships must be maintained as shown.

* D0 to D7: 2G bits DDR3 SDRAM
 Address, BA: A0 to A14, BA0 to BA2
 Command: /RAS, /CAS, /WE
 U0: 256 bytes EEPROM
 Rs1: 15Ω
 Rs2: 39Ω
 Rs3: 36Ω
 Rs4: 240Ω



Absolute Maximum Ratings

| Parameter | Symbol | Description | Units |
|-------------------------------------|-------------------|-------------------|-------|
| Voltage on VDD pin relative to Vss | V_{DD} | - 0.4 V ~ 1.975 V | V |
| Voltage on VDDQ pin relative to Vss | V_{DDQ} | - 0.4 V ~ 1.975 V | V |
| Voltage on any pin relative to Vss | V_{IN}, V_{OUT} | - 0.4 V ~ 1.975 V | V |
| Storage Temperature | TSTG | -55 to +100 | °C |

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6 x VDDQ, when VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | Units | Notes |
|-------------------|------------------------------------|----------|-------|-------|
| T _{OPER} | Normal Operating Temperature Range | 0 to 85 | °C | 1,2 |
| | Extended Temperature Range | 85 to 95 | °C | 1,3 |

Notes:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For measurement conditions please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported during operation, the DRAM case temperature must be maintained between 0°C - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs.
 - b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

Operating Conditions

Recommended DC Operating Conditions - DDR3 (1.5V) operation

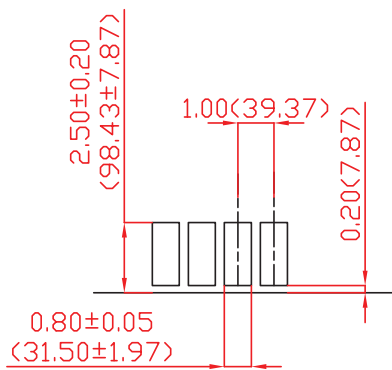
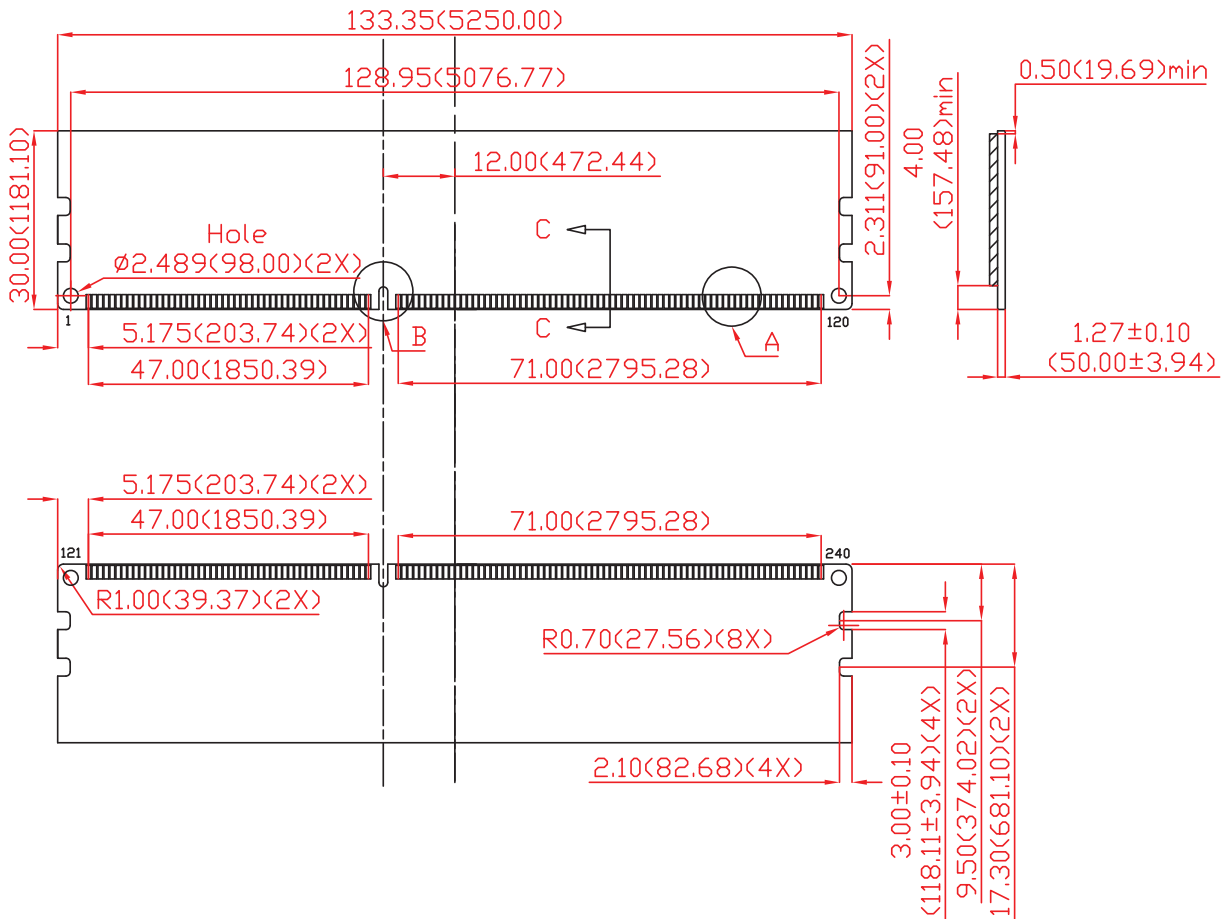
| Symbol | Parameter | Rating | | | Units |
|--------|---------------------------|--------|------|-------|-------|
| | | Min. | Typ. | Max. | |
| VDD | Supply Voltage | 1.425 | 1.5 | 1.575 | V |
| VDDQ | Supply Voltage for Output | 1.425 | 1.5 | 1.575 | V |

Notes:

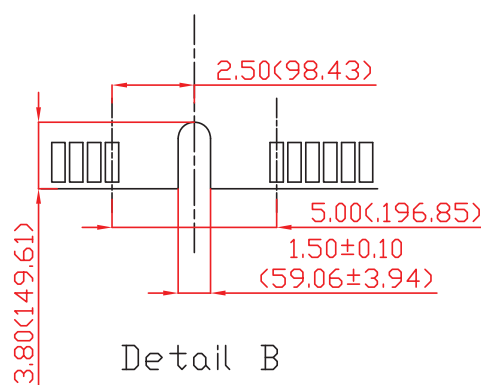
1. Under all conditions VDDQ must be less than or equal to VDD..
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

Mechanical Drawing

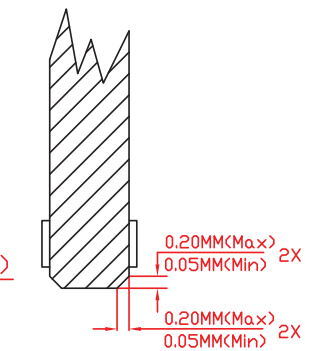
Unit: mm



Detail A



Detail B



VIEW C-C
OPTIONAL

(All dimensions are in millimeters with $\pm 0.15\text{mm}$ tolerance unless specified otherwise.)

Revision History

| Revision | Date | Description | Remark |
|-----------------|-------------|------------------------------|---------------|
| 0.9 | 08/28/2012 | Official release | |
| 1.0 | 08/29/2012 | release | |
| 1.1 | 07/23/2013 | Changed headquarters address | |

Global Presence

Taiwan (Headquarters)

Apacer Technology Inc.

1F., No.32, Zhongcheng Rd., Tucheng Dist.,

New Taipei City 236, Taiwan R.O.C.

Tel: +886-2-2267-8000

Fax: +886-2-2267-2261

amtsales@apacer.com

U.S.A.

Apacer Memory America, Inc.

386 Fairview Way, Suite 102,

Milpitas, CA 95035

Tel: 1-408-518-8699

Fax: 1-408-935-9611

sa@apacerus.com

Japan

Apacer Technology Corp.

5F, Matsura Bldg., Shiba, Minato-Ku

Tokyo, 105-0014, Japan

Tel: 81-3-5419-2668

Fax: 81-3-5419-0018

jpservices@apacer.com

Europe

Apacer Technology B.V.

Science Park Eindhoven 5051 5692 EB Son,

The Netherlands

Tel: 31-40-267-0000

Fax: 31-40-267-0000#6199

sales@apacer.nl

China

Apacer Electronic (Shanghai) Co., Ltd

1301, No.251, Xiaomujiao Road, Shanghai,

200032, China

Tel: 86-21-5529-0222

Fax: 86-21-5206-6939

sales@apacer.com.cn

India

Apacer Technologies Pvt Ltd,

535, 1st Floor, 8th cross, JP Nagar 3rd Phase,

Bangalore – 560078, India

Tel: 91-80-4152-9061

sales_india@apacer.com

Данный компонент на территории Российской Федерации

Вы можете приобрести в компании MosChip.

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: info@moschip.ru

Skype отдела продаж:

moschip.ru

moschip.ru_4

moschip.ru_6

moschip.ru_9