



# 35FS4500, 35FS6500

Grade 0 safety power system basis chip with CAN flexible data transceiver

Rev. 1.0 — 15 December 2017

Short data sheet: advance information

## 1 General description

The 35FS4500/35FS6500 SMARTMOS devices are a multi-output, power supply, integrated circuit, including CAN Flexible Data (FD) transceiver, dedicated to harsh automotive and transportation markets requiring high reliability (Grade 0) and high functional safety (fit for ASIL D) performance.

Multiple switching and linear voltage regulators, including low-power mode (32  $\mu$ A) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 1.5 A).

The 35FS4500/35FS6500 includes configurable fail-safe/fail silent safety behavior and features, with two fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level (up to ASIL D).

The built-in CAN FD interface fulfills the ISO 11898-2 and -5 standards.

High temperature capability up to  $T_A = 150\text{ }^{\circ}\text{C}$  and  $T_J = 175\text{ }^{\circ}\text{C}$ , compliant with AEC-Q100 Grade 0 automotive qualification.

## 2 Features

- Battery voltage sensing and MUX output pin
- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- 36 V maximum input operating voltage
- Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A or 1.5 A) or LDO (0.5 A)
- Linear voltage regulator dedicated to auxiliary functions, or to sensor supply ( $V_{CCA}$  tracker or independent), 5.0 V or 3.3 V
- Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply ( $V_{CCA}$ ), 5.0 V or 3.3 V
- 3.3 V keep alive memory supply available in low-power mode
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Multiple wake-up sources in low-power mode: CAN, I/Os, LDT
- Five configurable I/Os

## 3 Applications

- $T_A$  up to  $150\text{ }^{\circ}\text{C}$  and  $T_J$  up to  $175\text{ }^{\circ}\text{C}$
- Drive train electrification (BMS, hybrid EV and HEV, inverter, DCDC, alternator starter)
- Drive train - chassis and safety (active suspension, steering, safety domain gateway)
- Power train (EMS, TCU, gear box)



4 Simplified application diagram

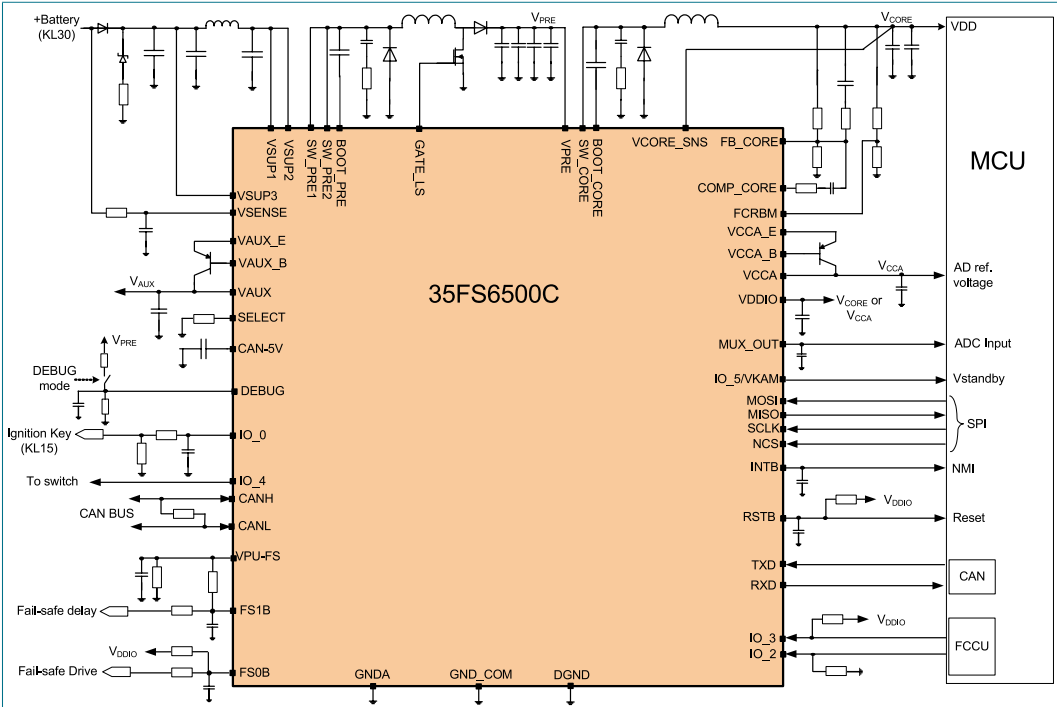


Figure 1. 35FS6500C simplified application diagram - buck boost configuration - FS1B

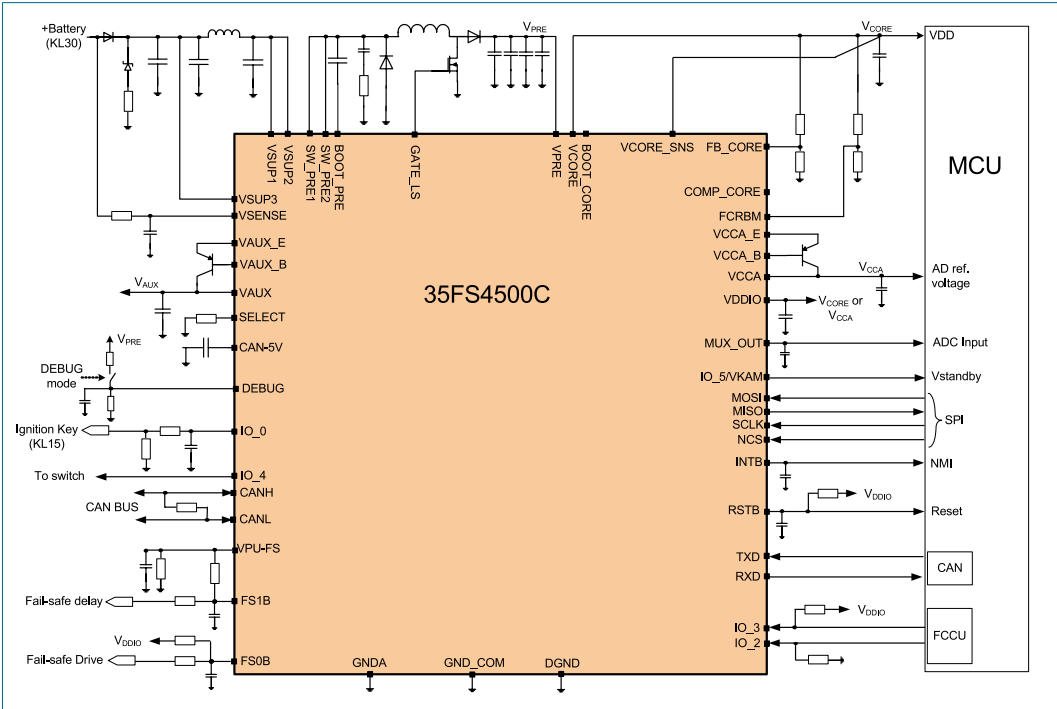


Figure 2. 35FS4500C simplified application diagram - buck boost configuration - FS1B

## 5 Ordering information

### 5.1 Part numbers definition

**MC35FS c 5 x y z AE/R2**

**Table 1. Part number breakdown**

| Code | Option   | Variable                  | Description    |
|------|----------|---------------------------|----------------|
| c    | 4 series | V <sub>CORE</sub> type    | Linear         |
|      | 6 series |                           | DCDC           |
| x    | 0        | V <sub>CORE</sub> current | 0.5 A or 0.8 A |
|      | 1        |                           | 1.5 A          |
| y    | 0        | Functions                 | none           |
|      | 1        |                           | FS1B           |
|      | 2        |                           | LDT            |
|      | 3        |                           | FS1B, LDT      |
| z    | N        | Physical interface        | none           |
|      | C        |                           | CAN FD         |

### 5.2 Part numbers list

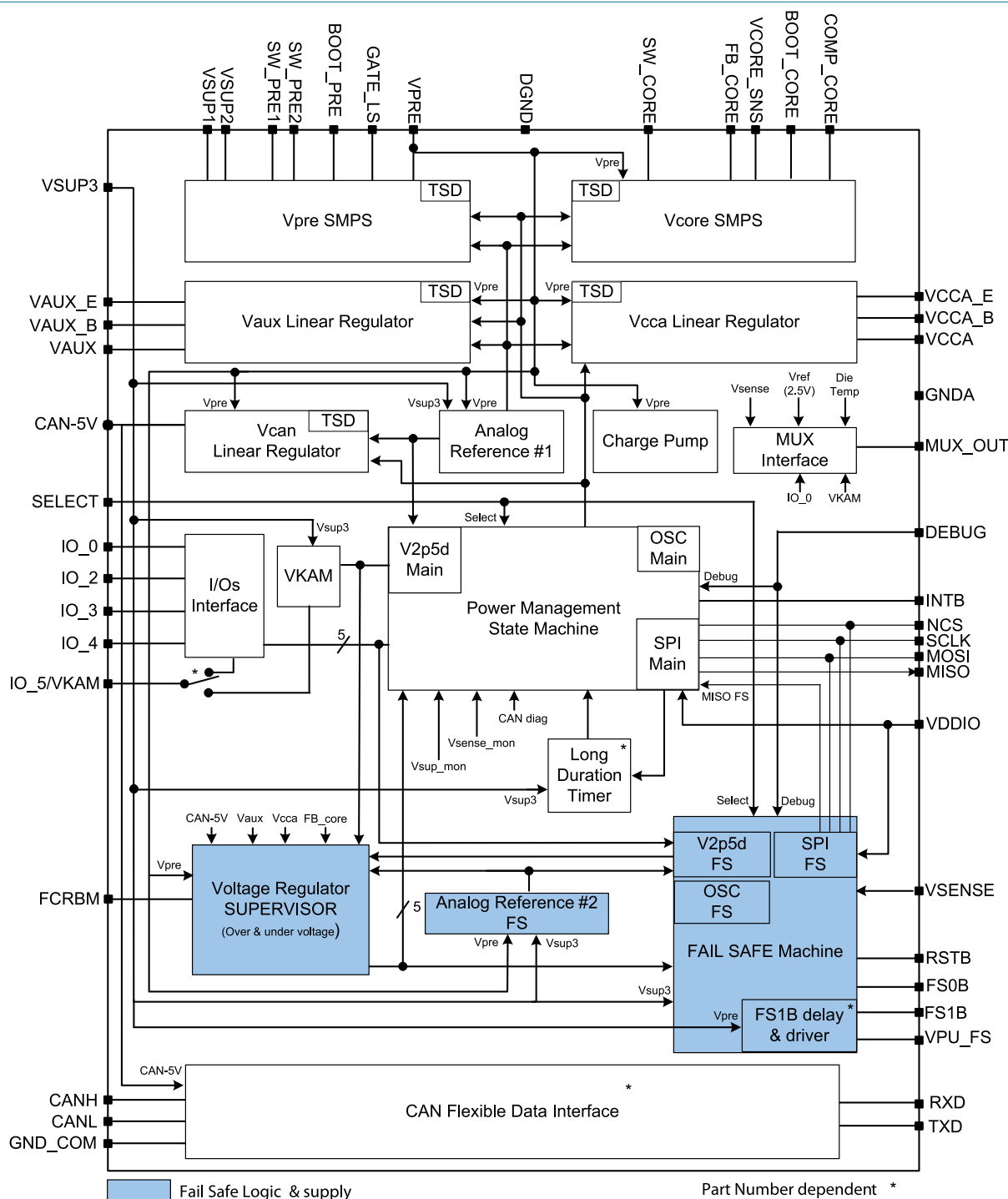
**Table 2. Orderable part variations**

| Part number   | Temperature (T <sub>A</sub> ) | Package                 | FS1B | LDT | V <sub>CORE</sub> | V <sub>CORE</sub> type | VKAM on | CAN FD | Notes |
|---------------|-------------------------------|-------------------------|------|-----|-------------------|------------------------|---------|--------|-------|
| MC35FS4500CAE | -40 °C to 150 °C              | 48-pin LQFP exposed pad | 0    | 0   | 0.5 A             | Linear                 | by SPI  | 1      | [1]   |
| MC35FS4500NAE |                               |                         | 0    | 0   | 0.5 A             | Linear                 | by SPI  | 0      |       |
| MC35FS4501CAE |                               |                         | 1    | 0   | 0.5 A             | Linear                 | by SPI  | 1      |       |
| MC35FS4501NAE |                               |                         | 1    | 0   | 0.5 A             | Linear                 | by SPI  | 0      |       |
| MC35FS4502CAE |                               |                         | 0    | 1   | 0.5 A             | Linear                 | by SPI  | 1      |       |
| MC35FS4502NAE |                               |                         | 0    | 1   | 0.5 A             | Linear                 | by SPI  | 0      |       |
| MC35FS4503CAE |                               |                         | 1    | 1   | 0.5 A             | Linear                 | by SPI  | 1      |       |
| MC35FS4503NAE |                               |                         | 1    | 1   | 0.5 A             | Linear                 | by SPI  | 0      |       |

| Part number   | Temperature (T <sub>A</sub> ) | Package                 | FS1B | LDT | VCORE | VCORE type | VKAM on | CAN FD | Notes |
|---------------|-------------------------------|-------------------------|------|-----|-------|------------|---------|--------|-------|
| MC35FS6500CAE | -40 °C to 150 °C              | 48-pin LQFP exposed pad | 0    | 0   | 0.8 A | DC DC      | by SPI  | 1      | [1]   |
| MC35FS6500NAE |                               |                         | 0    | 0   | 0.8 A | DC DC      | by SPI  | 0      |       |
| MC35FS6501CAE |                               |                         | 1    | 0   | 0.8 A | DC DC      | by SPI  | 1      |       |
| MC35FS6501NAE |                               |                         | 1    | 0   | 0.8 A | DC DC      | by SPI  | 0      |       |
| MC35FS6502CAE |                               |                         | 0    | 1   | 0.8 A | DC DC      | by SPI  | 1      |       |
| MC35FS6502NAE |                               |                         | 0    | 1   | 0.8 A | DC DC      | by SPI  | 0      |       |
| MC35FS6503CAE |                               |                         | 1    | 1   | 0.8 A | DC DC      | by SPI  | 1      |       |
| MC35FS6503NAE |                               |                         | 1    | 1   | 0.8 A | DC DC      | by SPI  | 0      |       |
| MC35FS6510CAE |                               |                         | 0    | 0   | 1.5 A | DC DC      | by SPI  | 1      |       |
| MC35FS6510NAE |                               |                         | 0    | 0   | 1.5 A | DC DC      | by SPI  | 0      |       |
| MC35FS6511CAE |                               |                         | 1    | 0   | 1.5 A | DC DC      | by SPI  | 1      |       |
| MC35FS6511NAE |                               |                         | 1    | 0   | 1.5 A | DC DC      | by SPI  | 0      |       |
| MC35FS6512CAE |                               |                         | 0    | 1   | 1.5 A | DC DC      | by SPI  | 1      |       |
| MC35FS6512NAE |                               |                         | 0    | 1   | 1.5 A | DC DC      | by SPI  | 0      |       |
| MC35FS6513CAE |                               |                         | 1    | 1   | 1.5 A | DC DC      | by SPI  | 1      |       |
| MC35FS6513NAE |                               |                         | 1    | 1   | 1.5 A | DC DC      | by SPI  | 0      |       |

[1] To order parts in tape and reel, add the R2 suffix to the part number.

## 6 Block diagram



**Figure 3. 35FS4500/35FS6500 simplified internal block diagram**

7 Pinning information

7.1 Pinning

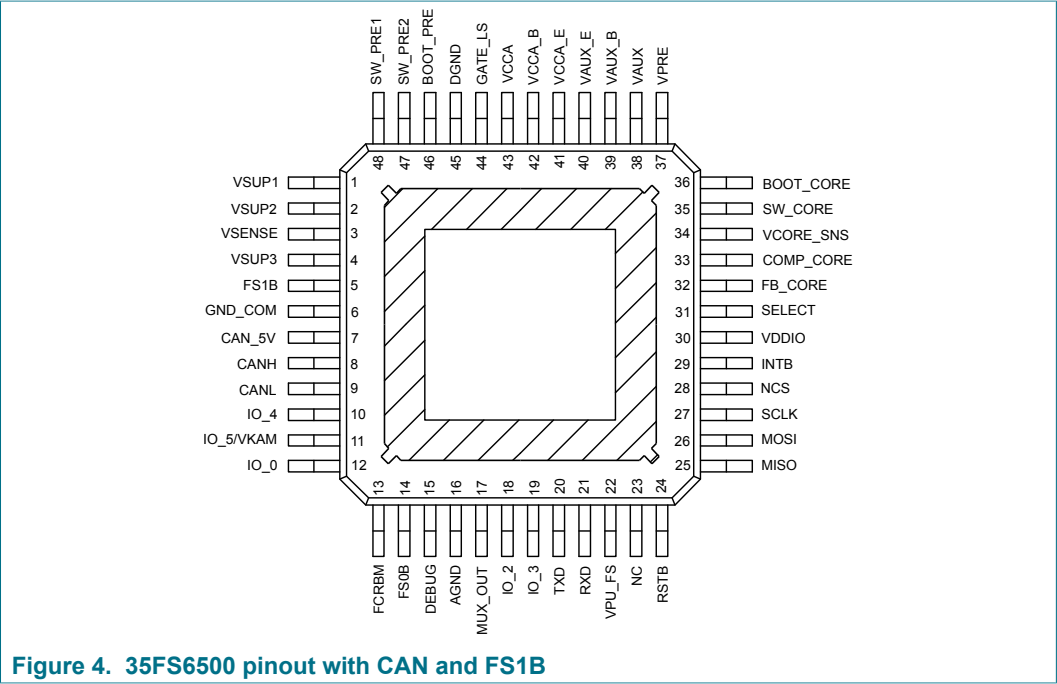


Figure 4. 35FS6500 pinout with CAN and FS1B

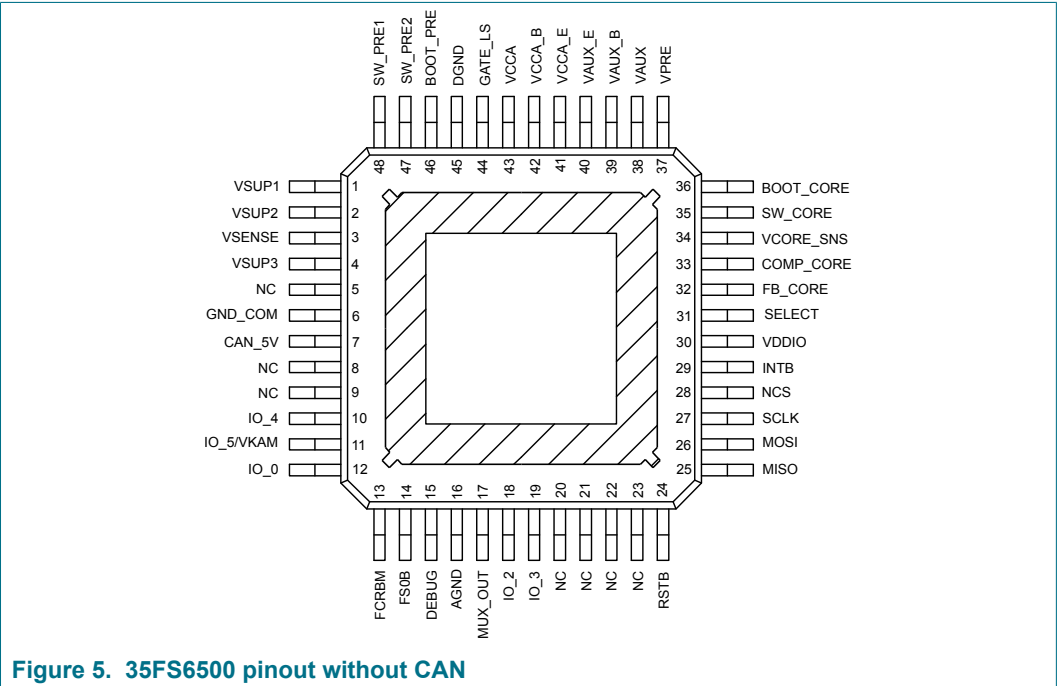


Figure 5. 35FS6500 pinout without CAN

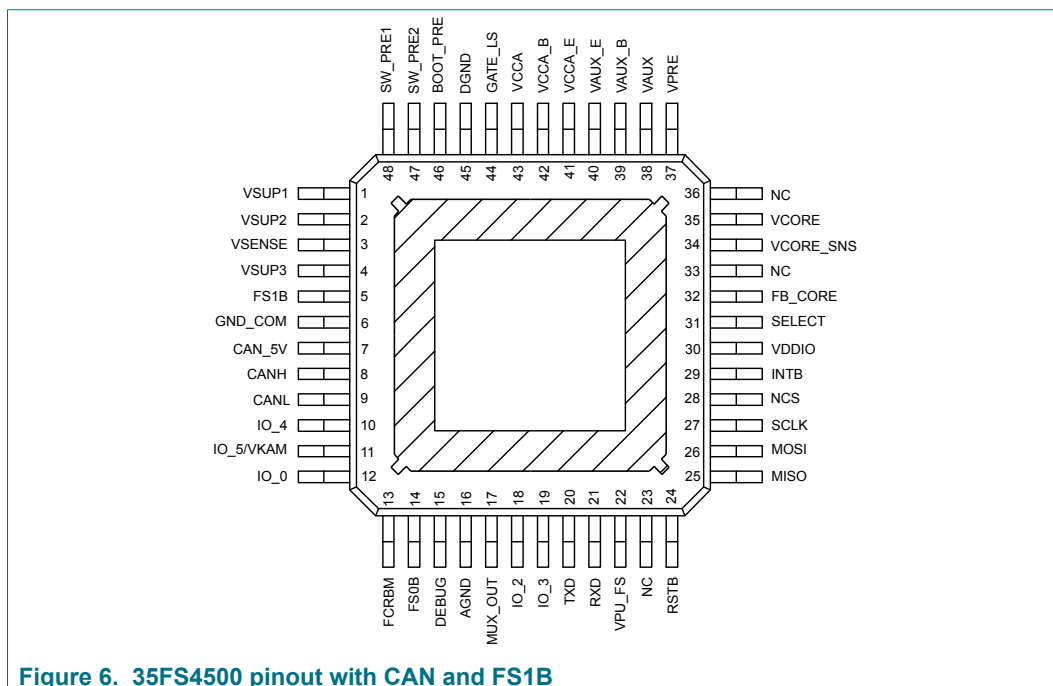


Figure 6. 35FS4500 pinout with CAN and FS1B

## 7.2 Pin description

Table 3. 35FS4500/35FS6500 pin definition

| Pin | Symbol  | Type     | Definition                                                                                                                                                                                                           |
|-----|---------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | VSUP1   | A_IN     | Power supply of the device. An external reverse battery protection diode in series is mandatory.                                                                                                                     |
| 2   | VSUP2   | A_IN     | Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally.                                                               |
| 3   | VSENSE  | A_IN     | Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.                                                                                                                     |
| 4   | VSUP3   | A_IN     | Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter.        |
| 5   | FS1B    | D_OUT    | Second output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected, with a configurable delay or duration versus FS0B output terminal. Open drain structure. |
| 6   | GND_COM | GROUND   | Dedicated ground for physical layers                                                                                                                                                                                 |
| 7   | CAN_5V  | A_OUT    | Output voltage for the embedded CAN FD interface                                                                                                                                                                     |
| 8   | CANH    | A_IN/OUT | CAN output high. If CAN function is not used, this pin must be left open.                                                                                                                                            |
| 9   | CANL    | A_IN/OUT | CAN output low. If CAN function is not used, this pin must be left open.                                                                                                                                             |

| Pin      | Symbol    | Type                  | Definition                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|----------|-----------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10       | IO_4      | D_IN<br>A_OUT         | Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver<br><b>Digital input:</b> Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used in conjunction with IO_5).<br><b>Wake-up capability:</b> Can be selectable to wake-up on edges or levels.<br><b>Output gate driver:</b> Can drive a logic level low-side NMOS transistor. Controlled by the SPI.                                                                                      |
| 11       | IO_5/VKAM | A_IN<br>D_IN<br>A_OUT | Can be used as digital input with wake-up capability or as an analog output providing keep alive memory supply in low-power mode.<br><b>Analog input:</b> Pin status can be read through the MUX output terminal.<br><b>Digital input:</b> Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used in conjunction with IO_4).<br><b>Wake-up capability:</b> Can be selectable to wake-up on edges or levels.<br><b>Supply output:</b> Provide keep alive memory supply in low-power mode. |
| 12       | IO_0      | A_IN<br>D_IN          | Can be used as analog or digital input (load dump proof) with wake-up capability (selectable).<br><b>Analog input:</b> Pin status can be read through the MUX output terminal.<br><b>Digital input:</b> Pin status can be read through the SPI.<br><b>Wake-up capability:</b> Can be selectable to wake-up on edges or levels.                                                                                                                                                                                                                                |
| 13       | FCRBM     | A_IN                  | Feedback core resistor bridge monitoring: For safety purposes, this pin is used to monitor the middle point of a redundant resistor bridge connected on V <sub>CORE</sub> (in parallel to the one used to set the V <sub>CORE</sub> voltage). If not used, this pin must be connected directly to FB_CORE.                                                                                                                                                                                                                                                    |
| 14       | FS0B      | D_OUT                 | First output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure.                                                                                                                                                                                                                                                                                                                                                                                                              |
| 15       | DEBUG     | D_IN                  | Debug mode entry input                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 16       | AGND      | GROUND                | Analog ground connection                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 17       | MUX_OUT   | A_OUT                 | Multiplexed output to be connected to a MCU ADC. Selection of the analog parameter is available at MUX-OUT through the SPI.                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 18<br>19 | IO_2:3    | D_IN                  | Digital input pin with wake-up capability (logic level compatible)<br><b>Digital input:</b> Pin status can be read through the SPI. Can be used to monitor FCCU error signals from MCU for safety purposes.<br><b>Wake-up capability:</b> Can be selectable to wake-up on edges or levels.                                                                                                                                                                                                                                                                    |
| 20       | TXD       | D_IN                  | Transceiver input from the MCU which controls the state of the CAN bus. Internal pull-up to VDDIO.<br>If CAN function is not used, this pin must be left open.                                                                                                                                                                                                                                                                                                                                                                                                |
| 21       | RXD       | D_OUT                 | Receiver output which reports the state of the CAN bus to the MCU<br>If CAN function is not used, this pin must be left open.                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 22       | VPU_FS    | A_OUT                 | Pull-up output for FS1B function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 23       | NC        | N/A                   | Not connected. Pin must be left open.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 24       | RSTB      | D_OUT                 | This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.                                                                                                                                                                                                                                                                                                                                |
| 25       | MISO      | D_OUT                 | SPI bus. Master input slave output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

| Pin | Symbol    | Type     | Definition                                                                                                                           |
|-----|-----------|----------|--------------------------------------------------------------------------------------------------------------------------------------|
| 26  | MOSI      | D_IN     | SPI bus. Master output slave input                                                                                                   |
| 27  | SCLK      | D_IN     | SPI Bus. Serial clock                                                                                                                |
| 28  | NCS       | D_IN     | Not chip select (active low)                                                                                                         |
| 29  | INTB      | D_OUT    | This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO. |
| 30  | VDDIO     | A_IN     | Input voltage for MISO output buffer<br>Allows voltage compatibility with MCU I/Os                                                   |
| 31  | SELECT    | D_IN     | Hardware selection pin for VAUX and VCCA output voltages                                                                             |
| 32  | FB_CORE   | A_IN     | VCORE voltage feedback. Input of the error amplifier.                                                                                |
| 33  | COMP_CORE | A_OUT    | Compensation network. Output of the error amplifier.<br>For FS4500 series, this pin must be left open (NC).                          |
| 34  | VCORE_SNS | A_IN     | VCORE input voltage sense                                                                                                            |
| 35  | SW_CORE   | A_OUT    | VCORE output switching point for FS6500 series                                                                                       |
|     | or VCORE  | A_OUT    | VCORE output voltage for FS4500 series                                                                                               |
| 36  | BOOT_CORE | A_IN/OUT | Bootstrap capacitor for VCORE internal NMOS gate drive.<br>For FS4500 series, this pin must be left open (NC).                       |
| 37  | VPRE      | A_IN     | VPRE input voltage sense                                                                                                             |
| 38  | VAUX      | A_OUT    | VAUX output voltage. External PNP ballast transistor. Collector connection                                                           |
| 39  | VAUX_B    | A_OUT    | VAUX voltage regulator. External PNP ballast transistor. Base connection                                                             |
| 40  | VAUX_E    | A_OUT    | VAUX voltage regulator. External PNP ballast transistor. Emitter connection                                                          |
| 41  | VCCA_E    | A_OUT    | VCCA voltage regulator. External PNP ballast transistor. Emitter connection                                                          |
| 42  | VCCA_B    | A_OUT    | VCCA voltage regulator. External PNP ballast transistor. Base connection                                                             |
| 43  | VCCA      | A_OUT    | VCCA output voltage. External PNP ballast transistor. Collector connection                                                           |
| 44  | GATE_LS   | A_OUT    | Low-side MOSFET gate drive for non-inverting buck-boost configuration                                                                |
| 45  | DGND      | GROUND   | Digital ground connection                                                                                                            |
| 46  | BOOT_PRE  | A_IN/OUT | Bootstrap capacitor for the VPRE internal NMOS gate drive                                                                            |
| 47  | SW_PRE2   | A_OUT    | Second pre-regulator output switching point                                                                                          |
| 48  | SW_PRE1   | A_OUT    | First pre-regulator output switching point                                                                                           |

## 8 Maximum ratings

**Table 4. Maximum ratings**

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol                         | Ratings                                                                             | Value       | Unit | Notes |
|--------------------------------|-------------------------------------------------------------------------------------|-------------|------|-------|
| <b>Electrical ratings</b>      |                                                                                     |             |      |       |
| V <sub>SUP1/2/3</sub>          | DC voltage at power supply pins                                                     | −1.0 to 40  | V    | [1]   |
| V <sub>SENSE</sub>             | DC voltage at battery sense pin (with ext R in series mandatory)                    | −14 to 40   | V    |       |
| V <sub>SW1,2</sub>             | DC voltage at SW_PRE1 and SW_PRE2 Pins                                              | −1.0 to 40  | V    |       |
| V <sub>PRE</sub>               | DC voltage at VPRE Pin                                                              | −0.3 to 8   | V    |       |
| V <sub>GATE_LS</sub>           | DC voltage at Gate_LS pin                                                           | −0.3 to 8   | V    |       |
| V <sub>BOOT_PRE</sub>          | DC voltage at BOOT_PRE pin                                                          | −1.0 to 50  | V    |       |
| V <sub>SW_CORE</sub>           | DC voltage at SW_CORE pin                                                           | −1.0 to 8   | V    |       |
| V <sub>CORE_SNS</sub>          | DC voltage at VCORE_SNS pin                                                         | 0.0 to 8    | V    |       |
| V <sub>BOOT_CORE</sub>         | DC voltage at BOOT_CORE pin                                                         | 0.0 to 15   | V    |       |
| V <sub>FB_CORE</sub>           | DC voltage at FB_CORE pin                                                           | −0.3 to 2.5 | V    |       |
| V <sub>COMP_CORE</sub>         | DC voltage at COMP_CORE pin                                                         | −0.3 to 2.5 | V    |       |
| V <sub>FCRBM</sub>             | DC voltage at FCRBM pin                                                             | −0.3 to 8   | V    |       |
| V <sub>AUX_B,E</sub>           | DC voltage at VAUX_B, VAUX_E pins                                                   | −0.3 to 40  | V    |       |
| V <sub>AUX</sub>               | DC voltage at VAUX pin                                                              | −2.0 to 40  | V    |       |
| V <sub>CCA_B,E</sub>           | DC voltage at VCCA_B, VCCA_E pins                                                   | −0.3 to 8   | V    |       |
| V <sub>CCA</sub>               | DC voltage at VCCA pin                                                              | −0.3 to 8   | V    |       |
| V <sub>DDIO</sub>              | DC voltage at VDDIO pin                                                             | −0.3 to 8   | V    |       |
| V <sub>CAN_5V</sub>            | DC voltage on CAN_5V pin                                                            | −0.3 to 8   | V    |       |
| V <sub>PU_FS</sub>             | DC voltage at VPU_FS pin                                                            | −0.3 to 8   | V    |       |
| V <sub>FSxB</sub>              | DC voltage at FS0B, FS1B pins (with ext R in series mandatory)                      | −0.3 to 40  | V    |       |
| V <sub>DEBUG</sub>             | DC voltage at DEBUG pin                                                             | −0.3 to 40  | V    |       |
| V <sub>IO_0,4</sub>            | DC voltage at IO_0, IO_4 pins (with ext R in series mandatory)                      | −0.3 to 40  | V    |       |
| V <sub>IO_5</sub>              | DC voltage at IO_5 pin                                                              | −0.3 to 20  | V    |       |
| V <sub>KAM</sub>               | DC voltage at VKAM pin                                                              | −0.3 to 8   | V    |       |
| V <sub>DIG</sub>               | DC voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, IO_2, IO_3 pins | −0.3 to 8   | V    |       |
| V <sub>SELECT</sub>            | DC voltage at SELECT pin                                                            | −0.3 to 8   | V    |       |
| V <sub>BUS_CAN</sub>           | DC voltage on CANL, CANH pins                                                       | −27 to 40   | V    |       |
| I <sub>I<sub>SENSE</sub></sub> | V <sub>SENSE</sub> maximum current capability                                       | −5.0 to 5.0 | mA   |       |
| I <sub>IO_0, 4, 5</sub>        | IOs maximum current capability (IO_0, IO_4, IO_5)                                   | −5.0 to 5.0 | mA   |       |

| Symbol                 | Ratings                                                               | Value      | Unit | Notes |
|------------------------|-----------------------------------------------------------------------|------------|------|-------|
| ESD voltage            |                                                                       |            |      |       |
| V <sub>ESD-HBM1</sub>  | Human body model (JESD22/A114) – 100 pF, 1.5 kΩ                       | ±2.0       | kV   | [2]   |
| V <sub>ESD-HBM2</sub>  | • All pins                                                            | ±4.0       | kV   |       |
| V <sub>ESD-HBM3</sub>  | • VSUP1,2,3, VSENSE, VAUX, IO_0,4, FS0B, FS1B, DEBUG                  | ±6.0       | kV   |       |
| V <sub>ESD-CDM1</sub>  | Charge device model (JESD22/C101):                                    |            |      |       |
| V <sub>ESD-CDM2</sub>  | • All pins                                                            | ±500       | V    |       |
|                        | • Corner pins                                                         | ±750       | V    |       |
|                        | <b>System level ESD (gun test)</b>                                    |            |      |       |
|                        | • VSUP1, 2, 3, VSENSE, VAUX, IO_0, 4, 5, FS0B, FS1B                   |            |      |       |
| V <sub>ESD-GUN1</sub>  | 330 Ω/150 pF unpowered according to IEC61000-4-2                      | ±8.0       | kV   |       |
| V <sub>ESD-GUN2</sub>  | 330 Ω/150 pF unpowered according to OEM LIN, CAN, FLExray Conformance | ±8.0       | kV   |       |
| V <sub>ESD-GUN3</sub>  | 2.0 kΩ/150 pF unpowered according to ISO10605.2008                    | ±8.0       | kV   |       |
| V <sub>ESD-GUN4</sub>  | 2.0 kΩ/330 pF powered according to ISO10605.2008                      | ±8.0       | kV   |       |
|                        | • CANH, CANL                                                          |            |      |       |
| V <sub>ESD-GUN5</sub>  | 330 Ω/150 pF unpowered according to IEC61000-4-2                      | ±15.0      | kV   |       |
| V <sub>ESD-GUN6</sub>  | 330 Ω/150 pF unpowered according to OEM LIN, CAN, FLExray Conformance | ±12.0      | kV   |       |
| V <sub>ESD-GUN7</sub>  | 2.0 kΩ/150 pF unpowered according to ISO10605.2008                    | ±15.0      | kV   |       |
| V <sub>ESD-GUN8</sub>  | 2.0 kΩ/330 pF powered according to ISO10605.2008                      | ±12.0      | kV   |       |
| Thermal ratings        |                                                                       |            |      |       |
| T <sub>A</sub>         | Ambient temperature                                                   | –40 to 150 | °C   |       |
| T <sub>J</sub>         | Junction temperature                                                  | –40 to 175 | °C   |       |
| T <sub>STG</sub>       | Storage temperature                                                   | –55 to 150 | °C   |       |
| Thermal resistance     |                                                                       |            |      |       |
| R <sub>θJA</sub>       | Thermal resistance junction to ambient                                | 30         | °C/W | [3]   |
| R <sub>θJCTOP</sub>    | Thermal resistance junction to case top                               | 23.8       | °C/W | [4]   |
| R <sub>θJCBOTTOM</sub> | Thermal resistance junction to case bottom                            | 0.9        | °C/W | [5]   |

[1] All VSUPs (V<sub>SUP1/2/3</sub>) must be connected to the same supply

[2] Compared to AGND

[3] Per JEDEC JESD51-6 with the board (JESD51-7) horizontal

[4] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1).

[5] Thermal resistance between the die and the solder par on the bottom of the packaged based on simulation without any interface resistance.

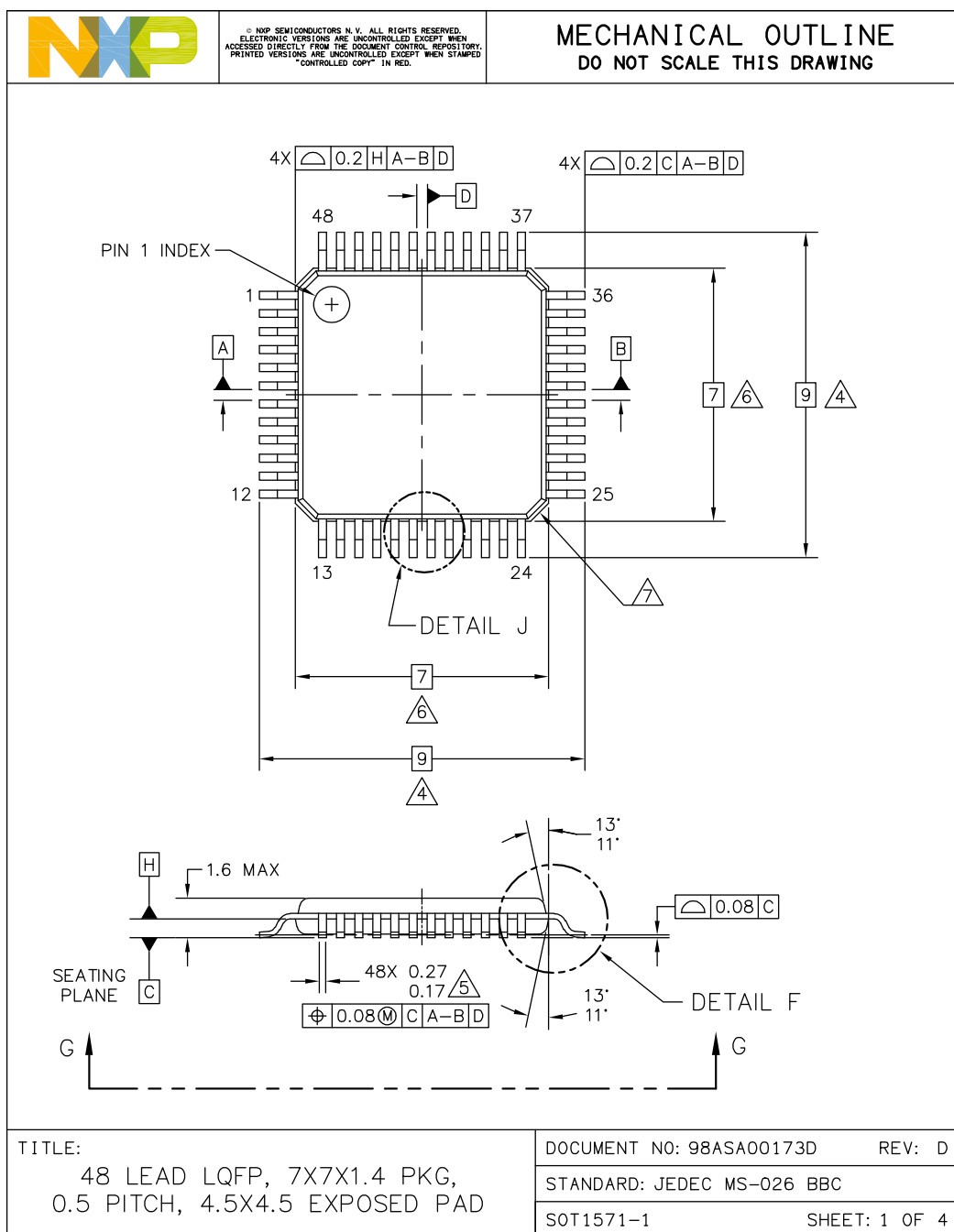
## 9 Packaging

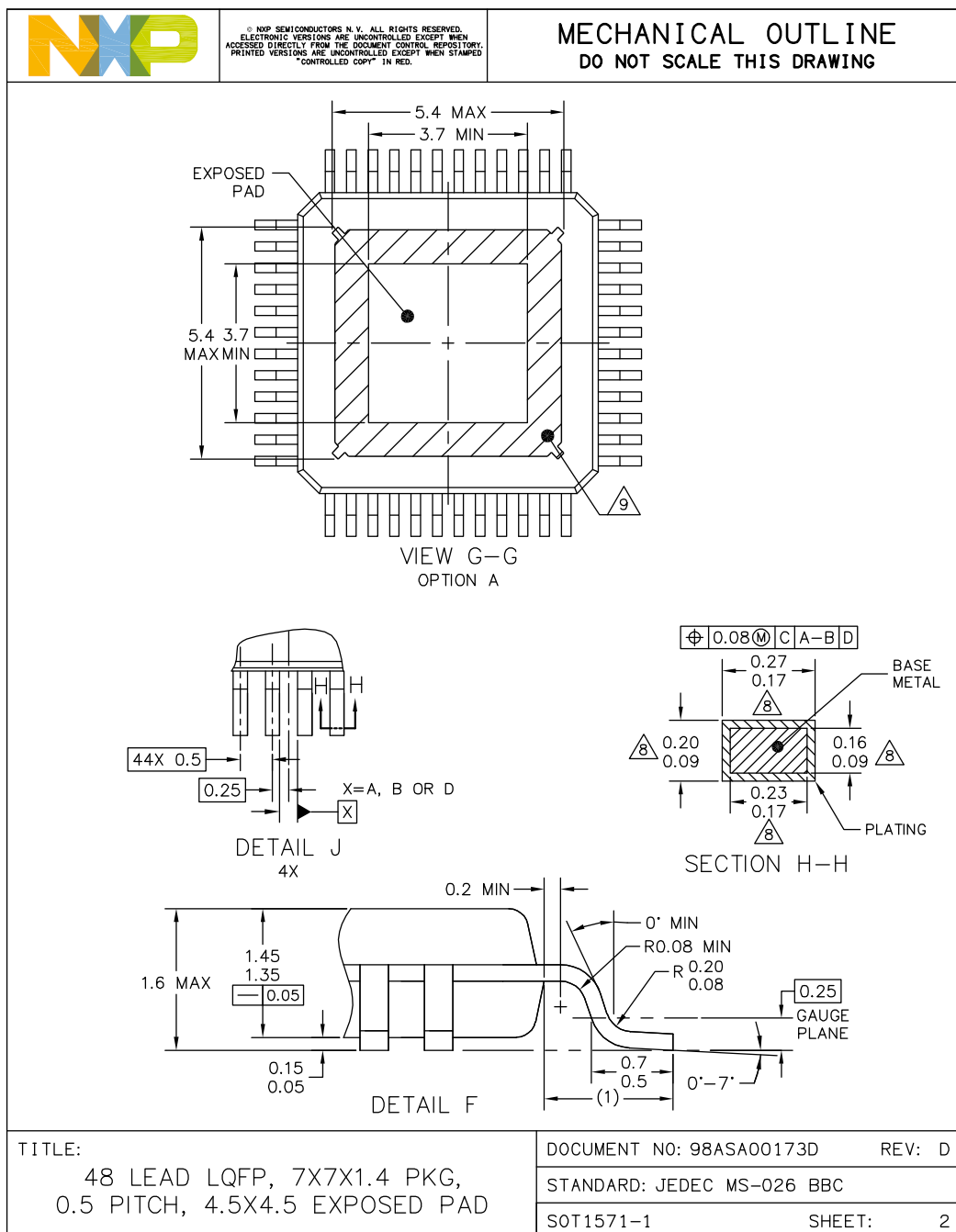
### 9.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to [www.nxp.com](http://www.nxp.com) and perform a keyword search for the drawing's document number.

Table 5. Package mechanical dimensions

| Package                                                                            | Suffix | Package outline drawing number |
|------------------------------------------------------------------------------------|--------|--------------------------------|
| 7.0 × 7.0, 48-Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad | AE     | 98ASA00173D                    |





|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |  |                                                                                                                                                                                                                                                                    |  |                                                                    |  |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--------------------------------------------------------------------|--|
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |  | <div>© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED.<br/>ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN<br/>ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY.<br/>PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED<br/>"CONTROLLED COPY" IN RED.</div> |  | <div>MECHANICAL OUTLINE</div> <div>DO NOT SCALE THIS DRAWING</div> |  |
| <div>NOTES:</div> <div><div>1.</div><div>DIMENSIONS ARE IN MILLIMETERS.</div></div> <div><div>2.</div><div>DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.</div></div> <div><div>3.</div><div>DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.</div></div> <div><div>4.</div><div>DIMENSION TO BE DETERMINED AT SEATING PLANE C.</div></div> <div><div>5.</div><div>THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.</div></div> <div><div>6.</div><div>THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.</div></div> <div><div>7.</div><div>EXACT SHAPE OF EACH CORNER IS OPTIONAL.</div></div> <div><div>8.</div><div>THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.</div></div> <div><div>9.</div><div>HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.</div></div> |  |                                                                                                                                                                                                                                                                    |  |                                                                    |  |
| <div>TITLE:</div> <div>48 LEAD LQFP, 7X7X1.4 PKG,<br/>0.5 PITCH, 4.5X4.5 EXPOSED PAD</div>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |  | <div>DOCUMENT NO: 98ASA00173D</div> <div>REV: D</div>                                                                                                                                                                                                              |  |                                                                    |  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |  | <div>STANDARD: JEDEC MS-026 BBC</div>                                                                                                                                                                                                                              |  |                                                                    |  |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |  | <div>SOT1571-1</div> <div>SHEET: 3</div>                                                                                                                                                                                                                           |  |                                                                    |  |

## 10 References

The following are URLs where you can obtain information on related NXP products and application solutions.

| NXP.com support pages                                        | Description                                                                    | URL                                                                                                                                                                                                         |
|--------------------------------------------------------------|--------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AN5238                                                       | Hardware design and product guidelines                                         | <a href="http://www.nxp.com/AN5238-DOWNLOAD">http://www.nxp.com/AN5238-DOWNLOAD</a>                                                                                                                         |
| AN4388                                                       | Quad flat package (QFP)                                                        | <a href="http://www.nxp.com/files/analog/doc/app_note/AN4388.pdf">http://www.nxp.com/files/analog/doc/app_note/AN4388.pdf</a>                                                                               |
| Power dissipation tool (Excel file)                          |                                                                                | <a href="http://www.nxp.com/files/analog/software_tools/FS6500-FS4500-power-dissipation-calculator.xlsx">http://www.nxp.com/files/analog/software_tools/FS6500-FS4500-power-dissipation-calculator.xlsx</a> |
| V <sub>CORE</sub> compensation network simulation tool (CNC) |                                                                                | Upon demand                                                                                                                                                                                                 |
| FMEDA                                                        | 35FS6500/35FS4500 FMEDA                                                        | Upon demand                                                                                                                                                                                                 |
| 35FS4500-35FS6500SMUG                                        | 35FS4500/35FS6500 Safety Manual – user guide                                   | <a href="https://www.nxp.com/webapp/Download?colCode=35FS4500-35FS6500SMUG">https://www.nxp.com/webapp/Download?colCode=35FS4500-35FS6500SMUG</a>                                                           |
| FS6500-FS4500                                                | Power System Basis Chip with CAN Flexible Data and LIN Transceivers data sheet | <a href="https://www.nxp.com/webapp/Download?colCode=FS6500-FS4500">https://www.nxp.com/webapp/Download?colCode=FS6500-FS4500</a>                                                                           |
| KITFS4503CAEEVM                                              | FS4500 evaluation board with FS1B                                              | <a href="http://www.nxp.com/KITFS4503CAEEVM">http://www.nxp.com/KITFS4503CAEEVM</a>                                                                                                                         |
| KITFS6523CAEEVM                                              | FS6500 evaluation board with FS1B                                              | <a href="http://www.nxp.com/KITFS6523CAEEVM">http://www.nxp.com/KITFS6523CAEEVM</a>                                                                                                                         |
| 35FS4500 product summary page                                |                                                                                | <a href="http://www.nxp.com/FS4500">http://www.nxp.com/FS4500</a>                                                                                                                                           |
| 35FS6500 product summary page                                |                                                                                | <a href="http://www.nxp.com/FS6500">http://www.nxp.com/FS6500</a>                                                                                                                                           |
| Analog power management home page                            |                                                                                | <a href="http://www.nxp.com/products/power-management">http://www.nxp.com/products/power-management</a>                                                                                                     |

## 11 Revision history

Table 6. Revision history

| Document ID                | Release date | Data sheet status               | Change notice | Supersedes |
|----------------------------|--------------|---------------------------------|---------------|------------|
| 35FS4500-35FS6500SDS v.1.0 | 20171215     | Data sheet: advance information | —             | —          |

## 12 Legal information

### 12.1 Data sheet status

| Document status <sup>[1][2]</sup>       | Product status <sup>[3]</sup> | Definition                                                                                                                                                                                           |
|-----------------------------------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [short] Data sheet: product preview     | Development                   | This document contains certain information on a product under development. NXP reserves the right to change or discontinue this product without notice.                                              |
| [short] Data sheet: advance information | Qualification                 | This document contains information on a new product. Specifications and information herein are subject to change without notice.                                                                     |
| [short] Data sheet: technical data      | Production                    | This document contains the product specification. NXP Semiconductors reserves the right to change the detail specifications as may be required to permit improvements in the design of its products. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 12.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a technical data data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the technical data data sheet.

### 12.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without

limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**Suitability for use in automotive applications** — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**NXP** — is a trademark of NXP B.V.

**SafeAssure** — is a trademark of NXP B.V.

**SMARTMOS** — is a trademark of NXP B.V.

Tables

|         |                                        |   |         |                                     |    |
|---------|----------------------------------------|---|---------|-------------------------------------|----|
| Tab. 1. | Part number breakdown .....            | 3 | Tab. 4. | Maximum ratings .....               | 10 |
| Tab. 2. | Orderable part variations .....        | 3 | Tab. 5. | Package mechanical dimensions ..... | 12 |
| Tab. 3. | 35FS4500/35FS6500 pin definition ..... | 7 | Tab. 6. | Revision history .....              | 15 |

Figures

|         |                                                                                     |   |         |                                                              |   |
|---------|-------------------------------------------------------------------------------------|---|---------|--------------------------------------------------------------|---|
| Fig. 1. | 35FS6500C simplified application diagram -<br>buck boost configuration - FS1B ..... | 2 | Fig. 3. | 35FS4500/35FS6500 simplified internal<br>block diagram ..... | 5 |
| Fig. 2. | 35FS4500C simplified application diagram -<br>buck boost configuration - FS1B ..... | 2 | Fig. 4. | 35FS6500 pinout with CAN and FS1B .....                      | 6 |
|         |                                                                                     |   | Fig. 5. | 35FS6500 pinout without CAN .....                            | 6 |
|         |                                                                                     |   | Fig. 6. | 35FS4500 pinout with CAN and FS1B .....                      | 7 |

## Contents

---

|           |                                             |           |
|-----------|---------------------------------------------|-----------|
| <b>1</b>  | <b>General description .....</b>            | <b>1</b>  |
| <b>2</b>  | <b>Features .....</b>                       | <b>1</b>  |
| <b>3</b>  | <b>Applications .....</b>                   | <b>1</b>  |
| <b>4</b>  | <b>Simplified application diagram .....</b> | <b>2</b>  |
| <b>5</b>  | <b>Ordering information .....</b>           | <b>3</b>  |
| 5.1       | Part numbers definition .....               | 3         |
| 5.2       | Part numbers list .....                     | 3         |
| <b>6</b>  | <b>Block diagram .....</b>                  | <b>5</b>  |
| <b>7</b>  | <b>Pinning information .....</b>            | <b>6</b>  |
| 7.1       | Pinning .....                               | 6         |
| 7.2       | Pin description .....                       | 7         |
| <b>8</b>  | <b>Maximum ratings .....</b>                | <b>10</b> |
| <b>9</b>  | <b>Packaging .....</b>                      | <b>11</b> |
| 9.1       | Package mechanical dimensions .....         | 11        |
| <b>10</b> | <b>References .....</b>                     | <b>15</b> |
| <b>11</b> | <b>Revision history .....</b>               | <b>15</b> |
| <b>12</b> | <b>Legal information .....</b>              | <b>16</b> |

---

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

---

© NXP B.V. 2017.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 15 December 2017

Document Identifier: 35FS4500-35FS6500SDS

## Данный компонент на территории Российской Федерации

**Вы можете приобрести в компании MosChip.**

Для оперативного оформления запроса Вам необходимо перейти по данной ссылке:

<http://moschip.ru/get-element>

Вы можете разместить у нас заказ для любого Вашего проекта, будь то серийное производство или разработка единичного прибора.

В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

На всех этапах разработки и производства наши партнеры могут получить квалифицированную поддержку опытных инженеров.

Система менеджмента качества компании отвечает требованиям в соответствии с ГОСТ Р ИСО 9001, ГОСТ РВ 0015-002 и ЭС РД 009

### Офис по работе с юридическими лицами:

105318, г.Москва, ул.Щербаковская д.3, офис 1107, 1118, ДЦ «Щербаковский»

Телефон: +7 495 668-12-70 (многоканальный)

Факс: +7 495 668-12-70 (доб.304)

E-mail: [info@moschip.ru](mailto:info@moschip.ru)

Skype отдела продаж:

moschip.ru

moschip.ru\_4

moschip.ru\_6

moschip.ru\_9