

Description

The 74AHC125 provides provides four independent buffer gates with 3-state outputs. Each buffer has a separate enable pin that when driven with a high logic level places the corresponding output in the high impedance state. The device is designed for operation with a power supply range of 2.0V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment.

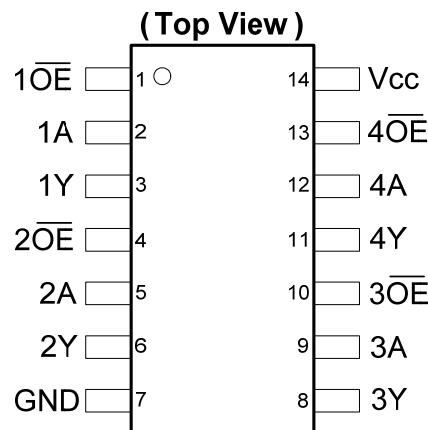
Features

- Wide Supply Voltage Range from 2.0V to 5.5V
- Outputs Sink or Source 8mA at $V_{CC} = 4.5V$
- CMOS Low Power Consumption
- Schmitt Trigger Action at All Inputs
- Inputs can be driven by 3.3 V or 5.5V allowing for voltage translation applications.
- ESD Protection Exceeds JESD 22
 - 200-V Machine Model (A115-A)
 - 2000-V Human Body Model (A114-A)
 - Exceeds 1000-V Charged Device Model (C101C)
- Latch-Up Exceeds 250mA per JESD 78, Class II
- Range of Package Options SO-14 and TSSOP-14
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Assignments



SO-14 / TSSOP-14

Applications

- General Purpose Logic
- Wide array of products such as:
 - PCs, Networking, Notebooks, Netbooks
 - Computer Peripherals, Hard Drives, CD/DVD ROM
 - TV, DVD, DVR, Set Top Box

[Click here for ordering information, located at the end of datasheet](#)

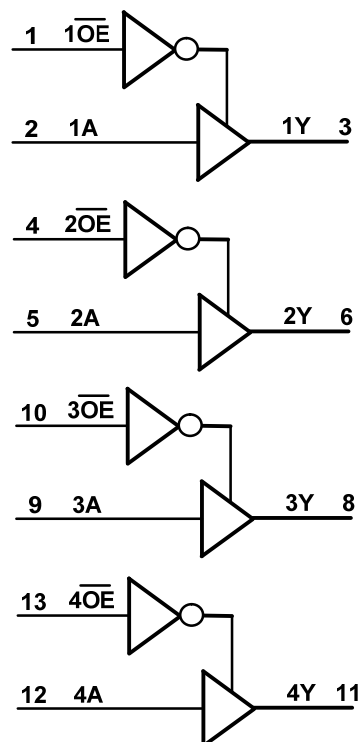
Pin Descriptions

Pin Number	Pin Name	Function
1	$\overline{1OE}$	Data Enable Input (active low)
2	1A	Data Input
3	1Y	Data Output
4	$\overline{2OE}$	Data Enable Input (active low)
5	2A	Data Input
6	2Y	Data Output
7	GND	Ground
8	3Y	Data Output
9	3A	Data Input
10	$\overline{3OE}$	Data Enable Input (active low)
11	4Y	Data Output
12	4A	Data Input
13	$\overline{4OE}$	Data Enable Input (active low)
14	V _{CC}	Supply Voltage

Function Table

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

Logic Diagram



Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD CDM	Charged Device Model ESD Protection	1	KV
ESD MM	Machine Model ESD Protection	200	V
V _{CC}	Supply Voltage Range	-0.5 to +7.0	V
V _I	Input Voltage Range	-0.5 to +7.0	V
I _{IK}	Input Clamp Current V _I < -0.5V	-20	mA
I _{OK}	Output Clamp Current V _O < -0.5V	-20	mA
I _{OK}	Output Clamp Current V _O > V _{CC} + 0.5V	25	mA
I _O	Continuous Output Current -0.5V < V _O < V _{CC} + 0.5V	+/- 25	mA
I _{CC}	Continuous Current Through V _{CC}	75	mA
I _{GND}	Continuous Current Through GND	-75	mA
T _J	Operating Junction Temperature	-40 to +150	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _{TOT}	Total Power Dissipation	500	mW

Note: 4. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 5) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage		2.0	5.5	V
V _I	Input Voltage		0	5.5	V
V _O	Output Voltage		0	V _{CC}	V
Δt/ΔV	Input Transition Rise or Fall Rate	V _{CC} = 3.0V to 3.6V		100	ns/V
		V _{CC} = 4.5V to 5.5V		20	
T _A	Operating Free-Air Temperature		-40	+125	°C

Note: 5. Unused inputs should be held at V_{CC} or Ground.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	V _{CC}	T _A = -40°C to +85°C		T _A = -40°C to +125°C		Unit
				Min	Max	Min	Max	
V _{IH}	High-Level Input Voltage		2.0V	1.5		1.5		V
			3.0V	2.1		2.1		
			5.5V	3.85		3.85		
V _{IL}	Low-Level Input Voltage		2.0V		0.5		0.5	V
			3.0V		0.9		0.9	
			5.5V		1.65		1.65	
V _{OH}	High-Level Output Voltage	I _{OH} = -50μA	2.0V	1.9		1.9		V
		I _{OH} = -50μA	3.0V	2.9		2.9		
		I _{OH} = -50μA	4.5V	4.4		4.4		
		I _{OH} = -4mA	3.0V	2.48		2.40		
		I _{OH} = -8mA	4.5V	3.80		3.70		
V _{OL}	Low-Level Output Voltage	I _{OL} = 50μA	2.0V		0.1		0.1	V
		I _{OL} = 50μA	3.0V		0.1		0.1	
		I _{OL} = 50μA	4.5V		0.1		0.1	
		I _{OL} = 4mA	3.0V		0.44		0.55	
		I _{OL} = 8mA	4.5V		0.44		0.55	
I _{oz}	Z State Leakage Current	V _O = 0 to 5.5V V _I = GND or 5.5V	5.5V		±2.5		±10	μA
I _I	Input Current	V _I = GND to 5.5V	3.6V		±1		±2	μA
I _{CC}	Supply Current	V _I = GND or V _{CC} , I _O = 0	3.6V		20		40	μA

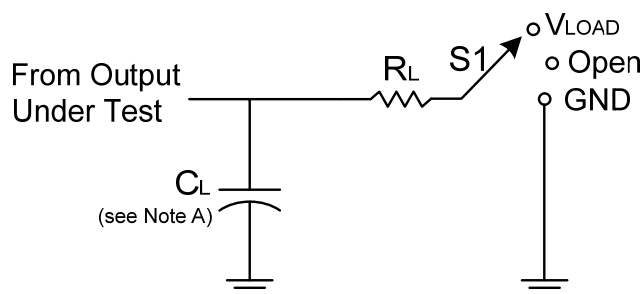
Operating Characteristics

Parameter		Test Conditions	V _{CC} = 2.0V	V _{CC} = 3.3V	V _{CC} = 5V	Unit
			Typ	Typ	Typ	
C _{pd}	Power Dissipation Capacitance per Gate	f = 1MHz	10.1	13.1	15	pF
C _i	Input Capacitance	V _i = V _{CC} – or GND	4.0	4.0	4.0	pF

Switching Characteristics

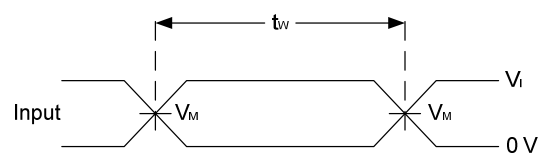
Symbol	Parameter	Test Conditions	V _{CC}	T _A = +25°C			-40°C to +85°C		-40°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t _{PD}	Propagation Delay A _N to Y _N	Figure 1 C _L = 15pF	3.0V to 3.6V	0.5	4.4	8.0	0.5	9.5	0.5	11.5	ns
			4.5V to 5.5V	0.5	3.0	5.5	0.5	6.5	0.5	7.0	
		Figure 1 C _L = 50pF	3.0V to 3.6V	0.5	6.2	11.5	0.5	13.0	0.5	14.5	
			4.5V to 5.5 V	0.5	4.3	7.5	0.5	8.5	0.5	9.5	
t _{EN}	Enable Time OE _N to Y _N	Figure 1 C _L = 15pF	3.0V to 3.6V	0.5	4.7	8.0	0.5	9.5	0.5	11.5	ns
			4.5V to 5.5V	0.5	3.3	5.1	0.5	6.0	0.5	7.5	
		Figure 1 C _L = 50pF	3.0V to 3.6V	0.5	6.8	11.5	0.5	13.0	0.5	14.5	
			4.5V to 5.5V	0.5	4.7	7.1	0.5	8.0	0.5	9.0	
t _{DIS}	Disable Time OE _N to Y _N	Figure 1 C _L = 15pF	3.0V to 3.6V	0.5	6.7	9.7	0.5	11.5	0.5	12.5	ns
			4.5V to 5.5V	0.5	4.8	6.8	0.5	8.0	0.5	8.5	
		Figure 1 C _L = 50pF	3.0 V to 3.6V	0.5	9.6	13.2	0.5	15.0	0.5	16.5	
			4.5V to 5.5V	0.5	6.8	8.8	0.5	10.0	0.5	11.0	

Parameter Measurement Information

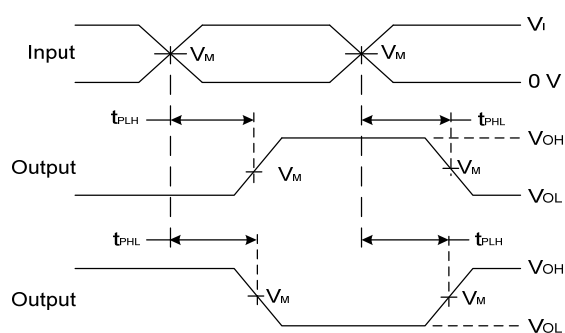


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	Vload
t_{PHZ}/t_{PZH}	GND

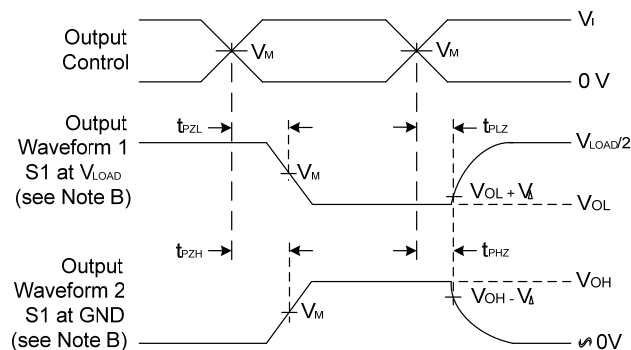
Vcc	Inputs		VM	VLOAD	CL	RL	VΔ
	VI	tr/td					
3.3V±0.3V	3 V	≤3ns	Vcc/2	Vcc	15,50 pF	1KΩ	0.3 V
5V±0.5V	Vcc	≤3ns	Vcc/2	Vcc	15,50 pF	1KΩ	0.3 V



Voltage Waveform Pulse Duration



**Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs**

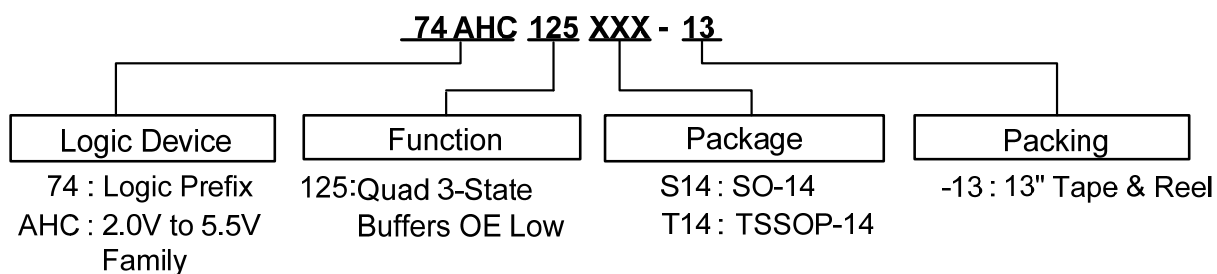


**Voltage Waveform Enable and Disable Times
Low and High Level Enabling**

Figure 1. Load Circuit and Voltage Waveforms

- Notes:
- A. Includes test lead and test apparatus capacitance.
 - B. All pulses are supplied at pulse repetition rate ≤ 1 MHz.
 - C. Inputs are measured separately one transition per measurement.
 - D. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - E. t_{PZL} and t_{PZH} are the same as t_{EN0} .
 - F. t_{PLH} and t_{PHL} are the same as t_{PD} .

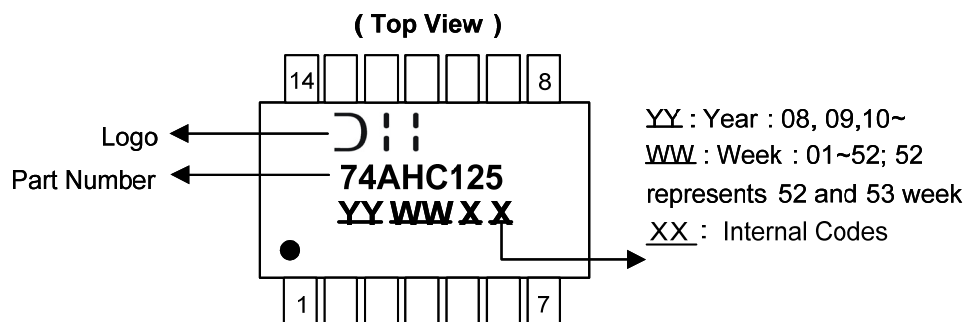
Ordering Information



Device	Package Code	Packaging	7" Tape and Reel	
			Quantity	Part Number Suffix
74AHC125S14-13	S14	SO-14	2500/Tape & Reel	-13
74AHC125T14-13	T14	TSSOP-14	2500/Tape & Reel	-13

Marking Information

(1) SO-14, TSSOP-14

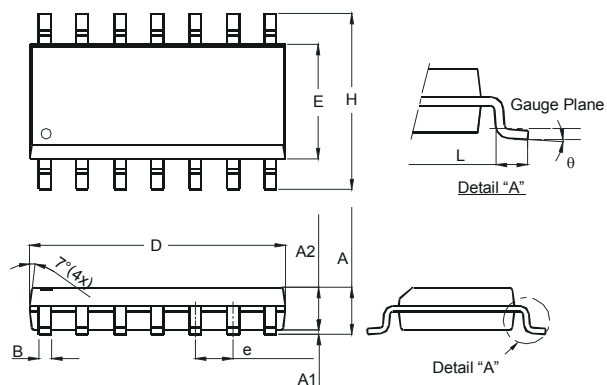


Part Number	Package
74AHC125S14	SO-14
74AHC125T14	TSSOP-14

Package Outline Dimensions (All dimensions in mm.)

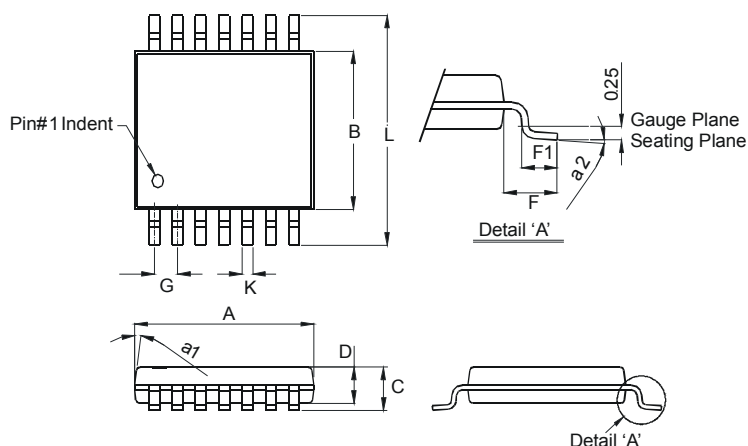
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

Package Type: SO-14



SO-14		
Dim	Min	Max
A	1.47	1.73
A1	0.10	0.25
A2	1.45 Typ	
B	0.33	0.51
D	8.53	8.74
E	3.80	3.99
e	1.27 Typ	
H	5.80	6.20
L	0.38	1.27
θ	0°	8°
All Dimensions in mm		

Package Type: TSSOP-14

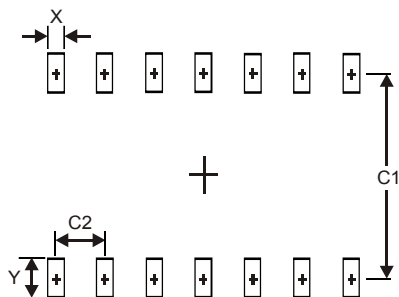


TSSOP-14		
Dim	Min	Max
a1	7° (4X)	
a2	0°	8°
A	4.9	5.10
B	4.30	4.50
C	—	1.2
D	0.8	1.05
F	1.00 Typ	
F1	0.45	0.75
G	0.65 Typ	
K	0.19	0.30
L	6.40 Typ	
All Dimensions in mm		

Suggested Pad Layout

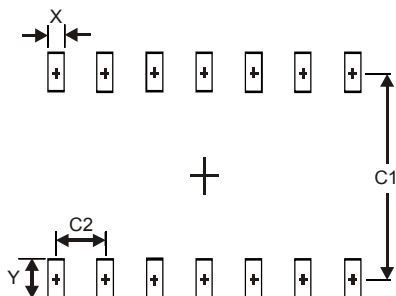
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

Package Type: SO-14



Dimensions	Value (in mm)
X	0.60
Y	1.50
C1	5.4
C2	1.27

Package Type: TSSOP-14



Dimensions	Value (in mm)
X	0.45
Y	1.45
C1	5.9
C2	0.65

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