# PIC12F519
# Data Sheet

## 8-Pin, 8-Bit Flash Microcontrollers

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# PIC12F519

## 8-Pin, 8-Bit Flash Microcontroller

### High-Performance RISC CPU:

- Only 33 Single-Word Instructions
- All Single-Cycle Instructions except for Program Branches which are Two-Cycle
- Two-Level Deep Hardware Stack
- Direct, Indirect and Relative Addressing modes for Data and Instructions
- Operating Speed:
  - DC – 8 MHz Oscillator
  - DC – 500 ns instruction cycle
- On-chip Flash Program Memory
  - 1024 x 12
- General Purpose Registers (SRAM)
  - 41 x 8
- Flash Data Memory
  - 64 x 8

### Special Microcontroller Features:

- 8 MHz Precision Internal Oscillator
  - Factory calibrated to ±1%
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Debugging (ICD) Support
- Power-on Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with Dedicated On-Chip RC Oscillator for Reliable Operation
- Programmable Code Protection
- Multiplexed $\overline{\text{MCLR}}$ Input Pin
- Internal Weak Pull-ups on I/O Pins
- Power-Saving Sleep mode
- Wake-up from Sleep on Pin Change
- Selectable Oscillator Options:
  - INTRC: 4 MHz or 8 MHz precision Internal RC oscillator
  - EXTRC: External low-cost RC oscillator
  - XT: Standard crystal/resonator
  - LP: Power-saving, low-frequency crystal

### Low-Power Features/CMOS Technology:

- Standby Current:
  - 100 nA @ 2.0V, typical
- Operating Current:
  - 11 μA @ 32 kHz, 2.0V, typical
  - 175 μA @ 4 MHz, 2.0V, typical
- Watchdog Timer Current:
  - 1 μA @ 2.0V, typical
  - 7 μA @ 5.0V, typical
- High Endurance Program and Flash Data Memory Cells
  - 100,000 write Program Memory endurance
  - 1,000,000 write Flash Data Memory endurance
  - Program and Flash Data retention: >40 years
- Fully Static Design
- Wide Operating Voltage Range: 2.0V to 5.5V
  - Wide temperature range
  - Industrial: -40°C to +85°C
  - Extended: -40°C to +125°C

### Peripheral Features:

- 6 I/O Pins
  - 5 I/O pins with individual direction control
  - 1 input-only pin
  - High current sink/source for direct LED drive
- 8-bit Real-Time Clock/Counter (TMR0) with 8-bit Programmable Prescaler.

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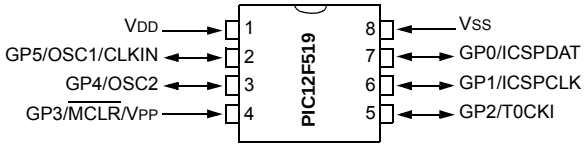
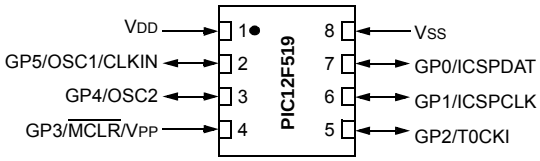
**FIGURE 1: PIC12F519 8-PIN PDIP, SOIC, MSOP, 2X3 DFN DIAGRAM**

**PDIP, SOIC, MSOP**




**DFN**




| Device | Program Memory | Data Memory | | I/O | Timers 8-bit |
|---|---|---|---|---|---|
| | Flash (words) | SRAM (bytes) | Flash (bytes) | | |
| PIC12F519 | 1024 | 41 | 64 | 6 | 1 |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## 1.0 GENERAL DESCRIPTION

The PIC12F519 device from Microchip Technology is low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontrollers. They employ a RISC architecture with only 33 single-word/single-cycle instructions. All instructions are single cycle except for program branches, which take two cycles. The PIC12F519 device delivers performance an order of magnitude higher than their competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy to remember instruction set reduces development time significantly.

The PIC12F519 product is equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. There are four oscillator configurations to choose from including INTRC Internal Oscillator mode and the power-saving LP (Low-power) Oscillator mode. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC12F519 device is available in the cost-effective Flash programmable version, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC12F519 product is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full featured programmer. All the tools are supported on PC and compatible machines.

### 1.1 Applications

The PIC12F519 device fits in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers perfect for applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC12F519 device very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

**TABLE 1-1: FEATURES AND MEMORY OF PIC12F519**

| | | PIC12F519 |
|---|---|---|
| Clock | Maximum Frequency of Operation (MHz) | 8 |
| Memory | Flash Program Memory | 1024 |
| | SRAM Data Memory (bytes) | 41 |
| | Flash Data Memory (bytes) | 64 |
| Peripherals | Timer Module(s) | TMR0 |
| | Wake-up from Sleep on Pin Change | Yes |
| Features | I/O Pins | 5 |
| | Input Pins | 1 |
| | Internal Pull-ups | Yes |
| | In-Circuit Serial Programming™ | Yes |
| | Number of Instructions | 33 |
| | Packages | 8-pin PDIP, SOIC, MSOP, 2X3 DFN |

The PIC12F519 device has Power-on Reset, selectable Watchdog Timer, selectable code-protect, high I/O current capability and precision internal oscillator.
The PIC12F519 device uses serial programming with data pin GP0 and clock pin GP1.

**NOTES:**


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## 2.0 PIC12F519 DEVICE VARIETIES

When placing orders, please use the PIC12F519 Product Identification System at the back of this data sheet to specify the correct part number. A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section.

### 2.1 Quick Turn Programming (QTP) Devices

Microchip offers a QTP programming service for factory production orders. This service is made available for users who choose not to program medium-to-high quantity units and whose code patterns have stabilized. The devices are identical to the Flash devices but with all Flash locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

### 2.2 Serialized Quick Turn Programming$^{SM}$ (SQTP$^{SM}$) Devices

Microchip offers a unique programming service, where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry code, password or ID number.

**NOTES:**


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## 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC12F519 device can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC12F519 device uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (500 ns @ 8 MHz, 1 μs @ 4 MHz) except for program branches.

Table 3-1 below lists memory supported by the PIC12F519 device.

**TABLE 3-1: PIC12F519 MEMORY**

| Device | Program Memory | Data Memory | |
|---|---|---|---|
| | Flash (words) | SRAM (bytes) | Flash Data (bytes) |
| PIC12F519 | 1024 | 41 | 64 |

The PIC12F519 device can directly or indirectly address its register files and data memory. All Special Function Registers (SFR), including the PC, are mapped in the data memory. The PIC12F519 device has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any addressing mode. This symmetrical nature and lack of “special optimal situations” make programming with the PIC12F519 device simple, yet efficient. In addition, the learning curve is reduced significantly.

The PIC12F519 device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two’s complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-2.

**FIGURE 3-1: PIC12F519 ARCHITECTURAL BLOCK DIAGRAM**

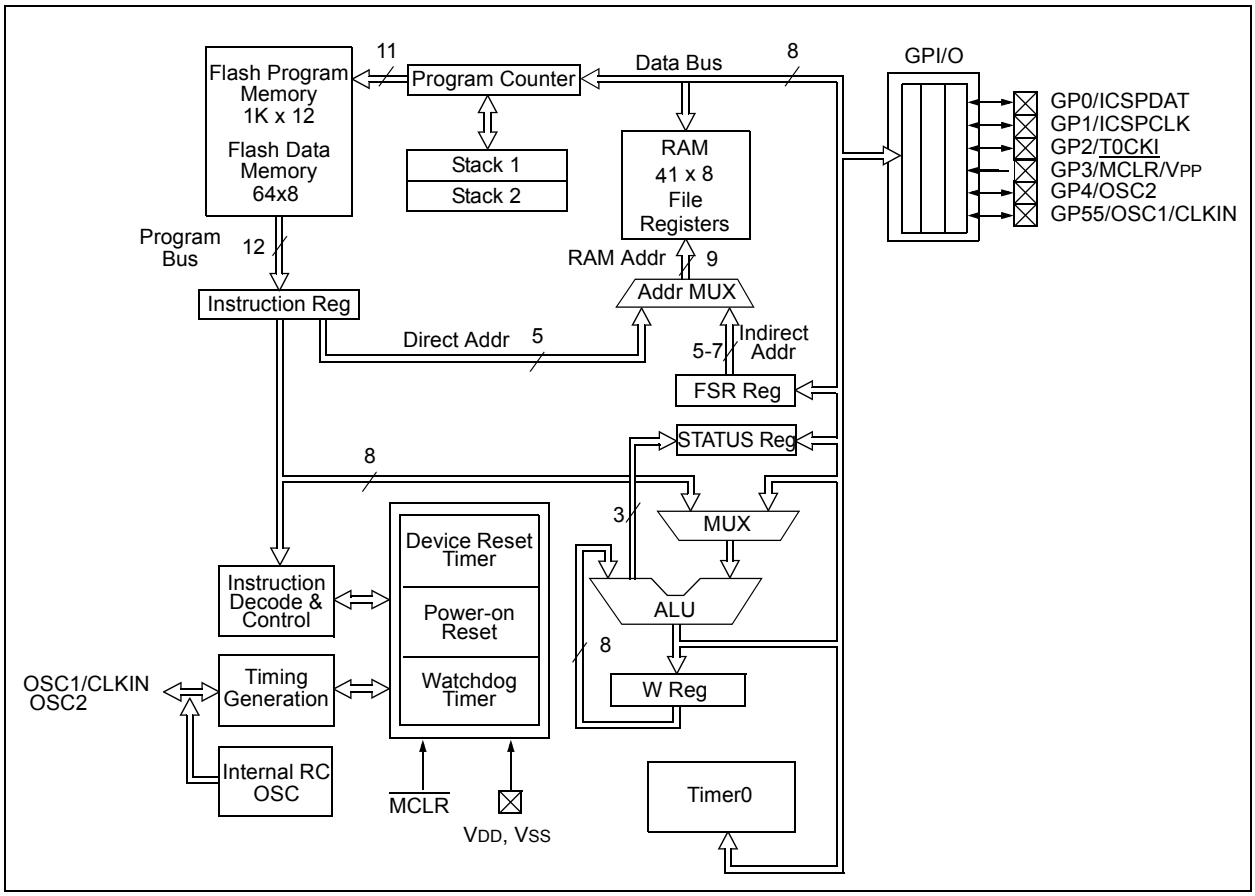



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**TABLE 3-2: PIC12F519 PINOUT DESCRIPTION**

| Name | Function | Type | Input Type | Output Type | Description |
|---|---|---|---|---|---|
| GP0/ICSPDAT | GP0 | I/O | TTL | CMOS | Bidirectional I/O port with weak pull-up |
| | ICSPDAT | I/O | ST | CMOS | ICSP™ mode Schmitt Trigger |
| GP1/ICSPCLK | GP1 | I/O | TTL | CMOS | Bidirectional I/O port with weak pull-up |
| | ICSPCLK | I | ST | — | ICSP™ mode Schmitt Trigger |
| GP2/T0CKI | GP2 | I/O | TTL | CMOS | Bidirectional I/O port |
| | T0CKI | I | ST | — | Timer0 clock input |
| GP3/$\overline{MCLR}$/$V_{PP}$ | GP3 | I | TTL | — | Standard TTL input with weak pull-up |
| | $\overline{MCLR}$ | I | ST | — | $\overline{MCLR}$ input (Weak pull-up always enabled in this mode) |
| | $V_{PP}$ | I | High Voltage | — | Test mode high voltage pin |
| GP4/OSC2 | GP4 | I/O | TTL | CMOS | Bidirectional I/O port |
| | OSC2 | O | — | XTAL | XTAL oscillator output pin |
| GP5/OSC1/ CLKIN | GP5 | I/O | TTL | CMOS | Bidirectional I/O port |
| | OSC1 | I | XTAL | — | XTAL oscillator input pin |
| | CLKIN | I | ST | — | EXTRC Schmitt Trigger input |
| $V_{DD}$ | $V_{DD}$ | P | — | — | Positive supply for logic and I/O pins |
| $V_{SS}$ | $V_{SS}$ | P | — | — | Ground reference for logic and I/O pins |

**Legend:** I = Input, O = Output, I/O = Input/Output, P = Power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input, AN = Analog Voltage

## 3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the PC is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

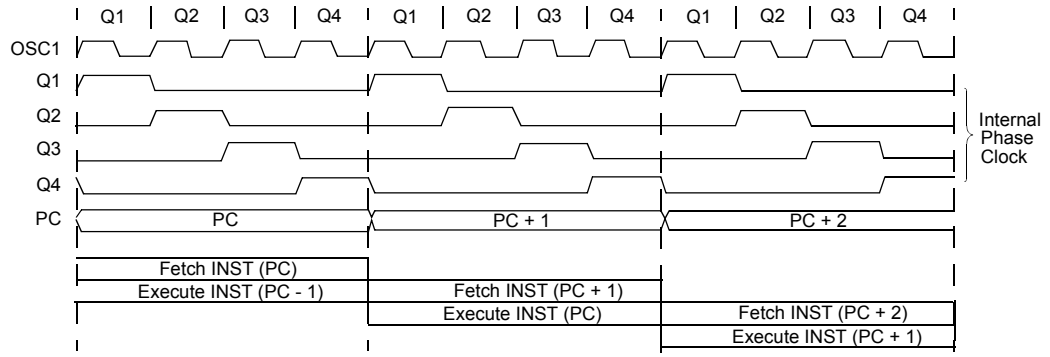
## 3.2 Instruction Flow/Pipelining

An instruction cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the PC to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the PC incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

**FIGURE 3-2: CLOCK/INSTRUCTION CYCLE**




**EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW**

```
1. MOVLW 03H
2. MOVWF GPIO
3. CALL  SUB_1
4. BSF  GPIO, 1
```

| | | | | | |
|---|---|---|---|---|---|
| Fetch 1 | Execute 1 | | | | |
| | Fetch 2 | Execute 2 | | | |
| | | Fetch 3 | Execute 3 | | |
| | | | Fetch 4 | Flush | |
| | | | | Fetch SUB_1 | Execute SUB_1 |

All instructions are single cycle, except for any program branches. These take two cycles, since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.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## 4.0 MEMORY ORGANIZATION

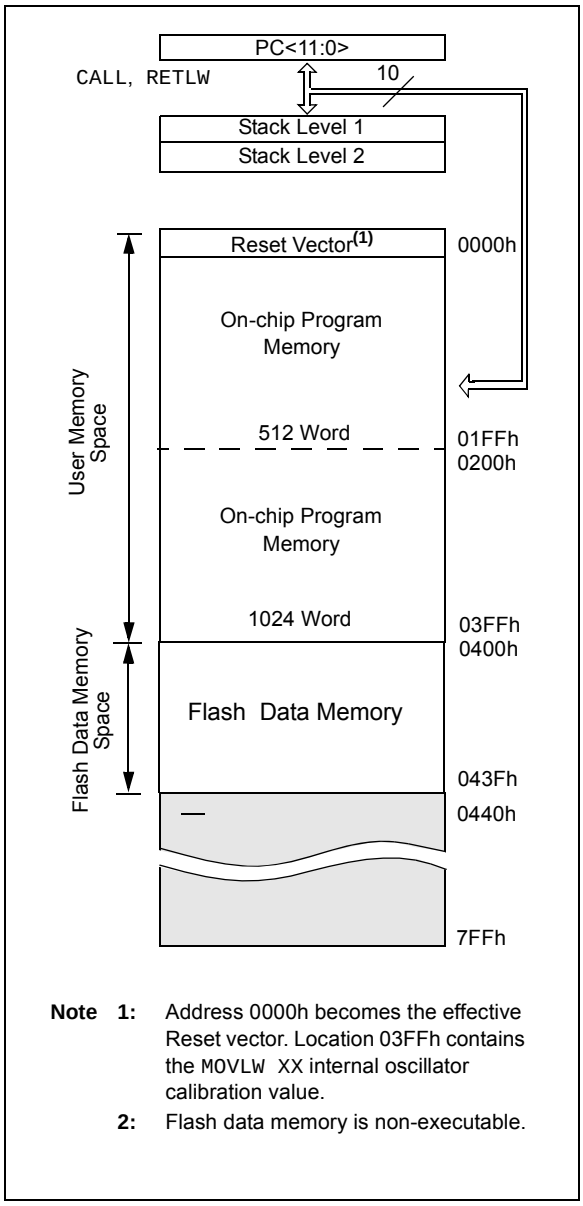
The PIC12F519 memory is organized into program memory and data memory (SRAM). The self-writable portion of the program memory called Flash data memory, is located at addresses 400h-43Fh. As the device has more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using STATUS register bit, PA0. For the PIC12F519, with data memory register files of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Select Register (FSR).

### 4.1 Program Memory Organization for the PIC12F519

The PIC12F519 device has an 11-bit Program Counter (PC) capable of addressing a 2K x 12 program memory space.

Only the first 1K x 12 (0000h-03FFh) are physically implemented (see Figure 4-1). Accessing a location above these boundaries will cause a wrap-around within the 1K x 12 space. The effective Reset vector is a 0000h (see Figure 4-1). Location 03FFh contains the internal clock oscillator calibration value. This value should never be overwritten.

**FIGURE 4-1: MEMORY MAP**




**Note 1:** Address 0000h becomes the effective Reset vector. Location 03FFh contains the MOVLW XX internal oscillator calibration value.

**2:** Flash data memory is non-executable.

## 4.2 Data Memory (SRAM and FSRs)

Data memory is composed of registers or bytes of SRAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers (SFR) and General Purpose Registers (GPR).

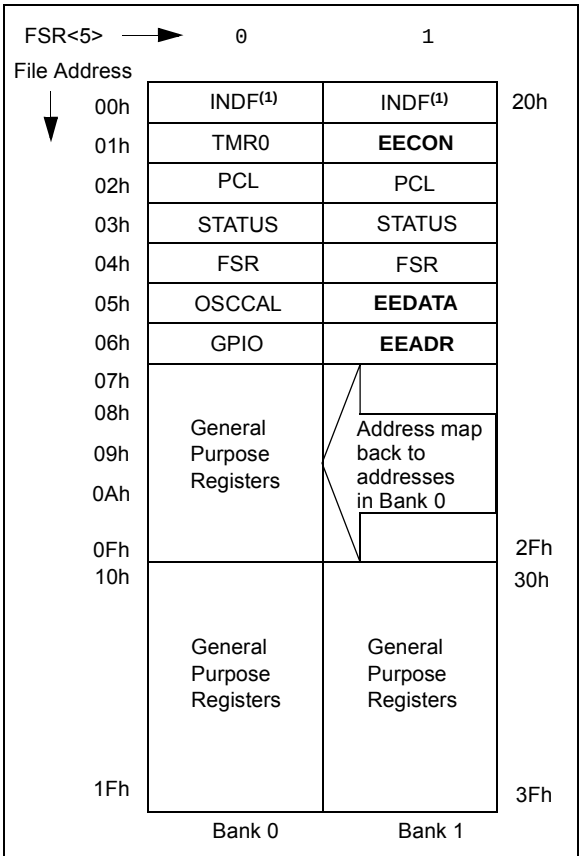
The Special Function Registers include the TMR0 register, the Program Counter Low (PCL), the STATUS register, the I/O register (port) and the File Select Register (FSR). In addition, the EECON, EEDATA and EEADR registers provide for interface with the Flash data memory.

The PIC12F519 register file is composed of 10 Special Function Registers and 41 General Purpose Registers.

### 4.2.1 GENERAL PURPOSE REGISTER FILE

The General Purpose Register file is accessed, either directly or indirectly, through the File Select Register (FSR). See **Section 4.8 "Indirect Data Addressing: INDF and FSR Registers"**.

**FIGURE 4-2: REGISTER FILE MAP**




**Note 1:** Not a physical register.

### 4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Function Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.


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**TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY**

| Addr | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset |
|---|---|---|---|---|---|---|---|---|---|---|
| N/A | TRISGPIO | — | — | TRISGPIO5 | TRISGPIO4 | TRISGPIO3 | TRISGPIO2 | TRISGPIO1 | TRISGPIO0 | --11 1111 |
| N/A | OPTION | Contains Control Bits to Configure Timer0 and Timer0/WDT Prescaler | | | | | | | | 1111 1111 |
| 00h | INDF | Uses Contents of FSR to Address Data Memory (not a physical register) | | | | | | | | xxxx xxxx |
| 01h | TMR0 | Timer0 Module Register | | | | | | | | xxxx xxxx |
| 02h(1) | PCL | Low Order 8 bits of PC | | | | | | | | 1111 1111 |
| 03h | STATUS | GPWUF | — | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0-01 1xxx |
| 04h | FSR | Indirect Data Memory Address Pointer | | | | | | | | 110x xxxx |
| 05h | OSCCAL | CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | — | 1111 111- |
| 06h | GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx |
| 21h | EECON | — | — | — | FREE | WRERR | WREN | WR | RD | ---0 x000 |
| 25h | EEDATA | EEDATA7 | EEDATA6 | EEDATA5 | EEDATA4 | EEDATA3 | EEDATA2 | EEDATA1 | EEDATA0 | xxxx xxxx |
| 26h | EEADR | — | — | EEADR5 | EEADR4 | EEADR3 | EEADR2 | EEADR1 | EEADR0 | --xx xxxx |

**Legend:** x = unknown, u = unchanged, – = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

**Note 1:** The upper byte of the Program Counter is not directly accessible. See **Section 4.6 "Program Counter"** for an explanation of how to access these bits.

## 4.3 STATUS register

This register contains the arithmetic status of the ALU, the Reset status and the page preselect bit.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS, will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u u1uu' (where u = unchanged).

Therefore, it is recommended that only BCF, BSF and MOVWF instructions be used to alter the STATUS register. These instructions do not affect the Z, DC or C bits from the STATUS register. For other instructions which do affect Status bits, see **Section 9.0 "Instruction Set Summary"**.

**REGISTER 4-1: STATUS: STATUS REGISTER**

| R/W-0 | U-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| GPWUF | — | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **GPWUF**: Wake-up From Sleep on Pin Change bit
1 = Reset due to wake-up from Sleep on pin change
0 = After power-up or other Reset

bit 6 **Unimplemented:** Read as '0'

bit 5 **PA0**: Program Page Preselect bit
1 = Page 1 (000h-1FFh)
0 = Page 0 (200h-3FFh)

bit 4 **$\overline{TO}$**: Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$**: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit carry/$\overline{\text{borrow}}$ bit (for ADDWF and SUBWF instructions)
ADDWF:
1 = A carry from the 4th low-order bit of the result occurred
0 = A carry from the 4th low-order bit of the result did not occur
SUBWF:
1 = A borrow from the 4th low-order bit of the result did not occur
0 = A borrow from the 4th low-order bit of the result occurred

bit 0 **C**: Carry/$\overline{\text{borrow}}$ bit (for ADDWF, SUBWF and RRF, RLF instructions)

| ADDWF: | SUBWF: | RRF or RLF: |
|---|---|---|
| 1 = A carry occurred | 1 = A borrow did not occur | Load bit with LSb or MSb, respectively |
| 0 = A carry did not occur | 0 = A borrow occurred | |


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## 4.4 OPTION Register

The OPTION register is a 8-bit wide, write-only register, which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the OPTION instruction, the contents of the W register will be transferred to the OPTION register. A Reset sets the OPTION<7:0> bits.

| **Note:** | If the T0SC bit is set to '1', it will override the TRIS function on the T0CKI pin. |
|---|---|

**REGISTER 4-2: OPTION: OPTION REGISTER**

| W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{GPWU}}$ | $\overline{\text{GPPU}}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | W = Writable bit | x = Bit is unknown |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |

bit 7 **$\overline{\text{GPWU}}$:** Enable Wake-up On Pin Change bit
1 = Disabled
0 = Enabled

bit 6 **$\overline{\text{GPPU}}$:** Enable Weak Pull-ups bit
1 = Disabled
0 = Enabled

bit 5 **T0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

| Bit Value | Timer0 Rate | WDT Rate |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

## 4.5 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the 8 MHz internal oscillator macro. It contains 7 bits of calibration that uses a two's complement scheme for controlling the oscillator speed. See Register 4-3 for details.

**REGISTER 4-3: OSCCAL: OSCILLATOR CALIBRATION REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | U-0 |
|---|---|---|---|---|---|---|---|
| CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-1 **CAL<6:0>**: Oscillator Calibration bits
0111111 = Maximum frequency
•
•
•
0000001
0000000 = Center frequency
1111111
•
•
•
1000000 =Minimum frequency

bit 0 **Unimplemented**: Read as '0'


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## 4.6 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one every instruction cycle, unless an instruction changes the PC.

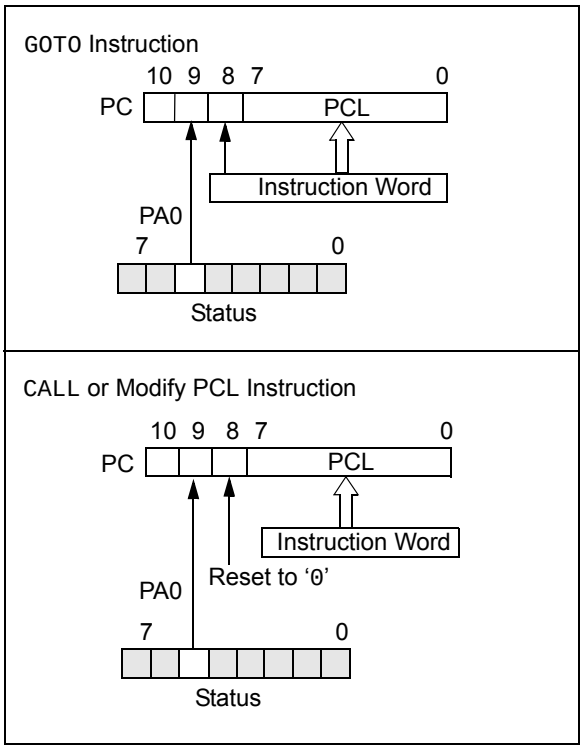
For a GOTO instruction, bits <8:0> of the PC are provided by the GOTO instruction word. The Program Counter (PCL) is mapped to PC<7:0>. Bit 5 of the STATUS register provides page information to bit 9 of the PC (Figure 4-3).

For a CALL instruction, or any instruction where the PCL is the destination, bits <7:0> of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-3).

Instructions where the PCL is the destination, or modify PCL instructions, include MOVWF PCL, ADDWF PCL and BSF PCL,5.

| **Note:** | Because PC<8> is cleared in the CALL instruction or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long). |
|---|---|

**FIGURE 4-3: LOADING OF PC BRANCH INSTRUCTIONS**




### 4.6.1 EFFECTS OF RESET

The PC is set upon a Reset, which means that the PC addresses the last location in the last page (i.e., the oscillator calibration instruction). After executing MOVLW XX, the PC will roll over to location 00h and begin executing user code.

The STATUS register page preselect bits are cleared upon a Reset, which means that page 0 is pre-selected.

Therefore, upon a Reset, a GOTO instruction will automatically cause the program to jump to page 0 until the value of the page bits is altered.

## 4.7 Stack

The PIC12F519 device has a two-deep, 12-bit wide hardware PUSH/POP stack.

A CALL instruction will PUSH the current value of Stack 1 into Stack 2 and then PUSH the current PC value, incremented by one, into Stack Level 1. If more than two sequential CALLs are executed, only the most recent two return addresses are stored.

A RETLW instruction will POP the contents of Stack Level 1 into the PC and then copy Stack Level 2 contents into Stack Level 1. If more than two sequential RETLWs are executed, the stack will be filled with the address previously stored in Stack Level 2. Note that the W register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

| **Note 1:** | There are no Status bits to indicate stack overflows or stack underflow conditions. |
|---|---|
| **2:** | There are no instruction mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL and RETLW instructions. |

## 4.8 Indirect Data Addressing: INDF and FSR Registers

The INDF register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register (FSR is a *pointer*). This is indirect addressing.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF register indirectly results in a no-operation (although Status bits may be affected).

The FSR is an 8-bit wide register. It is used in conjunction with the INDF Register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

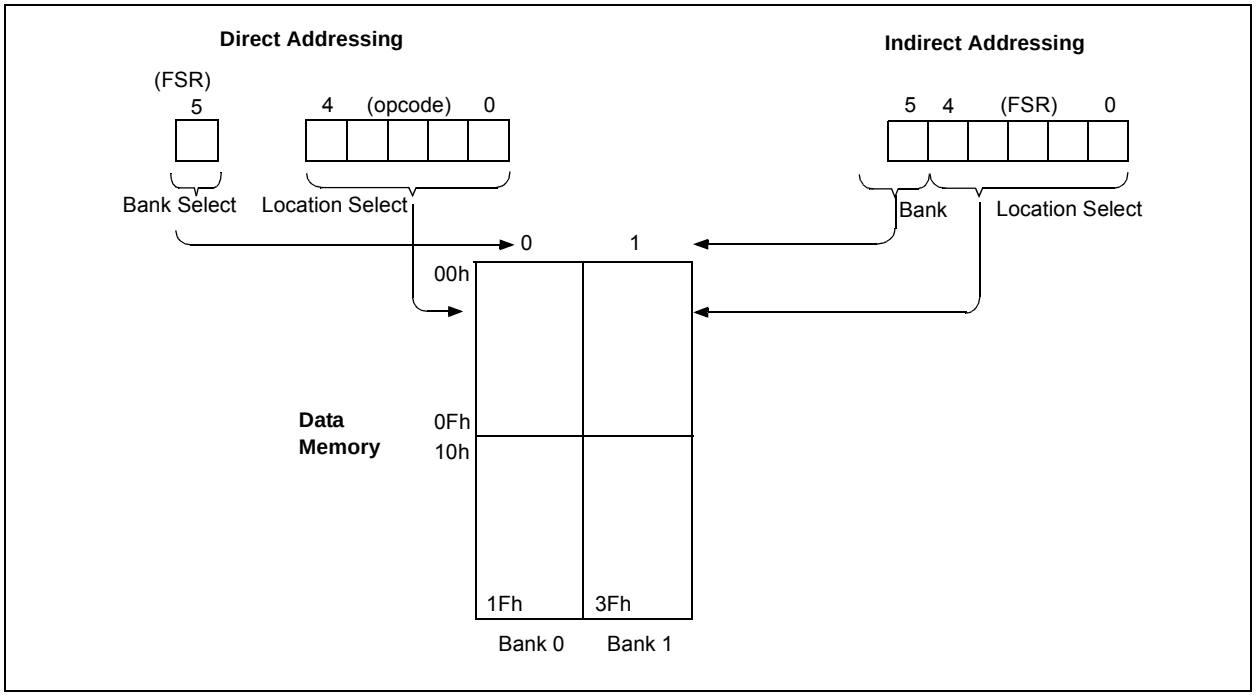
FSR<5> is used to select between banks (0 = Bank 0, 1 = Bank 1).

FSR<7:6> are unimplemented and read as '11'.

**EXAMPLE 4-1: HOW TO CLEAR RAM USING INDIRECT ADDRESSING**

```
          MOVLW  0x10    ;initialize pointer
          MOVWF  FSR     ;to RAM
NEXT      CLRF   INDF    ;clear INDF
                         ;register
          INCF   FSR,F   ;inc pointer
          BTFSC  FSR,4   ;all done?
          GOTO   NEXT    ;NO, clear next
CONTINUE
            :            ;YES, continue
            :
```

**FIGURE 4-4: DIRECT/INDIRECT ADDRESSING**





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## 5.0 FLASH DATA MEMORY CONTROL

The Flash data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (SFRs).

### 5.1 Reading Flash Data Memory

To read a Flash data memory location the user must:

- Write the EEADR register
- Set the RD bit of the EECON register

The value written to the EEADR register determines which Flash data memory location is read. Setting the RD bit of the EECON register initiates the read. Data from the Flash data memory read is available in the EEDATA register immediately. The EEDATA register will hold this value until another read is initiated or it is modified by a write operation. Program execution is suspended while the read cycle is in progress. Execution will continue with the instruction following the one that sets the WR bit. See Example 1 for sample code.

**EXAMPLE 1: READING FROM FLASH DATA MEMORY**

```
BANKSEL EEADR            ;
MOVF DATA_EE_ADDR, W     ;
MOVWF EEADR              ;Data Memory
                         ;Address to read
BANKSEL EECON1           ;

BSF EECON, RD            ;EE Read
MOVF EEDATA, W           ;W = EEDATA
```

**Note:** Only a BSF command will work to enable the Flash data memory read documented in Example 1. No other sequence of commands will work, no exceptions.

### 5.2 Writing and Erasing Flash Data Memory

Flash data memory is erased one row at a time and written one byte at a time. The 64-byte array is made up of eight rows. A row contains eight sequential bytes. Row boundaries exist every eight bytes.

Generally, the procedure to write a byte of data to Flash data memory is:

1. Identify the row containing the address where the byte will be written.
2. If there is other information in that row that must be saved, copy those bytes from Flash data memory to RAM.
3. Perform a row erase of the row of interest.
4. Write the new byte of data and any saved bytes back to the appropriate addresses in Flash data memory.

To prevent accidental corruption of the Flash Data Memory, an unlock sequence is required to initiate a write or erase cycle. This sequence requires that the bit set instructions used to configure the EECON register happen exactly as shown in Example 2 and Example 3, depending on the operation requested.

#### 5.2.1 ERASING FLASH DATA MEMORY

A row must be manually erased before writing new data. The following sequence must be performed for a single row erase.

1. Load EEADR with an address in the row to be erased.
2. Set the FREE bit to enable the erase.
3. Set the WREN bit to enable write access to the array.
4. Set the WR bit to initiate the erase cycle.

If the WREN bit is not set in the instruction cycle after the FREE bit is set, the FREE bit will be cleared in hardware.

If the WR bit is not set in the instruction cycle after the WREN bit is set, the WREN bit will be cleared in hardware.

Sample code that follows this procedure is included in Example 2.

Program execution is suspended while the erase cycle is in progress. Execution will continue with the instruction following the one that sets the WR bit.

**EXAMPLE 2: ERASING A FLASH DATA MEMORY ROW**

```
BANKSEL   EEADR
MOVLW     EE_ADR_ERASE   ; LOAD ADDRESS OF ROW TO
                         ; ERASE
MOVWF     EEADR          ;
BSF       EECON,FREE     ; SELECT ERASE
BSF       EECON,WREN     ; ENABLE WRITES
BSF       EECON,WR       ; INITITATE ERASE
```

**Note 1:** The FREE bit may be set by any command normally used by the core. However, the WREN and WR bits can only be set using a series of BSF commands, as documented in Example 1. No other sequence of commands will work, no exceptions.

**2:** Bits <5:3> of the EEADR register indicate which row is to be erased.

### 5.2.2 WRITING TO FLASH DATA MEMORY

Once a cell is erased, new data can be written. Program execution is suspended during the write cycle. The following sequence must be performed for a single byte write.

1. Load EEADR with the address.
2. Load EEDATA with the data to write.
3. Set the WREN bit to enable write access to the array.
4. Set the WR bit to initiate the erase cycle.

If the WR bit is not set in the instruction cycle after the WREN bit is set, the WREN bit will be cleared in hardware.

Sample code that follows this procedure is included in Example 3.

**EXAMPLE 3: WRITING A FLASH DATA MEMORY ROW**

```
BANKSEL   EEADR
MOVLW     EE_ADR_WRITE     ; LOAD ADDRESS
MOVWF     EEADR            ;
MOVLW     EE_DATA_TO_WRITE ; LOAD DATA
MOVWF     EEDATA           ; INTO EEDATA REGISTER
BSF       EECON,WREN       ; ENABLE WRITES
BSF       EECON,WR         ; INITITATE ERASE
```

**Note 1:** Only a series of BSF commands will work to enable the memory write sequence documented in Example 2. No other sequence of commands will work, no exceptions.

**2:** For reads, erases and writes to the Flash data memory, there is no need to insert a NOP into the user code as is done on mid-range devices. The instruction immediately following the "BSF EECON,WR/RD" will be fetched and executed properly.

## 5.3 Write Verify

Depending on the application, good programming practice may dictate that data written to the Flash data memory be verified. Example 4 is an example of a write verify.

**EXAMPLE 4: WRITE VERIFY OF DATA EEPROM**

```
MOVF      EEDATA, W    ;EEDATA has not changed
                       ;from previous write
BSF       EECON, RD    ;Read the value written
XORWF     EEDATA, W    ;
BTFSS     STATUS, Z    ;Is data the same
GOTO      WRITE_ERR    ;No, handle error
                       ;Yes, continue
```

## 5.4 Code Protection

Code protection does not prevent the CPU from performing read or write operations on the Flash data memory. Refer to the code protection chapter for more information.


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## 6.0 I/O PORT

As with any other register, the I/O register(s) can be written and read under program control. However, read instructions (e.g., MOVF PORTB,W) always read the I/O pins independent of the pin's Input/Output modes. On Reset, all I/O ports are defined as input (inputs are at high-impedance) since the I/O control registers are all set.

### 6.1 GPIO

GPIO is an 8-bit I/O register. Only the low-order 6 bits are used (GP<5:0>). Bits 7 and 6 are unimplemented and read as '0's. Please note that GP3 is an input-only pin. The Configuration Word can set several I/O's to alternate functions. When acting as alternate functions, the pins will read as '0' during a port read. Pins GP0, GP1, and GP3 can be configured with weak pull-ups and also for wake-up on change. The wake-up on change and weak pull-up functions are not pin select-able. If GP3/MCLR is configured as MCLR, weak pull-up is always on and wake-up on change for this pin is not enabled.

**TABLE 6-1: WEAK PULL-UP ENABLED PINS**

| Pin | WPU | WU |
|---|---|---|
| GP0 | Y | Y |
| GP1 | Y | Y |
| GP2 | N | N |
| GP3 | Y(1) | Y |
| GP4 | N | N |
| GP5 | N | N |
| GP6 | N | N |

**Note 1:** When MCLRE = 1, the weak pull-up on GP3/MCLR is always enabled.

**2:** WPU = Weak pull-up; WU = Wake-up.

### 6.2 TRIS Registers

The Output Driver Control registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRISGPIO Register bit puts the corresponding output driver in a high-impedance (Input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

The TRISGPIO register is "write-only". Bits <5:0> are set (output drivers disabled) upon Reset.

| **Note:** | If the T0CS bit is set to '1', it will override the TRISGPIO function on the T0CKI pin. |
|---|---|

**REGISTER 6-1: GPIO: GPIO REGISTER**

| U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **GP<5:0>**: GPIO I/O Pin bits
1 = GPIO pin is >$V_{IH}$ min.
0 = GPIO pin is <$V_{IL}$ max.

**REGISTER 6-2: TRISGPIO: TRI-STATE GPIO REGISTER**

| U-0 | U-0 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
|---|---|---|---|---|---|---|---|
| — | — | TRISGPIO5 | TRISGPIO4 | TRISGPIO3 | TRISGPIO2 | TRISGPIO1 | TRISGPIO0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TRISGPIO<5:0>:** GPIO Tri-State Control bits
1 = GPIO pin configured as an input (tri-stated)
0 = GPIO pin configured as an output


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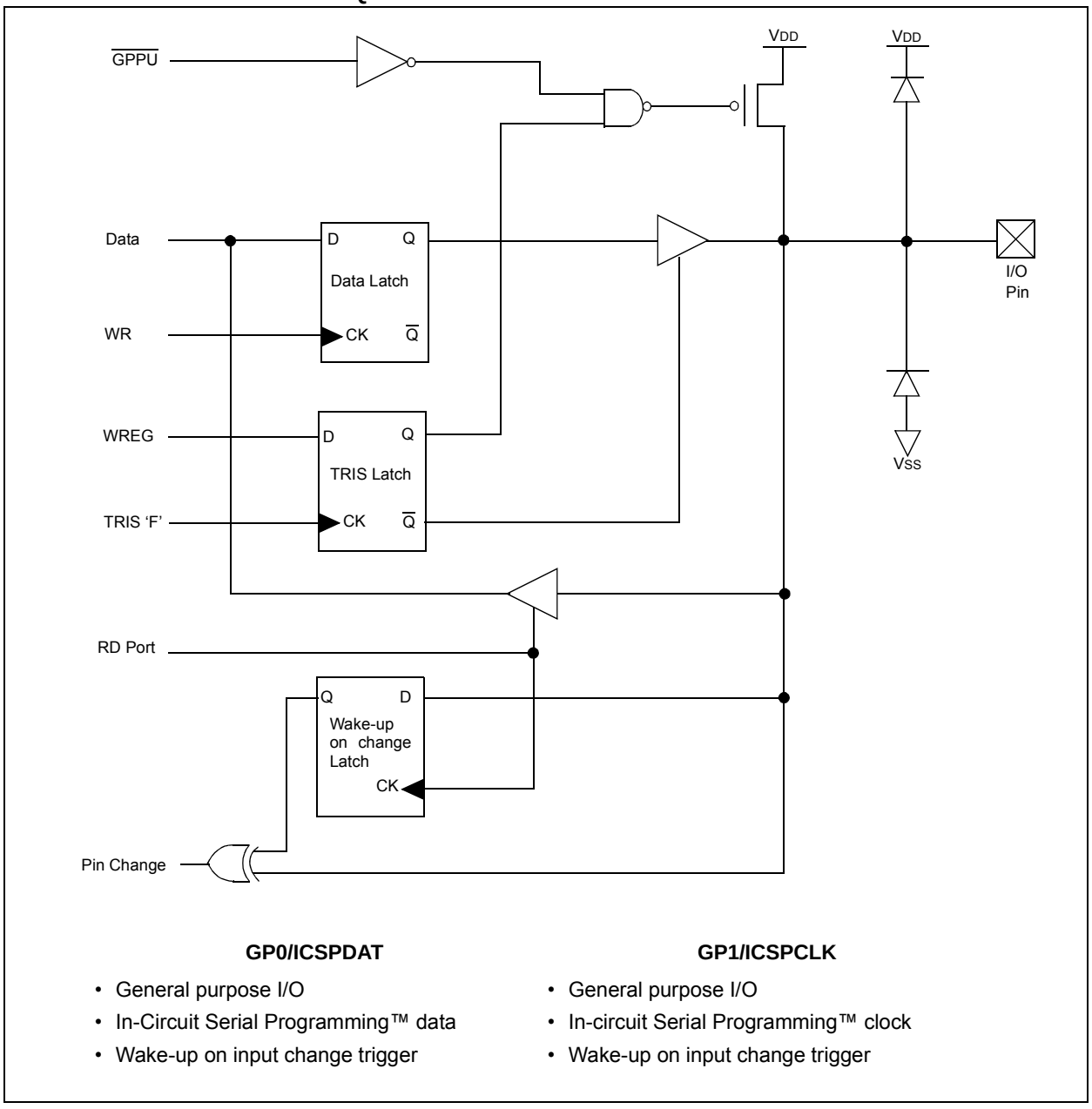
## 6.3 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 6-1. All port pins, except GP3 which is input only, may be used for both input and output operations. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF GPIO, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRISGPIO must be cleared (= `0`). For use as an input, the corresponding TRISGPIO bit must be set. Any I/O pin (except GP3) can be programmed individually as input or output.

**FIGURE 6-1: PIC12F519 EQUIVALENT CIRCUIT FOR I/O PINS – GP0/GP1**




**GP0/ICSPDAT**

- General purpose I/O
- In-Circuit Serial Programming™ data
- Wake-up on input change trigger

**GP1/ICSPCLK**

- General purpose I/O
- In-circuit Serial Programming™ clock
- Wake-up on input change trigger

**FIGURE 6-2: GP2/TOCK1**

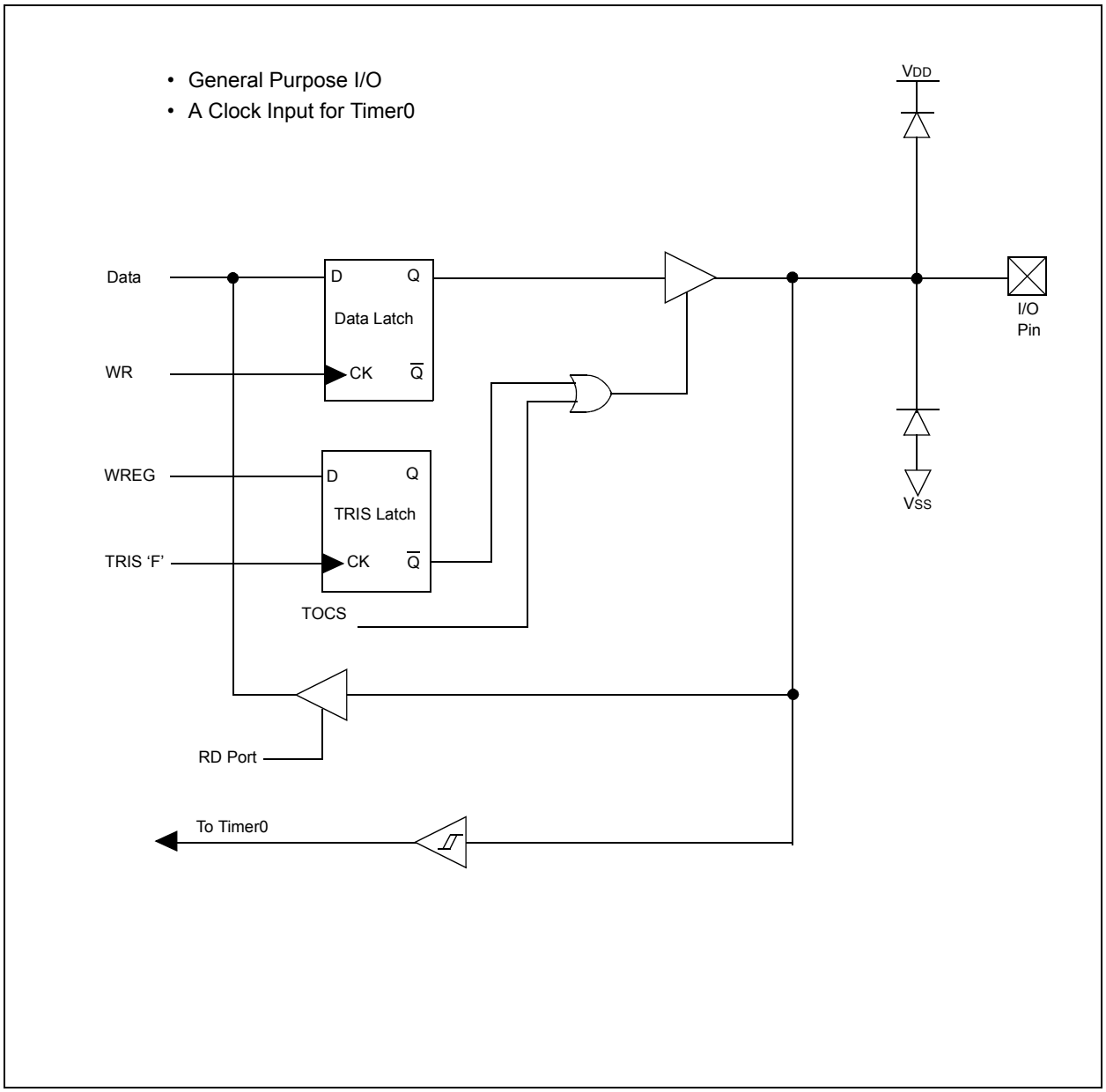




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**FIGURE 6-3: GP4/OSC2**

- General Purpose I/O
- A crystal resonator connection

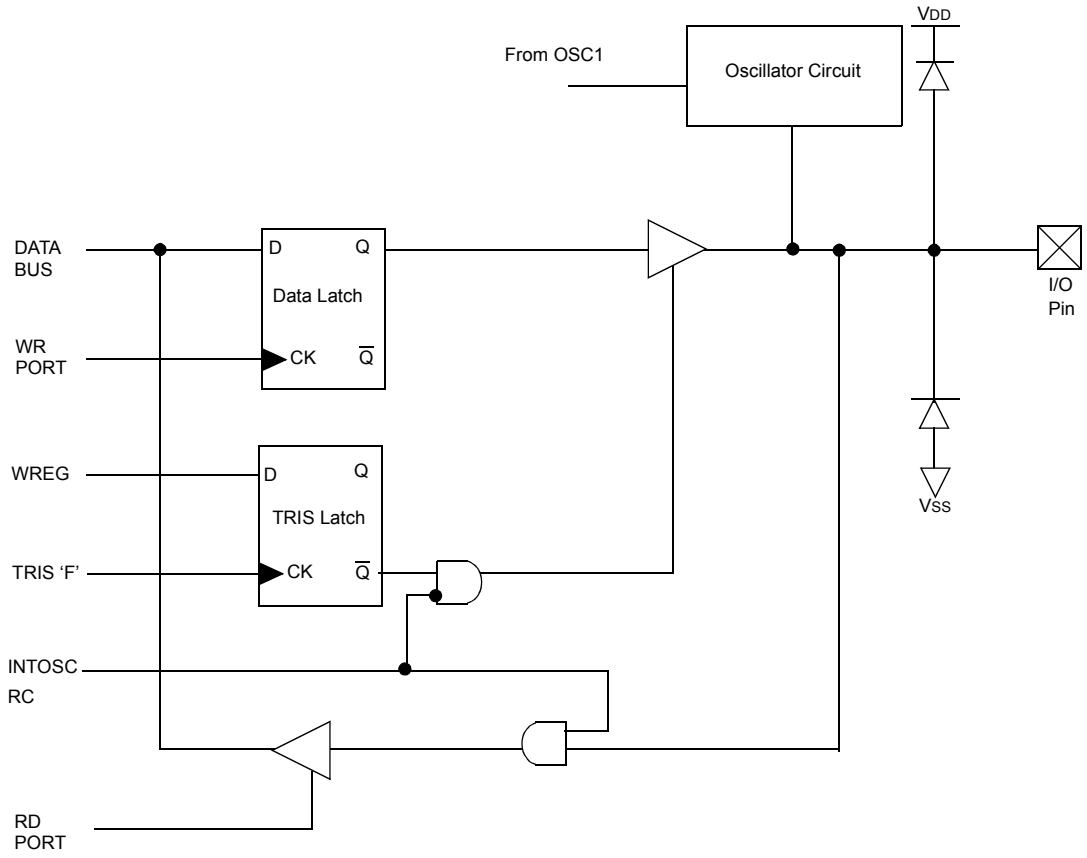

**FIGURE 6-4: GP5/OSC1/CLKIN**

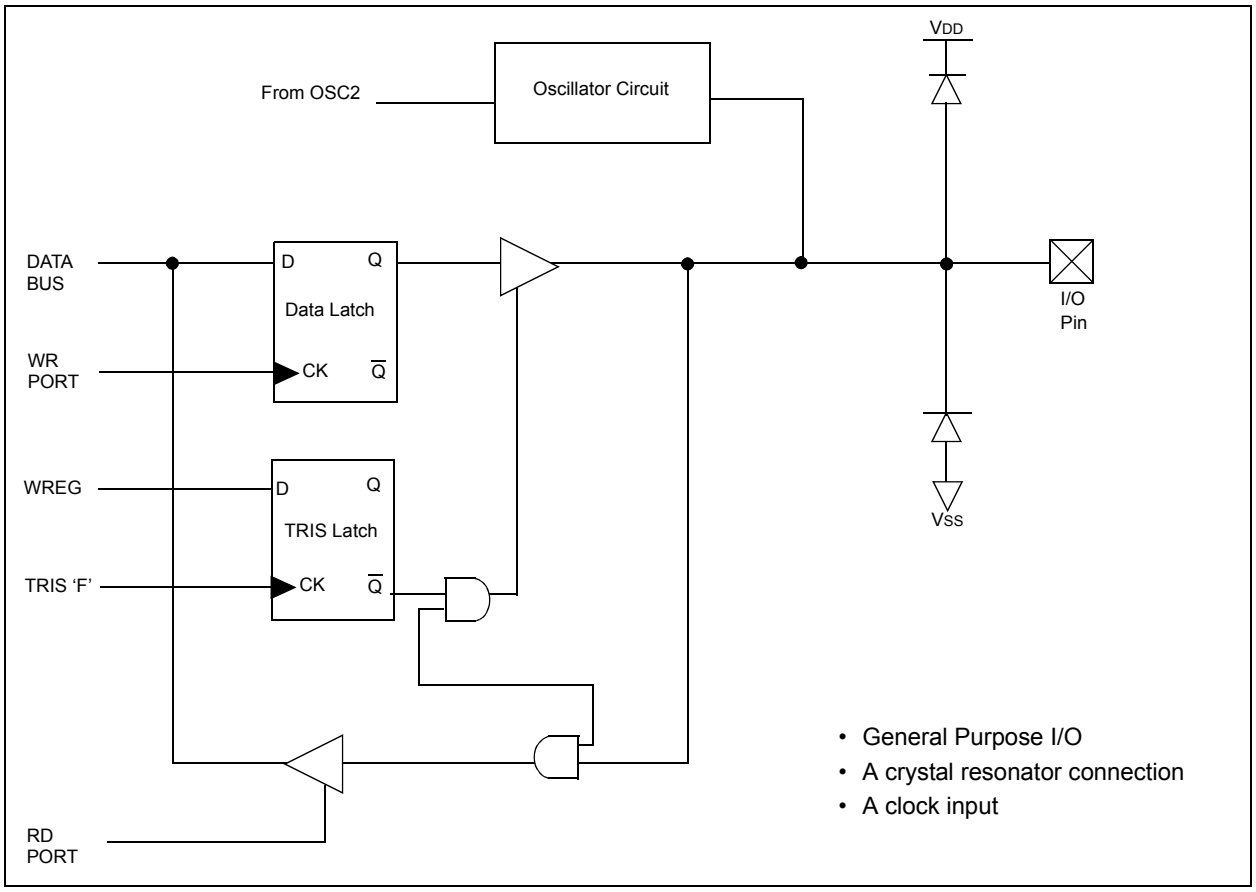



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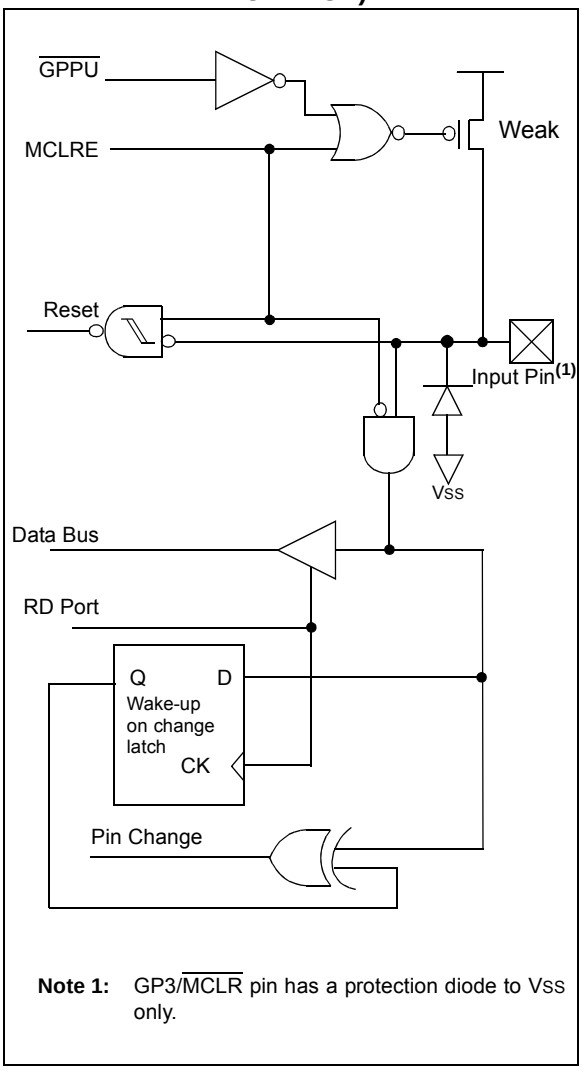
**FIGURE 6-5: GP3 (WITH WEAK PULL-UP AND WAKE-UP ON CHANGE)**




**Note 1:** GP3/$\overline{MCLR}$ pin has a protection diode to VSS only.

**TABLE 6-2: SUMMARY OF PORT REGISTERS**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| GPIO | — | — | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | --xx xxxx | --uu uuuu |
| TRISGPIO | — | — | TRISGPIO5 | TRISGPIO4 | TRISGPIO3 | TRISGPIO2 | TRISGPIO1 | TRISGPIO0 | --11 1111 | --11 1111 |
| STATUS | GPWUF | — | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0-01 1xxx | q-0q quuu |
| OPTION | $\overline{GPWU}$ | $\overline{GPPU}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |

**Legend:** x = unknown, u = unchanged, – = unimplemented, read as '0', Shaded cells = unimplemented, read as '0', q = depends on the condition

## 6.4 I/O Programming Considerations

### 6.4.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of GPIO will cause all eight bits of GPIO to be read into the CPU, bit 5 to be set and the GPIO value to be written to the output latches. If another bit of GPIO is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit 0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 6-1 shows the effect of two sequential Read-Modify-Write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired OR", "wired AND"). The resulting high output currents may damage the chip.

**EXAMPLE 6-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT**

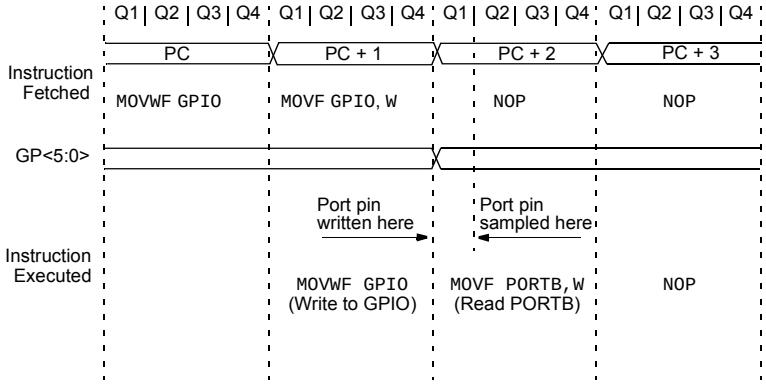
```
;Initial GPIO Settings
;GPIO<5:3> Inputs
;GPIO<2:0> Outputs
;
;                 GPIO latch   GPIO pins
;                 ----------   ----------
  BCF    GPIO, 5  ;--01 -ppp    --11 pppp
  BCF    GPIO, 4  ;--10 -ppp    --11 pppp
  MOVLW  007h;
  TRIS   GPIO     ;--10 -ppp    --11 pppp
;
```

**Note 1:** The user may have expected the pin values to be '--00 pppp'. The 2nd BCF caused GP5 to be latched as the pin value (High).

### 6.4.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 6-6). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

**FIGURE 6-6: SUCCESSIVE I/O OPERATION**




This example shows a write to GPIO followed by a read from GPIO.

Data setup time = (0.25 $T_{CY}$ – $T_{PD}$)

where: $T_{CY}$ = instruction cycle.

$T_{PD}$ = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.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## 7.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

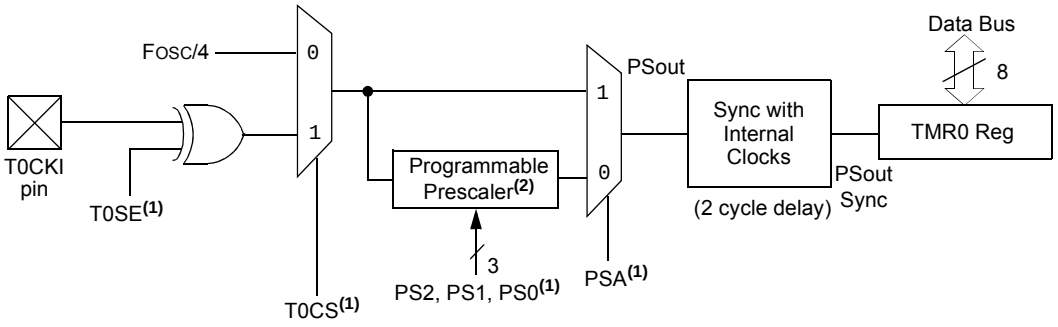
Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit (OPTION<4>) determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 7.1 "Using Timer0 with an External Clock"**.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit, PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. **Section 7.2 "Prescaler"** details the operation of the prescaler.

A summary of registers associated with the Timer0 module is found in Table 7-1.

The Timer0 contained in the CPU core follows the standard baseline definition.

**FIGURE 7-1: TIMER0 BLOCK DIAGRAM**




**Note 1:** Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
**2:** The prescaler is shared with the Watchdog Timer.

**FIGURE 7-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE**

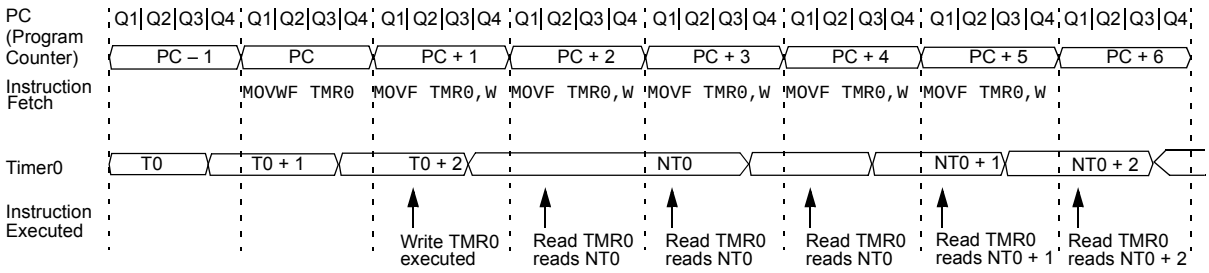


**FIGURE 7-3: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2**

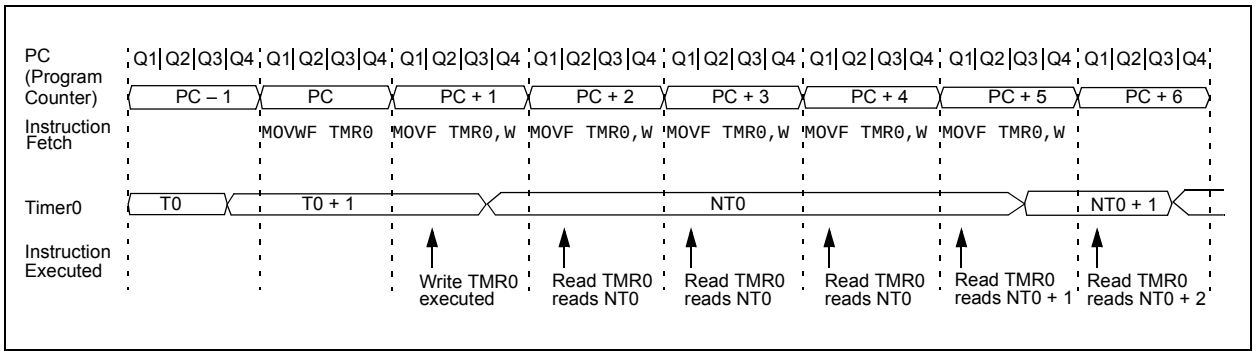



**TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on All Other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01h | TMR0 | Timer0 – 8-bit Real-Time Clock/Counter | | | | | | | | xxxx xxxx | uuuu uuuu |
| N/A | OPTION | $\overline{GPWU}$ | $\overline{GPPU}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |
| N/A | TRISGPIO | — | — | TRISGPIO5 | TRISGPIO4 | TRISGPIO3 | TRISGPIO2 | TRISGPIO1 | TRISGPIO0 | --11 1111 | --11 1111 |

**Legend:** x = unknown, u = unchanged, – = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'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## 7.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

### 7.1.1 EXTERNAL CLOCK SYNCHRONIZATION

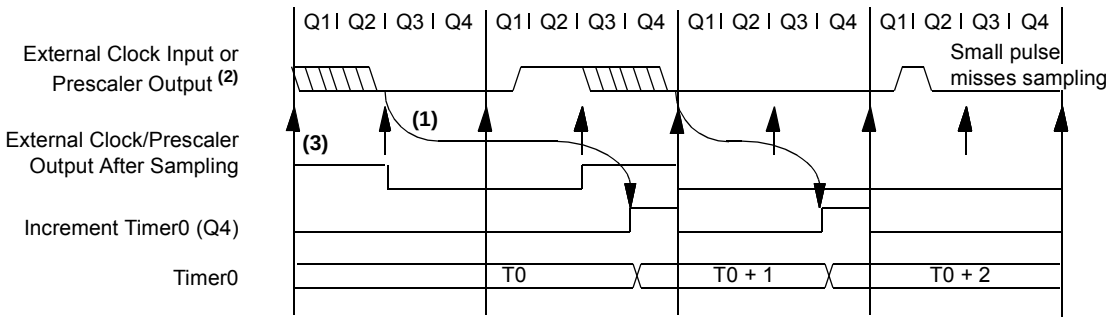
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-4). Therefore, it is necessary for T0CKI to be high for at least 2 TOSC (and a small RC delay of 2 Tt0H) and low for at least 2 TOSC (and a small RC delay of 2 Tt0H). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler, so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4 TOSC (and a small RC delay of 4 Tt0H) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of Tt0H. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

### 7.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-4 shows the delay from the external clock edge to the timer incrementing.

**FIGURE 7-4: TIMER0 TIMING WITH EXTERNAL CLOCK**




**Note 1:** Delay from clock input change to Timer0 increment is 3 TOSC to 7 TOSC. (Duration of Q = TOSC). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4 TOSC max.

**2:** External clock if no prescaler selected; prescaler output otherwise.

**3:** The arrows indicate the times at which sampling occurs.

## 7.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module or as a postscaler for the Watchdog Timer (WDT), respectively (see **Section 8.6 "Watchdog Timer (WDT)"**). For simplicity, this counter is being referred to as "prescaler" throughout this data sheet.

| **Note:** | The prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT and vice versa. |
|---|---|

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF TMR0`, `MOVWF TMR0`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a Reset, the prescaler contains all '0's.

### 7.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on-the-fly" during program execution). To avoid an unintended device Reset, the following instruction sequence (Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

**EXAMPLE 7-1: CHANGING PRESCALER (TIMER0 → WDT)**

```
CLRWDT              ;Clear WDT
CLRF   TMR0         ;Clear TMR0 and Prescaler
MOVLW  b'00xx1111'
OPTION

CLRWDT              ;PS<2:0> are 000 or 001
MOVLW  b'00xx1xxx'  ;Set Postscaler to
OPTION              ;desired WDT rate
```

To change the prescaler from the WDT to the Timer0 module, use the sequence shown in Example 7-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

**EXAMPLE 7-2: CHANGING PRESCALER (WDT → TIMER0)**

```
CLRWDT              ;Clear WDT and
                    ;prescaler
MOVLW  b'xxxx0xxx'  ;Select TMR0, new
                    ;prescale value and
                    ;clock source
OPTION
```


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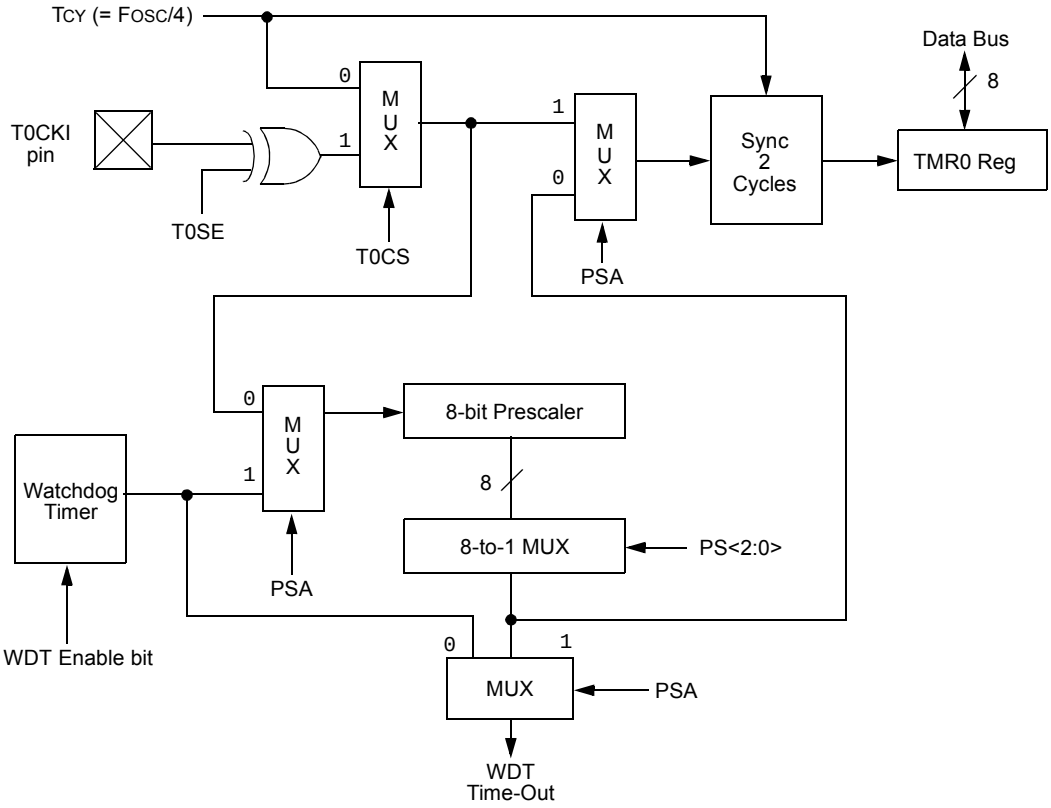
**FIGURE 7-5: BLOCK DIAGRAM OF THE TIMER0/ WDT PRESCALER(1)**




**Note 1:** T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

**NOTES:**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## 8.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC12F519 microcontroller has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These features are:

- Oscillator Selection
- Reset:
  - Power-on Reset (POR)
  - Device Reset Timer (DRT)
  - Wake-up from Sleep on Pin Change
- Watchdog Timer (WDT)
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™

The PIC12F519 device has a Watchdog Timer, which can be shut off only through Configuration bit WDTE. It runs off of its own RC oscillator for added reliability. If using XT or LP selectable oscillator options, there is always an 18 ms (nominal) delay provided by the Device Reset Timer (DRT), intended to keep the chip in Reset until the crystal oscillator is stable. If using INTRC or EXTRC, the DRT provides a 1 ms (nominal) delay.

The Sleep mode is designed to offer a very low-current Power-Down mode. The user can wake-up from Sleep through a change-on-input-pins or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application, including an internal 4 MHz or 8 MHz oscillator. The EXTRC oscillator option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options.

### 8.1 Configuration Bits

The PIC12F519 Configuration Words consist of 12 bits. Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type; one bit is the Watchdog Timer enable bit, one bit is the $\overline{\text{MCLR}}$ enable bit and one bit is for code protection (Register 8-1).

**REGISTER 8-1: CONFIG: CONFIGURATION WORD REGISTER(1)**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| — | $\overline{\text{CPDF}}$ | IOSCFS | MCLRE | $\overline{\text{CP}}$ | WDTE | FOSC1 | FOSC0 |
| bit 7 | | | | | | | bit 0 |

bit 7 **Unimplemented**: Read as '1'

bit 6 **$\overline{\text{CPDF}}$:** Code Protection bit - Flash Data Memory
1 = Code protection off
0 = Code protection on

bit 5 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz INTOSC frequency
0 = 4 MHz INTOSC frequency

bit 4 **MCLRE:** Master Clear Enable bit
1 = GP3/$\overline{\text{MCLR}}$ pin functions as $\overline{\text{MCLR}}$
0 = GP3/$\overline{\text{MCLR}}$ pin functions as GP3, $\overline{\text{MCLR}}$ internally tied to $V_{DD}$

bit 3 **$\overline{\text{CP}}$:** Code Protection bit - User Program Memory
1 = Code protection off
0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
00 = LP oscillator with 18 ms DRT(2)
01 = XT oscillator with 18 ms DRT(2)
10 = INTOSC with 1 ms DRT(2)
11 = EXTRC with 1 ms DRT(2)

**Note 1:** Refer to the "*PIC12F519 Memory Programming Specification*", DS41316 to determine how to program/erase the Configuration Word.

**2:** DRT length (18 ms or 1 ms) is a function of clock mode selection. It is the responsibility of the application designer to ensure the use of either 18 ms (nominal) DRT or the 1 ms (nominal) DRT will result in acceptable operation. Refer to Figure 11-1 and Table 11-2 for $V_{DD}$ rise time and stability requirements for this mode of operation.


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## 8.2 Oscillator Configurations

### 8.2.1 OSCILLATOR TYPES

The PIC12F519 device can be operated in up to four different oscillator modes. The user can program using the Configuration bits (FOSC<1:0>), to select one of these modes:

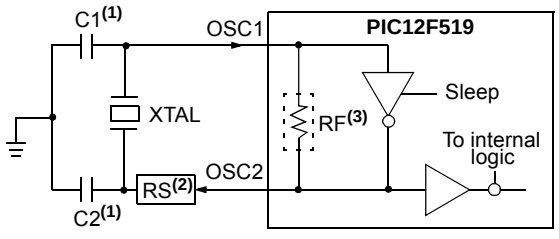
- LP: Low-Power Crystal
- XT: Crystal/Resonator
- INTRC: Internal 4 MHz or 8 MHz Oscillator
- EXTRC: External Resistor/Capacitor

### 8.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT or LP modes, a crystal or ceramic resonator is connected to the (GP5)/OSC1/(CLKIN) and (GP4)/OSC2 pins to establish oscillation (Figure 8-1). The PIC12F519 oscillator designs require the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT or LP modes, the device can have an external clock source drive the (GP5)/OSC1/CLKIN pin (Figure 8-2). When the part is used in this fashion, the output drive levels on the OSC2 pin are very weak. This pin should be left open and unloaded. Also when using this mode, the external clock should observe the frequency limits for the clock mode chosen (XT or LP).

| | |
|---|---|
| **Note 1:** | The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required. |

**FIGURE 8-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT OR LP OSC CONFIGURATION)**




**Note 1:** See Capacitor Selection tables for recommended values of C1 and C2.
**2:** A series resistor (RS) may be required for AT strip cut crystals.
**3:** RF approx. value = 10 MΩ.

**FIGURE 8-2: EXTERNAL CLOCK INPUT OPERATION (XT OR LP OSC CONFIGURATION)**

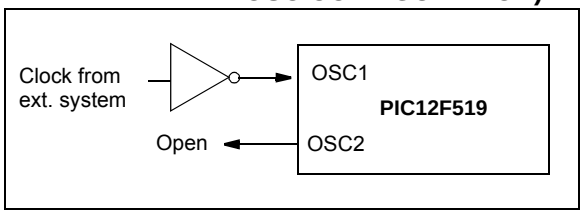



**TABLE 8-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS**

| Osc Type | Resonator Freq. | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| XT | 4.0 MHz | 30 pF | 30 pF |

**Note:** Component values shown are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

**TABLE 8-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR – PIC12F519(2)**

| Osc Type | Resonator Freq. | Cap.Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz(1) | 15 pF | 15 pF |
| XT | 200 kHz<br>1 MHz<br>4 MHz | 47-68 pF<br>15 pF<br>15 pF | 47-68 pF<br>15 pF<br>15 pF |

**Note 1:** For $V_{DD}$ > 4.5V, C1 = C2 ≈ 30 pF is recommended.
**2:** Component values shown are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

### 8.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 8-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

**FIGURE 8-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT**

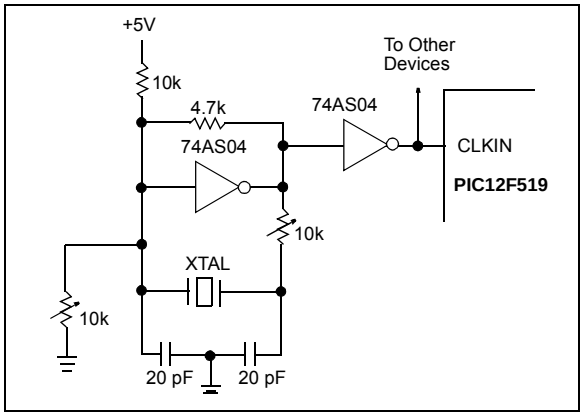
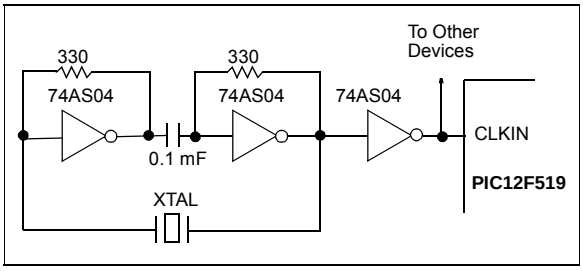



Figure 8-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330Ω resistors provide the negative feedback to bias the inverters in their linear region.

**FIGURE 8-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT**



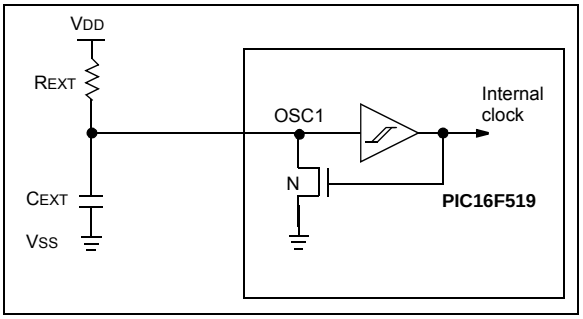

### 8.2.4 EXTERNAL RC OSCILLATOR

For timing insensitive applications, the RC circuit option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit-to-unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 8-5 shows how the R/C combination is connected to the PIC12F519 device. For REXT values below 3.0 kΩ, the oscillator operation may become unstable, or stop completely. For very high REXT values (e.g., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. It is recommended keeping REXT between 5.0 kΩ and 100 kΩ.

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), it is recommended using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance. See Figure 11-1 and Figure 11-2.

**FIGURE 8-5: EXTERNAL RC OSCILLATOR MODE**




### 8.2.5 INTERNAL 4/8 MHz RC OSCILLATOR

The internal RC oscillator provides a fixed 4/8 MHz (nominal) system clock at VDD = 3.5V and 25°C, (see **Section 11.0 "Electrical Characteristics"** for information on variation over voltage and temperature).

In addition, a calibration instruction is programmed into the last address of memory, which contains the calibration value for the internal RC oscillator. This location is always non-code protected, regardless of the code-protect settings. This value is programmed as a `MOVLW XX` instruction where XX is the calibration value, and is placed at the Reset vector. This will load the W register with the calibration value upon Reset and the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PC will then roll over to the users program at address 0x000. The user then has the option of writing the value to the OSCCAL Register (05h) or ignoring it.

OSCCAL, when written to with the calibration value, will "trim" the internal oscillator to remove process variation from the oscillator frequency.

| | |
|---|---|
| **Note:** | Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be read prior to erasing the part so it can be reprogrammed correctly later. |

For the PIC12F519 device, only bits <7:1> of OSCCAL are used for calibration. See Register 4-3 for more information.

| | |
|---|---|
| **Note:** | The bit 0 of the OSCCAL register is unimplemented and should be written as '0' when modifying OSCCAL for compatibility with future devices. |

## 8.3 Reset

The device differentiates between various kinds of Reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Time-out Reset during normal operation
- WDT Time-out Reset during Sleep
- Wake-up from Sleep on pin change

Some registers are not reset in any way, and they are unknown on Power-on Reset (POR) and unchanged in any other Reset. Most other registers are reset to "Reset state" on Power-on Reset (POR), $\overline{\text{MCLR}}$, WDT or Wake-up on pin change Reset during normal operation. They are not affected by a WDT Reset during Sleep or $\overline{\text{MCLR}}$ Reset during Sleep, since these Resets are viewed as resumption of normal operation. The exceptions to this are $\overline{\text{TO}}$, $\overline{\text{PD}}$ and GPWUF bits. They are set or cleared differently in different Reset situations. These bits are used in software to determine the nature of Reset. See Table 8-3 for a full description of Reset states of all registers.

**TABLE 8-3: RESET CONDITIONS FOR REGISTERS**

| Register | Address | Power-on Reset | $\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up On Pin Change |
|---|---|---|---|
| W | — | qqqq qqq0(1) | qqqq qqq0(1) |
| INDF | 00h | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h | xxxx xxxx | uuuu uuuu |
| PCL | 02h | 1111 1111 | 1111 1111 |
| STATUS | 03h | 0-01 1xxx | q-0q quuu(2), (3) |
| FSR | 04h | 110x xxxx | 11uu uuuu |
| OSCCAL | 05h | 1111 111- | uuuu uuu- |
| PORTB | 06h | --xx xxxx | --uu uuuu |
| OPTION | — | 1111 1111 | 1111 1111 |
| TRIS | — | --11 1111 | --11 1111 |
| EECON | 21h | ---0 x000 | ---0 q000 |
| EEDATA | 25h | xxxx xxxx | uuuu uuuu |
| EEADR | 26h | --xx xxxx | --uu uuuu |

**Legend:** u = unchanged, x = unknown, – = unimplemented bit, read as '0', q = value depends on condition.

**Note 1:** Bits <7:1> of W register contain oscillator calibration values due to MOVLW XX instruction at top of memory.

**2:** See Table 8-4 for Reset value for specific conditions.

**3:** If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

**TABLE 8-4: RESET CONDITION FOR SPECIAL REGISTERS**

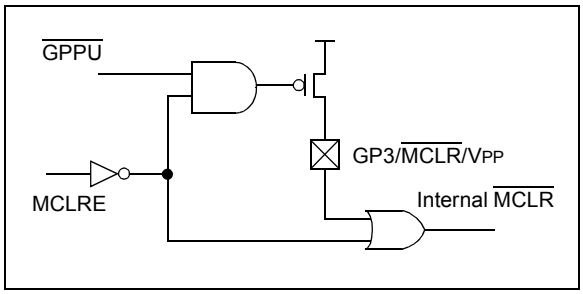
| | STATUS Addr: 03h |
|---|---|
| Power-on Reset | 0-01 1xxx |
| $\overline{MCLR}$ Reset during normal operation | 0-0u uuuu |
| $\overline{MCLR}$ Reset during Sleep | 0-01 0uuu |
| WDT Reset during Sleep | 0-00 0uuu |
| WDT Reset normal operation | 0-00 uuuu |
| Wake-up from Sleep on pin change | 1-01 0uuu |

**Legend:** u = unchanged, x = unknown

### 8.3.1 $\overline{MCLR}$ ENABLE

This Configuration bit, when unprogrammed (left in the '1' state), enables the external $\overline{MCLR}$ function. When programmed, the $\overline{MCLR}$ function is tied to the internal $V_{DD}$ and the pin is assigned to be a I/O. See Figure 8-6.

**FIGURE 8-6: $\overline{MCLR}$ SELECT**




## 8.4 Power-on Reset (POR)

The PIC12F519 device incorporates an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until $V_{DD}$ has reached a high enough level for proper operation. To take advantage of the internal POR, program the GP3/$\overline{MCLR}$/$V_{PP}$ pin as $\overline{MCLR}$ and tie through a resistor to $V_{DD}$, or program the pin as GP3, in which case, an internal weak pull-up resistor is implemented using a transistor (refer to Table 11-4 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for $V_{DD}$ is specified. See **Section 11.0 "Electrical Characteristics"** for details.

When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the devices must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 8-7.

The Power-on Reset circuit and the Device Reset Timer (see **Section 8.5 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{MCLR}$ to be high. After the time-out period, which is typically 18 ms or 1 ms, it will reset the Reset latch and thus end the on-chip Reset signal.

A power-up example where $\overline{MCLR}$ is held low is shown in Figure 8-8. $V_{DD}$ is allowed to rise and stabilize before bringing $\overline{MCLR}$ high. The chip will actually come out of Reset $T_{DRT}$ after $\overline{MCLR}$ goes high.

In Figure 8-9, the on-chip Power-on Reset feature is being used ($\overline{MCLR}$ and $V_{DD}$ are tied together or the pin is programmed to be GP3). The $V_{DD}$ is stable before the Start-up timer times out and there is no problem in getting a proper Reset. However, Figure 8-10 depicts a problem situation where $V_{DD}$ rises too slowly. The time between when the DRT senses that $\overline{MCLR}$ is high and when $\overline{MCLR}$ and $V_{DD}$ actually reach their full value, is too long. In this situation, when the start-up timer times out, $V_{DD}$ has not reached the $V_{DD}$ (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 8-9).

| | |
|---|---|
| **Note:** | When the devices start normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met. |

For additional information, refer to Application Note AN522, "*Power-Up Considerations*" (DS00522)


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**FIGURE 8-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**

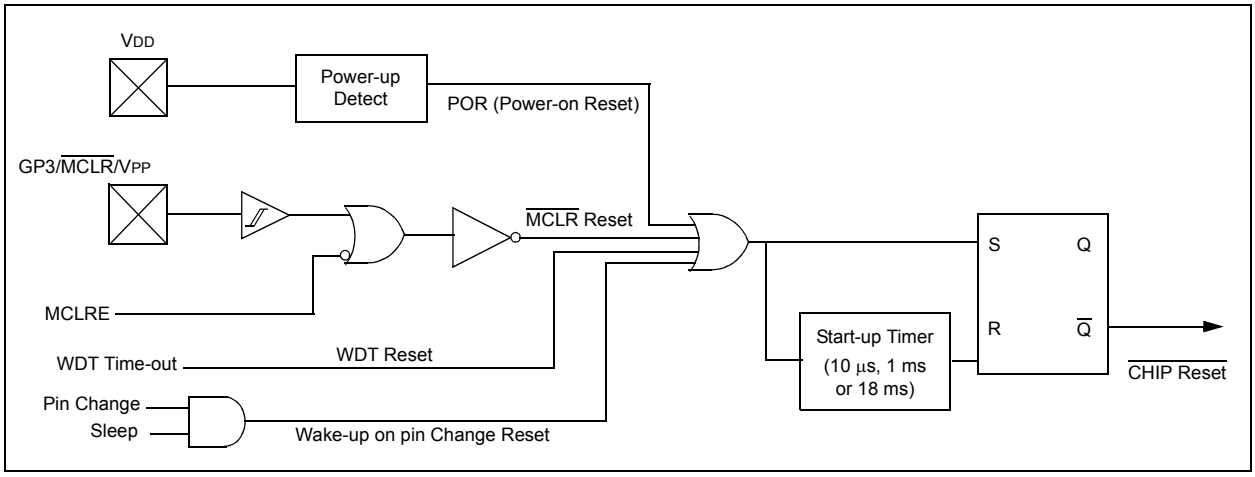



**FIGURE 8-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR PULLED LOW)**

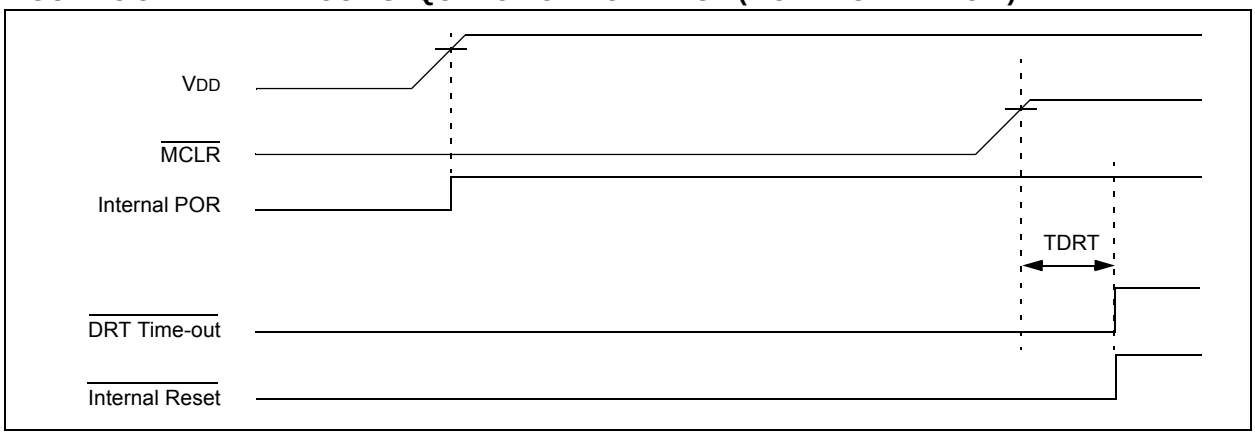



**FIGURE 8-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME**

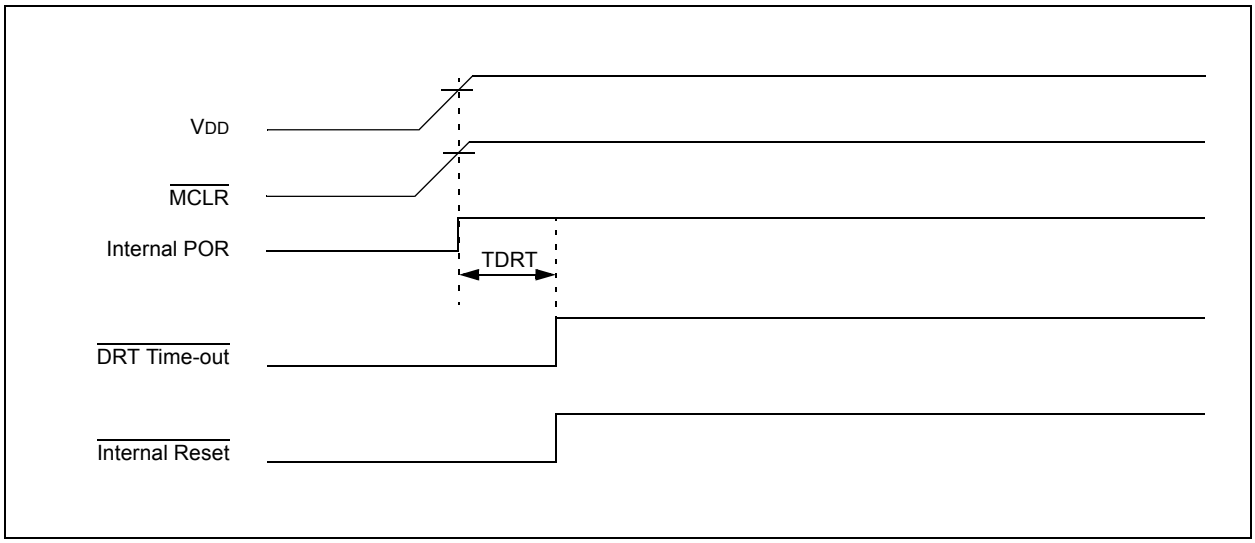
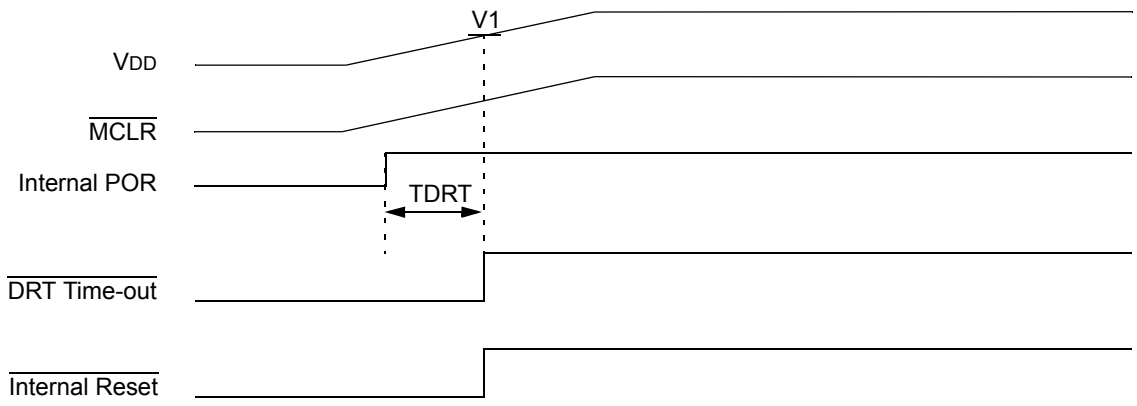


**FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO $V_{DD}$): SLOW $V_{DD}$ RISE TIME**




**Note:** When $V_{DD}$ rises slowly, the $T_{DRT}$ time-out expires long before $V_{DD}$ has reached its final value. In this example, the chip will reset properly if, and only if, V1 ≥ $V_{DD}$ min.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## 8.5 Device Reset Timer (DRT)

On the PIC12F519 device, the DRT runs any time the device is powered up. DRT runs from Reset and varies based on oscillator selection and Reset type (see Table 8-5).

The DRT operates on an internal RC oscillator. The processor is kept in Reset as long as the DRT is active. The DRT delay allows VDD to rise above VDD min. and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the devices in a Reset condition after MCLR has reached a logic high (VIH MCLR) level. Programming GP3/MCLR/VPP as MCLR and using an external RC network connected to the MCLR input is not required in most cases. This allows savings in cost-sensitive and/or space restricted applications, as well as allowing the use of the GP3/MCLR/VPP pin as a general purpose input.

The Device Reset Time delays will vary from chip-to-chip due to VDD, temperature and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out from Sleep. This is particularly important for applications using the WDT to wake from Sleep mode automatically.

Reset sources are POR, MCLR, WDT time-out and wake-up on pin change. See **Section 8.8.2 "Wake-up from Sleep", Notes 1, 2 and 3**.

**TABLE 8-5: DRT (DEVICE RESET TIMER PERIOD)**

| Oscillator Configuration | POR Reset | Subsequent Resets |
|---|---|---|
| INTOSC, EXTRC | 1 ms (typical) | 10 μs (typical) |
| LP, XT | 18 ms (typical) | 18 ms (typical) |

## 8.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the external RC oscillator of the (GP5)/OSC1/CLKIN pin and the internal 4 or 8 MHz oscillator. This means that the WDT will run even if the main processor clock has been stopped, for example, by execution of a SLEEP instruction. During normal operation or Sleep, a WDT Reset or wake-up Reset, generates a device Reset.

The TO bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration WDTE as a '0' (see **Section 8.1 "Configuration Bits"**). Refer to the PIC12F519 Programming Specification (DS41316) to determine how to access the Configuration Word.

### 8.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

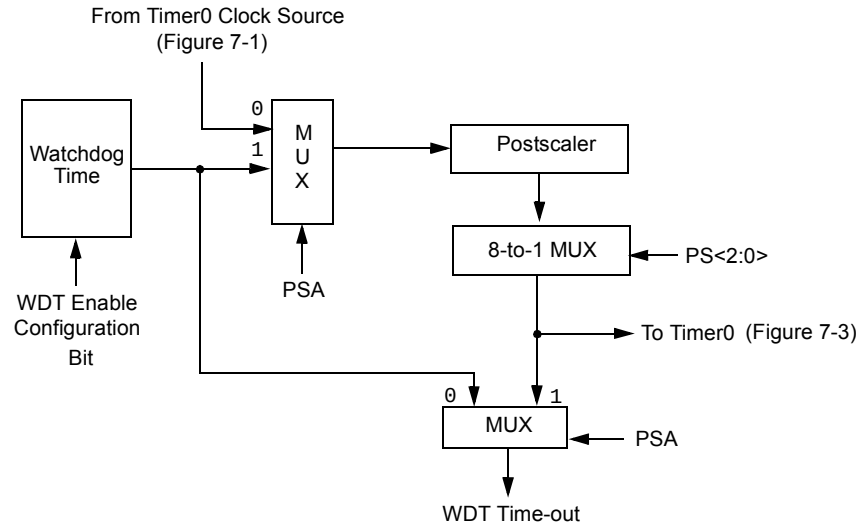
Under worst-case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

### 8.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device Reset.

The SLEEP instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum Sleep time before a WDT wake-up Reset.

**FIGURE 8-11: WATCHDOG TIMER BLOCK DIAGRAM**




**Note 1:** PSA, PS<2:0> are bits in the OPTION register.

**TABLE 8-6: SUMMARY OF REGISTER ASSOCIATED WITH THE WATCHDOG TIMER**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| OPTION | $\overline{GPWU}$ | $\overline{GPPU}$ | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | 1111 1111 | 1111 1111 |

**Legend:** Shaded boxes = Not used by Watchdog Timer.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## 8.7 Time-out Sequence, Power-down and Wake-up from Sleep Status Bits (TO, PD, GPWUF)

The $\overline{TO}$, $\overline{PD}$ and (GPWUF) bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) Reset.

**TABLE 8-7: $\overline{TO}$/$\overline{PD}$/(GPWUF) STATUS AFTER RESET**

| GPWUF | $\overline{TO}$ | $\overline{PD}$ | Reset Caused By |
|---|---|---|---|
| 0 | 0 | 0 | WDT wake-up from Sleep |
| 0 | 0 | u | WDT time-out (not from Sleep) |
| 0 | 1 | 0 | $\overline{MCLR}$ wake-up from Sleep |
| 0 | 1 | 1 | Power-up |
| 0 | u | u | $\overline{MCLR}$ not during Sleep |
| 1 | 1 | 0 | Wake-up from Sleep on pin change |

**Legend:** u = unchanged

**Note 1:** The $\overline{TO}$, $\overline{PD}$ and GPWUF bits maintain their status (u) until a Reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$, $\overline{PD}$ and GPWUF Status bits.

## 8.8 Power-down Mode (Sleep)

A device may be powered down (Sleep) and later powered up (wake-up from Sleep).

### 8.8.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low or high-impedance).

| **Note:** | A Reset generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low. |
|---|---|

For lowest current consumption while powered down, the T0CKI input should be at $V_{DD}$ or $V_{SS}$ and the GP3/$\overline{MCLR}$/$V_{PP}$ pin must be at a logic high level if $\overline{MCLR}$ is enabled.

### 8.8.2 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

5. An external Reset input on GP3/$\overline{MCLR}$/$V_{PP}$ pin, when configured as $\overline{MCLR}$.
6. A Watchdog Timer Time-out Reset (if WDT was enabled).
7. A change on input pin GP0, GP1 and GP3 when wake-up on change is enabled.

These events cause a device Reset. The $\overline{TO}$, $\overline{PD}$ and GPWUF bits can be used to determine the cause of device Reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The GPWUF bit indicates a change in state while in Sleep at pins GP0, GP1 and GP3 (since the last file or bit operation on GPIO port).

| **Note:** | **Caution:** Right before entering Sleep, read the input pins. When in Sleep, wake up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately even if no pins change while in Sleep mode. |
|---|---|

The WDT is cleared when the device wakes from Sleep, regardless of the wake-up source.

## 8.9 Program Verification/Code Protection

If the code protection bits have not been programmed, the on-chip program and data memory can be read out for verification purposes.

The first 64 locations and the last location (OSCCAL) can be read, regardless of the setting of the program memory's code protection bit. If the code protect bit specific to the FLASH data memory is programmed, then none of the contents of this memory region can be verified externally.

## 8.10 ID Locations

Four memory locations are designated as ID locations where users can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations. The upper bits should be programmed as 0s.

## 8.11 In-Circuit Serial Programming™

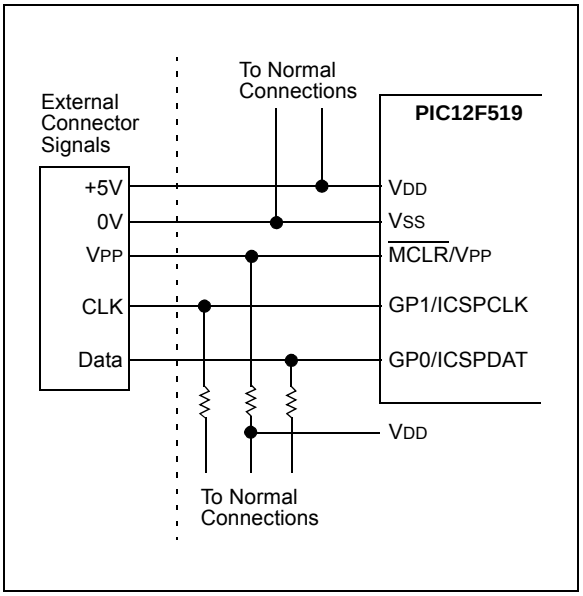
The PIC12F519 device can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows users to manufacture boards with unprogrammed PIC12F519 device and then program the PIC12F519 device just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The PIC12F519 device is placed into a Program/Verify mode by holding the GP1 and GP0 pins low while raising the $\overline{MCLR}$ ($V_{PP}$) pin from $V_{IL}$ to $V_{IHH}$ (see programming specification). The GP1 pin becomes the programming clock, and the GP0 pin becomes the programming data. Both GP1 and GP0 pins are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending if the command was a Load or a Read. For complete details of serial programming, please refer to the "*PIC12F519 Memory Programming Specification*," (DS41316).

A typical In-Circuit Serial Programming connection is shown in Figure 8-12.

**FIGURE 8-12: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION**





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## 9.0 INSTRUCTION SET SUMMARY

The PIC12F519 instruction set is highly orthogonal and is comprised of three basic categories.

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC12F519 instruction is a 12-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 9-1, while the various opcode fields are summarized in Table 9-1.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

**TABLE 9-1: OPCODE FIELD DESCRIPTIONS**

| Field | Description |
|---|---|
| f | Register file address (0x00 to 0x7F) |
| W | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= 0 or 1)<br>The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select;<br>d = 0 (store result in W)<br>d = 1 (store result in file register 'f')<br>Default is d = 1 |
| label | Label name |
| TOS | Top-of-Stack |
| PC | Program Counter |
| WDT | Watchdog Timer counter |
| $\overline{TO}$ | Time-out bit |
| $\overline{PD}$ | Power-down bit |
| dest | Destination, either the W register or the specified register file location |
| [ ] | Options |
| ( ) | Contents |
| → | Assigned to |
| < > | Register bit field |
| ∈ | In the set of |
| italics | User defined term (font is courier) |

All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Figure 9-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

**FIGURE 9-1: GENERAL FORMAT FOR INSTRUCTIONS**

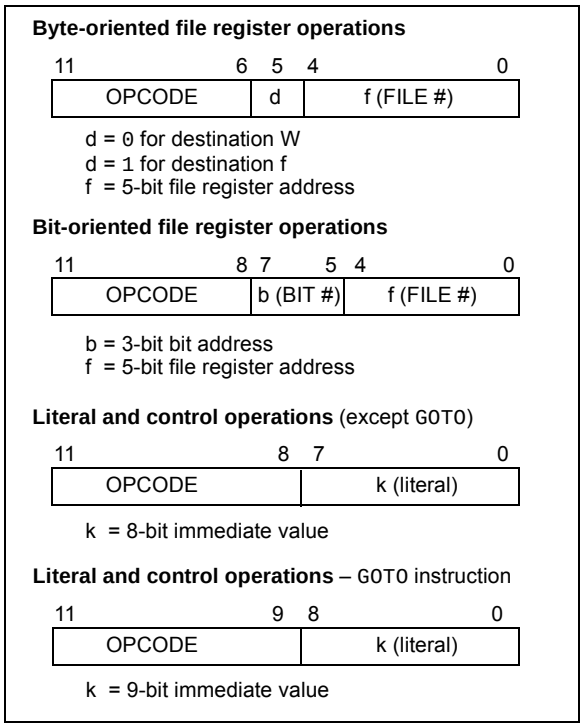

**TABLE 9-2: INSTRUCTION SET SUMMARY**

| Mnemonic, Operands | | Description | Cycles | 12-Bit Opcode | | | Status Affected | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | MSb | | LSb | | |
| ADDWF | f, d | Add W and f | 1 | 0001 | 11df | ffff | C, DC, Z | **1, 2, 4** |
| ANDWF | f, d | AND W with f | 1 | 0001 | 01df | ffff | Z | **2, 4** |
| CLRF | f | Clear f | 1 | 0000 | 011f | ffff | Z | **4** |
| CLRW | – | Clear W | 1 | 0000 | 0100 | 0000 | Z | |
| COMF | f, d | Complement f | 1 | 0010 | 01df | ffff | Z | |
| DECF | f, d | Decrement f | 1 | 0000 | 11df | ffff | Z | **2, 4** |
| DECFSZ | f, d | Decrement f, Skip if 0 | 1(2) | 0010 | 11df | ffff | None | **2, 4** |
| INCF | f, d | Increment f | 1 | 0010 | 10df | ffff | Z | **2, 4** |
| INCFSZ | f, d | Increment f, Skip if 0 | 1(2) | 0011 | 11df | ffff | None | **2, 4** |
| IORWF | f, d | Inclusive OR W with f | 1 | 0001 | 00df | ffff | Z | **2, 4** |
| MOVF | f, d | Move f | 1 | 0010 | 00df | ffff | Z | **2, 4** |
| MOVWF | f | Move W to f | 1 | 0000 | 001f | ffff | None | **1, 4** |
| NOP | – | No Operation | 1 | 0000 | 0000 | 0000 | None | |
| RLF | f, d | Rotate left f through Carry | 1 | 0011 | 01df | ffff | C | **2, 4** |
| RRF | f, d | Rotate right f through Carry | 1 | 0011 | 00df | ffff | C | **2, 4** |
| SUBWF | f, d | Subtract W from f | 1 | 0000 | 10df | ffff | C, DC, Z | **1, 2, 4** |
| SWAPF | f, d | Swap f | 1 | 0011 | 10df | ffff | None | **2, 4** |
| XORWF | f, d | Exclusive OR W with f | 1 | 0001 | 10df | ffff | Z | **2, 4** |
| **BIT-ORIENTED FILE REGISTER OPERATIONS** | | | | | | | | |
| BCF | f, b | Bit Clear f | 1 | 0100 | bbbf | ffff | None | **2, 4** |
| BSF | f, b | Bit Set f | 1 | 0101 | bbbf | ffff | None | **2, 4** |
| BTFSC | f, b | Bit Test f, Skip if Clear | 1(2) | 0110 | bbbf | ffff | None | |
| BTFSS | f, b | Bit Test f, Skip if Set | 1(2) | 0111 | bbbf | ffff | None | |
| **LITERAL AND CONTROL OPERATIONS** | | | | | | | | |
| ANDLW | k | AND literal with W | 1 | 1110 | kkkk | kkkk | Z | |
| CALL | k | Call Subroutine | 2 | 1001 | kkkk | kkkk | None | **1** |
| CLRWDT | – | Clear Watchdog Timer | 1 | 0000 | 0000 | 0100 | $\overline{TO}$, $\overline{PD}$ | |
| GOTO | k | Unconditional branch | 2 | 101k | kkkk | kkkk | None | |
| IORLW | k | Inclusive OR literal with W | 1 | 1101 | kkkk | kkkk | Z | |
| MOVLW | k | Move literal to W | 1 | 1100 | kkkk | kkkk | None | |
| OPTION | – | Load OPTION register | 1 | 0000 | 0000 | 0010 | None | |
| RETLW | k | Return, place literal in W | 2 | 1000 | kkkk | kkkk | None | |
| SLEEP | – | Go into Standby mode | 1 | 0000 | 0000 | 0011 | $\overline{TO}$, $\overline{PD}$ | |
| TRISGPIO | f | Load TRISGPIO register | 1 | 0000 | 0000 | 0fff | None | **3** |
| XORLW | k | Exclusive OR literal to W | 1 | 1111 | kkkk | kkkk | Z | |

**Note 1:** The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. See **Section 4.6 "Program Counter"**.

**2:** When an I/O register is modified as a function of itself (e.g. MOVF GPIO, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

**3:** The instruction TRIS f, where f = 6, causes the contents of the W register to be written to the tri-state latches of GPIO. A '1' forces the pin to a high-impedance state and disables the output buffers.

**4:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).


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| ADDWF | Add W and f |
|---|---|
| Syntax: | [ *label* ] ADDWF f,d |
| Operands: | 0 ≤ f ≤ 31<br>d ∈ [0,1] |
| Operation: | (W) + (f) → (dest) |
| Status Affected: | C, DC, Z |
| Description: | Add the contents of the W register and register 'f'. If 'd' is'0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

| ANDLW | AND literal with W |
|---|---|
| Syntax: | [ *label* ] ANDLW k |
| Operands: | 0 ≤ k ≤ 255 |
| Operation: | (W).AND. (k) → (W) |
| Status Affected: | Z |
| Description: | The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register. |

| ANDWF | AND W with f |
|---|---|
| Syntax: | [ *label* ] ANDWF f,d |
| Operands: | 0 ≤ f ≤ 31<br>d ∈ [0,1] |
| Operation: | (W) .AND. (f) → (dest) |
| Status Affected: | Z |
| Description: | The contents of the W register are AND'ed with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

| BCF | Bit Clear f |
|---|---|
| Syntax: | [ *label* ] BCF f,b |
| Operands: | 0 ≤ f ≤ 31<br>0 ≤ b ≤ 7 |
| Operation: | 0 → (f<b>) |
| Status Affected: | None |
| Description: | Bit 'b' in register 'f' is cleared. |

| BSF | Bit Set f |
|---|---|
| Syntax: | [ *label* ] BSF f,b |
| Operands: | 0 ≤ f ≤ 31<br>0 ≤ b ≤ 7 |
| Operation: | 1 → (f<b>) |
| Status Affected: | None |
| Description: | Bit 'b' in register 'f' is set. |

| BTFSC | Bit Test f, Skip if Clear |
|---|---|
| Syntax: | [ *label* ] BTFSC f,b |
| Operands: | 0 ≤ f ≤ 31<br>0 ≤ b ≤ 7 |
| Operation: | skip if (f<b>) = 0 |
| Status Affected: | None |
| Description: | If bit 'b' in register 'f' is '0', then the next instruction is skipped.<br>If bit 'b' is '0', then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a two-cycle instruction. |

| BTFSS | Bit Test f, Skip if Set |
|---|---|
| Syntax: | [ *label* ] BTFSS f,b |
| Operands: | $0 \le f \le 31$<br>$0 \le b < 7$ |
| Operation: | skip if (f<b>) = 1 |
| Status Affected: | None |
| Description: | If bit 'b' in register 'f' is '1', then the next instruction is skipped.<br>If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a two-cycle instruction. |

| CALL | Subroutine Call |
|---|---|
| Syntax: | [ *label* ] CALL k |
| Operands: | $0 \le k \le 255$ |
| Operation: | (PC) + 1→ Top-of-Stack;<br>k → PC<7:0>;<br>(STATUS<6:5>) → PC<10:9>;<br>0 → PC<8> |
| Status Affected: | None |
| Description: | Subroutine call. First, return address (PC + 1) is pushed onto the stack. The eight-bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two-cycle instruction. |

| CLRF | Clear f |
|---|---|
| Syntax: | [ *label* ] CLRF f |
| Operands: | $0 \le f \le 31$ |
| Operation: | 00h → (f);<br>1 → Z |
| Status Affected: | Z |
| Description: | The contents of register 'f' are cleared and the Z bit is set. |

| CLRW | Clear W |
|---|---|
| Syntax: | [ *label* ] CLRW |
| Operands: | None |
| Operation: | 00h → (W);<br>1 → Z |
| Status Affected: | Z |
| Description: | The W register is cleared. Zero bit (Z) is set. |

| CLRWDT | Clear Watchdog Timer |
|---|---|
| Syntax: | [ *label* ] CLRWDT |
| Operands: | None |
| Operation: | 00h → WDT;<br>0 → WDT prescaler (if assigned);<br>1 → $\overline{TO}$;<br>1 → $\overline{PD}$ |
| Status Affected: | $\overline{TO}$, $\overline{PD}$ |
| Description: | The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set. |

| COMF | Complement f |
|---|---|
| Syntax: | [ *label* ] COMF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | $(\bar{f}) \rightarrow$ (dest) |
| Status Affected: | Z |
| Description: | The contents of register 'f' are complemented. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |


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| DECF | Decrement f |
|---|---|
| Syntax: | [ *label* ] DECF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) – 1 → (dest) |
| Status Affected: | Z |
| Description: | Decrement register ‘f’. If ‘d’ is ‘0’, the result is stored in the W register. If ‘d’ is ‘1’, the result is stored back in register ‘f’. |

| DECFSZ | Decrement f, Skip if 0 |
|---|---|
| Syntax: | [ *label* ] DECFSZ f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) – 1 → d; skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register ‘f’ are decremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.<br>If the result is ‘0’, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction. |

| GOTO | Unconditional Branch |
|---|---|
| Syntax: | [ *label* ] GOTO k |
| Operands: | $0 \le k \le 511$ |
| Operation: | k → PC<8:0>;<br>STATUS<6:5> → PC<10:9> |
| Status Affected: | None |
| Description: | GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two-cycle instruction. |

| INCF | Increment f |
|---|---|
| Syntax: | [ *label* ] INCF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) + 1 → (dest) |
| Status Affected: | Z |
| Description: | The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’. |

| INCFSZ | Increment f, Skip if 0 |
|---|---|
| Syntax: | [ *label* ] INCFSZ f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) + 1 → (dest), skip if result = 0 |
| Status Affected: | None |
| Description: | The contents of register ‘f’ are incremented. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed back in register ‘f’.<br>If the result is ‘0’, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction. |

| IORLW | Inclusive OR literal with W |
|---|---|
| Syntax: | [ *label* ] IORLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | (W) .OR. (k) → (W) |
| Status Affected: | Z |
| Description: | The contents of the W register are OR’ed with the eight-bit literal ‘k’. The result is placed in the W register. |

| IORWF | Inclusive OR W with f |
|---|---|
| Syntax: | [ *label* ] IORWF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (W).OR. (f) → (dest) |
| Status Affected: | Z |
| Description: | Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. |

| MOVF | Move f |
|---|---|
| Syntax: | [ *label* ] MOVF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) → (dest) |
| Status Affected: | Z |
| Description: | The contents of register 'f' are moved to destination 'd'. If 'd' is '0', destination is the W register. If 'd' is '1', the destination is file register 'f'. 'd' = 1 is useful as a test of a file register, since status flag Z is affected. |

| MOVLW | Move Literal to W |
|---|---|
| Syntax: | [ *label* ] MOVLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | k → (W) |
| Status Affected: | None |
| Description: | The eight-bit literal 'k' is loaded into the W register. The "don't cares" will assembled as '0's. |

| MOVWF | Move W to f |
|---|---|
| Syntax: | [ *label* ] MOVWF f |
| Operands: | $0 \le f \le 31$ |
| Operation: | (W) → (f) |
| Status Affected: | None |
| Description: | Move data from the W register to register 'f'. |

| NOP | No Operation |
|---|---|
| Syntax: | [ *label* ] NOP |
| Operands: | None |
| Operation: | No operation |
| Status Affected: | None |
| Description: | No operation. |

| OPTION | Load OPTION Register |
|---|---|
| Syntax: | [ *label* ] Option |
| Operands: | None |
| Operation: | (W) → Option |
| Status Affected: | None |
| Description: | The content of the W register is loaded into the OPTION register. |


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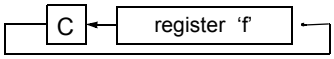
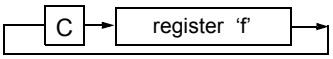
| RETLW | Return with Literal in W |
|---|---|
| Syntax: | [ *label* ] RETLW k |
| Operands: | $0 \le k \le 255$ |
| Operation: | $k \rightarrow (W)$;<br>$TOS \rightarrow PC$ |
| Status Affected: | None |
| Description: | The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction. |

| RLF | Rotate Left f through Carry |
|---|---|
| Syntax: | [ *label* ] RLF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | See description below |
| Status Affected: | C |
| Description: | The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'. |




| RRF | Rotate Right f through Carry |
|---|---|
| Syntax: | [ *label* ] RRF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | See description below |
| Status Affected: | C |
| Description: | The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'. |




| SLEEP | Enter SLEEP Mode |
|---|---|
| Syntax: | [*label* ] SLEEP |
| Operands: | None |
| Operation: | 00h → WDT;<br>0 → WDT prescaler;<br>1 → $\overline{TO}$;<br>0 → $\overline{PD}$ |
| Status Affected: | $\overline{TO}$, $\overline{PD}$, GPWUF |
| Description: | Time-out Status bit ($\overline{TO}$) is set. The Power-down Status bit ($\overline{PD}$) is cleared.<br>GPWUF is unaffected.<br>The WDT and its prescaler are cleared.<br>The processor is put into Sleep mode with the oscillator stopped. See **Section 8.8 "Power-down Mode (Sleep)"** on Sleep for more details. |

| SUBWF | Subtract W from f |
|---|---|
| Syntax: | [*label* ] SUBWF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f) – (W) → (dest) |
| Status Affected: | C, DC, Z |
| Description: | Subtract (two's complement method) the W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |

| SWAPF | Swap Nibbles in f |
|---|---|
| Syntax: | [ *label* ] SWAPF f,d |
| Operands: | $0 \le f \le 31$<br>$d \in [0,1]$ |
| Operation: | (f<3:0>) → (dest<7:4>);<br>(f<7:4>) → (dest<3:0>) |
| Status Affected: | None |
| Description: | The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W register. If 'd' is '1', the result is placed in register 'f'. |

| TRIS | Load TRIS Register |
|---|---|
| Syntax: | [ *label* ] TRIS f |
| Operands: | f = 6 |
| Operation: | (W) → TRIS register f |
| Status Affected: | None |
| Description: | TRIS register 'f' (f = 6 or 7) is loaded with the contents of the W register. |

| XORLW | Exclusive OR literal with W |
|---|---|
| Syntax: | [*label* ] XORLW k |
| Operands: | 0 ≤ k ≤ 255 |
| Operation: | (W) .XOR. k → (W) |
| Status Affected: | Z |
| Description: | The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register. |

| XORWF | Exclusive OR W with f |
|---|---|
| Syntax: | [ *label* ] XORWF f,d |
| Operands: | 0 ≤ f ≤ 31<br>d ∈ [0,1] |
| Operation: | (W) .XOR. (f) → (dest) |
| Status Affected: | Z |
| Description: | Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'. |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## 10.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C18 and MPLAB C30 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD 2
- Device Programmers
  - PICSTART® Plus Development Programmer
  - MPLAB PM3 Device Programmer
  - PICkit™ 2 Development Programmer
- Low-Cost Demonstration and Development Boards and Evaluation Kits

### 10.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
  - Simulator
  - Programmer (sold separately)
  - Emulator (sold separately)
  - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Visual device initializer for easy register initialization
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as HI-TECH Software C Compilers and IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - Source files (assembly or C)
  - Mixed assembly and C
  - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

## 10.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

## 10.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

## 10.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 10.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

## 10.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.


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## 10.7 MPLAB ICE 2000 High-Performance In-Circuit Emulator

The MPLAB ICE 2000 In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers. Software control of the MPLAB ICE 2000 In-Circuit Emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The architecture of the MPLAB ICE 2000 In-Circuit Emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE 2000 In-Circuit Emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows® 32-bit operating system were chosen to best make these features available in a simple, unified application.

## 10.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC® and MCU devices. It debugs and programs PIC® and dsPIC® Flash microcontrollers with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The MPLAB REAL ICE probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with the popular MPLAB ICD 2 system (RJ11) or with the new high speed, noise tolerant, low-voltage differential signal (LVDS) interconnection (CAT5).

MPLAB REAL ICE is field upgradeable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added, such as software breakpoints and assembly code trace. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, real-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 10.9 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low-cost, run-time development tool, connecting to the host PC via an RS-232 or high-speed USB interface. This tool is based on the Flash PIC MCUs and can be used to develop for these and other PIC MCUs and dsPIC DSCs. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the Flash devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost-effective, in-circuit Flash debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single stepping and watching variables, and CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real time. MPLAB ICD 2 also serves as a development programmer for selected PIC devices.

## 10.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDMIN}$ and $V_{DDMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an SD/MMC card for file storage and secure data applications.

## 10.11 PICSTART Plus Development Programmer

The PICSTART Plus Development Programmer is an easy-to-use, low-cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus Development Programmer supports most PIC devices in DIP packages up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus Development Programmer is CE compliant.

## 10.12 PICkit 2 Development Programmer

The PICkit™ 2 Development Programmer is a low-cost programmer and selected Flash device debugger with an easy-to-use interface for programming many of Microchip's baseline, mid-range and PIC18F families of Flash memory microcontrollers. The PICkit 2 Starter Kit includes a prototyping development board, twelve sequential lessons, software and HI-TECH's PICC™ Lite C compiler, and is designed to help get up to speed quickly using PIC® microcontrollers. The kit provides everything needed to program, evaluate and develop applications using Microchip's powerful, mid-range Flash memory family of microcontrollers.

## 10.13 Demonstration, Development and Evaluation Boards

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Check the Microchip web page (www.microchip.com) and the latest *"Product Selector Guide"* (DS00148) for the complete list of demonstration, development and evaluation kits.


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## 11.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +6.5V
Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ ..... 0 to +13.5V
Voltage on all other pins with respect to $V_{SS}$ ..... -0.3V to ($V_{DD}$ + 0.3V)
Total power dissipation(1) ..... 700 mW
Max. current out of $V_{SS}$ pin ..... 200 mA
Max. current into $V_{DD}$ pin ..... 150 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 25 mA
Max. output current sourced by I/O port ..... 75 mA
Max. output current sunk by I/O port ..... 75 mA

**Note 1:** Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

†NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**FIGURE 11-1: PIC12F519 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C**

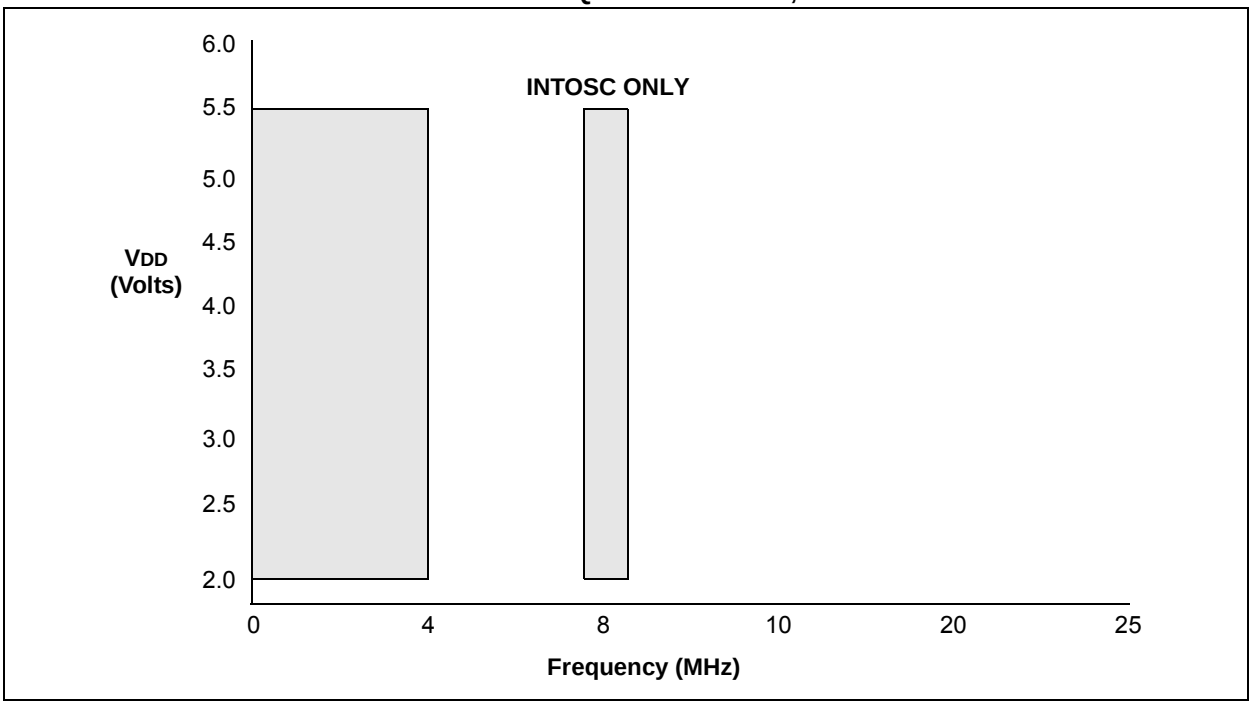
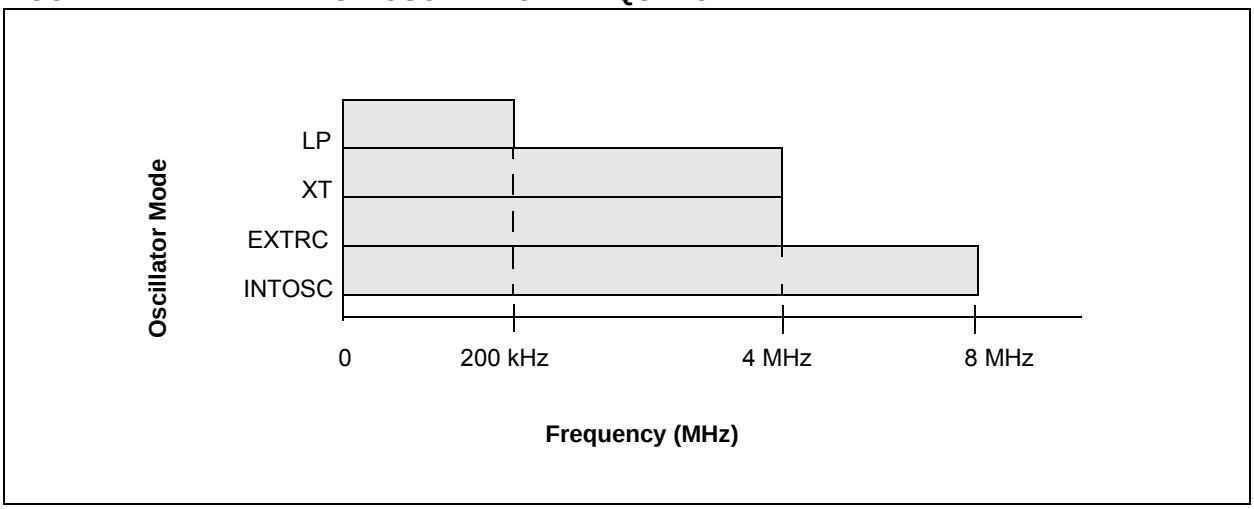



**FIGURE 11-2: MAXIMUM OSCILLATOR FREQUENCY TABLE**





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## 11.1 DC Characteristics

**TABLE 11-1: DC CHARACTERISTICS: PIC12F519 (INDUSTRIAL)**

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial) | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 2.0 | | 5.5 | V | See **Figure 11-1** |
| D002 | VDR | **RAM Data Retention Voltage(2)** | — | 1.5* | — | V | Device in Sleep mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See **Section 8.4 "Power-on Reset (POR)"** for details |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See **Section 8.4 "Power-on Reset (POR)"** for details |
| D005 | IDDP | **Supply Current** During Prog/ Erase. | — | 250* | — | µA | |
| D010 | IDD | **Supply Current(3,4)** | —<br>— | 175<br>400 | 250<br>700 | µA<br>µA | FOSC = 4 MHz, VDD = 2.0V<br>FOSC = 4 MHz, VDD = 5.0V |
| | | | —<br>— | 250<br>0.75 | 400<br>1.2 | µA<br>mA | FOSC = 8 MHz, VDD = 2.0V<br>FOSC = 8 MHz, VDD = 5.0V |
| | | | —<br>— | 11<br>38 | 20<br>54 | µA<br>µA | FOSC = 32 kHz, VDD = 2.0V<br>FOSC = 32 kHz, VDD = 5.0V |
| D020 | IPD | **Power-down Current(5)** | —<br>— | 0.1<br>0.35 | 1.2<br>2.2 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |
| D022 | IWDT | **WDT Current** | —<br>— | 1.0<br>7.0 | 3.0<br>16.0 | µA<br>µA | VDD = 2.0V<br>VDD = 5.0V |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

**4:** The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail for external clock modes; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

**5:** For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

**TABLE 11-2: DC CHARACTERISTICS: PIC12F519 (Extended)**

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 2.0 | | 5.5 | V | See **Figure 11-1** |
| D002 | VDR | **RAM Data Retention Voltage(2)** | — | 1.5* | — | V | Device in Sleep mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See **Section 8.4 "Power-on Reset (POR)"** for details |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See **Section 8.4 "Power-on Reset (POR)"** for details |
| D005 | IDDP | **Supply Current** During Prog/ Erase. | — | 250* | — | μA | |
| D010 | IDD | **Supply Current(3,4)** | —<br>— | 175<br>400 | 250<br>700 | μA<br>mA | FOSC = 4 MHz, VDD = 2.0V<br>FOSC = 4 MHz, VDD = 5.0V |
| | | | —<br>— | 250<br>0.75 | 400<br>1.2 | μA<br>mA | FOSC = 8 MHz, VDD = 2.0V<br>FOSC = 8 MHz, VDD = 5.0V |
| | | | —<br>— | 11<br>38 | 24<br>110 | μA<br>μA | FOSC = 32 kHz, VDD = 2.0V<br>FOSC = 32 kHz, VDD = 5.0V |
| D020 | IPD | **Power-down Current(5)** | —<br>— | 0.1<br>0.35 | 9.0<br>15.0 | μA<br>μA | VDD = 2.0V<br>VDD = 5.0V |
| D022 | IWDT | **WDT Current** | —<br>— | 1.0<br>7.0 | 18<br>22 | μA<br>μA | VDD = 2.0V<br>VDD = 5.0V |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**2:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

**4:** The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail for external clock modes; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

**5:** For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.


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## TABLE 11-3: DC CHARACTERISTICS: PIC12F519 (Industrial, Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating voltage VDD range as described in DC specification. | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | | | | | |
| D030 | | with TTL buffer | Vss | — | 0.8 | V | For all 4.5 ≤ VDD ≤ 5.5V |
| D030A | | | Vss | — | 0.15 VDD | V | Otherwise |
| D031 | | with Schmitt Trigger buffer | Vss | — | 0.15 VDD | V | |
| D032 | | $\overline{MCLR}$, T0CKI | Vss | — | 0.15 VDD | V | |
| D033 | | OSC1 (EXTRC mode) | Vss | — | 0.15 VDD | V | **(Note 1)** |
| D033A | | OSC1 (XT and LP modes) | Vss | — | 0.3 | V | |
| | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | | — | | | |
| D040 | | with TTL buffer | 2.0 | — | VDD | V | 4.5 ≤ VDD ≤ 5.5V |
| D040A | | | 0.25 VDD + 0.8V | — | VDD | V | Otherwise |
| D041 | | with Schmitt Trigger buffer | 0.85 VDD | — | VDD | V | For entire VDD range |
| D042 | | MCLR, T0CKI | 0.85 VDD | — | VDD | V | |
| D042A | | OSC1 (EXTRC mode) | 0.85 VDD | — | VDD | V | **(Note 1)** |
| D043 | | OSC1 (XT and LP modes) | 1.6 | — | VDD | V | |
| D070 | IPUR | **I/O PORT weak pull-up current(5)** | 50 | 250 | 400 | µA | VDD = 5V, VPIN = VSS |
| | IIL | **Input Leakage Current(2), (3)** | | | | | |
| D060 | | I/O ports | — | — | ±1 | µA | Vss ≤ VPIN ≤ VDD, Pin at high-impedance |
| D061 | | GP3/$\overline{MCLR}$(4) | — | ±0.7 | ±5 | µA | Vss ≤ VPIN ≤ VDD |
| D063 | | OSC1 | — | — | ±5 | µA | Vss ≤ VPIN ≤ VDD, XT and LP osc configuration |
| | | **Output Low Voltage** | | | | | |
| D080 | | I/O ports | — | — | 0.6 | V | IOL = 8.5 mA, VDD = 4.5V, –40°C to +85°C |
| D080A | | | — | — | 0.6 | V | IOL = 7.0 mA, VDD = 4.5V, –40°C to +125°C |
| | | **Output High Voltage** | | | | | |
| D090 | | I/O ports(3) | VDD – 0.7 | — | — | V | IOH = -3.0 mA, VDD = 4.5V, –40°C to +85°C |
| D090A | | | VDD – 0.7 | — | — | V | IOH = -2.5 mA, VDD = 4.5V, –40°C to +125°C |
| | | **Capacitive Loading Specs on Output Pins** | | | | | |
| D101 | | All I/O pins | — | — | 50 | pF | |
| | | **Flash Data Memory** | | | | | |
| D120 | ED | Byte endurance | 100K | 1M | — | E/W | –40°C ≤ TA ≤ +85°C |
| D120A | ED | Byte endurance | 10K | 100K | — | E/W | +85°C ≤ TA ≤ +125°C |
| D121 | VDRW | VDD for read/write | VMIN | — | 5.5 | V | |

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12F519 be driven with external clock in RC mode.

**2:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.

**4:** This specification applies to GP3/$\overline{MCLR}$ configured as GP3 with internal pull-up disabled.

**5:** This specification applies to all weak pull-up devices, including the weak pull-up found on GP3/$\overline{MCLR}$. The current value listed will be the same whether or not the pin is configured as GP3 with pull-up enabled or $\overline{MCLR}$.

**TABLE 11-4: PULL-UP RESISTOR RANGES**

| VDD (Volts) | Temperature (°C) | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **GP0/GP1** | | | | | |
| 2.0 | –40 | 73K | 105K | 186K | Ω |
| | 25 | 73K | 113K | 187K | Ω |
| | 85 | 82K | 123K | 190K | Ω |
| | 125 | 86K | 132K | 190K | Ω |
| 5.5 | –40 | 15K | 21K | 33K | Ω |
| | 25 | 15K | 22K | 34K | Ω |
| | 85 | 19K | 26K | 35K | Ω |
| | 125 | 23K | 29K | 35K | Ω |
| **GP3** | | | | | |
| 2.0 | –40 | 63K | 81K | 96K | Ω |
| | 25 | 77K | 93K | 116K | Ω |
| | 85 | 82K | 96K | 116K | Ω |
| | 125 | 86K | 100K | 119K | Ω |
| 5.5 | –40 | 16K | 20K | 22K | Ω |
| | 25 | 16K | 21K | 23K | Ω |
| | 85 | 24K | 25K | 28K | Ω |
| | 125 | 26K | 27K | 29K | Ω |


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## 11.2 Timing Parameter Symbology and Load Conditions – PIC12F519

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

| T | | | |
|---|---|---|---|
| F | Frequency | T | Time |

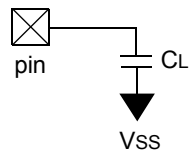
Lowercase subscripts (pp) and their meanings:

| pp | | | |
|---|---|---|---|
| 2 | to | mc | $\overline{\text{MCLR}}$ |
| ck | CLKOUT | osc | Oscillator |
| cy | Cycle time | os | OSC1 |
| drt | Device Reset Timer | t0 | T0CKI |
| io | I/O port | wdt | Watchdog Timer |

Uppercase letters and their meanings:

| S | | | |
|---|---|---|---|
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (high-impedance) | V | Valid |
| L | Low | Z | High-impedance |

**FIGURE 11-3: LOAD CONDITIONS – PIC12F519**

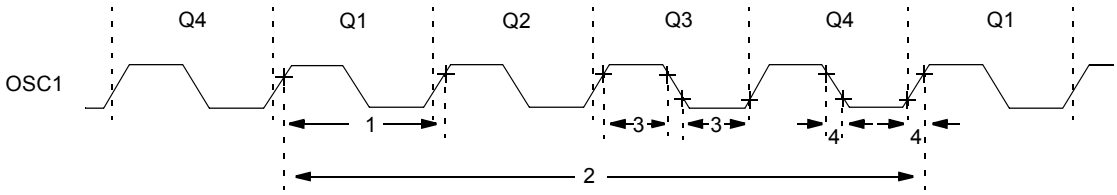



**Legend:**

$C_L$ = 50 pF for all pins except OSC2

15 pF for OSC2 in XT or LP modes when external clock is used to drive OSC1

**FIGURE 11-4: EXTERNAL CLOCK TIMING – PIC12F519**



## 11.3 AC Characteristics

**TABLE 11-5: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial),<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in **Section 11.0 "Electrical Characteristics"** | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| 1A | FOSC | External CLKIN Frequency(2) | DC | — | 4 | MHz | XT Oscillator mode |
| | | | DC | — | 200 | kHz | LP Oscillator mode |
| | | Oscillator Frequency(2) | DC | — | 4 | MHz | EXTRC Oscillator mode |
| | | | 0.1 | — | 4 | MHz | XT Oscillator mode |
| | | | DC | — | 200 | kHz | LP Oscillator mode |
| 1 | TOSC | External CLKIN Period(2) | 250 | — | — | ns | XT Oscillator mode |
| | | | 5 | — | — | μs | LP Oscillator mode |
| | | Oscillator Period(2) | 250 | — | — | ns | EXTRC Oscillator mode |
| | | | 250 | — | 10,000 | ns | XT Oscillator mode |
| | | | 5 | — | — | μs | LP Oscillator mode |
| 2 | TCY | Instruction Cycle Time | 200 | 4/FOSC | DC | ns | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 50* | — | — | ns | XT Oscillator |
| | | | 2* | — | — | μs | LP Oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT Oscillator |
| | | | — | — | 50* | ns | LP Oscillator |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.


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**TABLE 11-6: CALIBRATED INTERNAL RC FREQUENCIES**

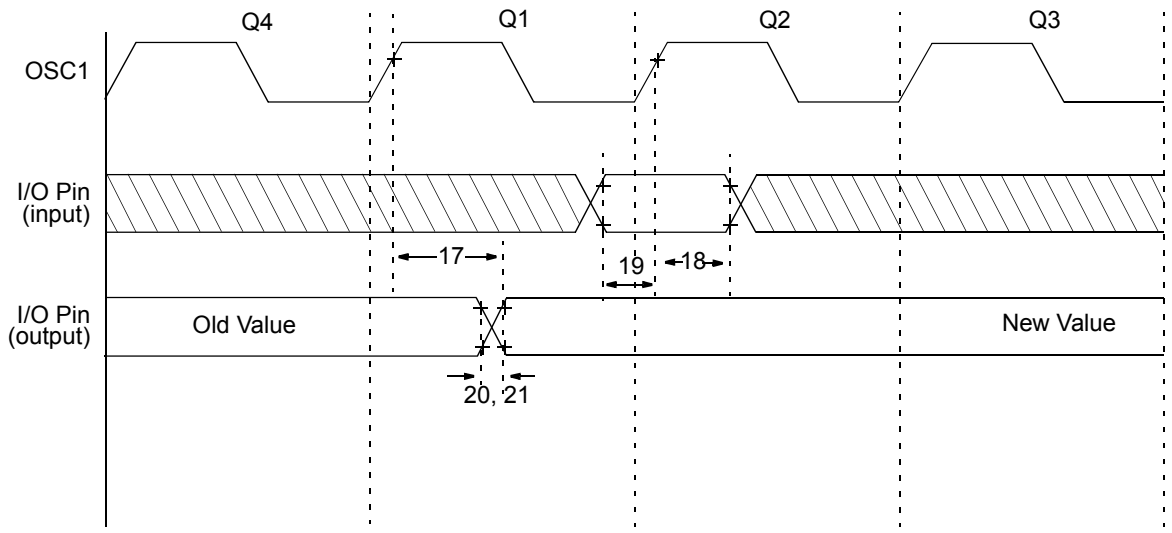
| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial),<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in Section 10.1 | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Freq. Tolerance** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| F10 | FOSC | Internal Calibrated INTOSC Frequency(1) | ±1% | 7.92 | 8.00 | 8.08 | MHz | 3.5V, 25C |
| | | | ±2% | 7.84 | 8.00 | 8.16 | MHz | 2.5V ≤ VDD ≤ 5.5V<br>0°C ≤ TA ≤ +85°C |
| | | | ±5% | 7.60 | 8.00 | 8.40 | MHz | 2.0V ≤ VDD ≤ 5.5V<br>-40°C ≤ TA ≤ +85°C (Ind.)<br>-40°C ≤ TA ≤ +125°C (Ext.) |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 uF and 0.01 uF values in parallel are recommended.

**FIGURE 11-5: I/O TIMING**




**Note:** All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

**TABLE 11-7: TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** |
| 17 | TOSH2IOV | OSC1↑ (Q1 cycle) to Port Out Valid(2), (3) | — | — | 100* | ns |
| 18 | TOSH2IOI | OSC1↑ (Q2 cycle) to Port Input Invalid (I/O in hold time)(2) | 50 | — | — | ns |
| 19 | TIOV2OSH | Port Input Valid to OSC1↑ (I/O in setup time) | 20 | — | — | ns |
| 20 | TIOR | Port Output Rise Time(3) | — | 10 | 50** | ns |
| 21 | TIOF | Port Output Fall Time(3) | — | 10 | 50** | ns |

TBD = To be determined.

* These parameters are characterized but not tested.

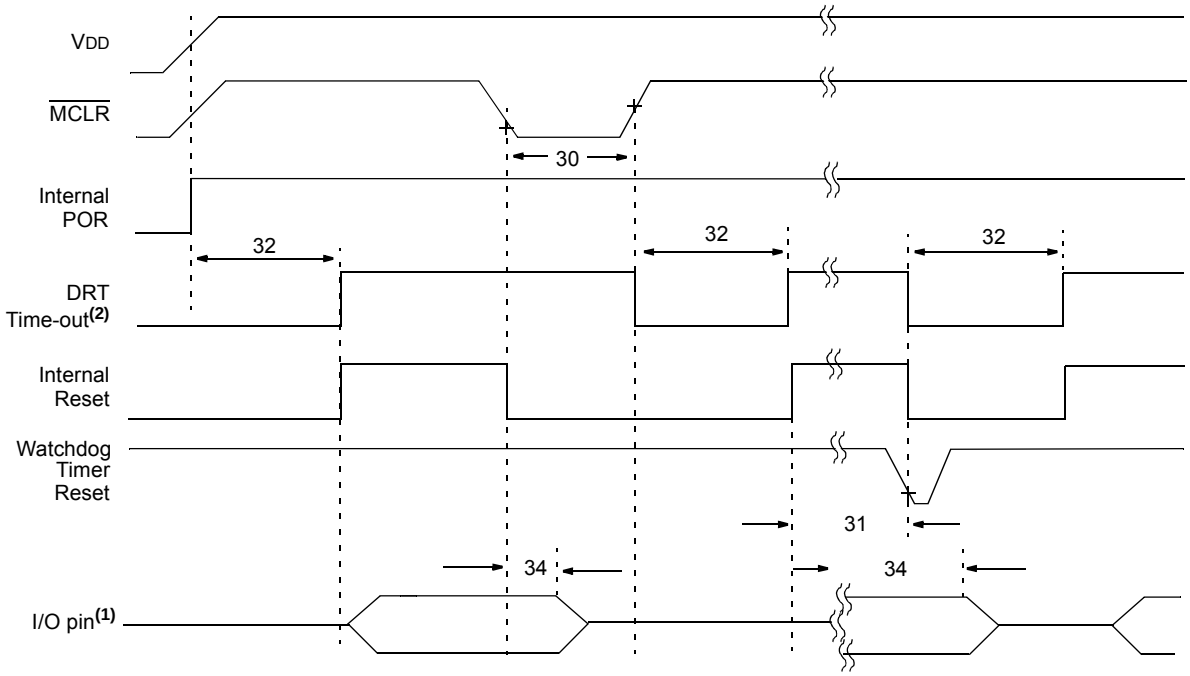
** These parameters are design targets and are not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** Measurements are taken in EXTRC mode.

**3:** See Figure 11-3 for loading conditions.

**FIGURE 11-6: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER TIMING**




**Note 1:** I/O pins must be taken out of High-Impedance mode by enabling the output drivers in software.

**2:** Runs in MCLR or WDT Reset only in XT and LP.


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**TABLE 11-8: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER – PIC12F519**

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in<br>*Section TABLE 11-3: "DC CHARACTERISTICS: PIC12F519 (Industrial, Extended)"* | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| 30 | TMCL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2000* | — | — | ns | VDD = 5.0V |
| 31 | TWDT | Watchdog Timer Time-out Period (no prescaler) | 9*<br>9* | 18*<br>18* | 30*<br>40* | ms<br>ms | VDD = 5.0V (Industrial)<br>VDD = 5.0V (Extended) |
| 32 | TDRT | Device Reset Timer Period | | | | | |
| | | Standard | 9*<br>9* | 18*<br>18* | 30*<br>40* | ms<br>ms | VDD = 5.0V (Industrial)<br>VDD = 5.0V (Extended) |
| | | Short | 0.5*<br>0.5* | 1.125*<br>1.125* | 2*<br>2.5* | ms<br>ms | VDD = 5.0V (Industrial)<br>VDD = 5.0V (Extended) |
| 34 | TIOZ | I/O High-impedance from $\overline{\text{MCLR}}$ low | — | — | 2000* | ns | |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 11-9: DRT (DEVICE RESET TIMER PERIOD)**

| Oscillator Configuration | POR Reset | Subsequent Resets |
|---|---|---|
| IntRC and ExtRC | 1 ms (typical) | 10 μs (typical) |
| XT and LP | 18 ms (typical) | 18 ms (typical) |

**FIGURE 11-7: TIMER0 CLOCK TIMINGS**

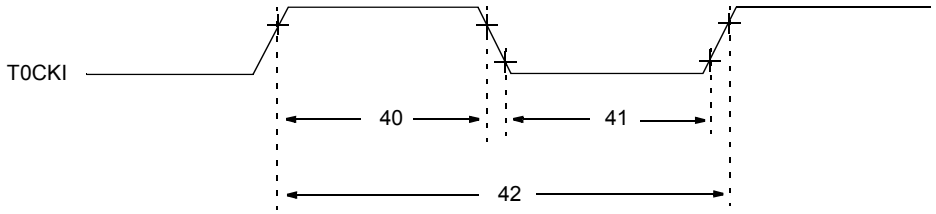

**TABLE 11-10: TIMER0 CLOCK REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in<br>***Section TABLE 11-3: "DC CHARACTERISTICS: PIC12F519 (Industrial, Extended)"*** | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width | No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | | 20 or TCY + 40* N | — | — | ns | Whichever is greater. N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**TABLE 11-11: FLASH DATA MEMORY WRITE/ERASE REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating Voltage VDD range is described in<br>**Section TABLE 11-3: "DC CHARACTERISTICS: PIC12F519 (Industrial, Extended)"** | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ(1)** | **Max.** | **Units** | **Conditions** |
| 43 | TDW | Flash Data Memory Write Cycle Time | 2 | 3.5 | 5 | ms | |
| 44 | TDE | Flash Data Memory Erase Cycle Time | 2 | 3 | 4 | ms | |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.


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## 12.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range. |
|---|---|

**"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.**

**FIGURE 12-1: TYPICAL IDD vs. FOSC OVER VDD (XT, EXTRC mode)**

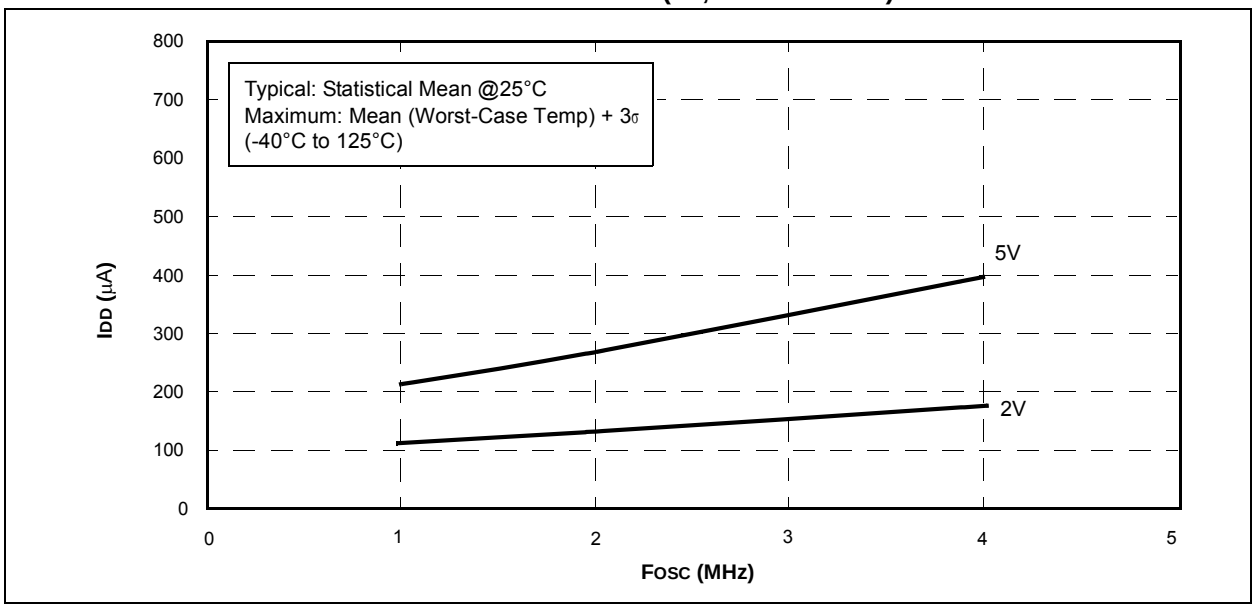


**FIGURE 12-2: MAXIMUM IDD vs. FOSC OVER VDD (XT, EXTRC mode)**

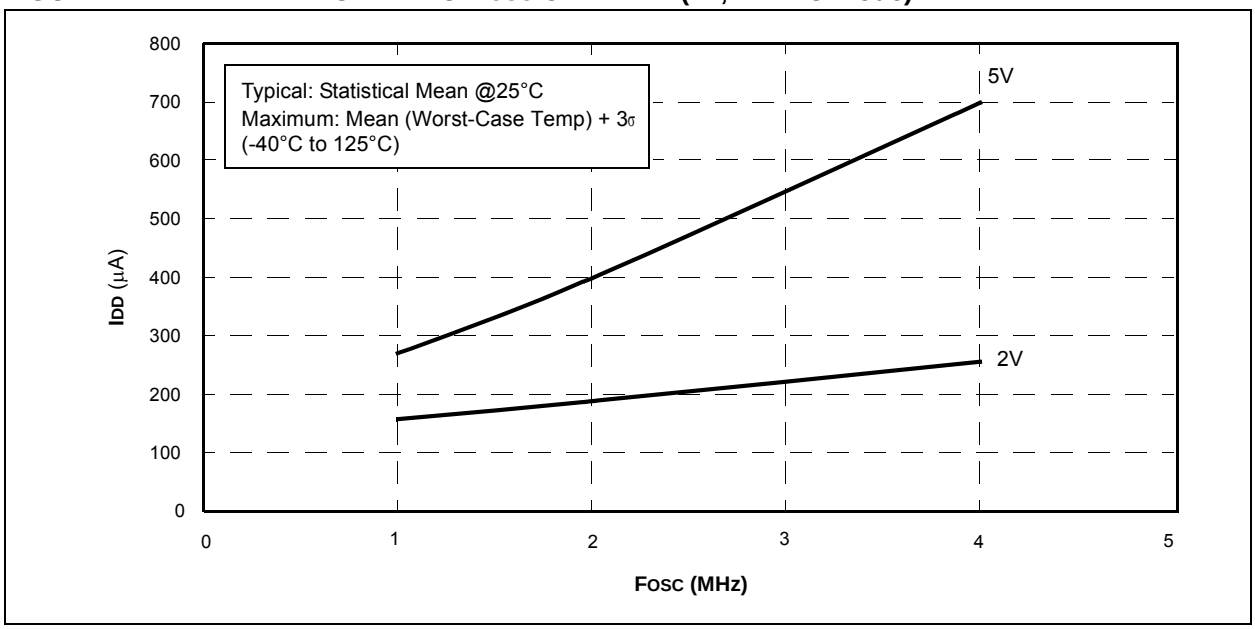

**FIGURE 12-3: IDD VS. VDD OVER FOSC (LP MODE)**

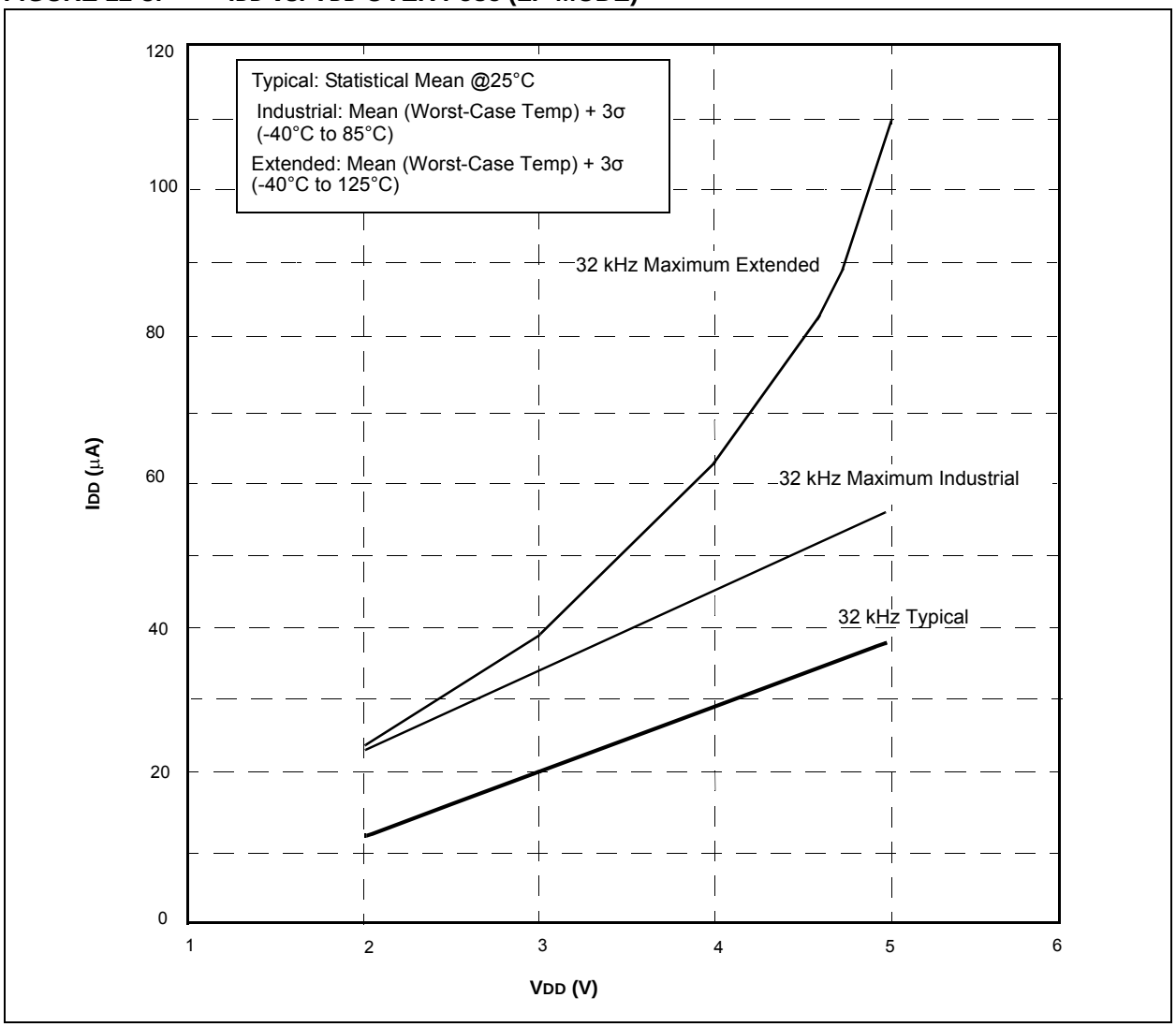



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**FIGURE 12-4: TYPICAL IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)**

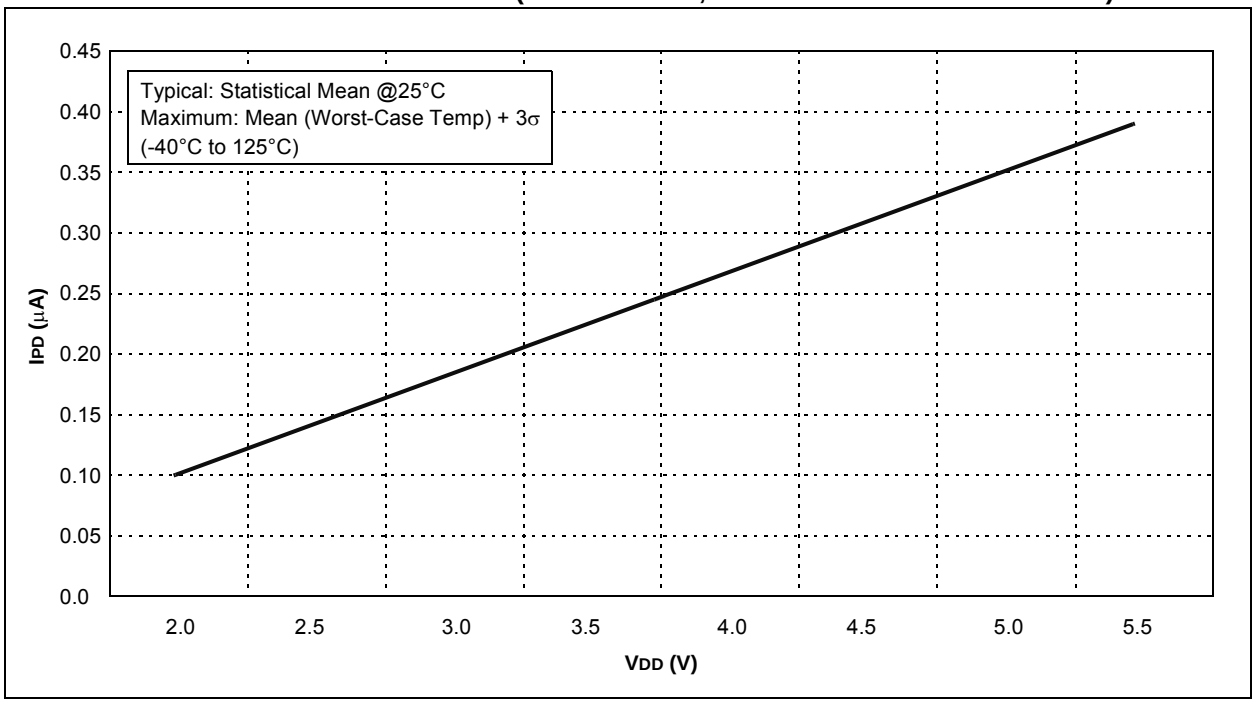


**FIGURE 12-5: MAXIMUM IPD vs. VDD (SLEEP MODE, ALL PERIPHERALS DISABLED)**

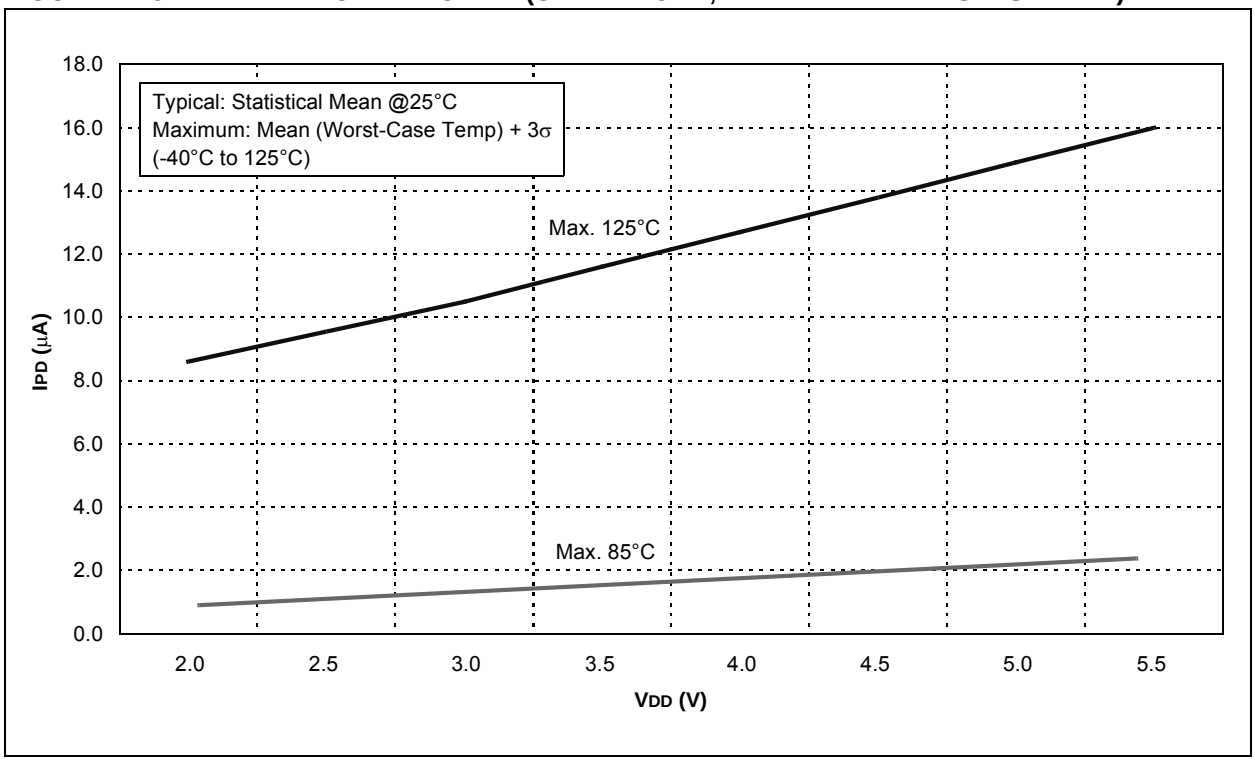

**FIGURE 12-6: TYPICAL WDT IPD vs. VDD**

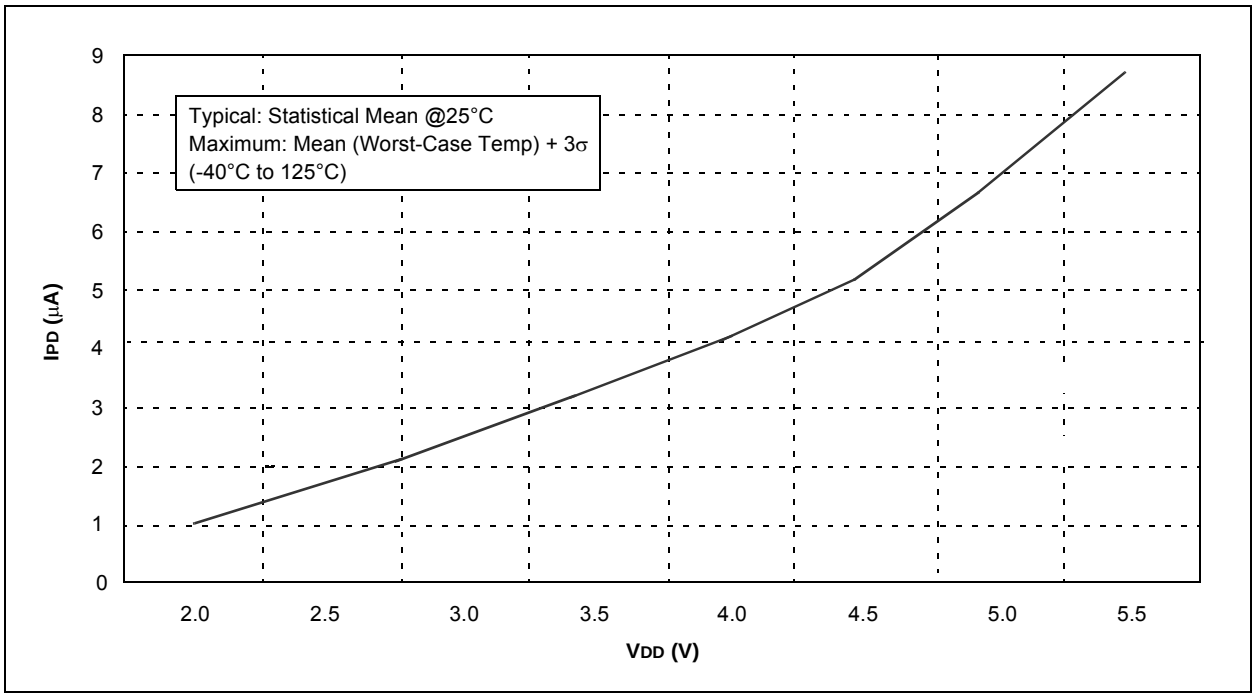


**FIGURE 12-7: MAXIMUM WDT IPD vs. VDD OVER TEMPERATURE**

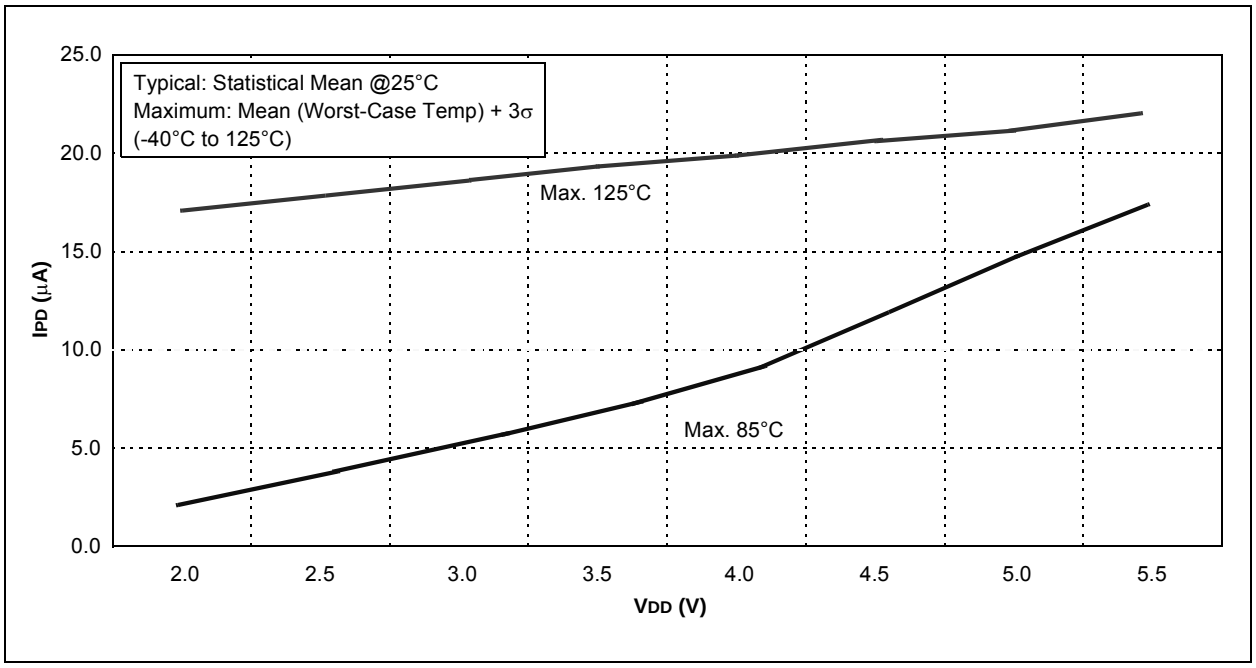



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**FIGURE 12-8: WDT TIME-OUT vs. VDD OVER TEMPERATURE (NO PRESCALER)**

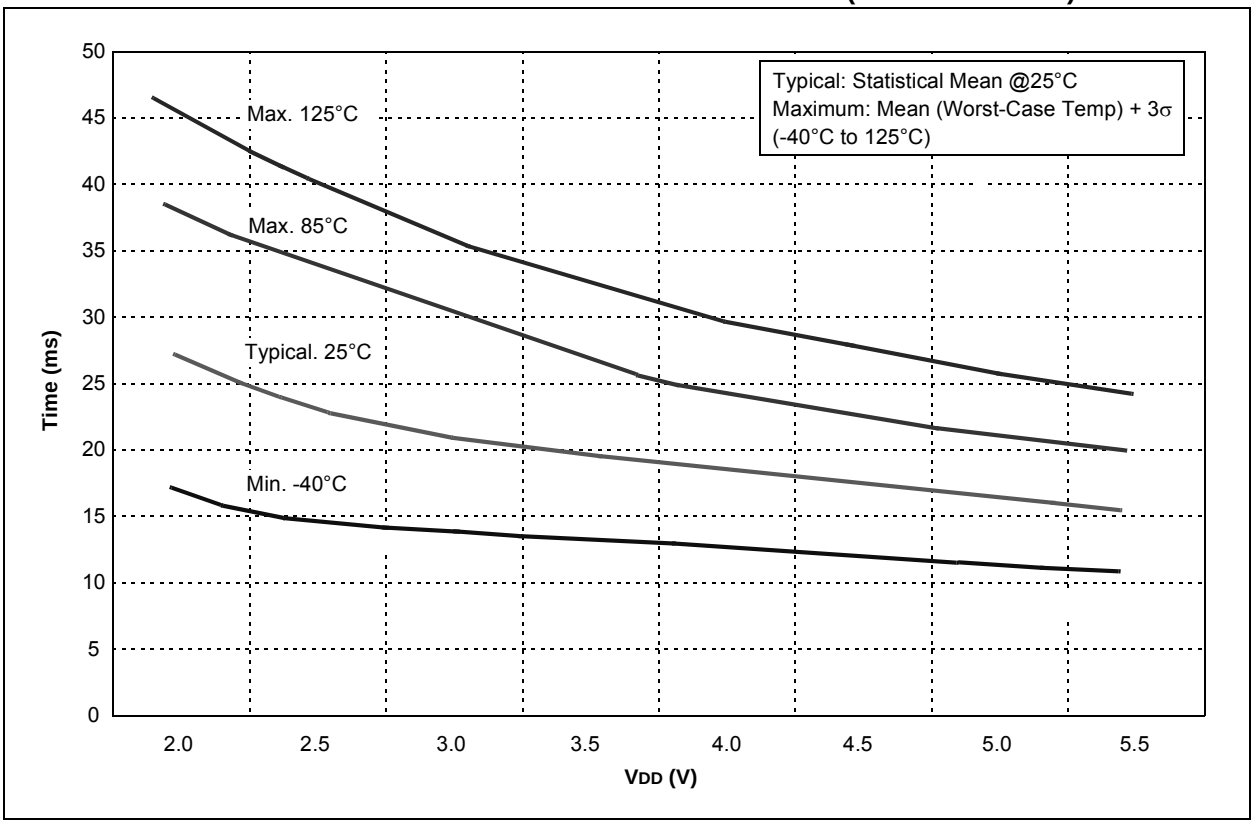


**FIGURE 12-9: VOL vs. IOL OVER TEMPERATURE (VDD = 3.0V)**

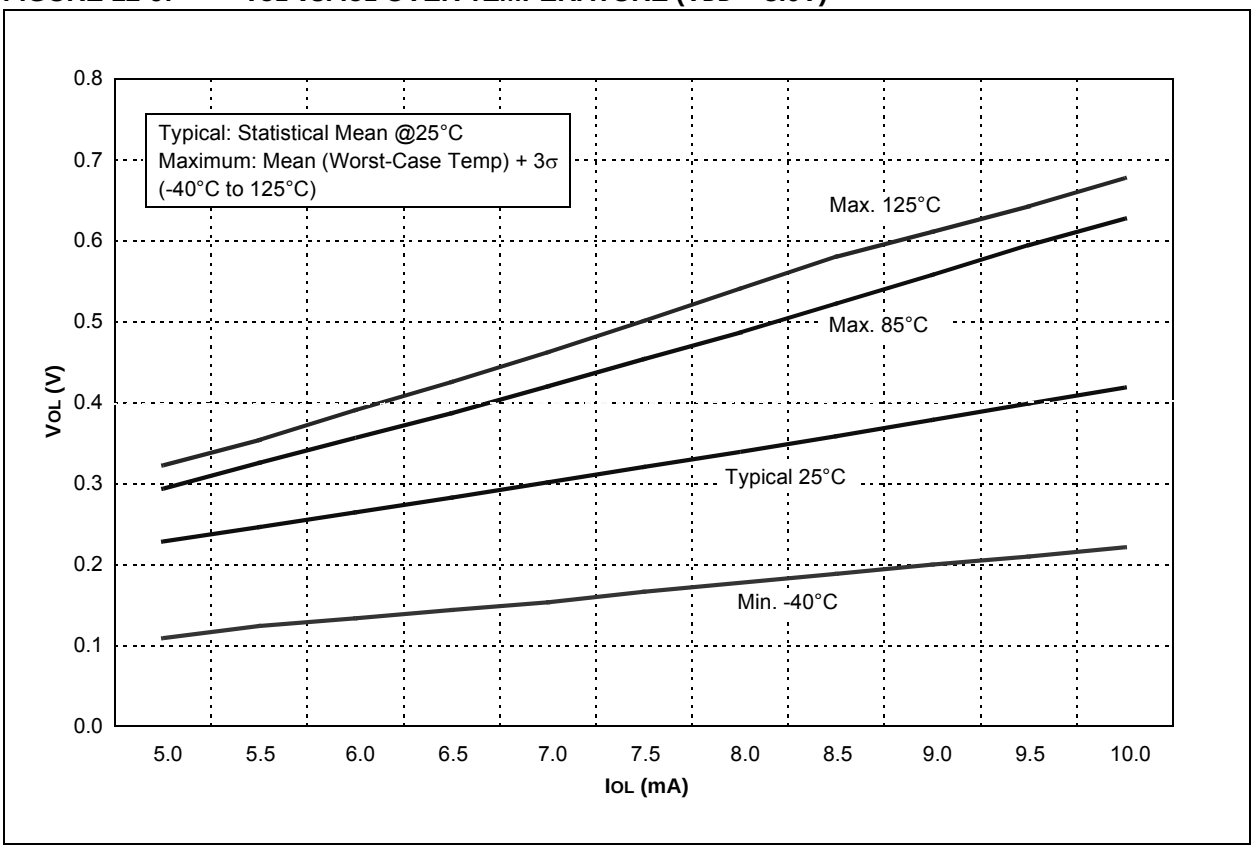

**FIGURE 12-10: VOL vs. IOL OVER TEMPERATURE (VDD = 5.0V)**

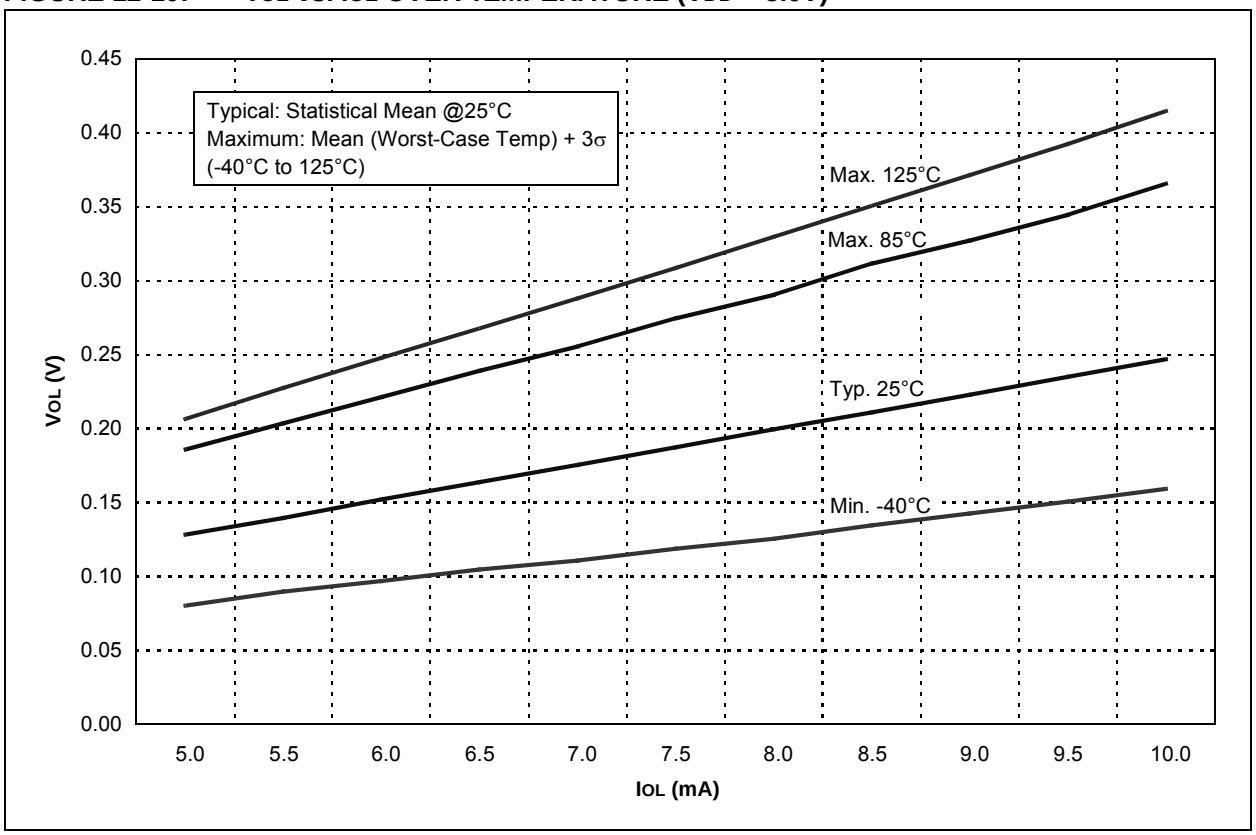


**FIGURE 12-11: VOH vs. IOH OVER TEMPERATURE (VDD = 3.0V)**

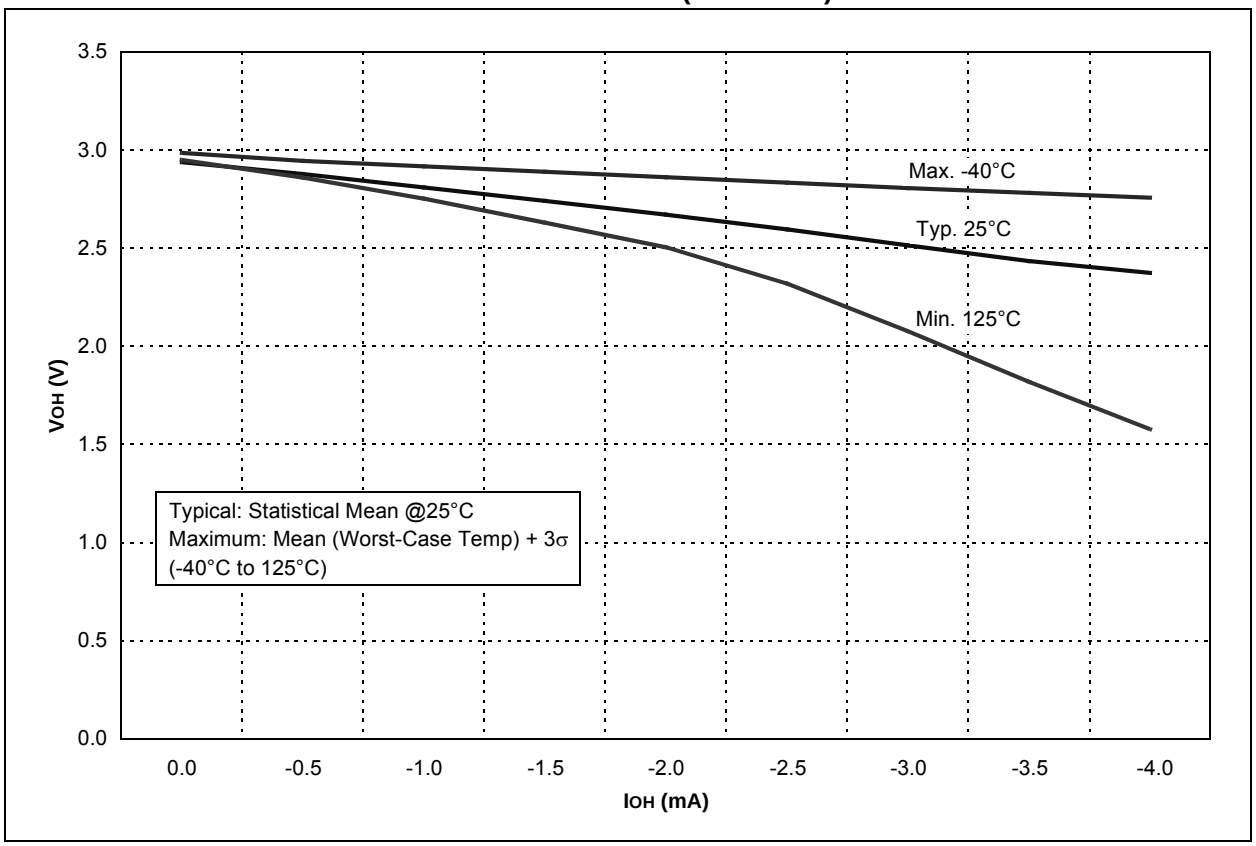



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**FIGURE 12-12: VOH vs. IOH OVER TEMPERATURE (VDD = 5.0V)**

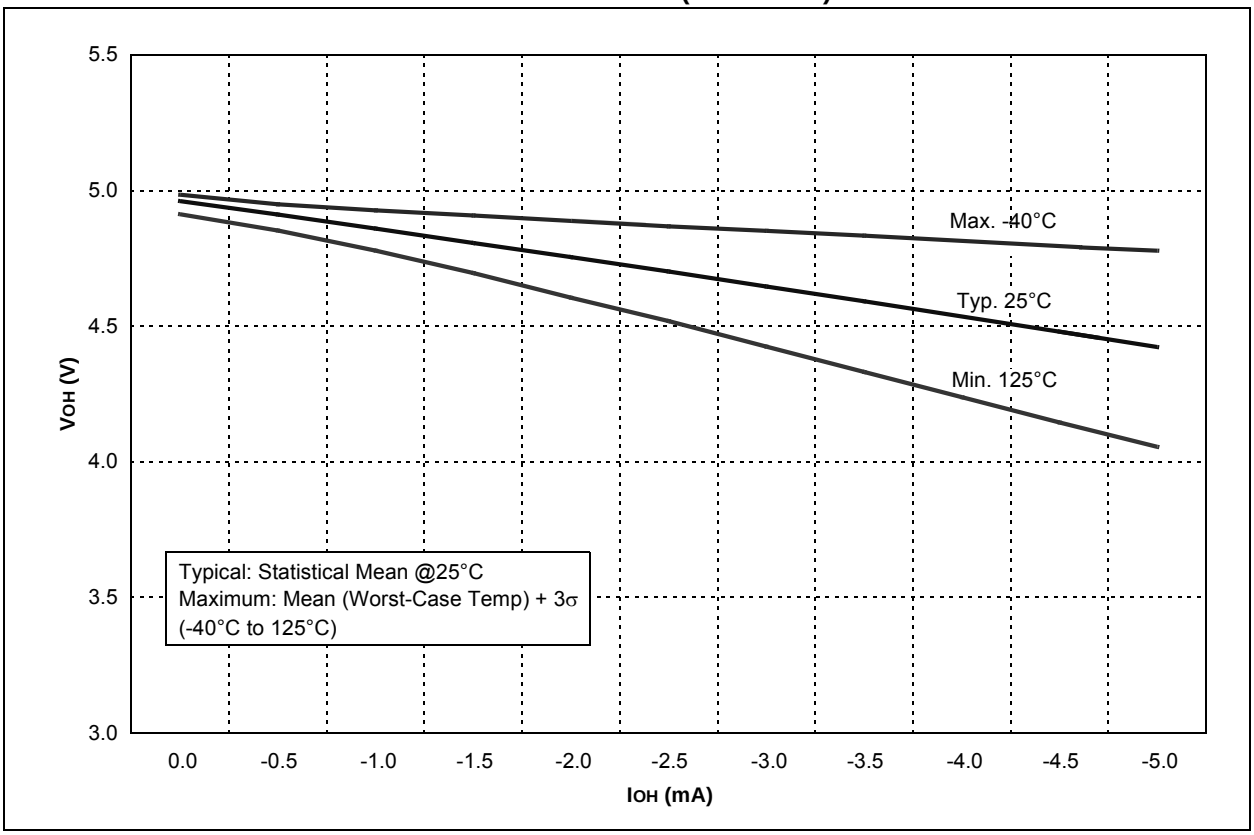



**FIGURE 12-13: TTL INPUT THRESHOLD VIN vs. VDD**

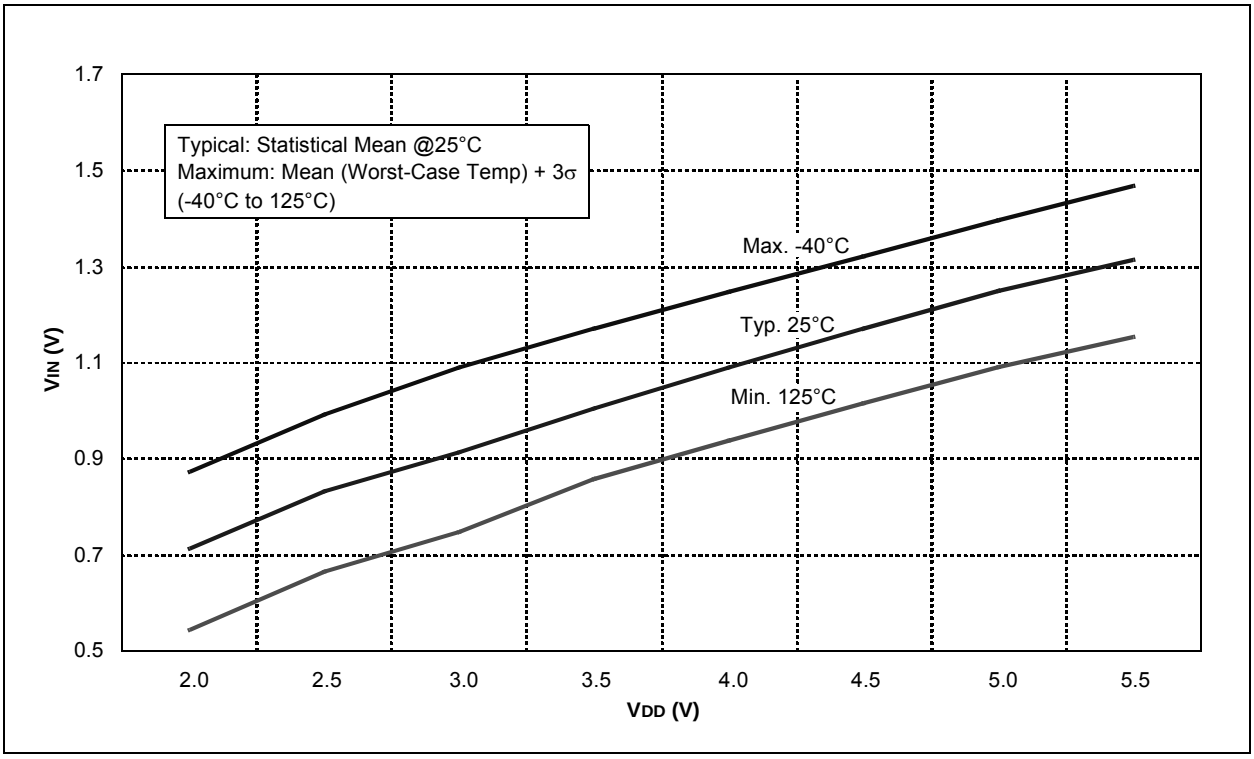


**FIGURE 12-14: SCHMITT TRIGGER INPUT THRESHOLD VIN vs. VDD**

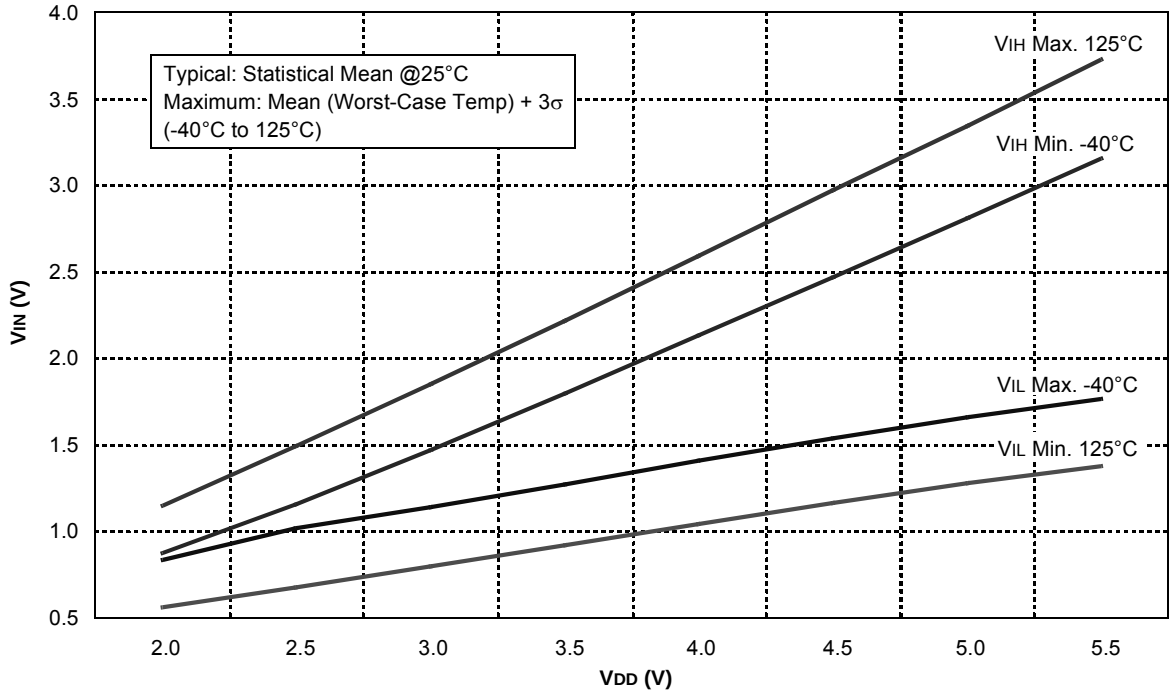
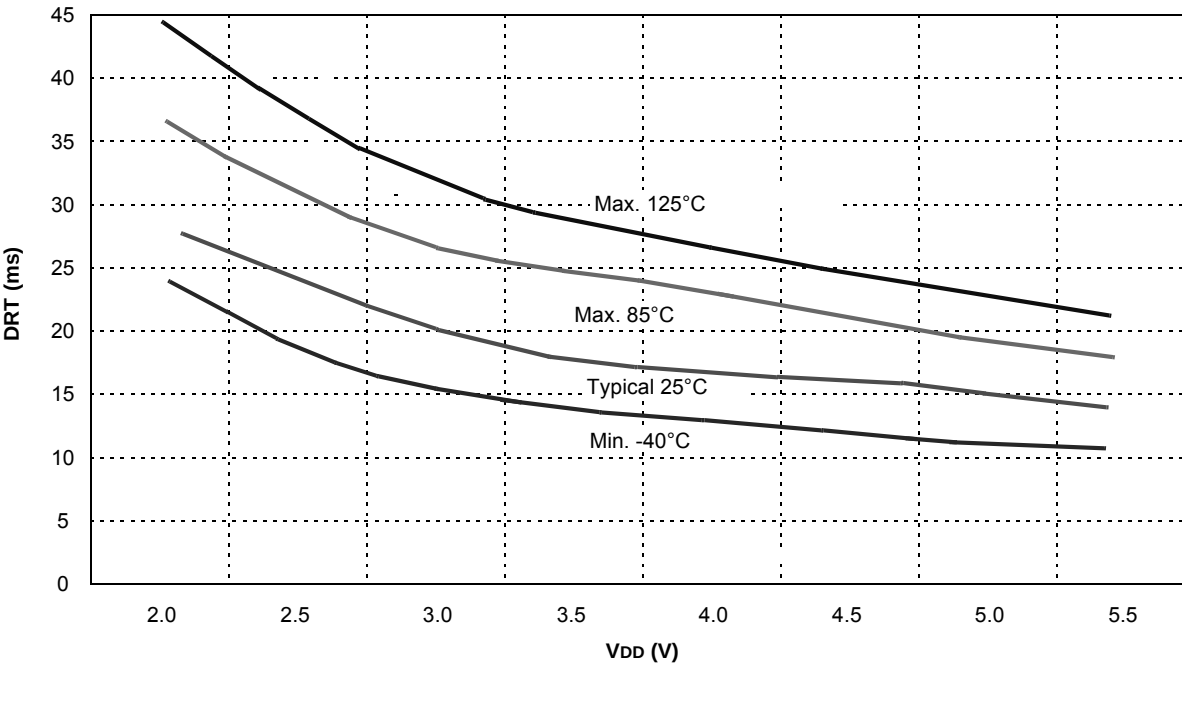



**FIGURE 12-15: DEVICE RESET TIMER (XT AND LP) vs. VDD**





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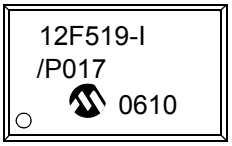
## 13.0 PACKAGING INFORMATION

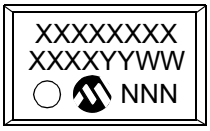
### 13.1 Package Marking Information

8-Lead PDIP

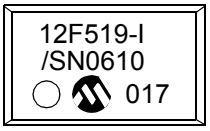
Example




8-Lead SOIC (3.90 mm)



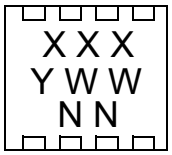

Example



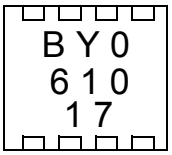

8-Lead MSOP

Example

8-Lead 2x3 DFN*




Example



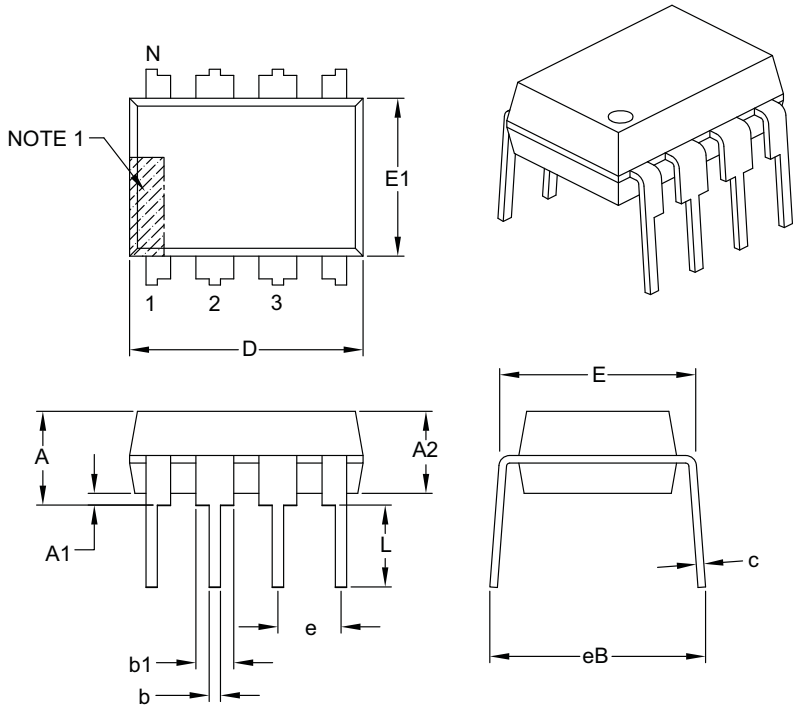

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

***** Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B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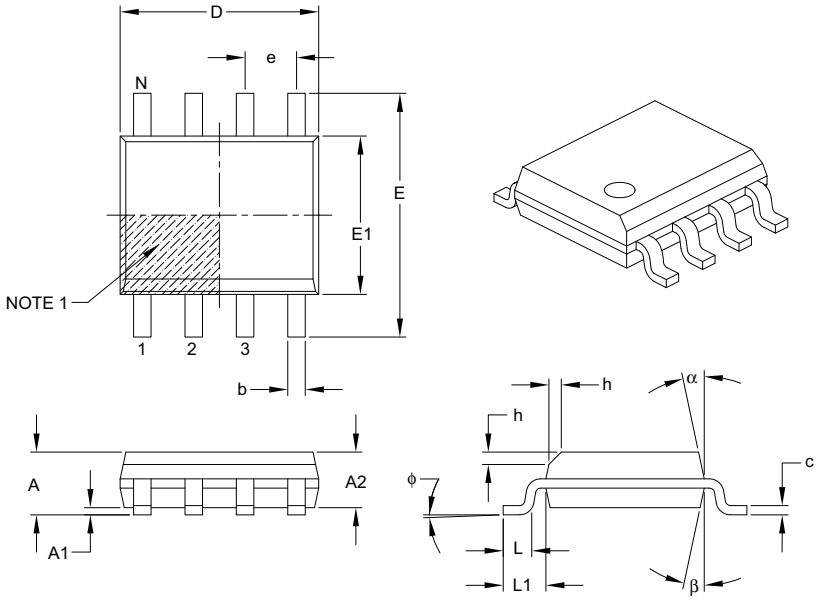
## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

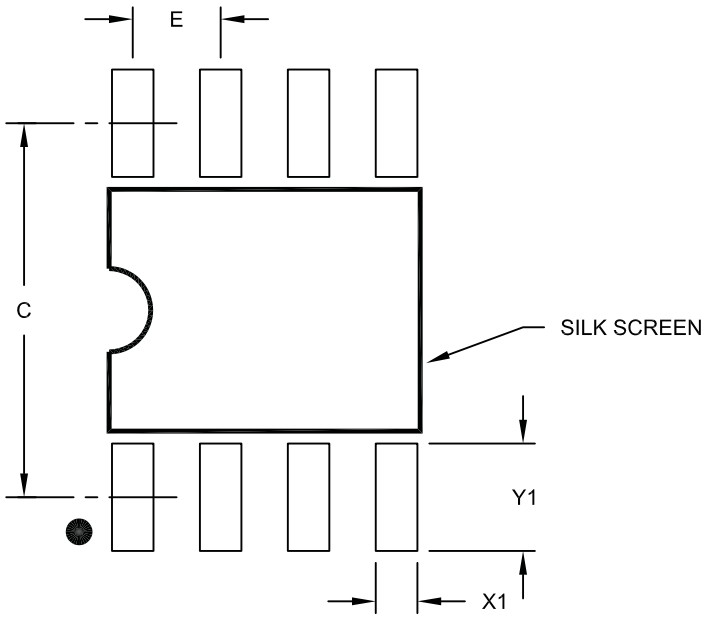
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

### 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A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## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

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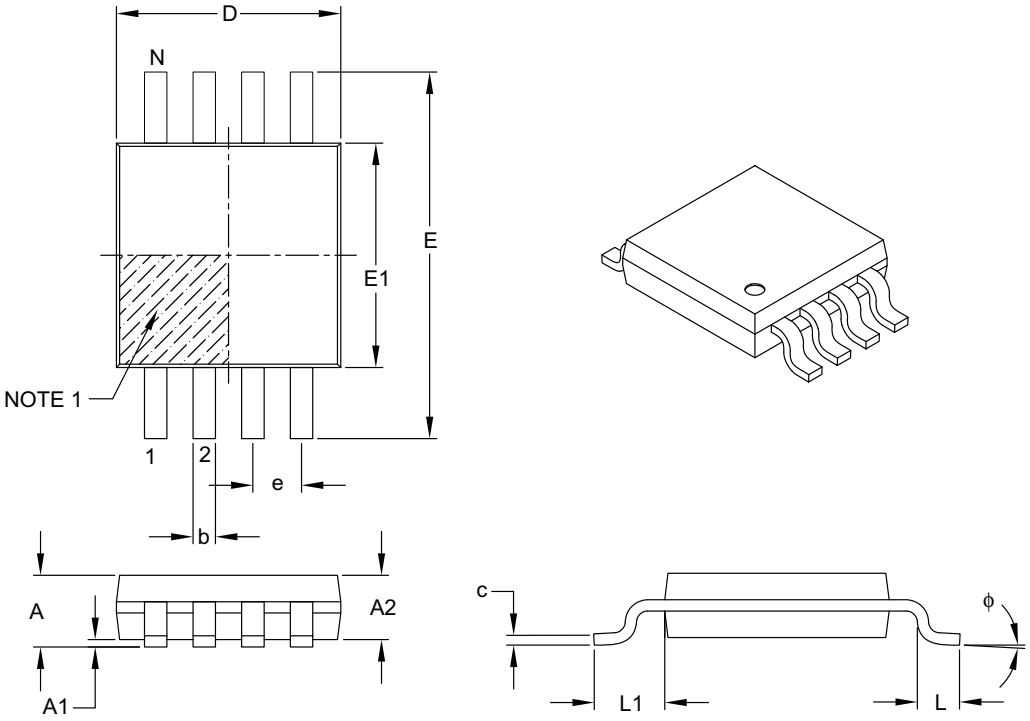



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Overall Length | D | | 3.00 BSC | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.08 | – | 0.23 |
| Lead Width | b | 0.22 | – | 0.40 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

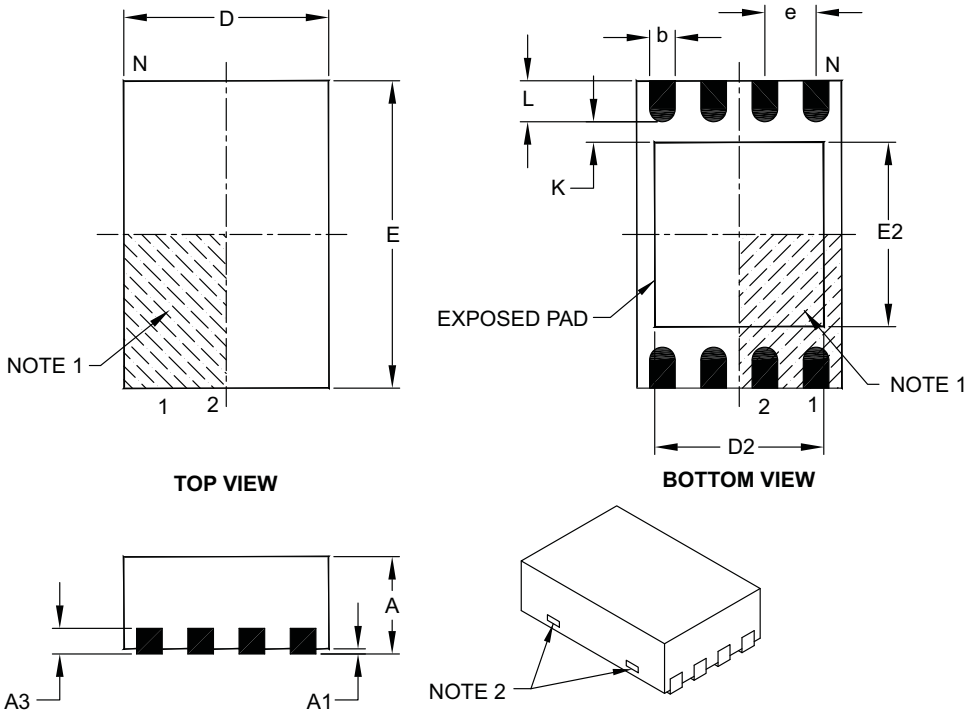
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

## 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 2.00 BSC | |
| Overall Width | E | | 3.00 BSC | |
| Exposed Pad Length | D2 | 1.30 | – | 1.55 |
| Exposed Pad Width | E2 | 1.50 | – | 1.75 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C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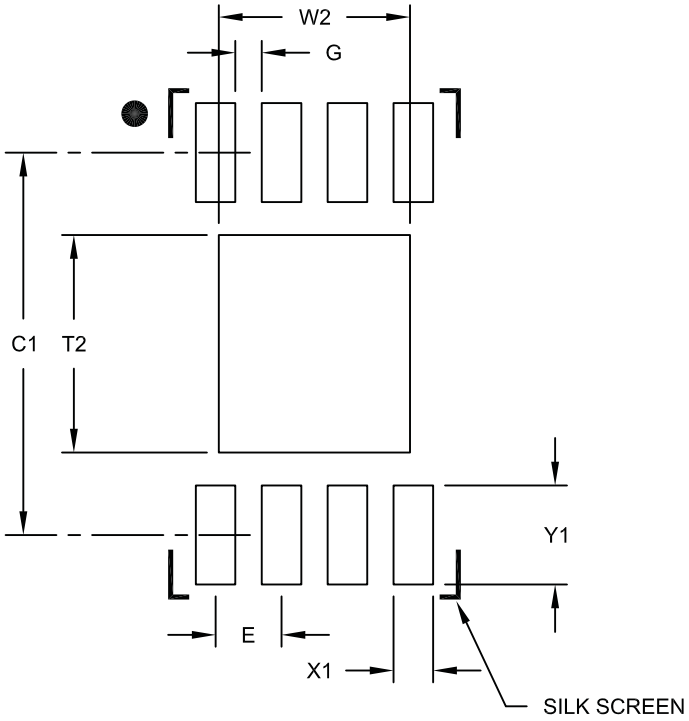
## 8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 1.45 |
| Optional Center Pad Length | T2 | | | 1.75 |
| Contact Pad Spacing | C1 | | 2.90 | |
| Contact Pad Width (X8) | X1 | | | 0.30 |
| Contact Pad Length (X8) | Y1 | | | 0.75 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123A

## APPENDIX A: REVISION HISTORY

**Revision A (May 2007)**

Original release of this document.

**Revision B (September 2008)**

Added DC and AC Characteristics graphs; Updated Electrical Characteristics section; Updated Package Drawings and made general edits.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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX | XXX |
|---|---|---|---|
| Device | Temperature Range | Package | Pattern |

| | |
|---|---|
| **Device:** | PIC12F519<br>PIC12F519T (Tape and Reel) |
| **Temperature Range:** | I = -40°C to +85°C (Industrial)<br>E = -40°C to +125°C (Extended) |
| **Package:** | MC = 8L DFN 2x3 (DUAL Flatpack No-Leads)<br>MS = MSOP (Pb-free)<br>P = 300 mil PDIP (Pb-free)<br>SN = 3.90 mm SOIC, 8-LD (Pb-free) |
| **Pattern:** | Special Requirements |

**Note:** Tape and Reel available for only the following packages: SOIC, DFN and MSOP.

**Examples:**

a) PIC12F519-I/P = Industrial temp., PDIP package (Pb-free)

b) PIC12F519T-I/SN = Tape and Reel, Industrial temp., SOIC package

c) PIC12F519 - E/MS 303 = Extended temp., MSOP package, QTP pattern #303

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В нашем ассортименте представлены ведущие мировые производители активных и пассивных электронных компонентов.

Нашей специализацией является поставка электронной компонентной базы двойного назначения, продукции таких производителей как XILINX, Intel (ex.ALTERA), Vicor, Microchip, Texas Instruments, Analog Devices, Mini-Circuits, Amphenol, Glenair.

Сотрудничество с глобальными дистрибьюторами электронных компонентов, предоставляет возможность заказывать и получать с международных складов практически любой перечень компонентов в оптимальные для Вас сроки.

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